LASP Demo Board

User's Guide

Literature Number: SCEU001
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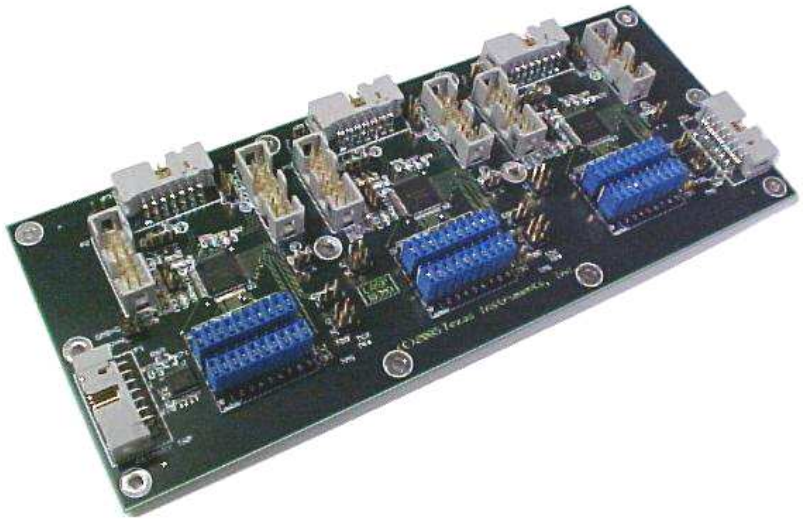
LASP Demo Board

The LASP demo board has three 'LVT8986 linking addressable scan ports (LASPs) implemented such that the capabilities and functionality of the LASP can be conveniently accessed. LASPs are multidrop bus-addressable IEEE Std 1149.1 (JTAG) test access port (TAP) transceivers with functions similar to the 'LVT8996 ASP, but with expanded capabilities. LASP linking is fully implemented on this board, with the capability to cascade the three LASPs on a single board. In addition, a multidrop bus-extension connector is provided to enable multiple LASP demo boards to be connected together. It is expected that readers are already familiar with JTAG but not the 'LVT8986. This document addresses the basics of the LASP and details how they are implemented on the LASP demo board, including a summary of LASP features, bypass mode and linking shadow protocol, board layout, and cascading, and an HSDL description of the board.



1.1 Introduction

The 'LVT8986 linking addressable scan port (LASP) is a multidrop addressable IEEE Std 1149.1 [Joint Test Action Group (JTAG)] test access port (TAP) transceiver similar to the 'LVT8996 ASP, but with a few expanded capabilities. The LASP has three IEEE Std 1149.1 secondary scan paths configurable to a single scan path. In addition, each LASP has the ability to be cascaded, allowing up to 8 LASPs to be connected in series, resulting in up to 24 configurable secondary scan paths to be connected to a single primary path on the same address. Each LASP demo board has three LASPs that can be cascaded. Each LASP demo board provides a multidrop bus connector to connect multiple boards, with a maximum of eight LASPs per address. The LASP is not an IEEE Std 1149.1 device itself, as it does not have all of the required test logic such as an instruction register or group of test data registers. Rather, the LASP is a scan support product, which improves the flexibility and quality of a boundary-scan system.

The LASP demo board is set up so that each LASP can be used individually (appearing as three single LASPs on three separate user-selectable addresses), or with two or more LASPs linked together sharing a user-selected address. This user's guide begins with an explanation of the workings of a single LASP on the demo board.

2.1 Summary

The 'LVT8996 addressable scan port (ASP) has a single IEEE Std 1149.1 port on its secondary side and it cannot cascade (link). However, with the LASP, for every address, each of the 24 possible STAPs can be uniquely configured. Each LASP can be given a 3-bit position to identify it in a cascade chain where each LASP would share a 10-bit address (see Figure 2-1). Controlling the LASP is similar to the ASP and can be done on the same backplane.

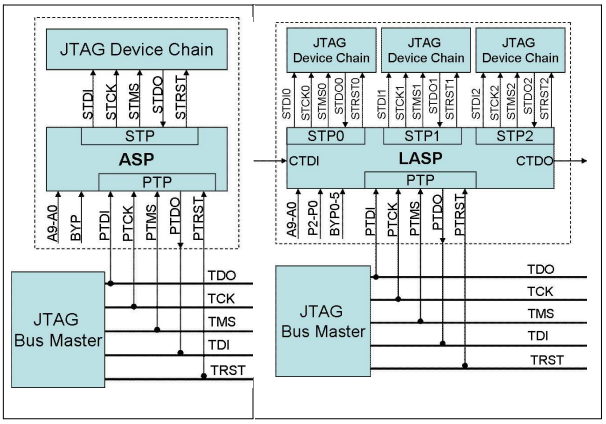


Figure 2-1. LASP Diagram

The most powerful use of the LASP is in system-level IEEE Std 1149.1 testing. At the system level, the LASP configurability allows boards to be removed from a system without breaking the scan chain. In the interest of speed, a dynamic set of boards can be selected for testing instead of running data through the IEEE Std 1149.1 system. Reducing the number of devices in the scan chain dramatically reduces the test vector lengths.

The LASP can also improve testing on a single board that would have used one long boundary scan chain. The board could be designed with the long single chain divided into three (for a single LASP) smaller chains. The division in the three chains can be logically based on scan speed, to group fast or slow testing devices together or programmable devices, or to isolate processor emulation ports. The ability to test between system boards gives the LASP a key advantage over the ASP. This improves the test, service, and programming speed by allowing the user to dynamically select only the necessary chains.

2.2 Main Features

- 10-bit address (A9–A0) pins and 3-bit position (P2–P0) pins allow up to 24 secondary scan paths connected to primary TDI/TDO per address.
- Linking shadow protocol can be used to address and configure secondary TAPs.
- Bypass mode offers a 6-pin ($\overline{BYP}_5$–$\overline{BYP}_0$) alternative to linking shadow protocol to control the LASP.
- $\overline{CON}_2$–$\overline{CON}_0$ provide indication of primary to secondary path connection status for each LASP.
- Secondary TAPs can be configured to high impedance via the $\overline{OE}$ pin, allowing an alternate test master to control secondary TAPs.

2.3 Configurations

There are two methods, as previously stated, that can be used to manipulate the state of the STAPs in the LASP – linking shadow protocol and bypass mode. The linking shadow protocol uses a bit pair signaling scheme that is broadcast to all the LASPs, whereas the bypass mode uses six pins on the LASP to indicate the state the STAPs should be in. For each LASP, there are eight STAP configurations (see Table 2-1) with their corresponding scan path configurations.

Table 2-1. Single LASP Configurations

CASCADE POSITION	STAP0	STAP1	STAP2	SCAN-PATH CONFIGURATION
Single Device	Inactive	Inactive	Inactive	None
Single Device	Active	Inactive	Inactive	PTDI–(1)–STAP0–(1)–PTDO
Single Device	Inactive	Active	Inactive	PTDI–(1)–STAP1–(1)–PTDO
Single Device	Active	Active	Inactive	PTDI–(1)–STAP0–(1)–STAP1–(1)–PTDO
Single Device	Inactive	Inactive	Active	PTDI–(1)–STAP2–(1)–PTDO
Single Device	Active	Inactive	Active	PTDI–(1)–STAP0–(1)–STAP2–(1)–PTDO
Single Device	Inactive	Active	Active	PTDI–(1)–STAP1–(1)–STAP2–(1)–PTDO
Single Device	Active	Active	Active	PTDI–(1)–STAP0–(1)–STAP1–(1)–STAP2–(1)–PTDO

2.3.1 Bypass Mode

Bypass mode uses the six $\overline{BYP_5}$–$\overline{BYP_0}$ pins to connect the primary TAP to selected secondary TAPs. This protocol connects the secondary scan paths without the use of linking shadow protocol, and the LASP does not respond to linking shadow protocol while in this mode. Entry into bypass mode is enabled by applying a logic low on the pin (see Figure 2-2). While in bypass mode, the LASP does not respond to linking shadow protocol.

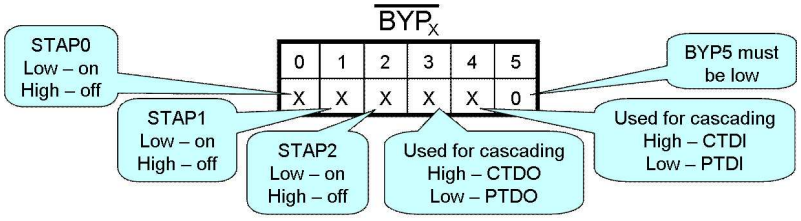


Figure 2-2. Bypass Pin Control Description

Pins $\overline{BYP_2}$–$\overline{BYP_0}$ correspond to the STAP connections. Pins $\overline{BYP_3}$ and $\overline{BYP_4}$ indicate the source pin for scan input data and drive pin for scan output data. Each LASP has a primary TDI and TDO (PTDI and PTDO) and a cascade TDI and TDO (CTDI and CTDO). $\overline{BYP_3}$ and $\overline{BYP_4}$ indicate to the LASP from which TDI the signal came from and to which TDO the signal should travel. For a single LASP, both of these bits should be kept low (see section 4.1). Configurations for a single LASP, based on example $\overline{BYP_5}$–$\overline{BYP_0}$ pin settings, are shown in Figure 2-3.

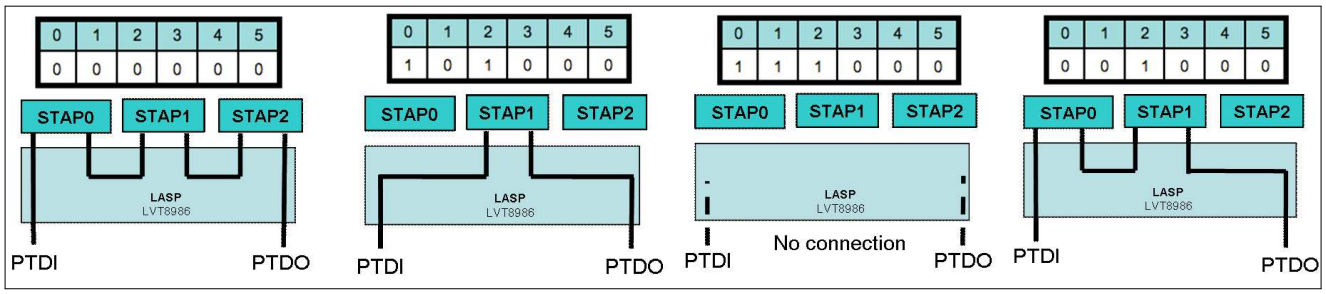
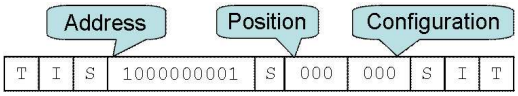


Figure 2-3. Single LASP Bypass Pin Configuration Examples

2.3.2 Linking Shadow Protocol

Linking shadow protocol is a serial bit-pair stream broadcast to the whole boundary-scan multidrop bus (see Figure 2-4 and Figure 2-5). Each LASP determines its status by address and position information in the linking shadow select protocol. When the single LASP recognizes its address and its position, it configures its STAPs based on the configuration information that immediately follows its position identifier. If the select protocol successfully completes, the LASP immediately echoes the acknowledge protocol back. No response is given for a failed linking shadow select protocol. Example linking shadow select protocols and successful configurations are shown in Figure 2-6.



Single LASP address 0001100101, position 000, all STAPs set to active.

Figure 2-4. Linking Shadow Protocol

I	S	D(1)	D(0)
HH	LL	LH	HL

D(0) and D(1) refer to the 0s and 1s in the address, position, and configuration.

Figure 2-5. Bit-Pair Signaling Scheme

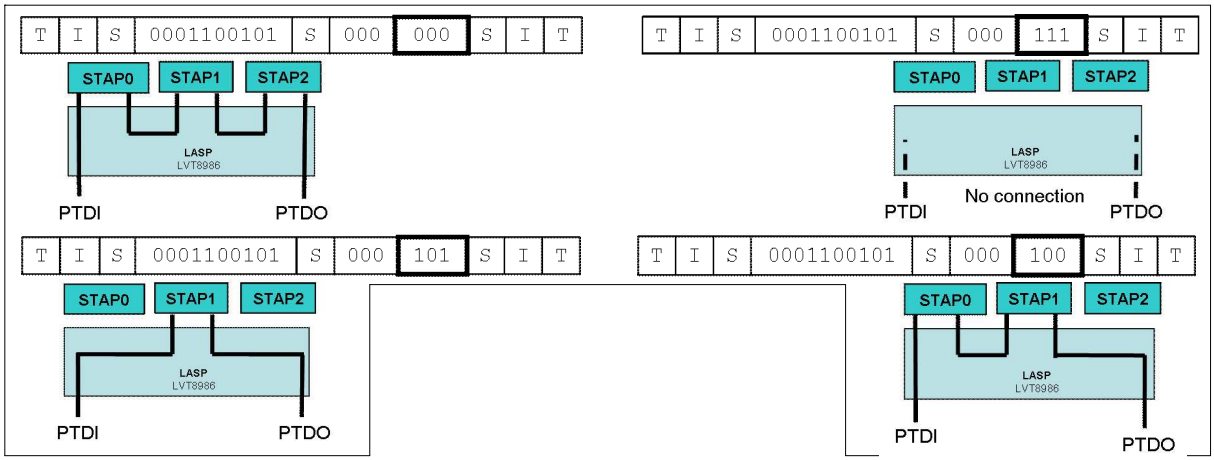


Figure 2-6. Linking Shadow Configuration Examples

2.4 Testing Limitation

IEEE Std 1149.1 bus masters, which control the test clock (TCK), can either use a gated or free-running clock. A gated clock, or gated TCK mode, halts the clock when pause is needed. A free-running clock, or free-running TCK mode, places the applicable scan chains into a stable state while the clock continues to run. If a pause is needed while scanning in or out data, as in the Shift-DR and Shift-IR states, the scan chains are put into Pause-DR and Pause-IR, respectively. While the LASP can successfully accept linking shadow protocols in the Pause-DR and Pause-IR states, boundary-scan tests cannot be successfully performed in free-running TCK mode through a LASP if, while shifting data in or out, the scan chains are placed in these states.

After the scan chain is placed in a Pause-DR or Pause-IR, and as long as the clock continues to cycle the datum in a pad bit is updated, causing it to lose its current value. In the pause states, the TDO upstream is not pushing data and the boundary cells downstream are not updating. Each pad bit is expected to hold its value designated for position x in the total chain. However, in free-running TCK mode, the pad bit could be overwritten each time the system is put into one of the pause states.

While it may not be possible to compatibly use the LASP with a free-running test clock, by using a gated clock, these difficulties are avoided.

2.5 Pad Bits

To create an upgrade to the ASP with the ability to cascade as the LASP does, pad bits are used to reduce propagation delays that reduce the allowable test clock speed. These pad bits are located along the internal scan path of the LASP and, therefore, must be accommodated in the boundary-scan test program. The number of these bits ranges from one to four. The number and location completely depends on the configuration of the LASP. In Table 2-2, each LASP relative position and configuration scan path uses a (1) to indicate a pad bit in the path.

A number of boundary-scan development tools suppliers support the LASP with the necessary pad bit inclusion. If not using one of these more user-friendly methods of incorporating the LASP in a design, the pad bits can be added manually, with some difficulty, to a serial vector file (.svf) or other type of boundary-scan vector file.

Table 2-2. Multiple LASP Scan-Path Configurations Including Pad Bit(s)

CASCADE POSITION	STAP0	STAP1	STAP2	SCAN-PATH CONFIGURATION	NO. OF PAD BITS
Single Device	Inactive	Inactive	Inactive	None	0
Single Device	Active	Inactive	Inactive	PTDI–(1)–STAP0–(1)–PTDO	2
Single Device	Inactive	Active	Inactive	PTDI–(1)–STAP1–(1)–PTDO	2
Single Device	Active	Active	Inactive	PTDI–(1)–STAP0–(1)–STAP1–(1)–PTDO	3
Single Device	Inactive	Inactive	Active	PTDI–(1)–STAP2–(1)–PTDO	2
Single Device	Active	Inactive	Active	PTDI–(1)–STAP0–(1)–STAP2–(1)–PTDO	3
Single Device	Inactive	Active	Active	PTDI–(1)–STAP1–(1)–STAP2–(1)–PTDO	3
Single Device	Active	Active	Active	PTDI–(1)–STAP0–(1)–STAP1–(1)–STAP2–(1)–PTDO	4
First Device	Inactive	Inactive	Inactive	None	0
First Device	Active	Inactive	Inactive	PTDI–(1)–STAP0–(1)–CTDO	2
First Device	Inactive	Active	Inactive	PTDI–(1)–STAP1–(1)–CTDO	2
First Device	Active	Active	Inactive	PTDI–(1)–STAP0–(1)–STAP1–(1)–CTDO	3
First Device	Inactive	Inactive	Active	PTDI–(1)–STAP2–(1)–CTDO	2
First Device	Active	Inactive	Active	PTDI–(1)–STAP0–(1)–STAP2–(1)–CTDO	3
First Device	Inactive	Active	Active	PTDI–(1)–STAP1–(1)–STAP2–(1)–CTDO	3
First Device	Active	Active	Active	PTDI–(1)–STAP0–(1)–STAP1–(1)–STAP2–(1)–CTDO	4
Last Device	Inactive	Inactive	Inactive	None	0
Last Device	Active	Inactive	Inactive	CTDI–(1)–STAP0–(1)–PTDO	2
Last Device	Inactive	Active	Inactive	CTDI–(1)–STAP1–(1)–PTDO	2
Last Device	Active	Active	Inactive	CTDI–(1)–STAP0–(1)–STAP1–(1)–PTDO	3
Last Device	Inactive	Inactive	Active	CTDI–(1)–STAP2–(1)–PTDO	2
Last Device	Active	Inactive	Active	CTDI–(1)–STAP0–(1)–STAP2–(1)–PTDO	3
Last Device	Inactive	Active	Active	CTDI–(1)–STAP1–(1)–STAP2–(1)–PTDO	3
Last Device	Active	Active	Active	CTDI–(1)–STAP0–(1)–STAP1–(1)–STAP2–(1)–PTDO	4
Middle Device	Inactive	Inactive	Inactive	None	1
Middle Device	Active	Inactive	Inactive	CTDI–(1)–STAP0–(1)–CTDO	2
Middle Device	Inactive	Active	Inactive	CTDI–(1)–STAP1–(1)–CTDO	2
Middle Device	Active	Active	Inactive	CTDI–(1)–STAP0–(1)–STAP1–(1)–CTDO	3
Middle Device	Inactive	Inactive	Active	CTDI–(1)–STAP2–(1)–CTDO	2
Middle Device	Active	Inactive	Active	CTDI–(1)–STAP0–(1)–STAP2–(1)–CTDO	3
Middle Device	Inactive	Active	Active	CTDI–(1)–STAP1–(1)–STAP2–(1)–CTDO	3
Middle Device	Active	Active	Active	CTDI–(1)–STAP0–(1)–STAP1–(1)–STAP2–(1)–CTDO	4

LASP Demo Board Layout

The LASP demo board has three LASP devices connected in parallel to the multidrop bus, with the option to connect the CTDI/CTDO lines using jumper cables (see Figure 3-1).

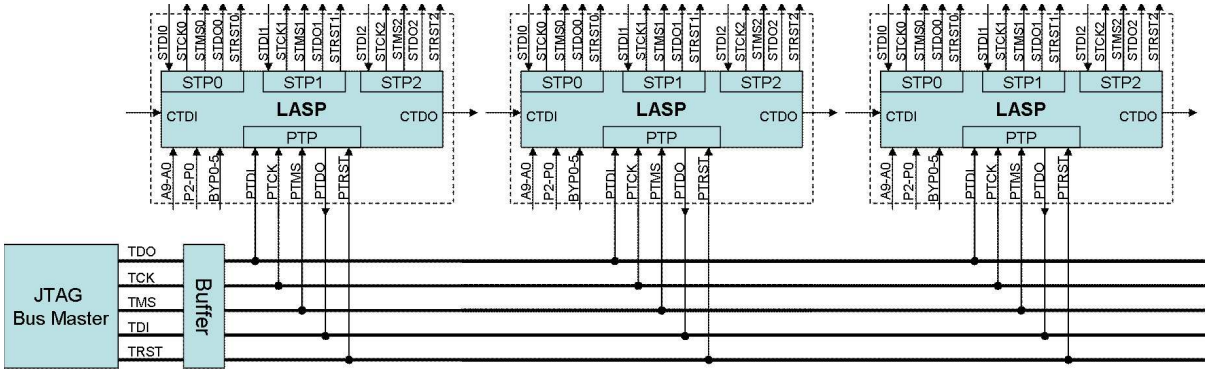


Figure 3-1. LASP Demo Board Block Diagram

There are multiple power and ground connections used to supply power to the board or serve as test points. For each LASP, there are nine test points with indicator LEDs (rightmost column of labels) corresponding to SX_2–SX_0, SY_2–SY_0, and $\overline{CON_2}$–$\overline{CON_0}$, which illuminate when the associated connection is active (see Figure 3-2 and Figure 3-3). In addition, each LASP has a CONCAT jumper block that can be used to connect CTDI and CTDO to another LASP's CTDI or CTDO.

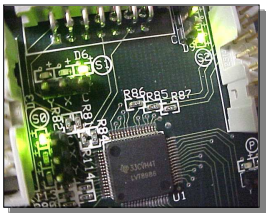


Figure 3-2. LASP Test Points

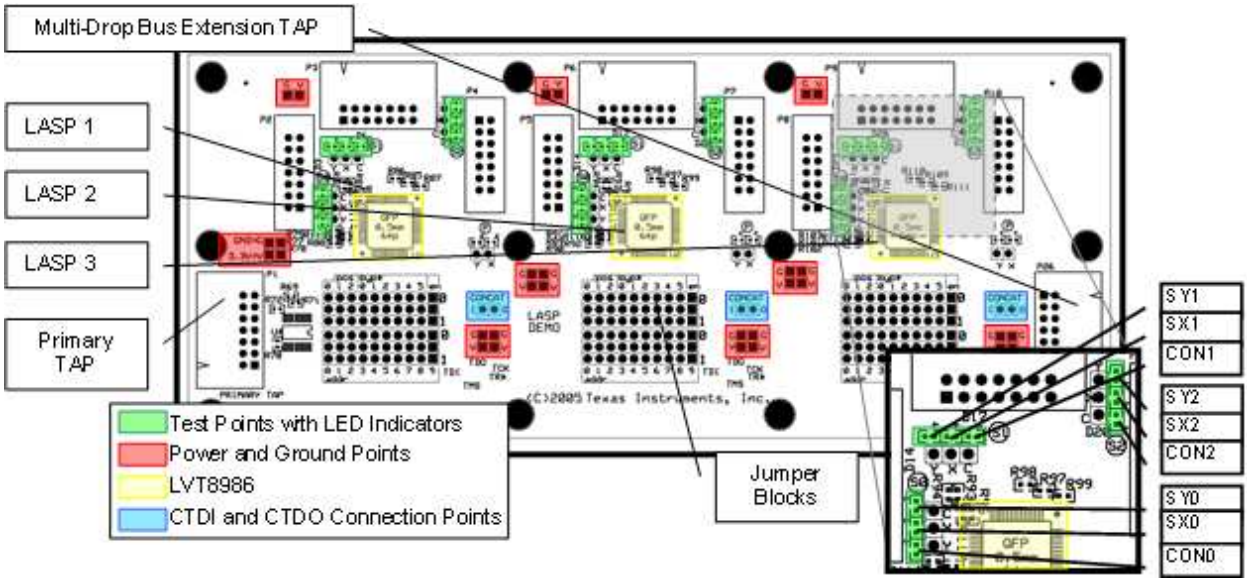


Figure 3-3. LASP Board Layout

Each LASP has one right-angle STAP header (STAP1) and two straight headers (STAP0, STAP2) (see Figure 3-4 and Figure 3-5). There are two rows of ten sets of jumper blocks that set the 10-bit address, 6-bit bypass, 3-bit position, and 1-bit output enable ($\overline{OE}$) labeled en (see Figure 3-5).

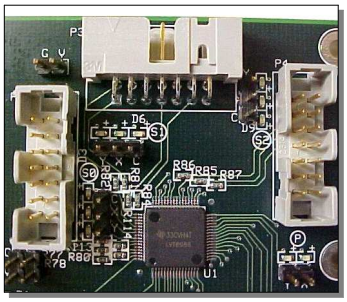


Figure 3-4. Single LASP on LASP Demo Board

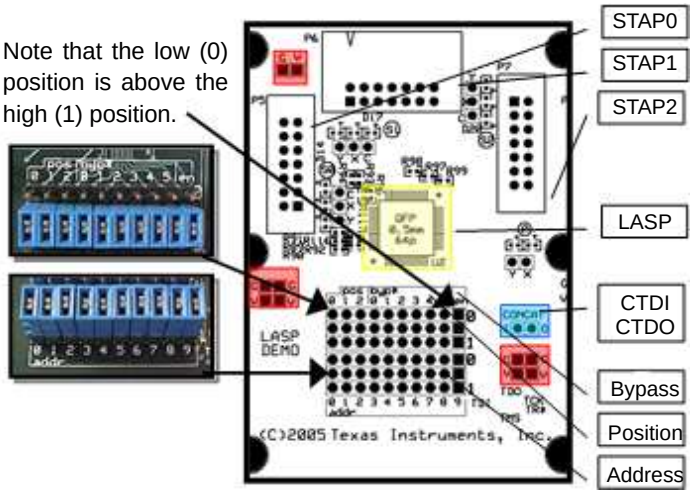


Figure 3-5. Single LASP on Demo Board

3.1 Board Pinout

Special care should be taken with the TDI and TDO connections between different boards to ensure they are connected correctly. On this board, traces are labeled by the 'LVT8986 pins; refer to the data sheet for a complete description of pin function. Figure 3-6 shows the pinout for the primary TAP. The lines are labeled on the board by their connection to the 'LVT8986. Silkscreens marking the multidrop bus traces are on the top of the board, while the actual traces are on the bottom.

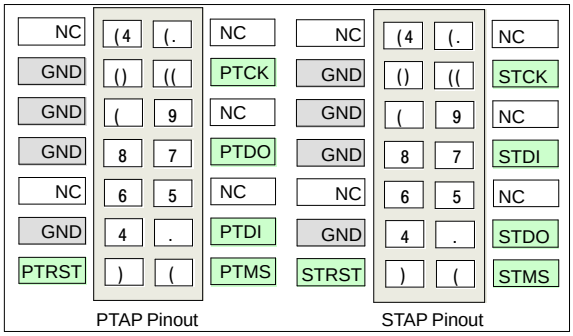


Figure 3-6. Multidrop Bus (PTAP) and STAP Pinouts

3.2 Cascading on LASP Demo Board

The three LASPs on each demo board are designed to function completely independent of the other LASPs or their physical location on the board. In order to cascade a LASP on the demo board, the I and O on the jumper block labeled CONCAT need to be connected (see Figure 3-7). The I stands for CTDI and the O for CTDO.

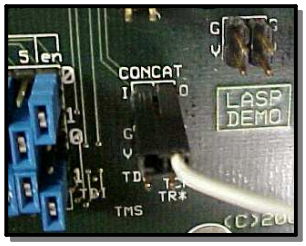


Figure 3-7. CONCAT

The LASPs can be connected in any order but, for clarity, the LASPs are connected and numbered in order from the primary TAP to the cascade primary TAP, or from left to right when the text “LASP Demo” is right side up.

In Figure 3-8, the LASPs are numbered from left to right (000, 001, and 010) and the concatenation jumper is going from 000 CTDO to 001 CTDI, and 001 CTDO is connected to 010 CTDI.

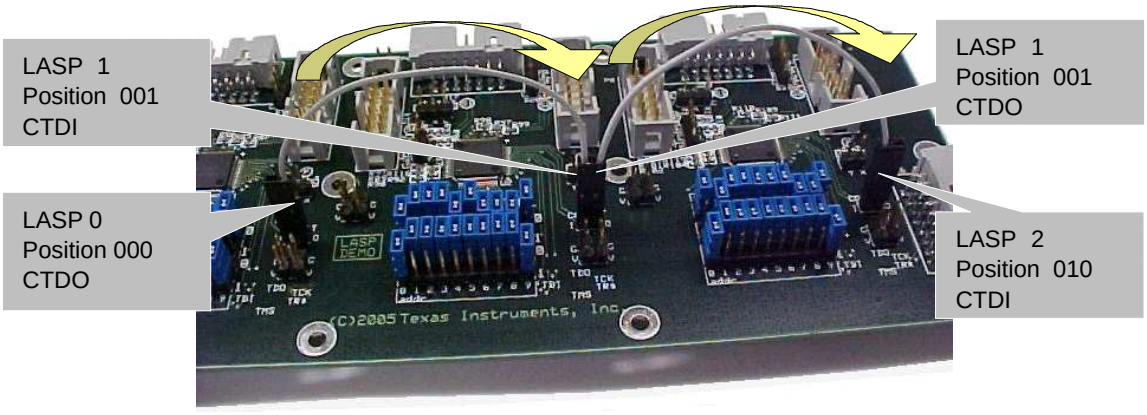


Figure 3-8. CTDI/CTDO Numerical Order Positions

The LASPs should be connected in numerical order by their designated position bits. Failure to properly connect the CTDI/CTDO sequence, relative to the LASP's position pin setting, does not result in any error response by the LASP; it may not work depending on the configuration.

3.3 Extending Multidrop Bus Between LASP Demo Boards

As previously mentioned, a connector was provided to enable the multidrop bus to be extended to additional LASP demo boards. Three additional connections that must be made are (1) connect the extension TAP connector to the primary TAP connector of the additional board using a 14-pin socket cable (see Figure 3-9), (2) connect the CTDO of the last LASP on the primary board to the CTDI on the first LASP of the new board, if cascading of those LASPs is sought, and (3) supply power and ground connections to the new board (see Figure 3-10).

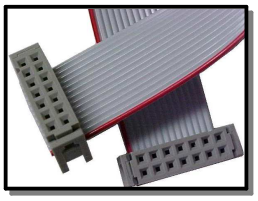


Figure 3-9. 14-Pin Socket Cable

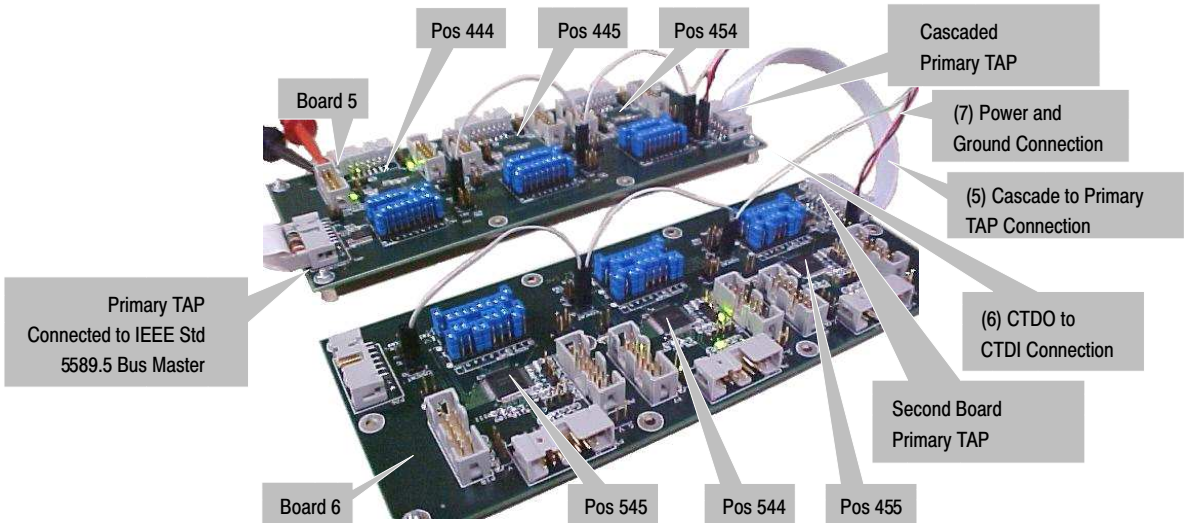


Figure 3-10. Cascaded LASP Demo Boards

Configuring the LASP Demo Board

Configuring the LASP demo board, as with the individual LASP, can use two different methods – linking shadow protocol and bypass mode. To use either, the enable pin ($\overline{OE}$) must be kept low.

4.1 Bypass Mode

To enter bypass mode, $\overline{BYP_5}$ must be low. The difference when using bypass mode on a single LASP versus multiple LASPs is the consideration given to the bypass pins 4 and 3 (previously held low for a single LASP), which select between CTDI/PTDI and CTDO/PTDO, respectively (see Figure 4-1).

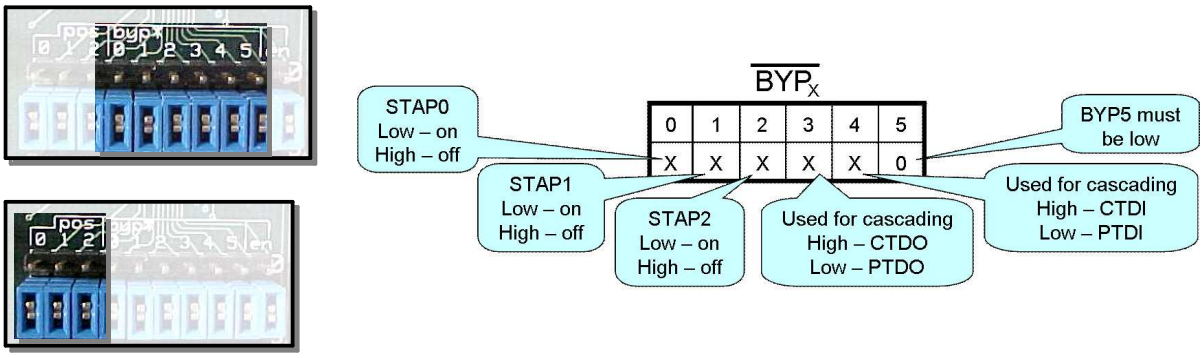
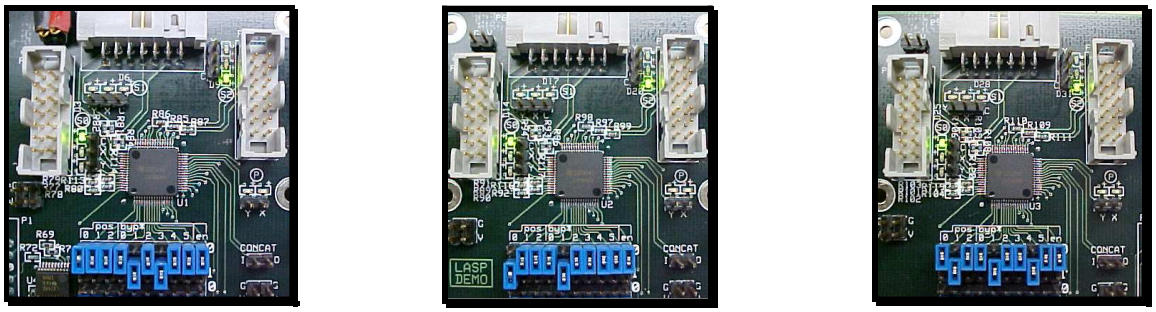


Figure 4-1. Multidrop Bus (PTAP) and STAP Pinouts

As seen in Figure 4-2, U1 has STAP0 and STAP2 active (bypass pins 0 and 2 low), bypass pin 3 is high, and bypass pin 4 is low, indicating the PTDI to CTDO active path. U2 also has STAP0 and STAP2 active while pins 3 and 4 are both high, indicating a CTDI to CTDO connection. Finally, U3 has STAP0 and STAP2 active, while pin 3 is low and pin 4 is high, meaning a CTDI to PTDO connection (see Figure 4-2 and Figure 4-3).



U1 U2 U3

Figure 4-2. Bypass Pin Configuration

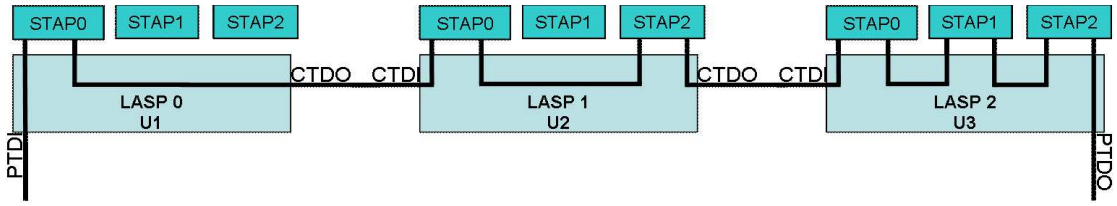


Figure 4-3. LASP Configuration From Bypass Pins

When in bypass mode, each LASP acts independently and the three position bits have no effect. If a CTDI or CTDO configuration is selected on a LASP and the adjoining LASP TDI/TDO paths do not feed into/from that LASP, the scan chain is broken. There is no formal error or response from the LASP, no matter how they are configured to confirm a functional cascade. The active STAP configuration selected, even if selected by an invalid bypass pin configuration, is indicated by the CON2–CON0 indicator LEDs.

4.2 Linking Shadow Protocol

The linking shadow protocol bit pair signaling scheme used to control the single LASP (described in section 2.3.2) is the same basic protocol used for multiple LASPs. All LASPs to be cascaded should share the same address. Some addresses are reserved; please reference the 'LVT8986 data sheet for more information concerning reserved addresses. The 3-bit position identifier on each LASP should be set to sequential binary numbers by the CTDI/CTDO connection and $\overline{BYP_5}$ must be high.

For each position requiring one or more STAPs to be activated, the corresponding position and configuration bits should be signaled before the closing select and idle bit pairs (see Figure 4-4). This example could apply for a single LASP demo board with the position numbers 000, 001, and 010, respectively, but also would work for any three properly configured LASPs with position numbers 000, 001, and 010. In any case, proper CTDI/CTDO connections using the jumper blocks must be made for linking shadow protocol functions as expected.

	Idle			LSB Address MSB	Select	Position 1	Config. 1	Position 2	Config. 2	Position 3	Config. 3	Select	Idle	
Received at PTDI	T	I	S	1000000001	S	000	011	100	010	010	000	S	I	T

Figure 4-4. Select Protocol

All LASPs receive the protocol on PTDI and immediately following a successful linking shadow protocol but, after the primary to secondary TAP connections have been made, only the last LASP responds without delay with an acknowledge protocol (see Figure 4-5 and Figure 4-6). For a failed protocol, no acknowledge message is sent. LASPs may reset for a failed protocol. See the 'LVT8986 data sheet for complete details regarding hard and soft errors using linking shadow protocol.

		Idle		LSB Address MSB	Select	Position 1	Config. 1	Position 2	Config. 2	Position 3	Config. 3	Select	Idle	
Transmitted at PTDO	T	I	S	1000000001	S	000	011	100	010	010	000	S	I	T

Figure 4-5. Acknowledge Protocol

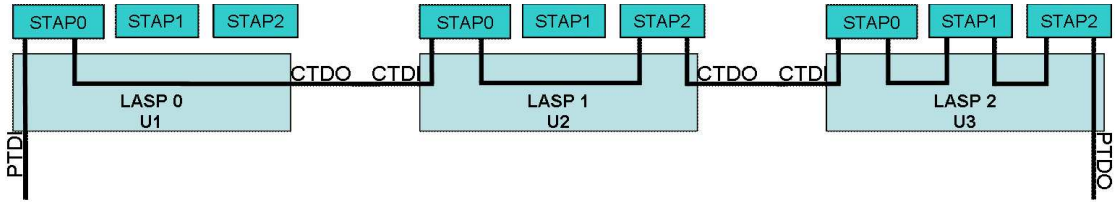


Figure 4-6. LASP Configuration Following Select Protocol

LASP Demo Board Ordering Information

LASP demo boards can be purchased from a TI preferred supplier with access to the TI EDGE system. Reference TI EDGE number 6473723 for the LASP demo board.

One possible supplier is:

Millennium Circuits
(972) 271-0246
2706 Country Valley Road
Garland, Texas

HSDL Description of LASP Demo Board

Hierarchical scan description language (HSDL) is the system-level complement to boundary scan description language (BSDL) and, likewise, is based on the same subset of VHSIC hardware description language (VHDL) statements. With HSDL, the scan description picks up where BSDL stops and describes scan interconnections at all levels of a system hierarchy.

Entities in HSDL, unlike in BSDL, are used to describe not just devices but modules as well. A module is any level of architecture including, but not limited to, boards, multichip modules, backplanes, subsystems, and systems. HSDL specifically improves three areas not well covered by BSDL descriptions alone.

- Describes test bus interconnections at board or module level
- Describes boards with dynamic and reconfigurable architectures
- Reduces risk during interactive design debug and verification

Using BSDL and HSDL together can create a full scan description of the unit under test.

A HSDL description for a system consists of the following elements:

- Entity descriptions
- Generic parameter
- Logical port description
- Use statements
- [Optional module descriptions]
- [Optional port description(s)]
- Pin mapping(s)
- Scan port identifications
- [Optional member descriptions(s)]
- [Optional bus description(s)]
- Path description
- [Optional member connections]
- [Optional constraint description(s)]
- [Optional design warning]

The following is an HSDL description of the LASP demo board using dummy devices. This example can be copied and modified where indicated to be adapted to an actual system design used with the LASP demo board or to incorporate a LASP in an existing HSDL design.

Comments begin with '--' and are in italics here for distinction.

```
entity LASP_Demo is
   generic (PHYSICAL_PIN_MAP : string := "UNDEFINED");

   port (PTDI  : in  bit;
         PTDO  : out bit;
         PTMS  : in  bit;
         PTCK  : in  bit;
         PTRST : in  bit);

   use STD_1149_1_1990.all;
   use HSDL_module.all;

   attribute PIN_MAP of LASP_Demo : entity is PHYSICAL_PIN_MAP;
   constant PCB : PIN_MAP_STRING :=
      "PTDI  : P1_3, " &
      "PTDO  : P1_7, " &
      "PTMS  : P1_1, " &
      "PTCK  : P1_11, " &
      "PTRST : P1_2";

   attribute TAP_SCAN_IN    of PTDI : signal is TRUE;
   attribute TAP_SCAN_OUT   of PTDO : signal is TRUE;
   attribute TAP_SCAN_MODE  of PTMS : signal is TRUE;
   attribute TAP_SCAN_CLOCK of PTCK : signal is (1.0e6, both);
   attribute TAP_SCAN_RESET of PTMS : signal is TRUE;

   attribute MEMBERS of LASP_Demo : entity is

--!!Instantiate all of your devices connected to any of P2 – P10
-- one per line in the following form: (uncommented, of course)

--   "your_Un (your_device, your_device_package)," &

--Instantiate all retiming ("pad") bits as discussed in earlier sections.
-- The amoeba entity represents a device with a single cell register in all
-- modes.
-- Such a device can't be described directly in HSDL, much less BSDL.
-- This HSDL was written for and validated by ScanWorks boundary-scan software
-- by ASSET InterTech, which provides the amoeba entity in a prebuilt fashion.
-- For other environments, please discuss the appropriate syntax with your
-- provider.

   "U1_pad0 (amoeba, membrane)," &  -- pad bit local to  U1 s0
   "U1_pad1 (amoeba, membrane)," &  -- pad bit local to  U1 s1
   "U1_pad2 (amoeba, membrane)," &  -- pad bit local to  U1 s2
   "U1_padg (amoeba, membrane)," &  -- pad bit global to U1
   "U2_pad0 (amoeba, membrane)," &  -- pad bit local to  U2 s0
   "U2_pad1 (amoeba, membrane)," &  -- pad bit local to  U2 s1
   "U2_pad2 (amoeba, membrane)," &  -- pad bit local to  U2 s2
   "U2_padg (amoeba, membrane)," &  -- pad bit global to U2
   "U3_pad0 (amoeba, membrane)," &  -- pad bit local to  U3 s0
   "U3_pad1 (amoeba, membrane)," &  -- pad bit local to  U3 s1
   "U3_pad2 (amoeba, membrane)," &  -- pad bit local to  U3 s2
   "U3_padg (amoeba, membrane)";    -- pad bit global to U3

   constant TAP : EXTERNAL_PATH := "PTDI, PTDO, PTCK, PTMS";

   constant short : STATIC_PATH := "";

--!!Change "" to list all devices connected at each "P" connector, respectively

   constant P2  : STATIC_PATH := "";
```

```
      constant P3  : STATIC_PATH := "";
      constant P4  : STATIC_PATH := "";
      constant P5  : STATIC_PATH := "";
      constant P6  : STATIC_PATH := "";
      constant P7  : STATIC_PATH := "";
      constant P8  : STATIC_PATH := "";
      constant P9  : STATIC_PATH := "";
      constant P10 : STATIC_PATH := "";

   --Defines the static path for each LASP secondary that includes the
   single pad bit
   -- required for each STAP connection

      constant P2_p  : STATIC_PATH := "U1_pad0, P2";
      constant P3_p  : STATIC_PATH := "U1_pad1, P3";
      constant P4_p  : STATIC_PATH := "U1_pad2, P4";
      constant P5_p  : STATIC_PATH := "U2_pad0, P5";
      constant P6_p  : STATIC_PATH := "U2_pad1, P6";
      constant P7_p  : STATIC_PATH := "U2_pad2, P7";
      constant P8_p  : STATIC_PATH := "U3_pad0, P8";
      constant P9_p  : STATIC_PATH := "U3_pad1, P9";
      constant P10_p : STATIC_PATH := "U3_pad2, P10";

   --Defines a dynamic path for each LASP STAP so that each STAP can be
   -- on (serially present) or off (serially absent)

      constant U1_s0 : DYNAMIC_PATH :=
        "0 (short:U1_s0, P2_p:1), " &  -- off
        "1 (short:1, P2_p:U1_s0)";     -- on

      constant U1_s1 : DYNAMIC_PATH :=
        "0 (short:U1_s1, P3_p:1), " &  -- off
        "1 (short:1, P3_p:U1_s1)";     -- on

      constant U1_s2 : DYNAMIC_PATH :=
        "0 (short:U1_s2, P4_p:1), " &  -- off
        "1 (short:1, P4_p:U1_s2)";     -- on

      constant U2_s0 : DYNAMIC_PATH :=
        "0 (short:U2_s0, P5_p:1), " &  -- off
        "1 (short:1, P5_p:U2_s0)";     -- on

      constant U2_s1 : DYNAMIC_PATH :=
        "0 (short:U2_s1, P6_p:1), " &  -- off
        "1 (short:1, P6_p:U2_s1)";     -- on

      constant U2_s2 : DYNAMIC_PATH :=
        "0 (short:U2_s2, P7_p:1), " &  -- off
        "1 (short:1, P7_p:U2_s2)";     -- on

      constant U3_s0 : DYNAMIC_PATH :=
        "0 (short:U3_s0, P8_p:1), " &  -- off
        "1 (short:1, P8_p:U3_s0)";     -- on

      constant U3_s1 : DYNAMIC_PATH :=
        "0 (short:U3_s1, P9_p:1), " &  -- off
        "1 (short:1, P9_p:U3_s1)";     -- on

      constant U3_s2 : DYNAMIC_PATH :=
        "0 (short:U3_s2, P10_p:1), " & -- off
        "1 (short:1, P10_p:U3_s2)";    -- on
```

```
--Defines a static path for each LASP that includes 3 STAPs and
-- the global pad bit that must be present for an LASP that is on

   constant U1_p : STATIC_PATH := "U1_s0, U1_s1, U1_s2, U1_padg";

   constant U2_p : STATIC_PATH := "U2_s0, U2_s1, U2_s2, U2_padg";

   constant U3_p : STATIC_PATH := "U3_s0, U3_s1, U3_s2, U3_padg";

--Defines a dynamic path for each LASP so that each can be
-- on (serially present) or off (serially absent)

   constant U1 : DYNAMIC_PATH :=
     "0 (short:U1, U1_p:1), " &  -- off
     "1 (short:1, U1_p:U1)";     -- on

   constant U2 : DYNAMIC_PATH :=
     "0 (short:U2, U2_p:1), " &  -- off
     "1 (short:1, U2_p:U2)";     -- on

   constant U3 : DYNAMIC_PATH :=
     "0 (short:U3, U3_p:1), " &  -- off
     "1 (short:1, U3_p:U3)";     -- on

--Defines the static path on the LASP Demo Board that includes 3 LASP
-- on a multidrop primary TAP

   constant primary : STATIC_PATH :=
     "TAP, U1, U2, U3";

end LASP_Demo;
```

Useful Links

For more information about SVF, BSDL, HSDL, and IEEE Std 1149.1, see the following link:

Testability Primer (Rev.D) – http://focus.ti.com/lit/an/ssya002d/ssya002d.pdf

If you require more in-depth or specific information about a format discussed in this document, please see the following links:

IEEE 1149.1-2001 (JTAG) – IEEE standards – online login required
1149.1-2001 (includes BSDL)
http://standards.ieee.org/reading/ieee/std/testtech/1149.1-2001.pdf

SN74LVT8986, LASP
http://focus.ti.com/docs/prod/folders/print/sn74lvt8986.html
Data sheet
http://focus.ti.com/lit/ds/symlink/sn74lvt8986.pdf

LASP Application Note – Programming CPLDs Via the 'LVT8986 LASP

SVF
SVF specification
http://www.asset-intertech.com/support/svf.html

HSDL
Hierarchical Scan Description Language
http://www.asset-intertech.com/support/hsdl.html

BSDL (IEEE Std 1149.1-2001)
BSDL
http://www.asset-intertech.com/support/bsdl.html

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