Texas Instruments

Digital Logic

Pocket Data Book

2007

SLL

SCYD013B

Digital Logic

Pocket Data Book

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Little Logic

Series	Supply Voltage V_{CC} (V)	Operating Free-air Temperature Ta (℃)
SN74AUP1G	0.8～3.6	–40～85
SN74AUC1G/2G/3G	0.8～2.7	–40～85
SN74LVC1G/2G/3G	1.65～5.5	–40～85
SN74AHC1G	2.0～5.5	–40～85
SN74AHCT1G	4.5～5.5	–40～85

GATE/OCTAL/Widebus™/Widebus+

Series	Supply Voltage V_{CC} (V)	Operating Free-air Temperature Ta (°C)
SN74ABT	4.5～5.5	–40～85
SN64BCT	4.5～5.5	–40～85
SN74BCT SN74F SN74ALS SN74AS	4.5～5.5	0～70
SN74LS SN74S SN74xx(TTL)	4.75～5.25	0～70
SN74AC SN74AC11xxx SN74AHC	2.0～5.5	–40～85
SN74HC	2.0～6.0	–40～85
SN74LV	2.0～5.5	–40～85
SN74LVC	2.0～3.6	–40～85
SN74LVT	2.7～3.6	–40～85
SN74ALVC	1.65～3.6	–40～85
SN74ALVT	2.3～3.6	–40～85
SN74AVC	1.4～3.6	–40～85
SN74AUC	0.8～2.7	–40～85

See **[www.ti.com/sc/logic]** for the most current data sheets.

INDEX

FUNCTION

Translation

Single-Supply Voltage-Translator

Description	Function	Device	CMOS Technology				
			Low-Voltage				Low-Power
			LV	LVC	ALVC	AVC	AUP
Configurable Gate	2-input AND gate	1G57					●
	2-input AND gate with both inputs inverted						
	2-input NOR gate						
	2-input NOR gate with both inputs inverted						
	2-input NAND gate with inverted input						
	2-input OR gate with inverted input						
	2-input XNOR						
	Inverter						
	Noninverted buffer						
	2-input NAND gate	1G58					●
	2-input NAND gate with both inputs inverted						
	2-input OR gate						
	2-input OR gate with both inputs inverted						
	2-input AND gate with inverted input						
	2-input NOR gate with inverted input						
	2-input XNOR						
	Inverter						
	Noninverted buffer						
	2-to-1 data selector	1G97					●
	2-input AND gate						
	2-input AND gate with one inverted input						
	2-input OR gate						
	2-input OR gate with one inverted input						
	2-input NAND gate with one inverted input						
	2-input NOR gate with one inverted input						
	Inverter						
	Noninverted buffer						
	2-to-1 data selector	1G98					●
	2-input AND gate						
	2-input AND gate with one inverted input						
	2-input OR gate						
	2-input OR gate with one inverted input						
	2-input NAND gate with one inverted input						
	2-input NOR gate with one inverted input						
	Inverter						
	Noninverted buffer						

Dual-Supply Bus Transceiver

Description		Device	Technology				
			Low-Voltage CMOS				Low-Power CMOS
			LV	LVC	ALVC	AVC	AUP
Voltage-Translation	Single BusTransceiver	1T45		●		●/H●	
	Dual BusTransceivers	2T45		●		●/H●	
	4-Bit BusTransceivers	4T245				●/H●	
	Octal BusTransceivers	8T245		●		●/H●	
		3245		C●			
		4245		●/C●			
	16-Bit BusTransceivers	16T245		●/H●		●/H●	
		164245			●	A●/AH● B●/BH●	
	20-Bit BusTransceivers	20T245				●/H●	
	24-Bit BusTransceivers	24T245				●/H●	
	32-Bit BusTransceivers	32T245				●/H●	
		324245				B●	

Status ● : Product available in technology indicated * : New product planned in technology indicated

APPLICATION SPECIFIC (CompactFlash™, SD CARD, MultiMediaCards, I²C)

Description	Device	Technology				
		Low-Voltage CMOS				Low-Power CMOS
		LV	LVC	ALVC	AVC	AUP
MMC, SD CARD, Memory Stick, SmartMedia, AND xD-Picture Card ±15-kV ESD VOLTAGE-TRANSLATION TRANSCEIVER	406				A●	
MMC, SD CARD, Memory Stick™ VOLTAGE-TRANSLATION TRANSCEIVER	406L				A●	
LOW-POWER, DUAL-SUPPY, LEVEL-TRANSLATING CompactFlash™ INTERFACE WITH DATA, 11-BIT ADRESS, AND 13BIT CONTROL LINES	4320	●A				

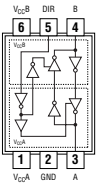
Status ● : Product available in technology indicated * : New product planned in technology indicated

PIN ASSIGNMENTS

Translation

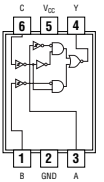
Pin Assignments

1T45
SINGLE-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS



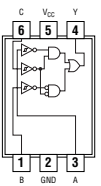
See page 23

1T98
SINGLE-SUPPLY VOLTAGE-LEVEL TRANSLATOR WITH NINE CONFIGURABLE GATE LOGIC FUNCTIONS



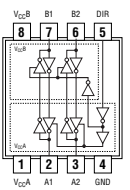
See page 30

1T57
SINGLE-SUPPLY VOLTAGE-LEVEL TRANSLATOR WITH NINE CONFIGURABLE GATE LOGIC FUNCTIONS



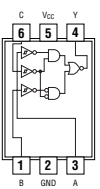
See page 27

2T45
DUAL-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS



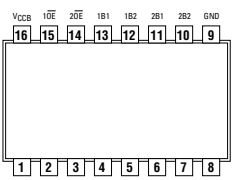
See page 31

1T58
SINGLE-SUPPLY VOLTAGE-LEVEL TRANSLATOR WITH NINE CONFIGURABLE GATE LOGIC FUNCTIONS



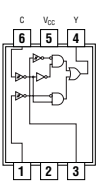
See page 28

4T245
4-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS



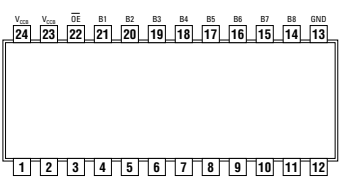
See page 35

1T97
SINGLE-SUPPLY VOLTAGE-LEVEL TRANSLATOR WITH NINE CONFIGURABLE GATE LOGIC FUNCTION



See page 29

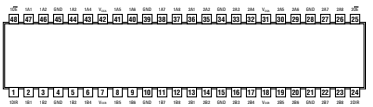
8T245
8-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS



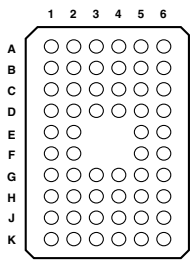
See page 37

16T245

16-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS



GQL OR ZQL PACKAGE
(TOP VIEW)



terminal assignments

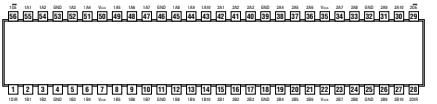
	1	2	3	4	5	6
A	1DIR	NC	NC	NC	NC	$1\overline{OE}$
B	1B2	1B1	GND	GND	1A1	1A2
C	1B4	1B3	V_{CCB}	V_{CCA}	1A3	1A4
D	1B6	1B5	GND	GND	1A5	1A6
E	1B8	1B7			1A7	1A8
F	2B1	2B2			2A2	2A1
G	2B3	2B4	GND	GND	2A4	2A3
H	2B5	2B6	V_{CCB}	V_{CCA}	2A6	2A5
J	2B7	2B8	GND	GND	2A8	2A7
K	2DIR	NC	NC	NC	NC	$2\overline{OE}$

(1) NC - No internal connection

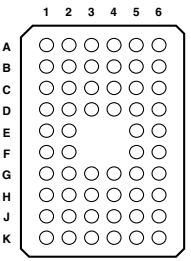
See page 41

20T245

20-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS



GQL OR ZQL PACKAGE
(TOP VIEW)



terminal assignments

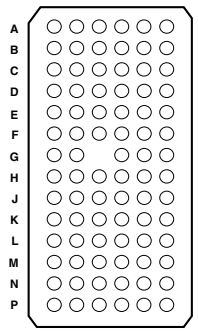
	1	2	3	4	5	6
A	1B1	1B2	1DIR	$1\overline{OE}$	1A2	1A1
B	1B3	1B4	GND	GND	1A4	1A3
C	1B5	1B6	V_{CCB}	V_{CCA}	1A6	1A5
D	1B7	1B8	GND	GND	1A8	1A7
E	1B9	1B10			1A10	1A9
F	2B1	2B2			2A2	2A1
G	2B3	2B4	GND	GND	2A4	2A3
H	2B5	2B6	V_{CCB}	V_{CCA}	2A6	2A5
J	2B7	2B8	GND	GND	2A8	2A7
K	2B9	2B10	2DIR	$2\overline{OE}$	2A10	2A9

See page 45

24T245

24-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

GRG OR ZRG PACKAGE
(TOP VIEW)



terminal assignments

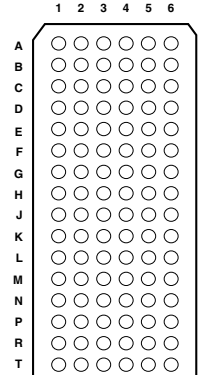
	1	2	3	4	5	6
A	6$\overline{OE}$	5$\overline{OE}$	4$\overline{OE}$	3$\overline{OE}$	2$\overline{OE}$	1$\overline{OE}$
B	1B1	1B2	V_{CCB}	V_{CCA}	1A2	1A1
C	1B3	1B4	GND	GND	1A4	1A3
D	2B1	2B2	V_{CCB}	V_{CCA}	2A2	2A1
E	2B3	2B4	GND	GND	2A4	2A3
F	3B1	3B2	GND	GND	3A2	3A1
G	3B3	3B4		GND	3A4	3A3
H	4B1	4B2	V_{CCB}	V_{CCA}	4A2	4A1
J	4B3	4B4	GND	GND	4A4	4A3
K	5B1	5B2	GND	GND	5A2	5A1
L	5B3	5B4	V_{CCB}	V_{CCA}	5A4	5A3
M	6B1	6B2	GND	GND	6A2	6A1
N	6B3	6B4	V_{CCB}	V_{CCA}	6A4	6A3
P	6DIR	5DIR	4DIR	3DIR	2DIR	1DIR

See page 47

32T245

32-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS WITH 3-STATE DESELECTED OUTPUT

GRG OR ZRG PACKAGE
(TOP VIEW)



terminal assignments

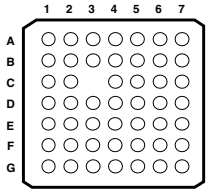
	1	2	3	4	5	6
A	1B2	1B1	1DIR	1$\overline{OE}$	1A1	1A2
B	1B4	1B3	GND	GND	1A3	1A4
C	1B6	1B5	V_{CCB}	V_{CCA}	1A5	1A6
D	1B8	1B7	GND	GND	1A7	1A8
E	2B2	2B1	GND	GND	2A1	2A2
F	2B4	2B3	V_{CCB}	V_{CCA}	2A3	2A4
G	2B6	2B5	GND	GND	2A5	2A6
H	2B7	2B8	2DIR	2$\overline{OE}$	2A8	2A7
J	3B2	3B1	3DIR	3$\overline{OE}$	3A1	3A2
K	3B4	3B3	GND	GND	3A3	3A4
L	3B6	3B5	V_{CCB}	V_{CCA}	3A5	3A6
M	3B8	3B7	GND	GND	3A7	3A8
N	4B2	4B1	GND	GND	4A1	4A2
P	4B4	4B3	V_{CCB}	V_{CCA}	4A3	4A4
R	4B6	4B5	GND	GND	4A5	4A6
T	4B7	4B8	4DIR	4$\overline{OE}$	4A8	4A7

See page 50

406

MMC, SD CARD, Memory Stick, SmartMedia, AND xD-Picture Card ±15-kV ESD-PROTECTED VOLTAGE-TRANSLATION TRANCEIVER

GQC/ZQC PACKAGE
(TOP VIEW)



TERMINAL ASSIGNMENTS (1)

	1	2	3	4	5	6	7
A	V_{CCA}	2A	4DIR	2DIR	MODE1	10B1	V_{CCB0}
B	10A1	3A	1A	1DIR	MODE0	9B1	1B
C	9A	10A2		3DIR	GND	2B	3B
D	9DIR	4A	56DIR	GND	4B	11B	12B
E	78DIR	6A	GND	$\overline{CS0}$	GND	10B2	9B2
F	7A	8A	12A	13A	7B	5B	14B
G	V_{CCA}	5A	11A	$\overline{CS1}$	8B	6B	V_{CCB1}

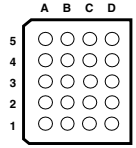
(1) V_{CCA} powers all A-port I/Os and control inputs.
V_{CCB0} powers 1B, 2B, 3B, 4B, 9B1, and 10B1.
V_{CCB1} powers 5B, 6B, 7B, 8B, 9B2, 10B2, 11B, 12B, and 14B.

See page 53

406L

MMC, SD CARD, Memory Stick, SmartMedia, AND xD-Picture Card ±15-kV ESD-PROTECTED VOLTAGE-TRANSLATION TRANCEIVER

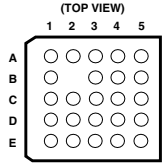
GXY OR ZXY PACKAGE
(TOP VIEW)



TERMINAL ASSIGNMENTS
(20-Ball GXY/ZXY Package)

	A	B	C	D
5	V_{CCA}	CMD-dir	DAT0-dir	V_{CCB}
4	DAT3A	DAT2A	DAT2B	DAT3B
3	CLKA	GND	GND	CLKB
2	DAT1A	DAT0A	CMDB	DAT0B
1	CLK-f	CMDA	DAT123-dir	DAT1B

GQS OR ZQS PACKAGE
(TOP VIEW)



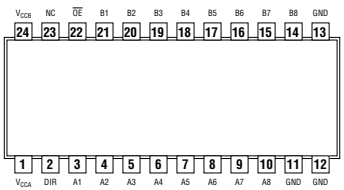
TERMINAL ASSIGNMENTS
(24-Ball GQS/ZQS Package)

	1	2	3	4	5
A	DAT2A	CMD-dir	DAT0-dir	RSV	DAT2B
B	DAT3A		V_{CCA}	V_{CCB}	DAT3B
C	CLKA	RSV	GND	GND	CLKB
D	DAT0A	CMDA	RSV	CMDB	DAT0B
E	DAT1A	CLK-f	DAT123-dir	RSV	DAT1B

See page 58

3245

OCTAL BUS TRANSCEIVER WITH ADJUSTABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS

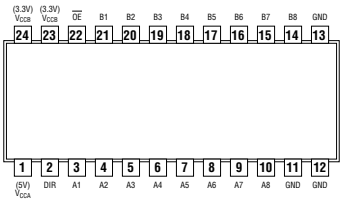


See page 61

4245

OCTAL BUS TRANSCEIVER AND 3.3-V TO 5-V SHIFTER WITH 3-STATE OUTPUTS (SN74LVC4245A)

OCTAL DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS (SN74LVCC4245A)

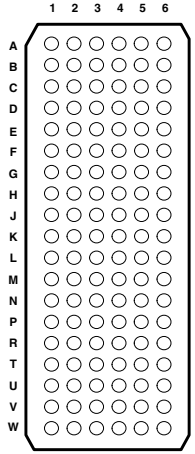


See page 62

4320

LOW-POWER, DUAL-SUPPLY, LEVEL-TRANSLATING CompactFlash™ INTERFACE WITH 16-BIT DATA, 11-BIT ADDRESS, AND 13-BIT CONTROL LINES

GKF PACKAGE
(TOP VIEW)



terminal assignments

	1	2	3	4	5	6
A	D12	D04	D03	SD14	SD12	SD11
B	D13	D05	D11	SD13	SD10	SD09
C	D14	D06	SD15	$\overline{\text{SINPACK}}$	SD08	SD07
D	D15	D07	VCC_CF	VCC_S	SD06	SD05
E	$\overline{\text{CE2}}$	$\overline{\text{CE1}}$	GND	GND	SD04	SD03
F	$\overline{\text{OE}}$	A10	VCC_CF	VCC_S	SD02	SD01
G	A09	$\overline{\text{IORD}}$	GND	GND	SD00	$\overline{\text{SCE1}}$
H	A08	$\overline{\text{IOWR}}$	VCC_CF	VCC_S	$\overline{\text{EN\_L}}$	$\overline{\text{EN\_H}}$
J	A07	$\overline{\text{WE}}$	GND	GND	MASTER_EN	$\overline{\text{BUF\_EN}}$
K	A06	READY	A05	$\overline{\text{SCE2}}$	$\overline{\text{SOE}}$	$\overline{\text{SIORD}}$
L	A04	RESET	GND	GND	$\overline{\text{SWE}}$	$\overline{\text{SIOWR}}$
M	A03	$\overline{\text{WAIT}}$	VCC_CF	VCC_S	SREADY	SRESET
N	A02	$\overline{\text{INPACK}}$	GND	GND	$\overline{\text{SWAIT}}$	$\overline{\text{SREG}}$
P	A01	$\overline{\text{REG}}$	VCC_CF	GND	SBVD2	SBVD1
R	A00	BVD2	VCC_CF	VCC_S	SA10	SWP
T	D00	BVD1	VCC_SD	DIR ($\overline{\text{S}}$/CF)	SA08	SA09
U	D01	D08	$\overline{\text{CD1}}$	DIR_OUT	SA06	SA07
V	D02	D09	$\overline{\text{CD2}}$	SA00	SA04	SA05
W	WP	D10	$\overline{\text{SCD}}$	SA01	SA02	SA03

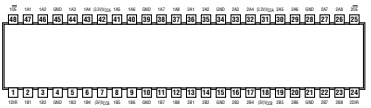
See page 63

164245

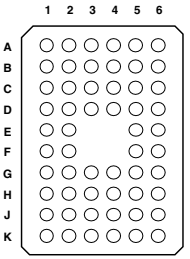
16-BIT TRANSCEIVER AND 3.3-V TO 5-V SHIFTER WITH 3-STATE OUTPUTS

- SN74ALVC164245:
  A port has V_{CCA}, which is set to operate at 2.5 V and 3.3 V
  B port has V_{CCB}, which is set to operate at 3.3 V and 5 V
- SN74AVCB164245, SN74AVCBH164245:
  The A-port is designed to track V_{CCA},
  V_{CCA} accepts any supply voltage
  from 1.4 V to 3.6 V

  The B-port is designed to track V_{CCB},
  V_{CCB} accepts any supply voltage
  from 1.4 V to 3.6 V



GQL OR ZQL PACKAGE
(TOP VIEW)



TERMINAL ASSIGNMENTS (1)

	1	2	3	4	5	6
A	1DIR	NC	NC	NC	NC	1$\overline{OE}$
B	1B2	1B1	GND	GND	1A1	1A2
C	1B4	1B3	V_{CCB}	V_{CCA}	1A3	1A4
D	1B6	1B5	GND	GND	1A5	1A6
E	1B8	1B7			1A7	1A8
F	2B1	2B2			2A2	2A1
G	2B3	2B4	GND	GND	2A4	2A3
H	2B5	2B6	V_{CCB}	V_{CCA}	2A6	2A5
J	2B7	2B8	GND	GND	2A8	2A7
K	2DIR	NC	NC	NC	NC	2$\overline{OE}$

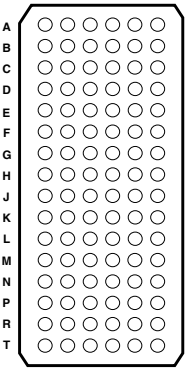
(1) NC - No internal connection

See page 67

324245

32-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

GKE PACKAGE
(TOP VIEW)



terminal assignments

	1	2	3	4	5	6
A	1B2	1B1	1DIR	1$\overline{OE}$	1A1	1A2
B	1B4	1B3	GND	GND	1A3	1A4
C	1B6	1B5	V_{CCB}	V_{CCA}	1A5	1A6
D	1B8	1B7	GND	GND	1A7	1A8
E	2B2	2B1	GND	GND	2A1	2A2
F	2B4	2B3	V_{CCB}	V_{CCA}	2A3	2A4
G	2B6	2B5	GND	GND	2A5	2A6
H	2B7	2B8	2DIR	2$\overline{OE}$	2A8	2A7
J	3B2	3B1	3DIR	3$\overline{OE}$	3A1	3A2
K	3B4	3B3	GND	GND	3A3	3A4
L	3B6	3B5	V_{CCB}	V_{CCA}	3A5	3A6
M	3B8	3B7	GND	GND	3A7	3A8
N	4B2	4B1	GND	GND	4A1	4A2
P	4B4	4B3	V_{CCB}	V_{CCA}	4A3	4A4
R	4B6	4B5	GND	GND	4A5	4A6
T	4B7	4B8	4DIR	4$\overline{OE}$	4A8	4A7

See page 69

FUNCTION AND ELECTRICAL CHARACTERISTICS

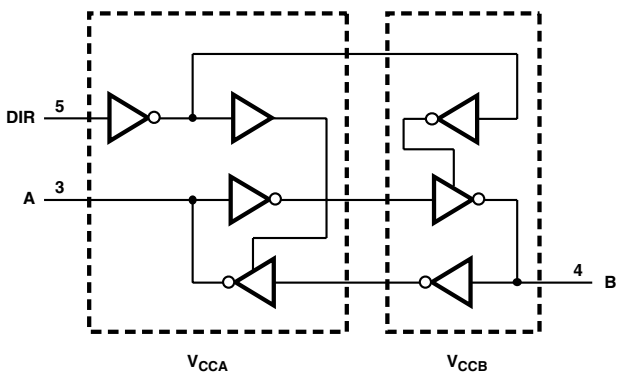
Translation

1T45

SINGLE-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

- V_{CC} Isolation Feature - If Either V_{CC} Input Is at GND, Both Ports Are in the High-Impedance State
- DIR Input Circuit Referenced to V_{CCA}
- This Single-Bit Noninverting Bus Transceiver Uses Two Separate Configurable Power-Supply Rails
- Designed for asynchronous Communication Between Two Data Buses

Logic Diagram



FUNCTION TABLE (1)

INPUT DIR	OPERATION
L	B data to A bus
H	A data to B bus

(1) Input circuits of the data I/Os always are active.

RECOMMENDED OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTECS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V	UNIT
I_{CC}*	MAX	0.004	0.004	0.004	0.004	0.02	0.02	0.02	0.02	0.02	0.02	0.02	0.02	mA
I_{OH}	MAX	-32	-24	-8	-4	-12	-9	-8	-6	-12	-9	-8	-6	mA
I_{OL}	MAX	32	24	8	4	12	9	8	6	12	9	8	6	mA

*$I_{CCA} + I_{CCB}$

SWITCHING CHARACTERISTICS

V_{CCA} = 1.5V												
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
t_{PLH}	A	B	MAX	3.3	4.2	5.2	5.6	3.3	4.2	5.2	5.6
t_{PHL}				3.8	4.2	5.2	5.6	3.8	4.2	5.2	5.6
t_{PLH}	B	A	MAX	4.8	4.9	5.3	5.5	4.8	4.9	5.3	5.5
t_{PHL}				4.8	4.9	5.3	5.5	4.8	4.9	5.3	5.5
t_{PHZ}	DIR	A	MAX	6.9	6.9	6.8	6.7	6.9	6.9	6.8	6.7
t_{PLZ}				6.9	6.9	6.8	6.7	6.9	6.9	6.8	6.7
t_{PHZ}	DIR	B	MAX	4.5	4.7	7.1	8.1	4.5	4.7	7.1	8.1
t_{PLZ}				4.5	4.7	7.1	8.1	4.5	4.7	7.1	8.1
t_{PZH}*	DIR	A	MAX	9.3	9.6	12.4	13.6	9.3	9.6	12.4	13.6
t_{PZL}*				9.3	9.6	12.4	13.6	9.3	9.6	12.4	13.6
t_{PZH}*	DIR	B	MAX	10.7	11.1	12	12.3	10.7	11.1	12	12.3
t_{PZL}*				10.7	11.1	12	12.3	10.7	11.1	12	12.3

UNIT : ns *The enable time is a calculated value, derived using the formula shown in the enable times section.

V_{CCA} = 1.8V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V
t_{PLH}	A	B	MAX	7.2	8.3	10.3	17.7	3.4	3.9	5	5.3
t_{PHL}				7	7.1	8.5	14.3	3.4	3.9	5	5.3
t_{PLH}	B	A	MAX	15.1	15.5	16	17.7	4.4	4.6	5	5.2
t_{PHL}				12.2	12.6	12.9	14.3	4.4	4.6	5	5.2
t_{PHZ}	DIR	A	MAX	17.1	18.4	18.5	19.4	6	5.9	5.9	5.9
t_{PLZ}				10.9	10.7	10.5	10.5	6	5.9	5.9	5.9
t_{PHZ}	DIR	B	MAX	8.2	10.3	11.5	21.9	5.3	4.4	6.8	7.7
t_{PLZ}				6.4	8.4	9.2	16	5.3	4.4	6.8	7.7
t_{PZH}*	DIR	A	MAX	12.8	23.9	25.2	33.7	8.7	9	11.8	12.9
t_{PZL}*				13.3	22.9	24.4	36.2	8.7	9	11.8	12.9
t_{PZH}*	DIR	B	MAX	10.9	19	20.8	28.2	9.4	9.8	10.9	11.2
t_{PZL}*				12.7	25.5	27	33.7	9.4	9.8	10.9	11.2

V_{CCA} = 1.8V							
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
t_{PLH}	A	B	MAX	3.4	3.9	5	5.3
t_{PHL}				3.4	3.9	5	5.3
t_{PLH}	B	A	MAX	4.4	4.6	5	5.2
t_{PHL}				4.4	4.6	5	5.2
t_{PHZ}	DIR	A	MAX	6	5.9	5.9	5.9
t_{PLZ}				6	5.9	5.9	5.9
t_{PHZ}	DIR	B	MAX	5.3	4.4	6.8	7.7
t_{PLZ}				5.3	4.4	6.8	7.7
t_{PZH}*	DIR	A	MAX	8.7	9	11.8	12.9
t_{PZL}*				8.7	9	11.8	12.9
t_{PZH}*	DIR	B	MAX	9.4	9.8	10.9	11.2
t_{PZL}*				9.4	9.8	10.9	11.2

UNIT : ns *The enable time is a calculated value, derived using the formula shown in the enable times section.

: **PREVIEW**

V_{CCA} = 2.5V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V
t_{PLH}	A	B	MAX	5.1	6.4	8.5	16	3	3.4	4.6	4.9
t_{PHL}				4.6	5.4	7.5	12.9	3	3.4	4.6	4.9
t_{PLH}	B	A	MAX	7.5	8	8.5	10.3	3.3	3.4	3.8	4.2
t_{PHL}				6.2	7	7.5	8.5	3.3	3.4	3.8	4.2
t_{PHZ}	DIR	A	MAX	8.1	8.1	8.1	8.1	3.8	3.8	3.8	3.8
t_{PLZ}				5.8	5.9	5.9	5.9	3.8	3.8	3.8	3.8
t_{PHZ}	DIR	B	MAX	7.1	10.2	11.4	23.7	4	4.1	6.5	7.6
t_{PLZ}				5.3	8.4	9.6	18.9	4	4.1	6.5	7.6
t_{PZH}*	DIR	A	MAX	12.8	16.4	18.1	29.2	7.3	7.5	10.3	11.8
t_{PZL}*				13.3	17.2	18.9	32.2	7.3	7.5	10.3	11.8
t_{PZH}*	DIR	B	MAX	10.9	12.3	14.4	21.9	6.6	7	8.1	8.6
t_{PZL}*				12.7	13.5	15.6	21	6.6	7	8.1	8.6

V_{CCA} = 2.5V							
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
t_{PLH}	A	B	MAX	3	3.4	4.6	4.9
t_{PHL}				3	3.4	4.6	4.9
t_{PLH}	B	A	MAX	3.3	3.4	3.8	4.2
t_{PHL}				3.3	3.4	3.8	4.2
t_{PHZ}	DIR	A	MAX	3.8	3.8	3.8	3.8
t_{PLZ}				3.8	3.8	3.8	3.8
t_{PHZ}	DIR	B	MAX	4	4.1	6.5	7.6
t_{PLZ}				4	4.1	6.5	7.6
t_{PZH}*	DIR	A	MAX	7.3	7.5	10.3	11.8
t_{PZL}*				7.3	7.5	10.3	11.8
t_{PZH}*	DIR	B	MAX	6.6	7	8.1	8.6
t_{PZL}*				6.6	7	8.1	8.6

UNIT : ns

*The enable time is a calculated value, derived using the formula shown in the enable times section.

V_{CCA} = 3.3V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V
t_{PLH}	A	B	MAX	4.4	5.8	8	15.5	2.8	3.3	4.4	4.7
t_{PHL}				4	5	7	12.6	2.8	3.3	4.4	4.7
t_{PLH}	B	A	MAX	5.4	5.8	6.4	8.3	2.8	3	3.4	3.8
t_{PHL}				4.5	5	5.4	7.1	2,8	3	3.4	3.8
t_{PHZ}	DIR	A	MAX	7.3	7.3	7.3	7.3	4.3	4.3	4.3	4.3
t_{PLZ}				5.7	5.7	5.6	5.6	4.3	4.3	4.3	4.3
t_{PHZ}	DIR	B	MAX	6.8	8.8	10.1	20.5	4.9	4	6.5	7.4
t_{PLZ}				4.9	7.1	7.8	14.5	4.9	4	6.5	7.4
t_{PZH}*	DIR	A	MAX	10.3	12.9	14.2	22.8	6.7	7	9.9	11.2
t_{PZL}*				11.3	13.8	15.5	27.6	6.7	7	9.9	11.2
t_{PZH}*	DIR	B	MAX	10.1	11.5	13.6	21.1	6.8	7.2	8.5	8.9
t_{PZL}*				11.3	12.3	14.3	19.9	6.8	7.2	8.5	8.9

V_{CCA} = 3.3V							
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
t_{PLH}	A	B	MAX	2.8	3.3	4.4	4.7
t_{PHL}				2.8	3.3	4.4	4.7
t_{PLH}	B	A	MAX	2.8	3	3.4	3.8
t_{PHL}				2,8	3	3.4	3.8
t_{PHZ}	DIR	A	MAX	4.3	4.3	4.3	4.3
t_{PLZ}				4.3	4.3	4.3	4.3
t_{PHZ}	DIR	B	MAX	4.9	4	6.5	7.4
t_{PLZ}				4.9	4	6.5	7.4
t_{PZH}*	DIR	A	MAX	6.7	7	9.9	11.2
t_{PZL}*				6.7	7	9.9	11.2
t_{PZH}*	DIR	B	MAX	6.8	7.2	8.5	8.9
t_{PZL}*				6.8	7.2	8.5	8.9

UNIT : ns

*The enable time is a calculated value, derived using the formula shown in the enable times section.

V_{CCA} = 5.0V							
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t_{PLH}	A	B	MAX	3.9	5.4	7.5	15.1
t_{PHL}				3.5	4.5	6.2	12.2
t_{PLH}	B	A	MAX	3.9	4.4	5.1	7.2
t_{PHL}				3.5	4	4.6	7
t_{PHZ}	DIR	A	MAX	5.4	5.5	5.4	5.4
t_{PLZ}				3.7	3.7	3.8	3.8
t_{PHZ}	DIR	B	MAX	6.5	8.5	9.8	20.2
t_{PLZ}				4.5	7	7.4	14.8
t_{PZH}*	DIR	A	MAX	8.4	11.4	12.5	22
t_{PZL}*				10	12.5	14.4	27.2
t_{PZH}*	DIR	B	MAX	7.6	9.1	11.3	18.9
t_{PZL}*				8.6	10	11.6	17.6

UNIT : ns

*The enable time is a calculated value, derived using the formula shown in the enable times section.

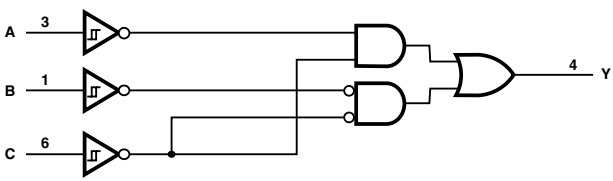
: **PREVIEW**

1T57

SINGLE-SUPPLY VOLTAGE-LEVEL TRANSLATOR WITH NINE CONFIGURABLE GATE LOGIC FUNCTIONS

- Single-Supply Voltage Translator
- Nine Configurable Gate Logic Functions
- Scmitt-Trigger Inputs Reject Input Noise and Provide Better Output Signal Integrity

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT
C	B	A	Y
L	L	L	H
L	L	H	L
L	H	L	H
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	H
H	H	H	H

FUNCTION SELECTION TABLE

LOGIC FUNCTION
2-input AND gate
2-input NOR gate with both inputs inverted
2-input NAND gate with inverted input
2-input OR gate with inverted input
2-input AND gate with both inputs inverted
2-input NOR gate
2-input XNOR gate
Inverter
Noninverted buffer

RECOMMENDED OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTECS

PARAMETER	MAX or MIN	AUP 3.3V	AUP 2.5V	UNIT
I_{CC}	MAX	0.0009	0.0009	mA
I_{OH}	MAX	-4	-3.1	mA
I_{OL}	MAX	4	3.1	mA

SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	AUP 3.3V	AUP 2.5V
t_{PLH}	V_I = 1.8V	A, B, or C	Y	MAX	8.5	7.9
t_{PHL}					8.5	7.9
t_{PLH}	V_I = 2.5V	A, B, or C	Y	MAX	6.1	7.1
t_{PHL}					6.1	7.1

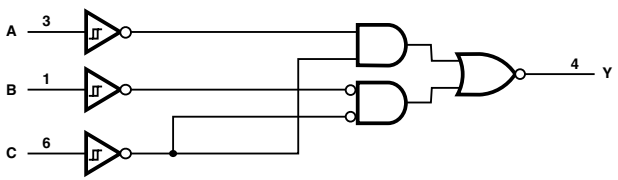
UNIT : ns

1T58

SINGLE-SUPPLY VOLTAGE-LEVEL TRANSLATOR WITH NINE CONFIGURABLE GATE LOGIC FUNCTIONS

- Single-Supply Voltage Translator
- Nine Configurable Gate Logic Functions
- Scmitt-Trigger Inputs Reject Input Noise and Provide Better Output Signal Integrity

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT
C	B	A	Y
L	L	L	L
L	L	H	H
L	H	L	L
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	L
H	H	H	L

FUNCTION SELECTION TABLE

LOGIC FUNCTION
2-input NAND gate
2-input OR gate with both inputs inverted
2-input AND gate with inverted input
2-input NOR gate with inverted input
2-input NAND gate with both inputs inverted
2-input OR gate
2-input XOR gate
Inverter
Noninverted buffer

RECOMMENDED OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTECS

PARAMETER	MAX or MIN	AUP 3.3V	AUP 2.5V	UNIT
I_{CC}	MAX	0.0009	0.0009	mA
I_{OH}	MAX	-4	-3.1	mA
I_{OL}	MAX	4	3.1	mA

SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	AUP 3.3V	AUP 2.5V
t_{PLH}	V_I = 1.8V	A, B, or C	Y	MAX	8.5	7.9
t_{PHL}					8.5	7.9
t_{PLH}	V_I = 2.5V	A, B, or C	Y	MAX	6.1	7.1
t_{PHL}					6.1	7.1

UNIT : ns

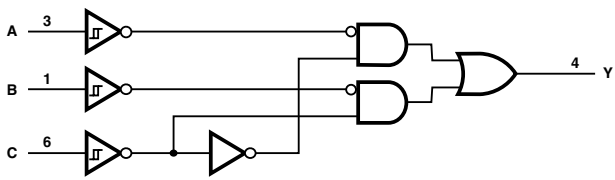
: **PREVIEW**

1T97

SINGLE-SUPPLY VOLTAGE-LEVEL TRANSLATOR WITH NINE CONFIGURABLE GATE LOGIC FUNCTION

- Single-Supply Voltage Translator
- Nine Configurable Gate Logic Functions
- Scmitt-Trigger Inputs Reject Input Noise and Provide Better Output Signal Integrity

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT
C	B	A	Y
L	L	L	L
L	L	H	L
L	H	L	H
L	H	H	H
H	L	L	L
H	L	H	H
H	H	L	L
H	H	H	H

FUNCTION SELECTION TABLE

LOGIC FUNCTION
2-to-1 data selector
2-input AND gate
2-input OR gate with one inverted input
2-input NAND gate with one inverted input
2-input AND gate with one inverted input
2-input NOR gate with one inverted input
2-input OR gate
Inverter
Noninverted buffer

RECOMMENDED OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTECS

PARAMETER	MAX or MIN	AUP 3.3V	AUP 2.5V	UNIT
I_{CC}	MAX	0.0009	0.0009	mA
I_{OH}	MAX	-4	-3.1	mA
I_{OL}	MAX	4	3.1	mA

SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	AUP 3.3V	AUP 2.5V
t_{PLH}	V_I = 1.8V	A, B, or C	Y	MAX	8.5	7.9
t_{PHL}					8.5	7.9
t_{PLH}	V_I = 2.5V	A, B, or C	Y	MAX	6.1	7.1
t_{PHL}					6.1	7.1
t_{PLH}	V_I = 3.3V	A, B, or C	Y	MAX	5.7	6.5
t_{PHL}					5.7	6.5

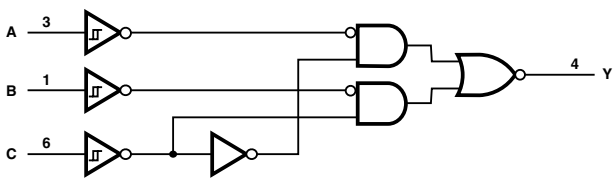
UNIT : ns

1T98

SINGLE-SUPPLY VOLTAGE-LEVEL TRANSLATOR WITH NINE CONFIGURABLE GATE LOGIC FUNCTIONS

- Single-Supply Voltage Translator
- Nine Configurable Gate Logic Functions
- Scmitt-Trigger Inputs Reject Input Noise and Provide Better Output Signal Integrity

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT
C	B	A	Y
L	L	L	H
L	L	H	H
L	H	L	L
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	H
H	H	H	L

FUNCTION SELECTION TABLE

LOGIC FUNCTION
2-to-1 data selector
2-input AND gate
2-input OR gate with one inverted input
2-input NAND gate with one inverted input
2-input AND gate with one inverted input
2-input NOR gate with one inverted input
2-input OR gate
Inverter
Noninverted buffer

RECOMMENDED OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTECS

PARAMETER	MAX or MIN	AUP 3.3V	AUP 2.5V	UNIT
I_{CC}	MAX	0.0009	0.0009	mA
I_{OH}	MAX	-4	-3.1	mA
I_{OL}	MAX	4	3.1	mA

SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	AUP 3.3V	AUP 2.5V
t_{PLH}	V_I = 1.8V	A, B, or C	Y	MAX	8.5	7.9
t_{PHL}					8.5	7.9
t_{PLH}	V_I = 2.5V	A, B, or C	Y	MAX	6.1	7.1
t_{PHL}					6.1	7.1
t_{PLH}	V_I = 3.3V	A, B, or C	Y	MAX	5.7	6.5
t_{PHL}					5.7	6.5

UNIT : ns

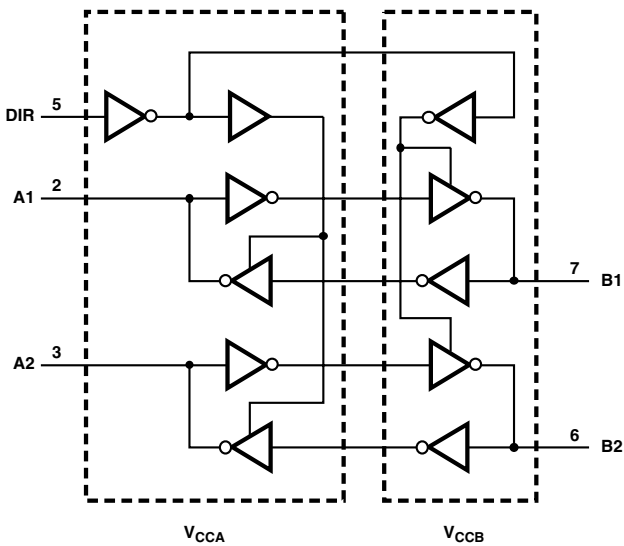
: **PREVIEW**

2T45

DUAL-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

- Control Inputs V_{IH}/V_{IL} Levels Are Referenced to V_{CCA} Voltage
- This Dual-Bit Noninverting Bus Transceiver Uses Two Separate Configurable Power-Supply Rails
- Designed for asynchronous Communication Between Two Data Buses

Logic Diagram



FUNCTION TABLE (1)
(each transceiver)

INPUT DIR	OPERATION
L	B data to A bus
H	A data to B bus

(1) Input circuits of the data I/Os always are active.

RECOMMENDED OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTECS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V	UNIT
I_{CC}*	MAX	0.004	0.004	0.004	0.004	0.02	0.02	0.02	0.02	0.02	0.02	0.02	0.02	mA
I_{OH}	MAX	-32	-24	-8	-4	-12	-9	-8	-6	-12	-9	-8	-6	mA
I_{OL}	MAX	32	24	8	4	12	9	8	6	12	9	8	6	mA

*I_{CCA} + I_{CCB}

SWITCHING CHARACTERISTICS

V_{CCA} = 1.5V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
t_{PLH}	A	B	MAX	3.5	3.7	4.6	5.4	3.5	3.7	4.6	5.4
t_{PHL}				3.5	3.7	4.6	5.4	3.5	3.7	4.6	5.4
t_{PLH}	B	A	MAX	4.7	4.9	5.2	5.4	4.7	4.9	5.2	5.4
t_{PHL}				4.7	4.9	5.2	5.4	4.7	4.9	5.2	5.4
t_{PHZ}	DIR	A	MAX	7.6	7.7	7.8	8.5	4.6	5.5	7.1	8.5
t_{PLZ}				7.6	7.7	7.8	8.5	4.6	5.5	7.1	8.5
t_{PHZ}	DIR	B	MAX	7.1	6.9	6.9	7	7.1	6.9	6.9	7
t_{PLZ}				7.1	6.9	6.9	7	7.1	6.9	6.9	7
t_{PZH}*	DIR	A	MAX	11.8	11.8	12.1	12.4	11.8	11.8	12.1	12.4
t_{PZL}*				11.8	11.8	12.1	12.4	11.8	11.8	12.1	12.4
t_{PZH}*	DIR	B	MAX	7.8	9.1	11.6	13.9	7.8	9.1	11.6	13.9
t_{PZL}*				7.8	9.1	11.6	13.9	7.8	9.1	11.6	13.9

UNIT : ns

*The enable time is a calculated value, derived using the formula shown in the enable times section.

V_{CCA} = 1.8V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V
t_{PLH}	A	B	MAX	7.2	8.3	10.3	17.7	3.1	3.4	4.3	5.2
t_{PHL}				7	7.1	8.5	14.3	3.1	3.4	4.3	5.2
t_{PLH}	B	A	MAX	15.1	15.5	16	17.7	3.8	4	4.4	4.7
t_{PHL}				12.2	12.6	12.9	14.3	3.8	4	4.4	4.7
t_{PHZ}	DIR	A	MAX	29.3	30.5	30.5	30.9	5.2	5.3	6.9	8.1
t_{PLZ}				19.4	19.5	19.6	19.7	5.2	5.3	6.9	8.1
t_{PHZ}	DIR	B	MAX	8.6	11.3	14.9	27.9	5.9	5.7	5.9	5.8
t_{PLZ}				7.1	9.7	12.6	19.5	5.9	5.7	5.9	5.8
t_{PZH}*	DIR	A	MAX	22.2	25.2	28.6	37.2	9.7	9.7	10.3	10.4
t_{PZL}*				20.8	23.9	27.8	42.2	9.7	9.7	10.3	10.4
t_{PZH}*	DIR	B	MAX	26.6	27.8	29.9	37.4	8.3	8.6	11.2	13.3
t_{PZL}*				36.3	37.6	39	45.2	8.3	8.6	11.2	13.3

V_{CCA} = 1.8V							
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
t_{PLH}	A	B	MAX	3.1	3.4	4.3	5.2
t_{PHL}				3.1	3.4	4.3	5.2
t_{PLH}	B	A	MAX	3.8	4	4.4	4.7
t_{PHL}				3.8	4	4.4	4.7
t_{PHZ}	DIR	A	MAX	4.5	5.3	6.9	8.1
t_{PLZ}				4.5	5.3	6.9	8.1
t_{PHZ}	DIR	B	MAX	5.9	5.7	5.9	5.8
t_{PLZ}				5.9	5.7	5.9	5.8
t_{PZH}*	DIR	A	MAX	9.7	9.7	10.3	10.4
t_{PZL}*				9.7	9.7	10.3	10.4
t_{PZH}*	DIR	B	MAX	7.4	8.6	11.2	13.3
t_{PZL}*				7.4	8.6	11.2	13.3

UNIT : ns

*The enable time is a calculated value, derived using the formula shown in the enable times section.

V_{CCA} = 2.5V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V
t_{PLH}	A	B	MAX	5.1	6.4	8.5	16	2.6	3	4	4.9
t_{PHL}				4.6	5.4	7.5	12.9	2.6	3	4	4.9
t_{PLH}	B	A	MAX	7.5	8	8.5	10.3	2.8	3	3.4	3.8
t_{PHL}				6.2	7	7.5	8.5	2.8	3	3.4	3.8
t_{PHZ}	DIR	A	MAX	16.5	16.8	16.8	17.1	4.3	5	6.4	7.9
t_{PLZ}				12.3	12.3	12.5	12.6	4.3	5	6.4	7.9
t_{PHZ}	DIR	B	MAX	7.6	10.5	13.9	27.9	4.1	4.2	4.3	4.3
t_{PLZ}				6.2	8.9	11.2	18.9	4.1	4.2	4.3	4.3
t_{PZH}*	DIR	A	MAX	13.7	16.9	19.7	29.2	6.9	7.2	7.7	7.9
t_{PZL}*				13.8	17.5	21.4	36.4	6.9	7.2	7.7	7.9
t_{PZH}*	DIR	B	MAX	17.4	18.7	21	28.6	6.8	7.9	10.4	12.8
t_{PZL}*				21.1	22.2	24.3	30	6.8	7.9	10.4	12.8

V_{CCA} = 2.5V							
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
t_{PLH}	A	B	MAX	2.6	3	4	4.9
t_{PHL}				2.6	3	4	4.9
t_{PLH}	B	A	MAX	2.8	3	3.4	3.8
t_{PHL}				2.8	3	3.4	3.8
t_{PHZ}	DIR	A	MAX	4.3	5	6.4	7.9
t_{PLZ}				4.3	5	6.4	7.9
t_{PHZ}	DIR	B	MAX	4.1	4.2	4.3	4.3
t_{PLZ}				4.1	4.2	4.3	4.3
t_{PZH}*	DIR	A	MAX	6.9	7.2	7.7	7.9
t_{PZL}*				6.9	7.2	7.7	7.9
t_{PZH}*	DIR	B	MAX	6.8	7.9	10.4	12.8
t_{PZL}*				6.8	7.9	10.4	12.8

UNIT : ns *The enable time is a calculated value, derived using the formula shown in the enable times section.

V_{CCA} = 3.3V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V
t_{PLH}	A	B	MAX	4.4	5.8	8	15.5	2.4	2.8	3.8	4.7
t_{PHL}				4	5	7	12.6	2.4	2,8	3.8	4.7
t_{PLH}	B	A	MAX	5.4	5.8	6.4	8.3	2.4	2.6	3.1	3.6
t_{PHL}				4.5	5	5.4	7.1	2.4	2.6	3.1	3.6
t_{PHZ}	DIR	A	MAX	10.4	10.8	10.8	10.9	4	4.7	6.5	8
t_{PLZ}				7.8	8.1	8.4	8.4	4	4.7	6.5	8
t_{PHZ}	DIR	B	MAX	7.4	10.4	13.7	27.3	4.2	4.6	5.6	6.6
t_{PLZ}				5.6	8.3	11.3	17.7	4.2	4.6	5.6	6.6
t_{PZH}*	DIR	A	MAX	11	14.1	17.7	26	6.6	6.2	6.6	6.9
t_{PZL}*				11.9	15.4	19.1	34.4	6.6	6.2	6.6	6.9
t_{PZH}*	DIR	B	MAX	12.2	13.9	16.4	23.9	6.3	7.4	10.3	12.7
t_{PZL}*				14.4	15.8	17.8	23.5	6.3	7.4	10.3	12.7

V_{CCA} = 3.3V							
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
t_{PLH}	A	B	MAX	2.4	2.8	3.8	4.7
t_{PHL}				2.4	2,8	3.8	4.7
t_{PLH}	B	A	MAX	2.4	2.6	3.1	3.6
t_{PHL}				2.4	2.6	3.1	3.6
t_{PHZ}	DIR	A	MAX	4	4.7	6.5	8
t_{PLZ}				4	4.7	6.5	8
t_{PHZ}	DIR	B	MAX	3.5	4.6	5.6	6.6
t_{PLZ}				3.5	4.6	5.6	6.6
t_{PZH}*	DIR	A	MAX	5.9	6.2	6.6	6.9
t_{PZL}*				5.9	6.2	6.6	6.9
t_{PZH}*	DIR	B	MAX	6.3	7.4	10.3	12.7
t_{PZL}*				6.3	7.4	10.3	12.7

UNIT : ns *The enable time is a calculated value, derived using the formula shown in the enable times section.

V_{CCA} = 5.0V							
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t_{PLH}	A	B	MAX	3.9	5.4	7.5	15.1
t_{PHL}				3.5	4.5	6.2	12.2
t_{PLH}	B	A	MAX	3.9	4.4	5.1	7.2
t_{PHL}				3.5	4	4.6	7
t_{PHZ}	DIR	A	MAX	5.4	5.5	5.4	5.4
t_{PLZ}				3.7	3.7	3.8	3.8
t_{PHZ}	DIR	B	MAX	6.5	8.5	9.8	20.2
t_{PLZ}				4.5	7	7.4	14.8
t_{PZH}*	DIR	A	MAX	8.4	11.4	12.5	22
t_{PZL}*				10	12.5	14.4	27.2
t_{PZH}*	DIR	B	MAX	7.6	9.1	11.3	18.9
t_{PZL}*				8.6	10	11.6	17.6

UNIT : ns

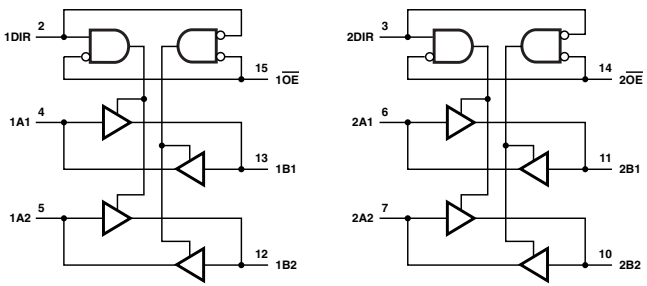
*The enable time is a calculated value, derived using the formula shown in the enable times section.

4T245

4-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

- Control Inputs V_{IH}/V_{IL} Levels Are Referenced to V_{CCA} Voltage
- This 4-Bit Noninverting Bus Transceiver Uses Two Separate Configurable Power-Supply Rails
- Designed for asynchronous Communication Between Data Buses

Logic Diagram



FUNCTION TABLE
(each 4-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	All output Hi-Z

RECOMMENDED OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTECS

PARAMETER	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V	UNIT
I_{CC}*	MAX	0.016	0.016	0.016	0.016	0.016	0.016	0.016	0.016	mA
I_{OH}	MAX	-12	-9	-8	-6	-12	-9	-8	-6	mA
I_{OL}	MAX	12	9	8	6	12	9	8	6	mA

*$I_{CCA} + I_{CCB}$

SWITCHING CHARACTERISTICS

				V_{CCA} = 1.5V							
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
t_{PLH}	A	B	MAX	4.2	4.2	5.2	6.3	4.2	4.2	5.2	6.3
t_{PHL}				4.2	4.2	5.2	6.3	4.2	4.2	5.2	6.3
t_{PLH}	B	A	MAX	5.6	5.7	6	6.3	5.6	5.7	6	6.3
t_{PHL}				5.6	5.7	6	6.3	5.6	5.7	6	6.3
t_{PZH}	$\overline{OE}$	A	MAX	9.4	9.4	9.5	9.6	9.4	9.4	9.5	9.6
t_{PZL}				9.4	9.4	9.5	9.6	9.4	9.4	9.5	9.6
t_{PZH}	$\overline{OE}$	B	MAX	5.6	5.8	7.7	9.6	5.6	5.8	7.7	9.6
t_{PZL}				5.6	5.8	7.7	9.6	5.6	5.8	7.7	9.6
t_{PHZ}	$\overline{OE}$	A	MAX	10.2	10.2	10.2	10.2	10.2	10.2	10.2	10.2
t_{PLZ}				10.2	10.2	10.2	10.2	10.2	10.2	10.2	10.2
t_{PHZ}	$\overline{OE}$	B	MAX	7.6	7.4	9.1	10.3	7.6	7.4	9.1	10.3
t_{PLZ}				7.6	7.4	9.1	10.3	7.6	7.4	9.1	10.3

UNIT : ns

V_{CCA} = 1.8V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
t_{PLH}	A	B	MAX	3.9	3.9	4.9	6	3.9	3.9	4.9	6
t_{PHL}				3.9	3.9	4.9	6	3.9	3.9	4.9	6
t_{PLH}	B	A	MAX	4.5	4.6	4.9	5.3	4.5	4.6	4.9	5.3
t_{PHL}				4.5	4.6	4.9	5.3	4.5	4.6	4.9	5.3
t_{PZH}	$\overline{OE}$	A	MAX	7.2	7.3	7.3	7.4	7.2	7.3	7.3	7.4
t_{PZL}				7.2	7.3	7.3	7.4	7.2	7.3	7.3	7.4
t_{PZH}	$\overline{OE}$	B	MAX	4.6	5.3	7.4	9.2	4.6	5.3	7.4	9.2
t_{PZL}				4.6	5.3	7.4	9.2	4.6	5.3	7.4	9.2
t_{PHZ}	$\overline{OE}$	A	MAX	8.7	8.7	8.7	8.6	8.7	8.7	8.7	8.6
t_{PLZ}				8.7	8.7	8.7	8.6	8.7	8.7	8.7	8.6
t_{PHZ}	$\overline{OE}$	B	MAX	6.9	6.9	8.7	9.9	6.9	6.9	8.7	9.9
t_{PLZ}				6.9	6.9	8.7	9.9	6.9	6.9	8.7	9.9

UNIT : ns

V_{CCA} = 2.5V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
t_{PLH}	A	B	MAX	3.6	3.5	4.6	5.7	3.6	3.5	4.6	5.7
t_{PHL}				3.6	3.5	4.6	5.7	3.6	3.5	4.6	5.7
t_{PLH}	B	A	MAX	3.3	3.4	3.9	4.2	3.3	3.4	3.9	4.2
t_{PHL}				3.3	3.4	3.9	4.2	3.3	3.4	3.9	4.2
t_{PZH}	$\overline{OE}$	A	MAX	4.8	4.8	5.2	6.5	4.8	4.8	5.2	6.5
t_{PZL}				4.8	4.8	5.2	6.5	4.8	4.8	5.2	6.5
t_{PZH}	$\overline{OE}$	B	MAX	4	4.8	7	8.8	4	4.8	7	8.8
t_{PZL}				4	4.8	7	8.8	4	4.8	7	8.8
t_{PHZ}	$\overline{OE}$	A	MAX	6.6	6.2	8.4	8.4	6.6	6.2	8.4	8.4
t_{PLZ}				6.6	6.2	8.4	8.4	6.6	6.2	8.4	8.4
t_{PHZ}	$\overline{OE}$	B	MAX	5.2	6.2	8.2	9.4	5.2	6.2	8.2	9.4
t_{PLZ}				5.2	6.2	8.2	9.4	5.2	6.2	8.2	8.8

UNIT : ns

V_{CCA} = 3.3V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
t_{PLH}	A	B	MAX	2.9	3.3	4.5	5.6	2.9	3.3	4.5	5.6
t_{PHL}				2.9	3.3	4.5	5.6	2.9	3.3	4.5	5.6
t_{PLH}	B	A	MAX	2.8	3	3.4	4.2	2.8	3	3.4	4.2
t_{PHL}				2.8	3	3.4	4.2	2.8	3	3.4	4.2
t_{PZH}	$\overline{OE}$	A	MAX	3.8	3.8	5.2	8.7	3.8	3.8	5.2	8.7
t_{PZL}				3.8	3.8	5.2	8.7	3.8	3.8	5.2	8.7
t_{PZH}	$\overline{OE}$	B	MAX	3.8	4.7	6.8	8.7	3.8	4.7	6.8	8.7
t_{PZL}				3.8	4.7	6.8	8.7	3.8	4.7	6.8	8.7
t_{PHZ}	$\overline{OE}$	A	MAX	6.6	5.6	8.3	9.3	6.6	5.6	8.3	9.3
t_{PLZ}				6.6	5.6	8.3	9.3	6.6	5.6	8.3	9.3
t_{PHZ}	$\overline{OE}$	B	MAX	6.2	6.4	8.1	9.3	6.2	6.4	8.1	9.3
t_{PLZ}				6.2	6.4	8.1	9.3	6.2	6.4	8.1	9.3

UNIT : ns

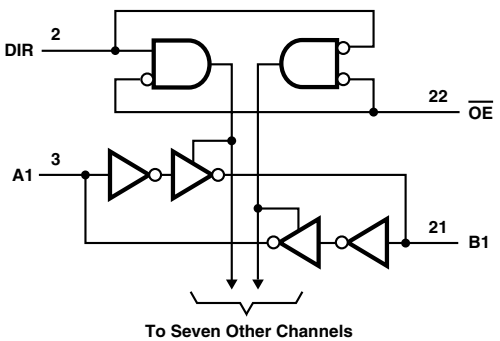
: **PREVIEW**

8T245

8-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

- Control Inputs V_{IH}/V_{IL} Levels Are Referenced to V_{CCA} Voltage
- V_{CC} Isolation Feature - If Either V_{CC} Input Is at GND, All I/O Ports Are in the High-Impedance State
- This 8-Bit Noninverting Bus Transceiver Uses Two Separate Configurable Power-Supply Rails
- Designed for asynchronous Communication Between Data Buses

Logic Diagram



FUNCTION TABLE(1)
(each 8-bit section)

CONTROL INPUTS		OUTPUTS CIRCUITS		OPERATION
$\overline{OE}$	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A bus
L	H	Hi-Z	Enabled	A data to B bus
H	X	Hi-Z	Hi-Z	Isolation

(1) Input circuits of the data I/Os are always active.

RECOMMENDED OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTECS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	LVCH 5V	LVCH 3.3V	LVCH 2.5V	LVCH 1.8V	UNIT
I_{CC}*	MAX	0.025	0.025	0.025	0.025	0.03	0.03	0.03	0.03	mA
I_{OH}	MAX	-32	-24	-8	-4	-32	-24	-8	-4	mA
I_{OL}	MAX	32	24	8	4	32	24	8	4	mA

PARAMETER	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V	UNIT
I_{CC}*	MAX	0.025	0.025	0.025	0.025	0.025	0.025	0.025	0.025	mA
I_{OH}	MAX	-12	-9	-8	-6	-12	-9	-8	-6	mA
I_{OL}	MAX	12	9	8	6	12	9	8	6	mA

*I_{CCA} + I_{CCB}

SWITCHING CHARACTERISTICS

V_{CCA} = 1.5V

PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
t_{PLH}	A	B	MAX	6.8	4.9	4.6	5.4	6.8	4.9	4.6	5.4
t_{PHL}				6.8	4.9	4.6	5.4	6.8	4.9	4.6	5.4
t_{PLH}	B	A	MAX	4.5	4.7	5.1	5.4	4.5	4.7	5.1	5.4
t_{PHL}				4.5	4.7	5.1	5.4	4.5	4.7	5.1	5.4
t_{PZH}	$\overline{OE}$	A	MAX	8.7	8.7	8.7	8.7	8.7	8.7	8.7	8.7
t_{PZL}				8.7	8.7	8.7	8.7	8.7	8.7	8.7	8.7
t_{PZH}	$\overline{OE}$	B	MAX	5.2	5.6	7.1	7.6	5.2	5.6	7.1	7.6
t_{PZL}				5.2	5.6	7.1	7.6	5.2	5.6	7.1	7.6
t_{PHZ}	$\overline{OE}$	A	MAX	8.6	8.6	8.6	8.6	8.6	8.6	8.6	8.6
t_{PLZ}				8.6	8.6	8.6	8.6	8.6	8.6	8.6	8.6
t_{PHZ}	$\overline{OE}$	B	MAX	7.8	7.2	7.6	8.4	7.8	7.2	7.6	8.4
t_{PLZ}				7.8	7.2	7.6	8.4	7.8	7.2	7.6	8.4

UNIT : ns

V_{CCA} = 1.8V

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	LVCH 5V	LVCH 3.3V	LVCH 2.5V	LVCH 1.8V
t_{PLH}	A	B	MAX	7.1	7.4	9.2	21.9	7.1	7.4	9.2	21.9
t_{PHL}				7.1	7.4	9.2	21.9	7.1	7.4	9.2	21.9
t_{PLH}	B	A	MAX	23.4	23.4	23.6	23.8	23.4	23.4	23.6	23.8
t_{PHL}				23.4	23.4	23.6	23.8	23.4	23.4	23.6	23.8
t_{PZH}	$\overline{OE}$	A	MAX	23.7	23.7	23.8	24	23.7	23.7	23.8	24
t_{PZL}				23.7	23.7	23.8	24	23.7	23.7	23.8	24
t_{PZH}	$\overline{OE}$	B	MAX	10.8	12.6	16	32	10.8	12.6	16	32
t_{PZL}				10.8	12.6	16	32	10.8	12.6	16	32
t_{PHZ}	$\overline{OE}$	A	MAX	29.2	29.3	29.4	29.6	29.2	29.3	29.4	29.6
t_{PLZ}				29.2	29.3	29.4	23.6	29.2	29.3	29.4	23.6
t_{PHZ}	$\overline{OE}$	B	MAX	10.3	12	13.1	32.2	10.3	12	13.1	32.2
t_{PLZ}				10.3	12	13.1	32.2	10.3	12	13.1	32.2

V_{CCA} = 1.8V

PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
t_{PLH}	A	B	MAX	3.9	4	4.4	5.1	3.9	4	4.4	5.1
t_{PHL}				3.9	4	4.4	5.1	3.9	4	4.4	5.1
t_{PLH}	B	A	MAX	3.7	3.9	4.4	4.6	3.7	3.9	4.4	4.6
t_{PHL}				3.7	3.9	4.4	4.6	3.7	3.9	4.4	4.6
t_{PZH}	$\overline{OE}$	A	MAX	6.8	6.8	6.8	6.8	6.8	6.8	6.8	6.8
t_{PZL}				6.8	6.8	6.8	6.8	6.8	6.8	6.8	6.8
t_{PZH}	$\overline{OE}$	B	MAX	4.5	5.1	6.7	8.2	4.5	5.1	6.7	8.2
t_{PZL}				4.5	5.1	6.7	8.2	4.5	5.1	6.7	8.2
t_{PHZ}	$\overline{OE}$	A	MAX	7.1	7.1	7.1	7.1	7.1	7.1	7.1	7.1
t_{PLZ}				7.1	7.1	7.1	7.1	7.1	7.1	7.1	7.1
t_{PHZ}	$\overline{OE}$	B	MAX	5.8	6	6.9	7.8	5.8	6	6.9	7.8
t_{PLZ}				5.8	6	6.9	7.8	5.8	6	6.9	7.8

UNIT : ns

: PREVIEW

V_{CCA} = 2.5V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	LVCH 5V	LVCH 3.3V	LVCH 2.5V	LVCH 1.8V
t_{PLH}	A	B	MAX	4.8	6.2	9	21.4	4.8	6.2	9	21.4
t_{PHL}				4.8	6.2	9	21.4	4.8	6.2	9	21.4
t_{PLH}	B	A	MAX	8.8	8.9	9.1	9.3	8.8	8.9	9.1	9.3
t_{PHL}				8.8	8.9	9.1	9.3	8.8	8.9	9.1	9.3
t_{PZH}	$\overline{OE}$	A	MAX	10.9	10.9	10.9	10.9	10.9	10.9	10.9	10.9
t_{PZL}				10.9	10.9	10.9	10.9	10.9	10.9	10.9	10.9
t_{PZH}	$\overline{OE}$	B	MAX	6.9	9.4	12.9	28.2	6.9	9.4	12.9	28.2
t_{PZL}				6.9	9.4	12.9	28.2	6.9	9.4	12.9	28.2
t_{PHZ}	$\overline{OE}$	A	MAX	9	9	9	9	9	9	9	9
t_{PLZ}				9	9	9	9	9	9	9	9
t_{PHZ}	$\overline{OE}$	B	MAX	6.9	9.3	11	29.6	6.9	9.3	11	29.6
t_{PLZ}				6.9	9.3	11	29.6	6.9	9.3	11	29.6

V_{CCA} = 2.5V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
t_{PLH}	A	B	MAX	2.8	3.1	3.9	4.7	2.8	3.1	3.9	4.7
t_{PHL}				2.8	3.1	3.9	4.7	2.8	3.1	3.9	4.7
t_{PLH}	B	A	MAX	2.9	3.1	4	4.9	2.9	3.1	4	4.9
t_{PHL}				2.9	3.1	4	4.9	2.9	3.1	4	4.9
t_{PZH}	$\overline{OE}$	A	MAX	4.8	4.8	4.8	4.8	4.8	4.8	4.8	4.8
t_{PZL}				4.8	4.8	4.8	4.8	4.8	4.8	4.8	4.8
t_{PZH}	$\overline{OE}$	B	MAX	4	4.6	6.4	7.9	4	4.6	6.4	7.9
t_{PZL}				4	4.6	6.4	7.9	4	4.6	6.4	7.9
t_{PHZ}	$\overline{OE}$	A	MAX	5.1	5.1	5.1	5.1	5.1	5.1	5.1	5.1
t_{PLZ}				5.1	5.1	5.1	5.1	5.1	5.1	5.1	5.1
t_{PHZ}	$\overline{OE}$	B	MAX	3.9	5.1	6.3	7.1	3.9	5.1	6.3	7.1
t_{PLZ}				3.9	5.1	6.3	7.1	3.9	5.1	6.3	7.1

UNIT : ns

V_{CCA} = 3.3V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	LVCH 5V	LVCH 3.3V	LVCH 2.5V	LVCH 1.8V
t_{PLH}	A	B	MAX	4.4	6.3	8.8	21.2	4.4	6.2	8.8	21.2
t_{PHL}				4.4	6.3	8.8	21.2	4.4	6.2	8.8	21.2
t_{PLH}	B	A	MAX	6	6.1	6.2	7.2	6	6.1	6.2	7.2
t_{PHL}				6	6.1	6.2	7.2	6	6.1	6.2	7.2
t_{PZH}	$\overline{OE}$	A	MAX	8.1	8.1	8.1	8.1	8.1	8.1	8.1	8.1
t_{PZL}				8.1	8.1	8.1	8.1	8.1	8.1	8.1	8.1
t_{PZH}	$\overline{OE}$	B	MAX	6.4	8.5	12.4	27.7	6.4	8.5	12.4	27.7
t_{PZL}				6.4	8.5	12.4	27.7	6.4	8.5	12.4	27.7
t_{PHZ}	$\overline{OE}$	A	MAX	8.2	8.2	8.2	8.2	8.2	8.2	8.2	8.2
t_{PLZ}				8.2	8.2	8.2	8.2	8.2	8.2	8.2	8.2
t_{PHZ}	$\overline{OE}$	B	MAX	6.3	8.6	10.3	29	6.3	8.6	10.3	29
t_{PLZ}				6.3	8.6	10.3	29	6.3	8.6	10.3	29

V_{CCA} = 3.3V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
t_{PLH}	A	B	MAX	2.5	2.9	3.7	4.5	2.5	2.9	3.7	4.5
t_{PHL}				2.5	2.9	3.7	4.5	2.5	2.9	3.7	4.5
t_{PLH}	B	A	MAX	2.5	2.8	3.9	6.8	2.5	2.8	3.9	6.8
t_{PHL}				2.5	2.8	3.9	6.8	2.5	2.8	3.9	6.8
t_{PZH}	$\overline{OE}$	A	MAX	4	4	4	4	4	4	4	4
t_{PZL}				4	4	4	4	4	4	4	4
t_{PZH}	$\overline{OE}$	B	MAX	3.9	4.5	6.2	7.8	3.9	4.5	6.2	7.8
t_{PZL}				3.9	4.5	6.2	7.8	3.9	4.5	6.2	7.8
t_{PHZ}	$\overline{OE}$	A	MAX	4	4	4	4	4	4	4	4
t_{PLZ}				4	4	4	4	4	4	4	4
t_{PHZ}	$\overline{OE}$	B	MAX	4.2	4.8	6	6.9	4.2	4.8	6	6.9
t_{PLZ}				4.2	4.8	6	6.9	4.2	4.8	6	6.9

UNIT : ns

V_{CCA} = 5.0V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	LVCH 5V	LVCH 3.3V	LVCH 2.5V	LVCH 1.8V
t_{PLH}	A	B	MAX	4.2	6	8.8	21.4	4.2	6	8.8	21.4
t_{PHL}				4.2	6	8.8	21.4	4.2	6	8.8	21.4
t_{PLH}	B	A	MAX	4.3	4.5	4.8	7	4.3	4.5	4.8	7
t_{PHL}				4.3	4.5	4.8	7	4.3	4.5	4.8	7
t_{PZH}	$\overline{OE}$	A	MAX	6.4	6.4	6.4	6.4	6.4	6.4	6.4	6.4
t_{PZL}				6.4	6.4	6.4	6.4	6.4	6.4	6.4	6.4
t_{PZH}	$\overline{OE}$	B	MAX	6	8.1	11.4	27.6	6	8.1	11.4	27.6
t_{PZL}				6	8.1	11.4	27.6	6	8.1	11.4	27.6
t_{PHZ}	$\overline{OE}$	A	MAX	5.4	5.4	5.4	5.4	5.4	5.4	5.4	5.4
t_{PLZ}				5.4	5.4	5.4	5.4	5.4	5.4	5.4	5.4
t_{PHZ}	$\overline{OE}$	B	MAX	5.7	8	9.7	28.7	5.7	8	9.7	28.7
t_{PLZ}				5.7	8	9.7	28.7	5.7	8	9.7	28.7

UNIT : ns

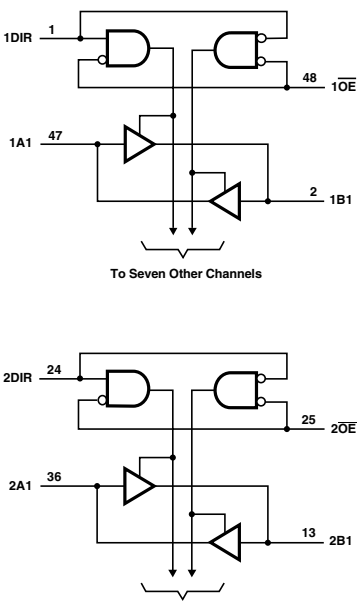
: **PREVIEW**

16T245

16-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

- Control Inputs V_{IH}/V_{IL} Levels Are Referenced to V_{CCA} Voltage
- V_{CC} Isolation Feature - If Either V_{CC} Input Is at GND, Both Ports Are in the High-Impedance State
- Overvoltage-Tolerant Inputs / Outputs Allow Mixed-Voltage-Mode Data Communications
- This 16-Bit Noninverting Bus Transceiver Uses Two Separate Configurable Power-Supply Rails
- Designed for asynchronous Communication Between Data Buses

Logic Diagram



FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

RECOMMENDED OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTECS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	LVCH 5V	LVCH 3.3V	LVCH 2.5V	LVCH 1.8V	UNIT
I_{CC}*	MAX	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03	mA
I_{OH}	MAX	-32	-24	-8	-4	-32	-24	-8	-4	mA
I_{OL}	MAX	32	24	8	4	32	24	8	4	mA

PARAMETER	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.8V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.8V	UNIT
I_{CC}*	MAX	0.045	0.045	0.045	0.045	0.045	0.045	0.045	0.045	mA
I_{OH}	MAX	-12	-9	-8	-6	-12	-9	-8	-6	mA
I_{OL}	MAX	12	9	8	6	12	9	8	6	mA

*I_{CCA} + I_{CCB}

SWITCHING CHARACTERISTICS

V_{CCA} = 1.5V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
t_{PLH}	A	B	MAX	3.7	4.1	5.2	6.2	3.7	4.1	5.2	6.2
t_{PHL}				3.7	4.1	5.2	6.2	3.7	4.1	5.2	6.2
t_{PLH}	B	A	MAX	5.5	5.6	5.9	6.2	5.5	5.6	5.9	6.2
t_{PHL}				5.5	5.6	5.9	6.2	5.5	5.6	5.9	6.2
t_{PZH}	$\overline{OE}$	A	MAX	10.1	10.1	10.1	10.1	10.1	10.1	10.1	10.1
t_{PZL}				10.1	10.1	10.1	10.1	10.1	10.1	10.1	10.1
t_{PZH}	$\overline{OE}$	B	MAX	5.2	5.9	8.1	10.1	5.2	5.9	8.1	10.1
t_{PZL}				5.2	5.9	8.1	10.1	5.2	5.9	8.1	10.1
t_{PHZ}	$\overline{OE}$	A	MAX	9.1	9.1	9.1	9.1	9.1	9.1	9.1	9.1
t_{PLZ}				9.1	9.1	9.1	9.1	9.1	9.1	9.1	9.1
t_{PHZ}	$\overline{OE}$	B	MAX	6.3	6.5	7.5	8.7	6.3	6.5	7.5	8.7
t_{PLZ}				6.3	6.5	7.5	8.7	6.3	6.5	7.5	8.7

UNIT : ns

V_{CCA} = 1.8V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	LVCH 5V	LVCH 3.3V	LVCH 2.5V	LVCH 1.8V
t_{PLH}	A	B	MAX	7.1	7.4	9.2	21.9	7.1	7.4	9.2	21.9
t_{PHL}				7.1	7.4	9.2	21.9	7.1	7.4	9.2	21.9
t_{PLH}	B	A	MAX	23.4	23.4	23.6	23.8	23.4	23.4	23.8	23.8
t_{PHL}				23.4	23.4	23.6	23.8	23.4	23.4	23.8	23.8
t_{PZH}	$\overline{OE}$	A	MAX	23.7	23.7	23.8	24	23.7	23.7	23.8	24
t_{PZL}				23.7	23.7	23.8	24	23.7	23.7	23.8	24
t_{PZH}	$\overline{OE}$	B	MAX	10.8	12.6	16	32	10.8	12.6	18	32
t_{PZL}				10.8	12.6	16	32	10.8	12.6	18	32
t_{PHZ}	$\overline{OE}$	A	MAX	29.2	29.3	29.4	29.6	29.2	29.3	29.4	29.6
t_{PLZ}				29.2	29.3	29.4	29.6	29.2	29.3	29.4	29.6
t_{PHZ}	$\overline{OE}$	B	MAX	10.3	12	13.1	32.2	10.3	12	13.1	32.2
t_{PLZ}				10.3	12	13.1	32.2	10.3	12	13.1	32.2

V_{CCA} = 1.8V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
t_{PLH}	A	B	MAX	3.3	3.7	4.8	5.9	3.3	3.7	4.8	5.9
t_{PHL}				3.3	3.7	4.8	5.9	3.3	3.7	4.8	5.9
t_{PLH}	B	A	MAX	4.4	4.5	4.8	5.2	4.4	4.5	4.8	5.2
t_{PHL}				4.4	4.5	4.8	5.2	4.4	4.5	4.8	5.2
t_{PZH}	$\overline{OE}$	A	MAX	7.8	7.8	7.8	7.8	7.8	7.8	7.8	7.8
t_{PZL}				7.8	7.8	7.8	7.8	7.8	7.8	7.8	7.8
t_{PZH}	$\overline{OE}$	B	MAX	4.5	5.3	7.4	9.2	4.5	5.3	7.4	9.2
t_{PZL}				4.5	5.3	7.4	9.2	4.5	5.3	7.4	9.2
t_{PHZ}	$\overline{OE}$	A	MAX	7.7	7.7	7.7	7.7	7.7	7.7	7.7	7.7
t_{PLZ}				7.7	7.7	7.7	7.7	7.7	7.7	7.7	7.7
t_{PHZ}	$\overline{OE}$	B	MAX	5.7	5.9	7.1	8.4	5.7	5.9	7.1	8.4
t_{PLZ}				5.7	5.9	7.1	8.4	5.7	5.9	7.1	8.4

UNIT : ns

: **PREVIEW**

V_{CCA} = 2.5V										
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	LVCH 5V	LVCH 3.3V	LVCH 2.5V	LVCH 1.8V
t_{PLH}	A	B	MAX	4.8	6.2	9	21.4	4.8	6.2	9	21.4
t_{PHL}				4.8	6.2	9	21.4	4.8	6.2	9	21.4
t_{PLH}	B	A	MAX	8.8	8.9	9.1	9.3	8.8	8.9	9.1	9.3
t_{PHL}				8.8	8.9	9.1	9.3	8.8	8.9	9.1	9.3
t_{PZH}	$\overline{OE}$	A	MAX	10.9	10.9	10.9	10.9	10.9	10.9	10.9	10.9
t_{PZL}				10.9	10.9	10.9	10.9	10.9	10.9	10.9	10.9
t_{PZH}	$\overline{OE}$	B	MAX	6.9	9.4	12.9	28.2	6.9	9.4	12.9	28.2
t_{PZL}				6.9	9.4	12.9	28.2	6.9	9.4	12.9	28.2
t_{PHZ}	$\overline{OE}$	A	MAX	9	9	9	9	9	9	9	9
t_{PLZ}				9	9	9	9	9	9	9	9
t_{PHZ}	$\overline{OE}$	B	MAX	6.9	9.3	11	29.6	6.9	9.3	11	29.6
t_{PLZ}				6.9	9.3	11	29.6	6.9	9.3	11	29.6

V_{CCA} = 2.5V										
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
t_{PLH}	A	B	MAX	2.8	3.3	4.5	5.6	2.8	3.3	4.5	5.6
t_{PHL}				2.8	3.3	4.5	5.6	2.8	3.3	4.5	5.6
t_{PLH}	B	A	MAX	3.2	3.3	3.7	4.1	3.2	3.3	3.7	4.1
t_{PHL}				3.2	3.3	3.7	4.1	3.2	3.3	3.7	4.1
t_{PZH}	$\overline{OE}$	A	MAX	5.3	5.3	5.3	5.3	5.3	5.3	5.3	5.3
t_{PZL}				5.3	5.3	5.3	5.3	5.3	5.3	5.3	5.3
t_{PZH}	$\overline{OE}$	B	MAX	4.5	5.1	7.3	9.4	4.5	5.1	7.3	9.4
t_{PZL}				4.5	5.1	7.3	9.4	4.5	5.1	7.3	9.4
t_{PHZ}	$\overline{OE}$	A	MAX	6.1	6.1	6.1	6.1	6.1	6.1	6.1	6.1
t_{PLZ}				6.1	6.1	6.1	6.1	6.1	6.1	6.1	6.1
t_{PHZ}	$\overline{OE}$	B	MAX	5.2	6.1	6.6	7.9	5.2	6.1	6.6	7.9
t_{PLZ}				5.2	6.1	6.6	7.9	5.2	6.1	6.6	7.9

UNIT : ns

V_{CCA} = 3.3V										
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	LVCH 5V	LVCH 3.3V	LVCH 2.5V	LVCH 1.8V
t_{PLH}	A	B	MAX	4.4	6.1	8.8	21.2	4.4	6.2	8.8	21.2
t_{PHL}				4.4	6.1	8.8	21.2	4.4	6.2	8.8	21.2
t_{PLH}	B	A	MAX	6	6.1	6.2	7.2	6	6.1	6.2	7.2
t_{PHL}				6	6.1	6.2	7.2	6	6.1	6.2	7.2
t_{PZH}	$\overline{OE}$	A	MAX	7.8	7.8	7.8	7.8	8.1	8.1	8.1	7.8
t_{PZL}				7.8	7.8	7.8	7.8	8.1	8.1	8.1	7.8
t_{PZH}	$\overline{OE}$	B	MAX	8.4	8.5	12.4	27.7	6.4	8.5	12.4	27.7
t_{PZL}				8.4	8.5	12.4	27.7	6.4	8.5	12.4	27.7
t_{PHZ}	$\overline{OE}$	A	MAX	8.2	6.2	8.2	8.2	8.2	8.2	8.2	8.2
t_{PLZ}				8.2	6.2	8.2	8.2	8.2	8.2	8.2	8.2
t_{PHZ}	$\overline{OE}$	B	MAX	6.3	8.6	10.3	29	6.3	8.8	10.3	29
t_{PLZ}				6.3	8.6	10.3	29	6.3	8.8	10.3	29

V_{CCA} = 3.3V										
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
t_{PLH}	A	B	MAX	2.7	3.2	4.4	5.5	2.7	3.2	4.4	5.5
t_{PHL}				2.7	3.2	4.4	5.5	2.7	3.2	4.4	5.5
t_{PLH}	B	A	MAX	2.7	2.8	3.3	3.7	2.7	2.8	3.3	3.7
t_{PHL}				2.7	2.8	3.3	3.7	2.7	2.8	3.3	3.7
t_{PZH}	$\overline{OE}$	A	MAX	4	4.1	4.2	4.3	4	4.1	4.2	4.3
t_{PZL}				4	4.1	4.2	4.3	4	4.1	4.2	4.3
t_{PZH}	$\overline{OE}$	B	MAX	4	4.9	7.2	9.3	4	4.9	7.2	9.3
t_{PZL}				4	4.9	7.2	9.3	4	4.9	7.2	9.3
t_{PHZ}	$\overline{OE}$	A	MAX	5	5	5	5	5	5	5	5
t_{PLZ}				5	5	5	5	5	5	5	5
t_{PHZ}	$\overline{OE}$	B	MAX	5	5.2	6.5	7.7	5	5.2	6.5	7.7
t_{PLZ}				5	5.2	6.5	7.7	5	5.2	6.5	7.7

UNIT : ns

V_{CCA} = 5.0V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	LVCH 5V	LVCH 3.3V	LVCH 2.5V	LVCH 1.8V
t_{PLH}	A	B	MAX	4.2	6	8.8	21.4	4.2	6	8.8	21.4
t_{PHL}				4.2	6	8.8	21.4	4.2	6	8.8	21.4
t_{PLH}	B	A	MAX	4.3	4.5	4.8	6.8	4.3	4.5	4.8	7
t_{PHL}				4.3	4.5	4.8	6.8	4.3	4.5	4.8	7
t_{PZH}	$\overline{OE}$	A	MAX	5.5	5.5	5.5	5.5	5.4	5.4	5.4	5.4
t_{PZL}				5.5	5.5	5.5	5.5	5.4	5.4	5.4	5.4
t_{PZH}	$\overline{OE}$	B	MAX	6	8.1	11.4	27.6	6	8.1	11.4	27.6
t_{PZL}				6	8.1	11.4	27.6	6	8.1	11.4	27.6
t_{PHZ}	$\overline{OE}$	A	MAX	6.4	5.4	5.4	5.4	5.4	5.4	5.4	5.4
t_{PLZ}				6.4	5.4	5.4	5.4	5.4	5.4	5.4	5.4
t_{PHZ}	$\overline{OE}$	B	MAX	5.7	8	9.7	28.7	5.7	8	9.7	28.7
t_{PLZ}				5.7	8	9.7	28.7	5.7	8	9.7	28.7

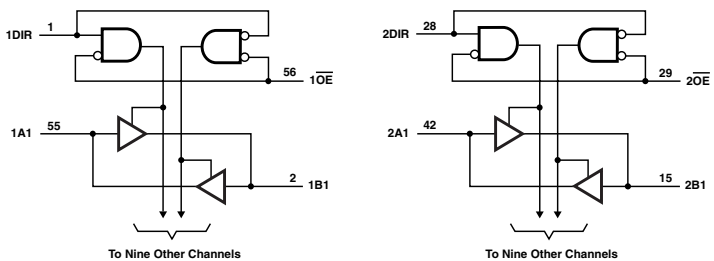
UNIT : ns

20T245

20-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

- Control Inputs V_{IH}/V_{IL} Levels Are Referenced to V_{CCA} Voltage
- V_{CC} Isolation Feature - If Either V_{CC} Input Is at GND, Both Ports Are in the High-Impedance State
- Overvoltage-Tolerant Inputs / Outputs Allow Mixed-Voltage-Mode Data Communications
- This 20-Bit Noninverting Bus Transceiver Uses Two Separate Configurable Power-Supply Rails
- Designed for asynchronous Communication Between Data Buses

Logic Diagram



FUNCTION TABLE
(each 10-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

RECOMMENDED OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTECS

PARAMETER	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.8V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.8V	UNIT
I_{CC}*	MAX	0.065	0.065	0.065	0.065	0.065	0.065	0.065	0.065	mA
I_{OH}	MAX	-12	-9	-8	-6	-12	-9	-8	-6	mA
I_{OL}	MAX	12	9	8	6	12	9	8	6	mA

*$I_{CCA} + I_{CCB}$

SWITCHING CHARACTERISTICS

				V_{CCA} = 1.5V							
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
t_{PLH}	A	B	MAX	3.9	4.3	5.4	6.4	3.9	4.3	5.4	6.4
t_{PHL}				3.9	4.3	5.4	6.4	3.9	4.3	5.4	6.4
t_{PLH}	B	A	MAX	5.7	5.8	6.1	6.4	5.7	5.8	6.1	6.4
t_{PHL}				5.7	5.8	6.1	6.4	5.7	5.8	6.1	6.4
t_{PZH}	$\overline{OE}$	A	MAX	10.2	10.2	10.3	10.3	10.2	10.2	10.3	10.3
t_{PZL}				10.2	10.2	10.3	10.3	10.2	10.2	10.3	10.3
t_{PZH}	$\overline{OE}$	B	MAX	5.3	6.1	8.4	10.3	5.3	6.1	8.4	10.3
t_{PZL}				5.3	6.1	8.4	10.3	5.3	6.1	8.4	10.3
t_{PHZ}	$\overline{OE}$	A	MAX	9	9	9	9	9	9	9	9
t_{PLZ}				9	9	9	9	9	9	9	9
t_{PHZ}	$\overline{OE}$	B	MAX	5.9	6.4	7.8	9	5.9	6.4	7.8	9
t_{PLZ}				5.9	6.4	7.8	9	5.9	6.4	7.8	9

UNIT : ns

V_{CCA} = 1.8V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
t_{PLH}	A	B	MAX	3.5	3.9	5	6.1	3.5	3.9	5	6.1
t_{PHL}				3.5	3.9	5	6.1	3.5	3.9	5	6.1
t_{PLH}	B	A	MAX	4.6	4.7	5	5.4	4.6	4.7	5	5.4
t_{PHL}				4.6	4.7	5	5.4	4.6	4.7	5	5.4
t_{PZH}	$\overline{OE}$	A	MAX	7.9	7.9	7.9	8.1	7.9	7.9	7.9	8.1
t_{PZL}				7.9	7.9	7.9	8.1	7.9	7.9	7.9	8.1
t_{PZH}	$\overline{OE}$	B	MAX	4.8	5.7	7.9	10	4.8	5.7	7.9	10
t_{PZL}				4.8	5.7	7.9	10	4.8	5.7	7.9	10
t_{PHZ}	$\overline{OE}$	A	MAX	7.4	7.4	7.4	7.4	7.4	7.4	7.4	7.4
t_{PLZ}				7.4	7.4	7.4	7.4	7.4	7.4	7.4	7.4
t_{PHZ}	$\overline{OE}$	B	MAX	5.1	5.8	7.4	8.7	5.1	5.8	7.4	8.7
t_{PLZ}				5.1	5.8	7.4	8.7	5.1	5.8	7.4	8.7

UNIT : ns

V_{CCA} = 2.5V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
t_{PLH}	A	B	MAX	3	3.5	4.7	5.8	3	3.5	4.7	5.8
t_{PHL}				3	3.5	4.7	5.8	3	3.5	4.7	5.8
t_{PLH}	B	A	MAX	3.4	3.5	3.9	4.3	3.4	3.5	3.9	4.3
t_{PHL}				3.4	3.5	3.9	4.3	3.4	3.5	3.9	4.3
t_{PZH}	$\overline{OE}$	A	MAX	5.2	5.2	5.3	5.4	5.2	5.2	5.3	5.4
t_{PZL}				5.2	5.2	5.3	5.4	5.2	5.2	5.3	5.4
t_{PZH}	$\overline{OE}$	B	MAX	4.3	5.3	7.6	9.6	4.3	5.3	7.6	9.6
t_{PZL}				4.3	5.3	7.6	9.6	4.3	5.3	7.6	9.6
t_{PHZ}	$\overline{OE}$	A	MAX	5.2	5.2	5.2	5.2	5.2	5.2	5.2	5.2
t_{PLZ}				5.2	5.2	5.2	5.2	5.2	5.2	5.2	5.2
t_{PHZ}	$\overline{OE}$	B	MAX	5	5.3	6.9	8.2	5	5.3	6.9	8.2
t_{PLZ}				5	5.3	6.9	8.2	5	5.3	6.9	8.2

UNIT : ns

V_{CCA} = 3.3V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
t_{PLH}	A	B	MAX	2.9	3.4	4.6	5.7	2.9	3.4	4.6	5.7
t_{PHL}				2.9	3.4	4.6	5.7	2.9	3.4	4.6	5.7
t_{PLH}	B	A	MAX	2.9	3	3.5	3.9	2.9	3	3.5	3.9
t_{PHL}				2.9	3	3.5	3.9	2.9	3	3.5	3.9
t_{PZH}	$\overline{OE}$	A	MAX	4.1	4.2	4.3	4.4	4.1	4.2	4.3	4.4
t_{PZL}				4.1	4.2	4.3	4.4	4.1	4.2	4.3	4.4
t_{PZH}	$\overline{OE}$	B	MAX	4.1	5.1	7.5	9.6	4.1	5.1	7.5	9.6
t_{PZL}				4.1	5.1	7.5	9.6	4.1	5.1	7.5	9.6
t_{PHZ}	$\overline{OE}$	A	MAX	5	5	5	5	5	5	5	5
t_{PLZ}				5	5	5	5	5	5	5	5
t_{PHZ}	$\overline{OE}$	B	MAX	5	5.1	6.7	8.1	5	5.1	6.7	8.1
t_{PLZ}				5	5.1	6.7	8.1	5	5.1	6.7	8.1

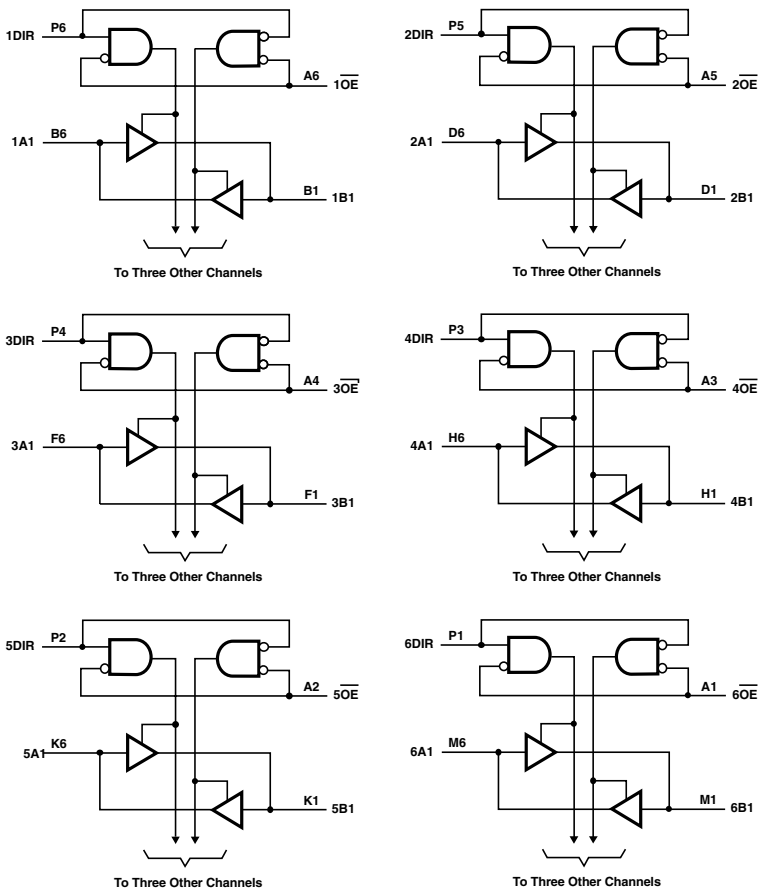
UNIT : ns

24T245

24-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

- Control Inputs V_{IH}/V_{IL} Levels Are Referenced to V_{CCA} Voltage
- V_{CC} Isolation Feature - If Either V_{CC} Input Is at GND, All Outputs Are in the High-Impedance State
- Overvoltage-Tolerant Inputs / Outputs Allow Mixed-Voltage-Mode Data Communications
- This 24-Bit Noninverting Bus Transceiver Uses Two Separate Configurable Power-Supply Rails
- Designed for asynchronous Communication Between Data Buses

Logic Diagram



FUNCTION TABLE
(each 4-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

RECOMMENDED OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTECS

PARAMETER	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.8V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.8V	UNIT
I_{CC}*	MAX	0.075	0.075	0.075	0.075	0.075	0.075	0.075	0.075	mA
I_{OH}	MAX	-12	-9	-8	-6	-12	-9	-8	-6	mA
I_{OL}	MAX	12	9	8	6	12	9	8	6	mA

*$I_{CCA} + I_{CCB}$

SWITCHING CHARACTERISTICS

V_{CCA} = 1.5V

PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
t_{PLH}	A	B	MAX	3.7	4.1	5.2	6.2	3.7	4.1	5.2	6.2
t_{PHL}				3.7	4.1	5.2	6.2	3.7	4.1	5.2	6.2
t_{PLH}	B	A	MAX	5.5	5.6	5.9	6.2	5.5	5.6	5.9	6.2
t_{PHL}				5.5	5.6	5.9	6.2	5.5	5.6	5.9	6.2
t_{PZH}	$\overline{OE}$	A	MAX	10.1	10.1	10.1	10.1	10.1	10.1	10.1	10.1
t_{PZL}				10.1	10.1	10.1	10.1	10.1	10.1	10.1	10.1
t_{PZH}	$\overline{OE}$	B	MAX	5.2	5.9	8.1	10.1	5.2	5.9	8.1	10.1
t_{PZL}				5.2	5.9	8.1	10.1	5.2	5.9	8.1	10.1
t_{PHZ}	$\overline{OE}$	A	MAX	9.1	9.1	9.1	9.1	9.1	9.1	9.1	9.1
t_{PLZ}				9.1	9.1	9.1	9.1	9.1	9.1	9.1	9.1
t_{PHZ}	$\overline{OE}$	B	MAX	6.3	6.5	7.5	8.7	6.3	6.5	7.5	8.7
t_{PLZ}				6.3	6.5	7.5	8.7	6.3	6.5	7.5	8.7

UNIT : ns

V_{CCA} = 1.8V

PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
t_{PLH}	A	B	MAX	3.3	3.7	4.8	5.9	3.3	3.7	4.8	5.9
t_{PHL}				3.3	3.7	4.8	5.9	3.3	3.7	4.8	5.9
t_{PLH}	B	A	MAX	4.4	4.5	4.8	5.2	4.4	4.5	4.8	5.2
t_{PHL}				4.4	4.5	4.8	5.2	4.4	4.5	4.8	5.2
t_{PZH}	$\overline{OE}$	A	MAX	7.8	7.8	7.8	7.8	7.8	7.8	7.8	7.8
t_{PZL}				7.8	7.8	7.8	7.8	7.8	7.8	7.8	7.8
t_{PZH}	$\overline{OE}$	B	MAX	4.5	5.3	7.4	9.2	4.5	5.3	7.4	9.2
t_{PZL}				4.5	5.3	7.4	9.2	4.5	5.3	7.4	9.2
t_{PHZ}	$\overline{OE}$	A	MAX	7.7	7.7	7.7	7.7	7.7	7.7	7.7	7.7
t_{PLZ}				7.7	7.7	7.7	7.7	7.7	7.7	7.7	7.7
t_{PHZ}	$\overline{OE}$	B	MAX	5.7	5.9	7.1	8.4	5.7	5.9	7.1	8.4
t_{PLZ}				5.7	5.9	7.1	8.4	5.7	5.9	7.1	8.4

UNIT : ns

: **PREVIEW**

V_{CCA} = 2.5V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
t_{PLH}	A	B	MAX	2.8	3.3	4.5	5.6	2.8	3.3	4.5	5.6
t_{PHL}				2.8	3.3	4.5	5.6	2.8	3.3	4.5	5.6
t_{PLH}	B	A	MAX	3.2	3.3	3.7	4.1	3.2	3.3	3.7	4.1
t_{PHL}				3.2	3.3	3.7	4.1	3.2	3.3	3.7	4.1
t_{PZH}	$\overline{OE}$	A	MAX	5.3	5.3	5.3	5.3	5.3	5.3	5.3	5.3
t_{PZL}				5.3	5.3	5.3	5.3	5.3	5.3	5.3	5.3
t_{PZH}	$\overline{OE}$	B	MAX	4.5	5.1	7.3	9.4	4.5	5.1	7.3	9.4
t_{PZL}				4.5	5.1	7.3	9.4	4.5	5.1	7.3	9.4
t_{PHZ}	$\overline{OE}$	A	MAX	6.1	6.1	6.1	6.1	6.1	6.1	6.1	6.1
t_{PLZ}				6.1	6.1	6.1	6.1	6.1	6.1	6.1	6.1
t_{PHZ}	$\overline{OE}$	B	MAX	5.2	6.1	6.6	7.9	5.2	6.1	6.6	7.9
t_{PLZ}				5.2	6.1	6.6	7.9	5.2	6.1	6.6	7.9

UNIT : ns

V_{CCA} = 3.3V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
t_{PLH}	A	B	MAX	2.7	3.2	4.4	5.5	2.7	3.2	4.4	5.5
t_{PHL}				2.7	3.2	4.4	5.5	2.7	3.2	4.4	5.5
t_{PLH}	B	A	MAX	2.7	2.8	3.3	3.7	2.7	2.8	3.3	3.7
t_{PHL}				2.7	2.8	3.3	3.7	2.7	2.8	3.3	3.7
t_{PZH}	$\overline{OE}$	A	MAX	4	4.1	4.2	4.3	4	4.1	4.2	4.3
t_{PZL}				4	4.1	4.2	4.3	4	4.1	4.2	4.3
t_{PZH}	$\overline{OE}$	B	MAX	4	4.9	7.2	9.3	4	4.9	7.2	9.3
t_{PZL}				4	4.9	7.2	9.3	4	4.9	7.2	9.3
t_{PHZ}	$\overline{OE}$	A	MAX	5	5	5	5	5	5	5	5
t_{PLZ}				5	5	5	5	5	5	5	5
t_{PHZ}	$\overline{OE}$	B	MAX	5	5.2	6.5	7.7	5	5.2	6.5	7.7
t_{PLZ}				5	5.2	6.5	7.7	5	5.2	6.5	7.7

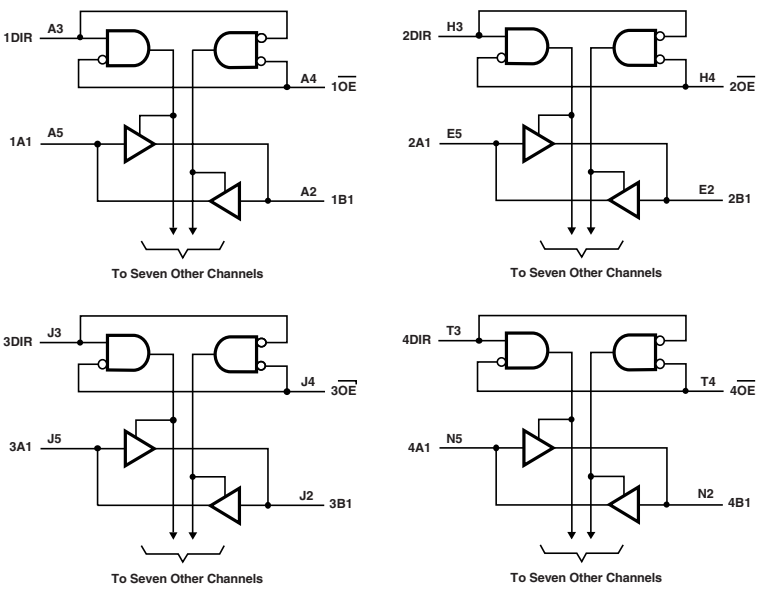
UNIT : ns

32T245

32-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

- Control Inputs V_{IH}/V_{IL} Levels Are Referenced to V_{CCA} Voltage
- V_{CC} Isolation Feature - If Either V_{CC} Input Is at GND, Both Ports Are in the High-Impedance State
- Overvoltage-Tolerant Inputs / Outputs Allow Mixed-Voltage-Mode Data Communications
- This 24-Bit Noninverting Bus Transceiver Uses Two Separate Configurable Power-Supply Rails
- Designed for asynchronous Communication Between Data Buses

Logic Diagram



FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

: **PREVIEW**

RECOMMENDED OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTECS

PARAMETER	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.8V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.8V	UNIT
I_{CC}*	MAX	0.09	0.09	0.09	0.09	0.09	0.09	0.09	0.09	mA
I_{OH}	MAX	-12	-9	-8	-6	-12	-9	-8	-6	mA
I_{OL}	MAX	12	9	8	6	12	9	8	6	mA

*I_{CCA} + I_{CCB}

SWITCHING CHARACTERISTICS

V_{CCA} = 1.5V

PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
t_{PLH}	A	B	MAX	3.7	4.1	5.2	6.2	3.7	4.1	5.2	6.2
t_{PHL}				3.7	4.1	5.2	6.2	3.7	4.1	5.2	6.2
t_{PLH}	B	A	MAX	5.5	5.6	5.9	6.2	5.5	5.6	5.9	6.2
t_{PHL}				5.5	5.6	5.9	6.2	5.5	5.6	5.9	6.2
t_{PZH}	$\overline{OE}$	A	MAX	10.1	10.1	10.1	10.1	10.1	10.1	10.1	10.1
t_{PZL}				10.1	10.1	10.1	10.1	10.1	10.1	10.1	10.1
t_{PZH}	$\overline{OE}$	B	MAX	5.2	5.9	8.1	10.1	5.2	5.9	8.1	10.1
t_{PZL}				5.2	5.9	8.1	10.1	5.2	5.9	8.1	10.1
t_{PHZ}	$\overline{OE}$	A	MAX	9.1	9.1	9.1	9.1	9.1	9.1	9.1	9.1
t_{PLZ}				9.1	9.1	9.1	9.1	9.1	9.1	9.1	9.1
t_{PHZ}	$\overline{OE}$	B	MAX	6.3	6.5	7.5	8.7	6.3	6.5	7.5	8.7
t_{PLZ}				6.3	6.5	7.5	8.7	6.3	6.5	7.5	8.7

UNIT : ns

V_{CCA} = 1.8V

PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
t_{PLH}	A	B	MAX	3.3	3.7	4.8	5.9	3.3	3.7	4.8	5.9
t_{PHL}				3.3	3.7	4.8	5.9	3.3	3.7	4.8	5.9
t_{PLH}	B	A	MAX	4.4	4.5	4.8	5.2	4.4	4.5	4.8	5.2
t_{PHL}				4.4	4.5	4.8	5.2	4.4	4.5	4.8	5.2
t_{PZH}	$\overline{OE}$	A	MAX	7.8	7.8	7.8	7.8	7.8	7.8	7.8	7.8
t_{PZL}				7.8	7.8	7.8	7.8	7.8	7.8	7.8	7.8
t_{PZH}	$\overline{OE}$	B	MAX	4.5	5.3	7.4	9.2	4.5	5.3	7.4	9.2
t_{PZL}				4.5	5.3	7.4	9.2	4.5	5.3	7.4	9.2
t_{PHZ}	$\overline{OE}$	A	MAX	7.7	7.7	7.7	7.7	7.7	7.7	7.7	7.7
t_{PLZ}				7.7	7.7	7.7	7.7	7.7	7.7	7.7	7.7
t_{PHZ}	$\overline{OE}$	B	MAX	5.7	5.9	7.1	8.4	5.7	5.9	7.1	8.4
t_{PLZ}				5.7	5.9	7.1	8.4	5.7	5.9	7.1	8.4

UNIT : ns

V_{CCA} = 2.5V

PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
t_{PLH}	A	B	MAX	2.8	3.3	4.5	5.6	2.8	3.3	4.5	5.6
t_{PHL}				2.8	3.3	4.5	5.6	2.8	3.3	4.5	5.6
t_{PLH}	B	A	MAX	3.2	3.3	3.7	4.1	3.2	3.3	3.7	4.1
t_{PHL}				3.2	3.3	3.7	4.1	3.2	3.3	3.7	4.1
t_{PZH}	$\overline{OE}$	A	MAX	5.3	5.3	5.3	5.3	5.3	5.3	5.3	5.3
t_{PZL}				5.3	5.3	5.3	5.3	5.3	5.3	5.3	5.3
t_{PZH}	$\overline{OE}$	B	MAX	4.5	5.1	7.3	9.4	4.5	5.1	7.3	9.4
t_{PZL}				4.5	5.1	7.3	9.4	4.5	5.1	7.3	9.4
t_{PHZ}	$\overline{OE}$	A	MAX	6.1	6.1	6.1	6.1	6.1	6.1	6.1	6.1
t_{PLZ}				6.1	6.1	6.1	6.1	6.1	6.1	6.1	6.1
t_{PHZ}	$\overline{OE}$	B	MAX	5.2	6.1	6.6	7.9	5.2	6.1	6.6	7.9
t_{PLZ}				5.2	6.1	6.6	7.9	5.2	6.1	6.6	7.9

UNIT : ns

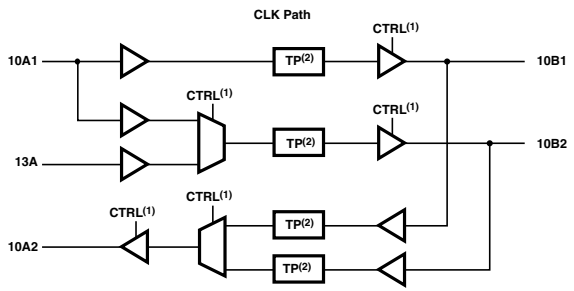
V_{CCA} = 3.3V											
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3.3V	AVC 2.5V	AVC 1.8V	AVC 1.5V	AVCH 3.3V	AVCH 2.5V	AVCH 1.8V	AVCH 1.5V
t_{PLH}	A	B	MAX	2.7	3.2	4.4	5.5	2.7	3.2	4.4	5.5
t_{PHL}				2.7	3.2	4.4	5.5	2.7	3.2	4.4	5.5
t_{PLH}	B	A	MAX	2.7	2.8	3.3	3.7	2.7	2.8	3.3	3.7
t_{PHL}				2.7	2.8	3.3	3.7	2.7	2.8	3.3	3.7
t_{PZH}	$\overline{OE}$	A	MAX	4	4.1	4.2	4.3	4	4.1	4.2	4.3
t_{PZL}				4	4.1	4.2	4.3	4	4.1	4.2	4.3
t_{PZH}	$\overline{OE}$	B	MAX	4	4.9	7.2	9.3	4	4.9	7.2	9.3
t_{PZL}				4	4.9	7.2	9.3	4	4.9	7.2	9.3
t_{PHZ}	$\overline{OE}$	A	MAX	5	5	5	5	5	5	5	5
t_{PLZ}				5	5	5	5	5	5	5	5
t_{PHZ}	$\overline{OE}$	B	MAX	5	5.2	6.5	7.7	5	5.2	6.5	7.7
t_{PLZ}				5	5.2	6.5	7.7	5	5.2	6.5	7.7

UNIT : ns

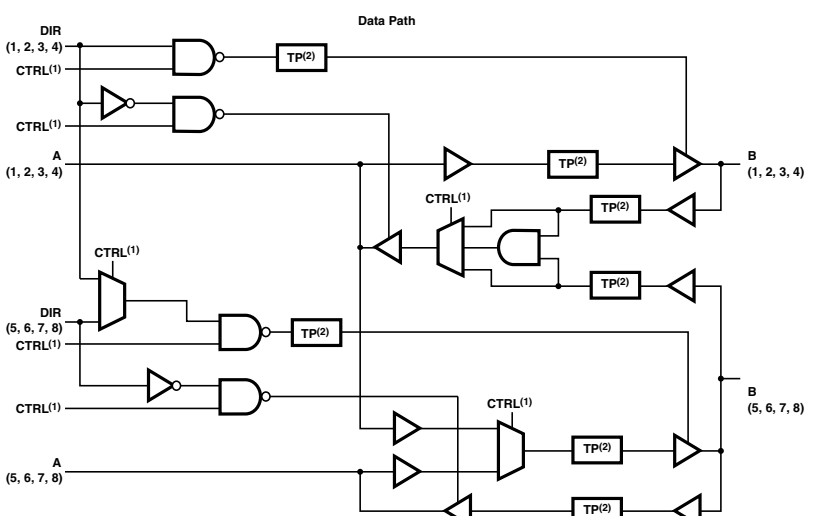
MMC, SD CARD, Memory Stick, SmartMedia, AND xD-Picture Card ±15-kV ESD-PROTECTED VOLTAGE-TRANSLATION TRANCEIVER

- Transceiver for Memory Card Interface
  [MultiMediaCard (MMC), Secure Digital (SD), Memory Stick™ Complliant Products, SmartMedia Card, and xD-Picture Card™]
- For Low-Power Operation, A ports Are Placed in High-Impedance State When Card-Side Supply Voltage Is Switched Off

Logic Diagram

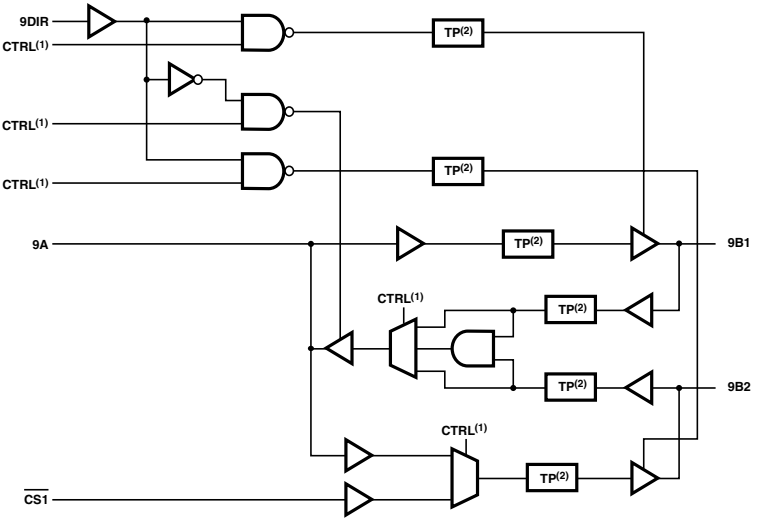


(1) CTRL represents a decoded MODE0, MODE1, $\overline{CS0}$, and $\overline{CS1}$ state.
(2) Translation point



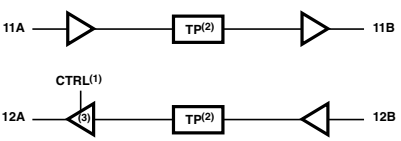
(1) CTRL represents a decoded MODE0, MODE1, $\overline{CS0}$, and $\overline{CS1}$ state.
(2) Translation point

CMD Path



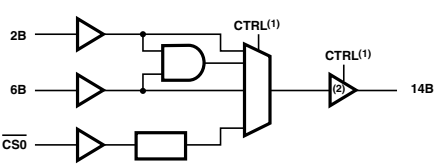
(1) CTRL represents a decoded MODE0, MODE1, $\overline{CS0}$, and $\overline{CS1}$ state.
(2) Translation point

$\overline{WP}$ and R/B Paths



(1) CTRL represents a decoded MODE0, MODE1, $\overline{CS0}$, and $\overline{CS1}$ state.
(2) Translation point
(3) 12A is open drain in NAND (XD) mode and pushúpull in other modes.

$\overline{IRQ}$ and CEout Paths



(1) CTRL represents a decoded MODE0, MODE1, $\overline{CS0}$, and $\overline{CS1}$ state.
(2) Pushúpull in NAND flash (XD) mode and open drain in other modes

: PREVIEW

ELECTRICAL CHARACTERISTICS

PARAMETER	MAX or MIN	AVCA V_{CCA} = 3.3V V_{CCB} = 0V	AVCA V_{CCA} = 3.3V VCCB = 3.3V	AVCA V_{CCA} = 2.5V V_{CCB} = 2.5V	AVCA V_{CCA} = 1.8V V_{CCB} = 0V	AVCA V_{CCA} = 1.8V VCCB = 1.8V	AVCA V_{CCA} = 1.5V V_{CCB} = 1.5V	UNIT
I_{CCA}	MAX	0.01	0.01	0.0055	0.005	0.005	0.0045	mA
I_{CCB}	MAX	0.01	0.001	0.0075	0.0005	0.007	0.0065	mA

RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	AVCA 3.3V	AVCA 2.5V	AVCA 1.8V	AVCA 1.5V	UNIT
I_{OH}	A port	MAX	-8	-4	-2	-1	mA
I_{OL}			8	4	2	1	mA
I_{OH}	B port	MAX	-16	-8	-4	-2	mA
I_{OL}			16	8	4	2	mA

*I_{O_SD} = 0

SWITCHING CHARACTERISTICS

V_{CCA} = 1.5V						
PARAMETER	INPUT (FROM	OUTPUT (TO)	MAX or MIN	AVCA V_{CCA} 3.3V	AVCA V_{CCA} 2.5V	AVCA V_{CCA} 1.8V
t_{pd}	A	B	MAX	4.4	4.9	7.7
t_{pd}	B	A	MAX	5	5	6.3
t_{pd}	CLK, or SCLK.h	CLK, or SCLK.0	MAX	4.9	5	7.7
t_{pd}	CLK, or SCLK.h	CLK, or SCLK.-f.h	MAX	9.7	12	19
t_{pd}	CMD.h	CMD.0	MAX	3.6	4.1	7.1
t_{pd}	CMD.h	CMD.1	MAX	4.2	4.6	7
t_{pd}	CMD.0	CMD.h	MAX	4.7	4.9	6.2
t_{pd}	CS0	B	MAX	3.9	4.2	6
t_{pd}	R/B	R/B.h	MAX	4.8	4.8	5.7
t_{pd}	WE	WE.h	MAX	4.2	4.3	7.4
t_{pd}	WP	WP.h	MAX	4.3	4.5	6.6
t_{en}	DAT1.0 or DATA1.0	IRQ	MAX	3.3	3.3	4.8
t_{en}	DAT1.0 or DATA1.1	IRQ	MAX	3.3	3.4	4.9
t_{en}	DIR	B	MAX	4.6	4.5	6.7
t_{en}	DIR	A	MAX	9.5	9.6	10.3
t_{en}	R/B	R/B.h open drain	MAX	5.4	5.4	5.9
t_{dis}	DAT1.0 or DATA1.0	IRQ	MAX	5.5	4.9	6.7
t_{dis}	DAT1.0 or DATA1.1	IRQ	MAX	5.4	4.7	6.5
t_{dis}	DIR	B	MAX	6.3	6.4	6.9
t_{dis}	DIR	A	MAX	5.2	5.3	5.3
t_{dis}	R/B	R/B.h open drain	MAX	4.1	17.4	16.9

UNIT : ns

V_{CCA} = 1.8V						
PARAMETER	INPUT (FROM	OUTPUT (TO)	MAX or MIN	AVCA V_{CCA} 3.3V	AVCA V_{CCA} 2.5V	AVCA V_{CCA} 1.8V
t_{pd}	A	B	MAX	3.7	4.6	7.5
t_{pd}	B	A	MAX	4	4.2	4.6
t_{pd}	CLK, or SCLK.h	CLK, or SCLK.0	MAX	4,2	4.8	8
t_{pd}	CLK, or SCLK.h	CLK, or SCLK.-f.h	MAX	8.3	9.4	17.9
t_{pd}	CMD.h	CMD.0	MAX	3.3	3.7	7.4
t_{pd}	CMD.h	CMD.1	MAX	3.5	4.4	6.2
t_{pd}	CMD.0	CMD.h	MAX	3.8	4	4.5
t_{pd}	CS0	B	MAX	3.8	4	6.6
t_{pd}	R/B	R/B.h	MAX	3.8	4	4.4
t_{pd}	WE	WE.h	MAX	3.7	3.9	7.3
t_{pd}	WP	WP.h	MAX	3.8	4	5.6
t_{en}	DAT1.0 or DATA1.0	IRQ	MAX	3.3	3.3	5
t_{en}	DAT1.0 or DATA1.1	IRQ	MAX	3.1	3.1	4.6
t_{en}	DIR	B	MAX	3.6	3.8	6.4
t_{en}	DIR	A	MAX	6.9	6.9	7.7
t_{en}	R/B	R/B.h open drain	MAX	4.1	4.1	4.4
t_{dis}	DAT1.0 or DATA1.0	IRQ	MAX	5.5	4.8	6.5
t_{dis}	DAT1.0 or DATA1.1	IRQ	MAX	5.3	4.8	6.6
t_{dis}	DIR	B	MAX	5.7	5.4	6.3
t_{dis}	DIR	A	MAX	5.2	5.3	5.2
t_{dis}	R/B	R/B.h open drain	MAX	3.8	19.5	15.9

UNIT : ns

V_{CCA} = 2.5V					
PARAMETER	INPUT (FROM	OUTPUT (TO)	MAX or MIN	AVCA V_{CCA} 3.3V	AVCA V_{CCA} 2.5V
t_{pd}	A	B	MAX	3,1	4
t_{pd}	B	A	MAX	3,6	3.7
t_{pd}	CLK, or SCLK.h	CLK, or SCLK.0	MAX	3,5	3.9
t_{pd}	CLK, or SCLK.h	CLK, or SCLK.-f.h	MAX	7	8.3
t_{pd}	CMD.h	CMD.0	MAX	2,7	3.2
t_{pd}	CMD.h	CMD.1	MAX	2,8	3.6
t_{pd}	CMD.0	CMD.h	MAX	3	3
t_{pd}	CS0	B	MAX	3.3	4.2
t_{pd}	R/B	R/B.h	MAX	2.9	3.1
t_{pd}	WE	WE.h	MAX	3	3.6
t_{pd}	WP	WP.h	MAX	2.9	3.5
t_{en}	DAT1.0 or DATA1.0	IRQ	MAX	3.2	3.3
t_{en}	DAT1.0 or DATA1.1	IRQ	MAX	3.2	3.6
t_{en}	DIR	B	MAX	3.6	4.7
t_{en}	DIR	A	MAX	5.1	5.3
t_{en}	R/B	R/B.h open drain	MAX	3	3.2
t_{dis}	DAT1.0 or DATA1.0	IRQ	MAX	5.4	7.2
t_{dis}	DAT1.0 or DATA1.1	IRQ	MAX	5.4	7
t_{dis}	DIR	B	MAX	5.1	4.5
t_{dis}	DIR	A	MAX	3.7	3.7
t_{dis}	R/B	R/B.h open drain	MAX	3.9	3.2

UNIT : ns

V_{CCA} = 3.3V				
PARAMETER	INPUT (FROM	OUTPUT (TO)	MAX or MIN	AVCA V_{CCA} 3.3V
t_{pd}	A	B	MAX	2.9
t_{pd}	B	A	MAX	3.8
t_{pd}	CLK, or SCLK.h	CLK, or SCLK.0	MAX	3.3
t_{pd}	CLK, or SCLK.h	CLK, or SCLK.-f.h	MAX	6.1
t_{pd}	CMD.h	CMD.0	MAX	2.7
t_{pd}	CMD.h	CMD.1	MAX	2.7
t_{pd}	CMD.0	CMD.h	MAX	2.6
t_{pd}	CS0	B	MAX	3.7
t_{pd}	R/B	R/B.h	MAX	2.5
t_{pd}	WE	WE.h	MAX	3
t_{pd}	WP	WP.h	MAX	2.8
t_{en}	DAT1.0 or DATA1.0	IRQ	MAX	3.2
t_{en}	DAT1.0 or DATA1.1	IRQ	MAX	3.2
t_{en}	DIR	B	MAX	3.7
t_{en}	DIR	A	MAX	4.7
t_{en}	R/B	R/B.h open drain	MAX	4.9
t_{dis}	DAT1.0 or DATA1.0	IRQ	MAX	5.3
t_{dis}	DAT1.0 or DATA1.1	IRQ	MAX	5.2
t_{dis}	DIR	B	MAX	5
t_{dis}	DIR	A	MAX	4.7
t_{dis}	R/B	R/B.h open drain	MAX	6

UNIT : ns

: PREVIEW

MAXIMUM FREQUENCY AND OUTPUT SKEW

V_{CCB} = 3.3V									
PARAMETER		INPUT (FROM	OUTPUT (TO)	MAX or MIN	AVCA V_{CCA} 3.3V	AVCA V_{CCA} 2.5V	AVCA V_{CCA} 1.8V	AVCA V_{CCA} 1.5V	UNIT
f_{max}	Clock	A	B	MIN	52	52	52	52	MHz
		B	A		52	52	52	52	MHz
	Data	A	B	MIN	26	26	26	26	MHz
		B	A		26	26	26	26	MHz
$t_{sk(o)}$		A	B	MAX	0.7	0.7	0.8	1.5	ns

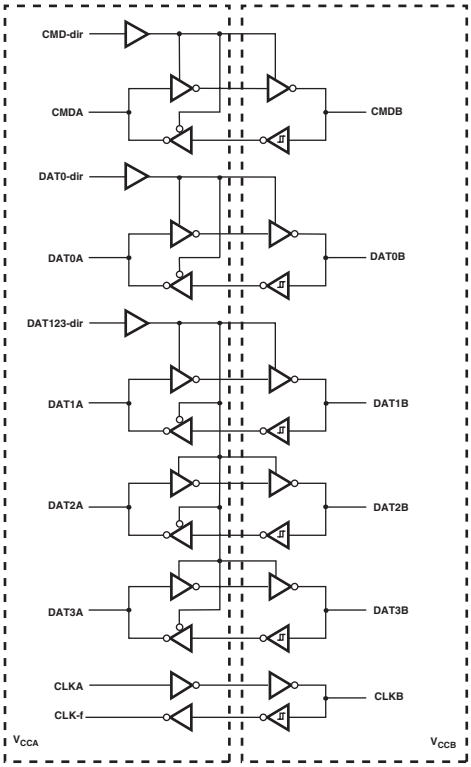
UNIT : ns

406L

MMC, SD CARD, Memory Stick, SmartMedia, AND xD-Picture Card ±15-kV ESD-PROTECTED VOLTAGE-TRANSLATION TRANCEIVER

- Transceiver for Memory Card Interface
  [MultiMediaCard (MMC), Secure Digital (SD), Memory Stick™ Complliant Products]
- For Low-Power Operation, A and B ports Are Placed in High-Impedance State When Either Supply Voltage Is Switched Off

Logic Diagram



FUNCTION TABLES

CONTROL INPUT CMD-dir	OUTPUT CIRCUITS		OPERATION
	CMDA	CMDB	
High	Hi-Z	Enabled	CMDA to CMDB
Low	Enabled	Hi-Z	CMDB to CMDA

CONTROL INPUT DAT0-dir	OUTPUT CIRCUITS		FUNCTION
	DAT0A	DAT0B	
High	Hi-Z	Enabled	DAT0A to DAT0B
Low	Enabled	Hi-Z	DAT0B to DAT0A

: **PREVIEW**

ELECTRICAL CHARACTERISTICS

PARAMETER	MAX or MIN	AVCA V_{CCA} = 3.3V V_{CCB} = 0V	AVCA V_{CCA} = 0V V_{CCB} = 3.3V	AVCA V_{CCA} = 1.2 to 3.3V V_{CCB} = 1.2 to 3.3V	UNIT
I_{CCA}	MAX	0.01	-0.001	10	mA
I_{CCB}	MAX	-0.001	0.01	10	mA
$I_{CCA} + I_{CCB}$	MAX	-	-	15	mA

RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	AVCA 3.3V	AVCA 2.5V	AVCA 1.8V	AVCA 1.5V	UNIT
I_{OH}	A port	MAX	-8	-4	-2	-1	mA
I_{OL}			8	4	2	1	mA
I_{OH}	B port	MAX	-16	-8	-4	-2	mA
I_{OL}			16	8	4	2	mA

*I_{O_SD} = 0

SWITCHING CHARACTERISTICS

V_{CCA} = 1.5V

PARAMETER	INPUT (FROM	OUTPUT (TO)	MAX or MIN	AVCA V_{CCA} 3.3V	AVCA V_{CCA} 2.5V	AVCA V_{CCA} 1.8V	AVCA V_{CCA} 1.5V
t_{pd}	A	B	MAX	3.8	3.9	4.8	5.6
t_{pd}	B	A	MAX	5.2	5.2	5.6	6
t_{pd}	CLKA	CLKB	MAX	3.8	3.9	4.8	5.6
t_{pd}		CLK-f	MAX	9	9.1	10.4	116
t_{pd}	CMDA	CMDB	MAX	3.8	3.9	4.8	5.6
t_{pd}	CMDB	CMDA	MAX	5.2	5.2	5.6	6
t_{en}	DIR	B	MAX	5.9	6.1	6.9	7.7
t_{en}		A	MAX	7.7	8.2	7.4	7
t_{dis}	DIR	B	MAX	11.4	8.7	10.4	8.9
t_{dis}		A	MAX	6.6	6.5	6.8	7

UNIT : ns

V_{CCA} = 1.8V

PARAMETER	INPUT (FROM	OUTPUT (TO)	MAX or MIN	AVCA V_{CCA} 3.3V	AVCA V_{CCA} 2.5V	AVCA V_{CCA} 1.8V	AVCA V_{CCA} 1.5V
t_{pd}	A	B	MAX	3.1	3.5	4.4	5.2
t_{pd}	B	A	MAX	4.3	4.3	4.8	5.2
t_{pd}	CLKA	CLKB	MAX	3.1	3.5	4.4	5.2
t_{pd}		CLK-f	MAX	7.4	7.8	9.1	10.4
t_{pd}	CMDA	CMDB	MAX	3.1	3.5	4.4	5.2
t_{pd}	CMDB	CMDA	MAX	4.3	4.3	4.8	5.2
t_{en}	DIR	B	MAX	4.8	5.1	6	6.8
t_{en}		A	MAX	5.3	5.1	5.2	4.7
t_{dis}	DIR	B	MAX	8.2	8.2	9.5	8.4
t_{dis}		A	MAX	7.6	7.5	7.9	7.7

UNIT : ns

V_{CCA} = 2.5V

PARAMETER	INPUT (FROM	OUTPUT (TO)	MAX or MIN	AVCA V_{CCA} 3.3V	AVCA V_{CCA} 2.5V	AVCA V_{CCA} 1.8V	AVCA V_{CCA} 1.5V
t_{pd}	A	B	MAX	2.5	2.9	3.8	4.7
t_{pd}	B	A	MAX	3.2	3.3	3.9	4.4
t_{pd}	CLKA	CLKB	MAX	2.5	2.9	3.8	4.7
t_{pd}		CLK-f	MAX	5.7	6.2	7.7	9.1
t_{pd}	CMDA	CMDB	MAX	2.5	2.9	3.8	4.7
t_{pd}	CMDB	CMDA	MAX	3.2	3.3	3.9	4.4
t_{en}	DIR	B	MAX	3.6	3.9	4.8	5.7
t_{en}		A	MAX	4.7	4.4	4.3	3.5
t_{dis}	DIR	B	MAX	7.5	7.2	8.4	7.6
t_{dis}		A	MAX	5.8	5.5	5.4	5.6

UNIT : ns

V_{CCA} = 3.3V							
PARAMETER	INPUT (FROM	OUTPUT (TO)	MAX or MIN	AVCA V_{CCA} 3.3V	AVCA V_{CCA} 2.5V	AVCA V_{CCA} 1.8V	AVCA V_{CCA} 1.5V
t_{pd}	A	B	MAX	2.3	2.7	3.6	4.5
t_{pd}	B	A	MAX	2.7	3	3.7	4.3
t_{pd}	CLKA	CLKB	MAX	2.3	2.7	3.6	4.5
t_{pd}		CLK-f	MAX	5	5.7	7.3	8.8
t_{pd}	CMDA	CMDB	MAX	2.3	2.7	3.6	4.5
t_{pd}	CMDB	CMDA	MAX	2.7	3	3.7	4.3
t_{en}	DIR	B	MAX	3	3.4	4.3	5.1
t_{en}		A	MAX	5.4	5.4	5.4	3.1
t_{dis}	DIR	B	MAX	7.3	7	8.3	7.4
t_{dis}		A	MAX	8	7.9	7.9	8.1

UNIT : ns

MAXIMUM FREQUENCY

PARAMETER		INPUT (FROM	OUTPUT (TO)	MAX or MIN	AVCA V_{CCA} 3.3V	AVCA V_{CCA} 2.5V	AVCA V_{CCA} 1.8V	AVCA V_{CCA} 1.5V	UNIT
f_{max}	Clock	CLKA	CLKB	MIN	95	95	95	95	MHz
			CLK-f		95	95	95	95	MHz
	Data	A	B	MIN	95	95	95	95	MHz
		B	A		95	95	95	95	MHz

OUTPUT SKEW

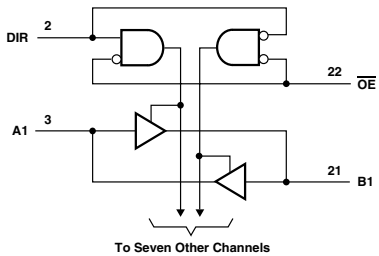
PARAMETER	V_{CCA}	INPUT (FROM	OUTPUT (TO)	MAX or MIN	AVCA V_{CCA} 3.3V	AVCA V_{CCA} 2.5V	AVCA V_{CCA} 1.8V	AVCA V_{CCA} 1.5V	UNIT
$t_{sk(o)}$	3.3V	DIR	B	MIN	0.4	0.3	0.4	0.3	ns
	2.5V	DIR	B	MIN	0.3	0.2	0.3	0.3	ns
	1.8V	DIR	B	MIN	0.3	0.3	0.3	0.3	ns
	1.5V	DIR	B	MIN	0.4	0.3	0.3	0.3	ns

: **PREVIEW**

3245

OCTAL BUS TRANSCEIVER WITH ADJUSTABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	V_{CCA}(V)	V_{CCB}(V)	LVCC	UNIT
I_{CCA}	B to A	MAX	3.6	3.6	0.05	mA
				5.5	0.05	mA
I_{CCB}	A to B	MAX	3.6	3.6	0.05	mA
				5.5	0.08	mA
I_{OHA}		MAX	2.3	3.0	-8	mA
			2.7		-12	
			3.3		-24	
I_{OHB}		MAX	2.3	3.3	-8	mA
			2.7		-12	
			3.3	3.0	-24	
I_{OLA}		MAX	2.3	3.0	8	mA
			2.7		12	
			3.3		24	
I_{OLB}		MAX	2.3	3.3	8	mA
			2.7		12	
			3.3	3.0	24	

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVCC V_{CCA} = 2.3V V_{CCB} = 3.0V	LVCC V_{CCA} = 2.7V V_{CCB} = 5.5V	LVCC V_{CCA} = 3.6V V_{CCB} = 5.5V	LVCC V_{CCA} = 2.7V V_{CCB} = 3.0V	LVCC V_{CCA} = 3.6V V_{CCB} = 3.0V
t_{PLH}	A	B	MAX	9.4	6.0	6.0	7.1	7.1
t_{PHL}				9.1	5.3	5.3	7.2	7.2
t_{PLH}	B	A	MAX	11.2	5.8	5.8	6.4	6.4
t_{PHL}				9.9	7.0	7.0	7.6	7.6
t_{PZL}	$\overline{OE}$	$\overline{A}$	MAX	14.5	9.2	9.2	9.7	9.7
t_{PZH}				12.9	9.5	9.5	9.5	9.5
t_{PZL}	$\overline{OE}$	$\overline{B}$	MAX	13	8.1	8.1	9.2	9.2
t_{PZH}				12.8	8.4	8.4	9.9	9.9
t_{PLZ}	$\overline{OE}$	$\overline{A}$	MAX	7.1	7.0	7.0	6.6	6.6
t_{PHZ}				6.9	7.8	7.8	6.9	6.9
t_{PLZ}	$\overline{OE}$	$\overline{B}$	MAX	8.8	7.3	7.3	7.5	7.5
t_{PHZ}				8.9	7.0	7.0	7.9	7.9

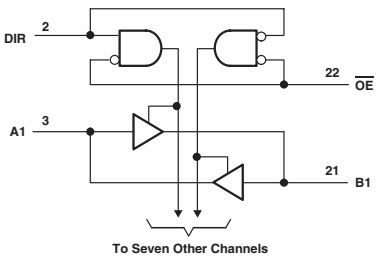
UNIT: ns

4245

OCTAL BUS TRANSCEIVER AND 3.3-V TO 5-V SHIFTER WITH 3-STATE OUTPUTS (SN74LVC4245A)

OCTAL DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS (SN74LVCC4245A)

Logic Diagram



FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LVC	LVCC	UNIT
I_{CCA}	V_{CCA}=5.5V V_{CCB}=5.5V	MAX	0.08	0.08	mA
	V_{CCA}=5.5V V_{CCB}=3.6V	MAX	0.08	0.08	mA
I_{CCB}	V_{CCA}=5.5V V_{CCB}=5.5V	MAX	0.05	0.08	mA
	V_{CCA}=5.5V V_{CCB}=3.6V	MAX	0.05	0.05	mA
I_{OH}	V_{CCB}=3.3V	MAX	-24	-24	mA
I_{OL}			24	24	
I_{OH}	V_{CCB}=2.7V	MAX	-12	-24	mA
I_{OL}			12	24	
I_{OH}	V_{CCA}=4.5V	MAX	-24	-24	mA
I_{OL}			24	24	

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC		LVCC		
				V_{CCA}=5.5V V_{CCB}=2.7V	V_{CCA}=5.5V V_{CCB}=3.6V	V_{CCA}=5.5V V_{CCB}=5.5V	V_{CCA}=5.5V V_{CCB}=2.7V	V_{CCA}=5.5V V_{CCB}=3.6V
t_{PLH}	A	B	MAX	6.3	6.3	7.1	7.0	7.0
t_{PHL}				6.7	6.7	6.0	7.0	7.0
t_{PLH}	B	A	MAX	6.1	6.1	6.8	6.2	6.2
t_{PHL}				5.0	5.0	6.1	5.3	5.3
t_{PZL}	$\overline{OE}$	A	MAX	9.0	9.0	9.0	9.0	9.0
t_{PZH}				8.1	8.1	8.3	8.0	8.0
t_{PZL}	$\overline{OE}$	B	MAX	8.8	8.8	8.2	10.0	10.0
t_{PZH}				9.8	9.8	8.1	10.2	10.2
t_{PLZ}	$\overline{OE}$	A	MAX	7.0	7.0	4.7	5.2	5.2
t_{PHZ}				5.8	5.8	4.9	5.2	5.2
t_{PLZ}	$\overline{OE}$	B	MAX	7.7	7.7	5.4	5.4	5.4
t_{PHZ}				7.8	7.8	6.3	7.4	7.4

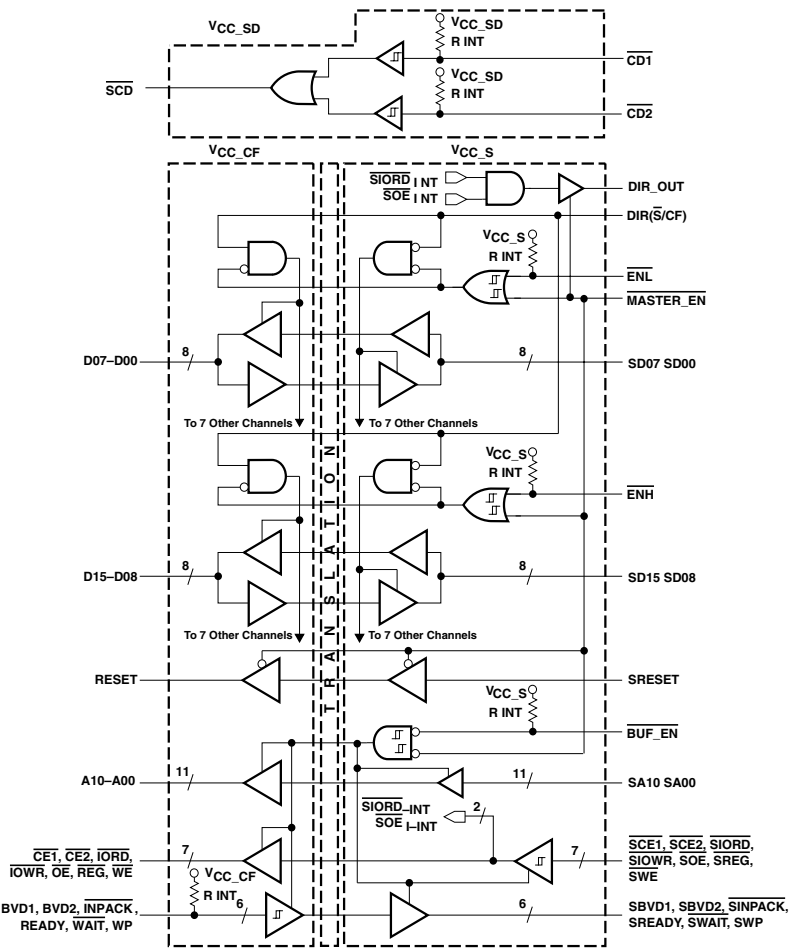
UNIT: ns

: **PREVIEW**

LOW-POWER, DUAL-SUPPLY, LEVEL-TRANSLATING CompactFlash™ INTERFACE WITH 16-BIT DATA, 11-BIT ADDRESS, AND 13-BIT CONTROL LINES

- Designed to Optimize Power Savings in Portable Applications
- Matched Pinout with CompactFlash™ (CF) Connector Pin Configurations to Optimize PCB Layout
- Input-Disable Feature Allows Floating Input Conditions

Logic Diagram



NOTE: R INT ≥ 100 kΩ

FUNCTION TABLES

Lower 8-Bit Data Bus Transceivers (D07-D00, SD07-SD00)

INPUTS			OPERATION
MASTER_EN	ENL	DIR (S/CF)	
L	L	H	SD data to D bus
L	L	L	D data to SD bus
L	H	X	Isolation. D07-D00 and SD07-SD00 inputs can float.
H	X	X	Isolation, low power mode

X = H or L

Upper 8-Bit Data Bus Transceivers (D15-D08, SD15-SD08)

INPUTS			OPERATION
MASTER_EN	ENH	DIR (S/CF)	
L	L	H	SD data to D bus
L	L	L	D data to SD bus
L	H	X	Isolation. D15-D08 and SD15-SD08 inputs can float.
H	X	X	Isolation, low power mode

X = H or L

Address Bus Buffers

INPUTS			OUTPUT A
MASTER_EN	BUF_EN	SA	
L	L	H	H
L	L	L	L
L	H	X	Z. SA inputs can float.
H	X	X	Z, low power mode

X = H or L

Command Line Buffers
(BVD1, BVD2, INPACK, OE, IORD, IOWR, READY, REG, CE1, CE2, WAIT, WE, WP,)

INPUTS			OUTPUT
MASTER_EN	BUF_EN	INPUT	
L	L	H	H
L	L	L	L
L	H	X	Z. Command line buffer inputs can float.
H	X	X	Z, low power mode

X = H or L

Reset

INPUTS		OUTPUT RESET
MASTER_EN	SRESET	
L	H	H
L	L	L
H	X	Z, low power mode

X = H or L

DIR_OUT

INPUTS				OUTPUT DIR_OUT
BUF_EN	MASTER_EN	SOE	SIORD	
L	L	L	L	L
L	L	L	H	L
L	L	H	L	L
L	L	H	H	H
H	L	X	X	L
X	H	X	X	Z, low power mode

X = H or L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER			MAX or MIN	LV 5V	LV 3.3V	LV 2.5V	LV 1.8V	UNIT
I_{CC_SD}	$\overline{CD1}$ and $\overline{CD2}$ = V_{CC_SD}		MAX	0.001	-	-	-	mA
	$\overline{CD1}$ or $\overline{CD2}$ = GND, $\overline{CD1}$ or $\overline{CD2}$ = V_{CC_SD}		MAX	0.01	-	-	-	mA
I_{CC_S}*	Inputs SD12-SD00, SA10-SA00, $\overline{SCE1}$, $\overline{SCE2}$, $\overline{SIORD}$ $\overline{SIOWR}$, $\overline{SOE}$, $\overline{SREG}$, $\overline{SWE}$		MAX	-	0.003	0.003	0.003	mA
	Control inputs ($\overline{ENL}$, $\overline{ENH}$, $\overline{BUF\_EN}$)	V_{CC_S}	MAX	-	0.003	0.003	0.003	mA
		GND, Other = V_{CC_S}		-	0.036	0.036	0.036	mA
I_{CC_CF}	Input (D15- D00)		MAX	-	0.003	0.003	0.003	mA
	Input (BVD1, BVD2, $\overline{INPACK}$, READY, $\overline{WAIT}$, WP)	V_{CC_CF}	MAX	-	0.003	0.003	0.003	mA
		GND, Other = V_{CC_CF}		-	0.06	0.06	0.06	mA
I_{OH}	Card detect		MAX	-12	-8	-4	-2	mA
I_{OL}				12	8	4	2	mA
I_{OH}	System port		MAX	-	12	6	2	mA
I_{OL}				-	12	6	2	mA
I_{OH}	CF port		MAX	16	12	-	-	mA
I_{OL}				16	12	-	-	mA

*I_{O_SD} = 0

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	V_{CC_SD}	LV 5V	LV 3.3V	LV 2.5V	LV 1.8V
t_{PLH}	$\overline{CD1}$ or $\overline{CD2}$	$\overline{SCD}$	MAX	5.5	5.5	6.8	9.1	15.5
t_{PHL}				5.5	5.5	6.8	9.1	15.5

PARAMETER	INPUT	OUTPUT	MAX or MIN	V_{CC_CF}	LV V_{CC_S} 3.3V	LV V_{CC_S} 2.5V	LV V_{CC_S} 1.8V
t_{PLH}	CF input	S output	MAX	3.3V	8.8	10	12.9
t_{PHL}					8.8	10	12.9
t_{PLH}	CF input	S output	MAX	5V	7	8.6	13.9
t_{PHL}					7	8.6	13.9
t_{PZH}	$\overline{MASTER\_EN}$	S output	MAX	3.3V	18.3	22.6	35.5
t_{PZL}					18.3	22.6	35.5
t_{PZH}	$\overline{MASTER\_EN}$	S output	MAX	5V	18.2	22.6	35.6
t_{PZL}					18.2	22.6	35.6
t_{PHZ}	$\overline{MASTER\_EN}$	S output	MAX	3.3V	13.2	14.5	25.1
t_{PLZ}					13.2	14.5	25.1
t_{PHZ}	$\overline{MASTER\_EN}$	S output	MAX	5V	18.2	14.5	23.3
t_{PLZ}					18.2	14.5	23.3
t_{PZH}	$\overline{BUF\_EN}$	S output	MAX	3.3V	18.3	22.6	35.5
t_{PZL}					18.3	22.6	35.5
t_{PZH}	$\overline{BUF\_EN}$	S output	MAX	5V	18.2	22.6	35.6
t_{PZL}					18.2	22.6	35.6
t_{PHZ}	$\overline{BUF\_EN}$	S output	MAX	3.3V	12.3	14.5	24.2
t_{PLZ}					12.3	14.5	24.2
t_{PHZ}	$\overline{BUF\_EN}$	S output	MAX	5V	12.4	14.2	22.8
t_{PLZ}					12.4	14.2	22.8
t_{PLH}	D	SD	MAX	3.3V	8.8	10	13.7
t_{PHL}					8.8	10	13.7
t_{PLH}	D	SD	MAX	5V	7	12.4	13.9
t_{PHL}					7	12.4	13.9
t_{PLH}	SD	D	MAX	3.3V	7.6	8.2	11.1
t_{PHL}					7.6	8.2	11.1
t_{PLH}	SD	D	MAX	5V	6	7	9.6
t_{PHL}					6	7	9.6

UNIT : ns

PARAMETER	INPUT	OUTPUT	MAX or MIN	V_{CC_CF}	LV V_{CC_S} 3.3V	LV V_{CC_S} 2.5V	LV V_{CC_S} 1.8V
t_{PZH}	$\overline{MASTER\_EN}$	D	MAX	3.3V	21.4	23	27.9
t_{PZL}					21.4	23	27.9
t_{PZH}	$\overline{MASTER\_EN}$	D	MAX	5V	20.3	21.8	31
t_{PZL}					20.3	21.8	31
t_{PZH}	$\overline{MASTER\_EN}$	SD	MAX	3.3V	18.3	22.6	36.3
t_{PZL}					18.3	22.6	36.3
t_{PZH}	$\overline{MASTER\_EN}$	SD	MAX	5V	18.2	22.6	36.2
t_{PZL}					18.2	22.6	36.2
t_{PHZ}	$\overline{MASTER\_EN}$	D	MAX	3.3V	15	16.4	20.2
t_{PLZ}					15	16.4	20.2
t_{PHZ}	$\overline{MASTER\_EN}$	D	MAX	5V	12.5	13.8	17.8
t_{PLZ}					12.5	13.8	17.8
t_{PHZ}	$\overline{MASTER\_EN}$	SD	MAX	3.3V	12	14.5	24.2
t_{PLZ}					12	14.5	24.2
t_{PHZ}	$\overline{MASTER\_EN}$	SD	MAX	5V	18.2	14.2	22.8
t_{PLZ}					18.2	14.2	22.8
t_{PZH}	$\overline{ENL}$ or $\overline{ENH}$	D	MAX	3.3V	21.4	22.8	27.2
t_{PZL}					21.4	22.8	27.2
t_{PZH}	$\overline{ENL}$ or $\overline{ENH}$	D	MAX	5V	20.3	21.6	27.8
t_{PZL}					20.3	21.6	27.8
t_{PZH}	$\overline{ENL}$ or $\overline{ENH}$	SD	MAX	3.3V	18.3	22.6	35.5
t_{PZL}					18.3	22.6	35.5
t_{PZH}	$\overline{ENL}$ or $\overline{ENH}$	SD	MAX	5V	18.2	22.6	35.6
t_{PZL}					18.2	22.6	35.6
t_{PHZ}	$\overline{ENL}$ or $\overline{ENH}$	D	MAX	3.3V	15	16.4	20.2
t_{PLZ}					15	16.4	20.2
t_{PHZ}	$\overline{ENL}$ or $\overline{ENH}$	D	MAX	5V	12	13.1	16.6
t_{PLZ}					12	13.1	16.6
t_{PHZ}	$\overline{ENL}$ or $\overline{ENH}$	SD	MAX	3.3V	12	14.5	24.2
t_{PLZ}					12	14.5	24.2
t_{PHZ}	$\overline{ENL}$ or $\overline{ENH}$	SD	MAX	5V	18.2	14.2	22.8
t_{PLZ}					18.2	14.2	22.8

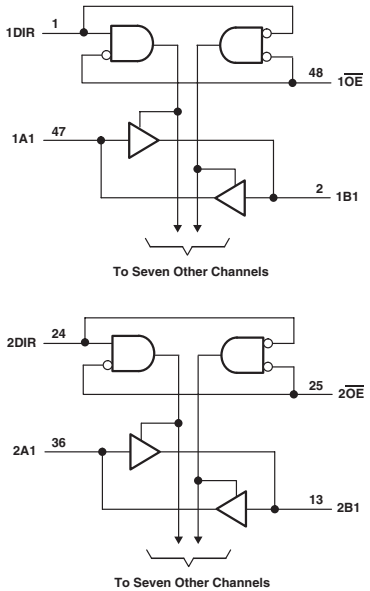
UNIT : ns

: **PREVIEW**

16-BIT TRANSCEIVER AND 3.3-V TO 5-V SHIFTER WITH 3-STATE OUTPUTS

- SN74ALVC164245:
  A port has V_{CCA}, which is set to operate at 2.5 V and 3.3 V
  B port has V_{CCB}, which is set to operate at 3.3 V and 5 V
- SN74AVCB164245, SN74AVCBH164245:
  The A-port is designed to track V_{CCA}, V_{CCA} accepts any supply voltage from 1.4 V to 3.6 V
  The B-port is designed to track V_{CCB}, V_{CCB} accepts any supply voltage from 1.4 V to 3.6 V

Logic Diagram



FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	ALVC	AVCA	AVCAH	AVCB	AVCBH	UNIT
I_{CC}	V_{CCA}=3.6V V_{CCB}=5.5V	MAX	0.04	-	-	-	-	mA
	V_{CCA}=2.3V V_{CCB}=3.3V	MAX	0.02	-	-	-	-	mA
	V_{CCA}=3.6V V_{CCB}=3.6V	MAX	-	0.04	0.04	0.04	0.04	mA
	V_{CCA}=3.6V V_{CCB}=0V	MAX	-	-0.04	-0.04	-0.04	-0.04	mA
	V_{CCA}=0V V_{CCB}=3.6V	MAX	-	0.04	0.04	0.04	0.04	mA
	V_{CCA}=2.7V V_{CCB}=2.7V	MAX	-	0.03	0.03	0.03	0.03	mA
	V_{CCA}=1.6V V_{CCB}=1.6V	MAX	-	0.02	0.02	0.02	0.02	mA
I_{OH}	V_{CCB}=3.3V	MAX	-24	-12	-12	-12	-12	mA
I_{OL}			24	12	12	12	12	
I_{OH}	V_{CCA}=3.0V	MAX	-24	-12	-12	-12	-12	mA
I_{OL}			24	12	12	12	12	
I_{OH}	V_{CCA}=2.3V	MAX	-18	-8	-8	-8	-8	mA
I_{OL}			18	8	8	8	8	
I_{OH}	V_{CCA}=1.4V	MAX	-	-2	-2	-2	-2	mA
I_{OL}			-	2	2	2	2	

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVC		
				V_{CCB}=3.3V V_{CCA}=2.3V	V_{CCB}=5.5V V_{CCA}=2.7V	V_{CCB}=5.5V V_{CCA}=3.3V
t_{PLH}	A	B	MAX	7.6	5.9	5.8
t_{PHL}				7.6	5.9	5.8
t_{PLH}	B	A	MAX	7.6	6.7	5.8
t_{PHL}				7.6	6.7	5.8
t_{PZL}	$\overline{OE}$	B	MAX	11.5	9.3	8.9
t_{PZH}				11.5	9.3	8.9
t_{PZL}	$\overline{OE}$	A	MAX	12.3	10.2	9.1
t_{PZH}				12.3	10.2	9.1
t_{PLZ}	$\overline{OE}$	B	MAX	10.5	9.2	9.5
t_{PHZ}				10.5	9.2	9.5
t_{PLZ}	$\overline{OE}$	A	MAX	9.3	9.0	8.6
t_{PHZ}				9.3	9.0	8.6

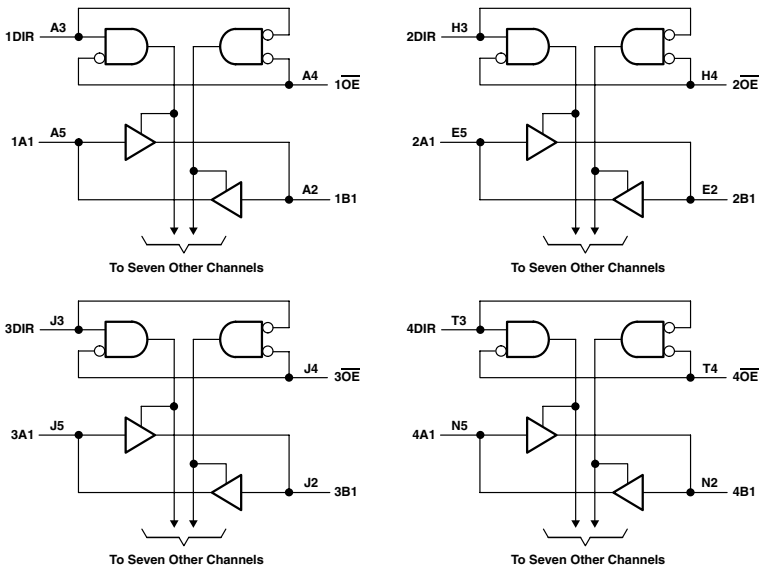
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVCA/AVCAH					
				V_{CCA}=1.4V V_{CCB}=2.3V	V_{CCA}=1.4V V_{CCB}=3.6V	V_{CCA}=2.3V V_{CCB}=1.4V	V_{CCA}=2.3V V_{CCB}=3.6V	V_{CCA}=3.6V V_{CCB}=1.4V	V_{CCA}=3.6V V_{CCB}=2.3V
t_{PLH}	A	B	MAX	5.5	5.8	6.0	3.4	5.9	3.7
t_{PHL}				5.5	5.8	6.0	3.4	5.9	3.7
t_{PLH}	B	A	MAX	7.6	7.3	4.6	3.7	4.5	3.3
t_{PHL}				7.6	7.3	4.6	3.7	4.5	3.3
t_{PZL}	$\overline{OE}$	B	MAX	10.8	10.7	4.1	5.3	2.6	4.1
t_{PZH}				10.8	10.7	4.1	5.3	2.6	4.1
t_{PZL}	$\overline{OE}$	A	MAX	6.3	5.6	7.4	4.5	7.0	5.0
t_{PZH}				6.3	5.6	7.4	4.5	7.0	5.0
t_{PLZ}	$\overline{OE}$	B	MAX	6.5	6.4	4.5	3.7	5.4	3.6
t_{PHZ}				6.5	6.4	4.5	3.7	5.4	3.6
t_{PLZ}	$\overline{OE}$	A	MAX	5.3	6.1	5.7	4.0	5.4	3.3
t_{PHZ}				5.3	6.1	5.7	4.0	5.4	3.3

PARAMETER	INPUT	OUTPUT	MAX or MIN	AVCB/AVCBH					
				V_{CCA}=1.4V V_{CCB}=2.3V	V_{CCA}=1.4V V_{CCB}=3.6V	V_{CCA}=2.3V V_{CCB}=1.4V	V_{CCA}=2.3V V_{CCB}=3.6V	V_{CCA}=3.6V V_{CCB}=1.4V	V_{CCA}=3.6V V_{CCB}=2.3V
t_{PLH}	A	B	MAX	5.5	5.8	6.0	3.4	5.9	3.7
t_{PHL}				5.5	5.8	6.0	3.4	5.9	3.7
t_{PLH}	B	A	MAX	7.6	7.3	4.6	3.7	4.5	3.3
t_{PHL}				7.6	7.3	4.6	3.7	4.5	3.3
t_{PZL}	$\overline{OE}$	B	MAX	10.0	9.8	5.7	5.1	4.9	4.3
t_{PZH}				10.0	9.8	5.7	5.1	4.9	4.3
t_{PZL}	$\overline{OE}$	A	MAX	5.2	4.2	8.5	4.2	8.3	5.2
t_{PZH}				5.2	4.2	8.5	4.2	8.3	5.2
t_{PLZ}	$\overline{OE}$	B	MAX	5.1	4.8	5.8	3.3	6.9	3.8
t_{PHZ}				5.1	4.8	5.8	3.3	6.9	3.8
t_{PLZ}	$\overline{OE}$	A	MAX	3.6	3.0	7.0	3.0	7.0	3.5
t_{PHZ}				3.6	3.0	7.0	3.0	7.0	3.5

UNIT: ns

32-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	AVCB	UNIT
I_{CC}	V_{CCA}=3.6V V_{CCB}=3.6V	MAX	0.08	mA
	V_{CCA}=3.6V V_{CCB}=0V	MAX	-0.08	mA
	V_{CCA}=0V V_{CCB}=3.6V	MAX	0.08	mA
	V_{CCA}=2.7V V_{CCB}=2.7V	MAX	0.04	mA
	V_{CCA}=1.6V V_{CCB}=1.6V	MAX	0.04	mA
I_{OH}	V_{CCB}=3.3V	MAX	-12	mA
I_{OL}			12	
I_{OH}	V_{CCA}=3.0V	MAX	-12	mA
I_{OL}			12	
I_{OH}	V_{CCA}=2.3V	MAX	-8	mA
I_{OL}			8	
I_{OH}	V_{CCA}=1.4V	MAX	-2	mA
I_{OL}			2	

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AVCB					
				V_{CCA}=1.4V V_{CCB}=2.3V	V_{CCA}=1.4V V_{CCB}=3.6V	V_{CCA}=2.3V V_{CCB}=1.4V	V_{CCA}=2.3V V_{CCB}=3.6V	V_{CCA}=3.6V V_{CCB}=1.4V	V_{CCA}=3.6V V_{CCB}=2.3V
t_{PLH}	A	B	MAX	5.5	5.8	6.0	3.4	5.9	3.7
t_{PHL}				5.5	5.8	6.0	3.4	5.9	3.7
t_{PLH}	B	A	MAX	5.9	5.9	5.4	3.7	5.8	3.3
t_{PHL}				5.9	5.9	5.4	3.7	5.8	3.3
t_{PZL}	$\overline{OE}$	B	MAX	7.6	7.5	6.1	4.2	5.1	5.2
t_{PZH}				7.6	7.5	6.1	4.2	5.1	5.2
t_{PZL}	$\overline{OE}$	A	MAX	10.0	9.8	5.7	5.1	4.9	4.3
t_{PZH}				10.0	9.8	5.7	5.1	4.9	4.3
t_{PLZ}	$\overline{OE}$	B	MAX	5.8	5.7	6.0	3.0	5.5	3.5
t_{PHZ}				5.8	5.7	6.0	3.0	5.5	3.5
t_{PLZ}	$\overline{OE}$	A	MAX	5.1	4.8	5.8	3.3	6.9	3.8
t_{PHZ}				5.1	4.8	5.8	3.3	6.9	3.8

UNIT: ns

FUNCTION

1G / 2G / 3G

LITTLE LOGIC GATE (AND/NAND/OR/NOR/EX-OR)

Description	No. of Input	Curcuit	Input	Output	Device	Technology				
						Advanced CMOS		Low-Voltage CMOS		Low-Power CMOS
						AHC	AHCT	LVC	AUC	AUP
POSITIVE AND	2	1			1G08	●	●	●	●	●
		2			2G08			●	●	
	3	1			1G11			●	*	
POSITIVE NAND	2	1			1G00	●	●	●	●	●
				OD	1G38			●		
			SCH		1G132			●		
		2			2G00			●	●	
				OD	2G38			●		
			SCH		2G132					
	3	1			1G10			●	*	
POSITIVE OR	2	1			1G32	●	●	●	●	●
		2			2G32			●	●	
	3	1			1G332			●		
POSITIVE NOR	2	1			1G02	●	●	●	●	●
		2			2G02			●	●	
	3	1			1G27			●		
EXCLUSIVE OR	2	1			1G86	●	●	●	●	
		2			2G86			●	●	
	3	1			1G386			●		
POSITIVE AND-OR	3	1			1G0832			●		
POSITIVE OR-AND	3	1			1G3208			●		

Explanatory notes [Input] SCH: Schmitt-Trigger Inputs
[Output] BUF: Buffered Output OC: Open-Collector Output 3S: 3-State Output

Status ●: Product available in technology indicated *: New product planned in technology indicated

LITTLE LOGIC GATE (INVERTER / NON-INVERTER)

Description	No. of Input	Curcuit	Input	Output	Device	Technology				
						Advanced CMOS		Low-Voltage CMOS		Low-Power CMOS
						AHC	AHCT	LVC	AUC	AUP
INVERTING	1	1		BUF	1G04	●	●	●	●	●
				UBF	1GU04	●		●	●	
				UBF/BUF	1GX04			●		
				OC	1G06			●	●	●
			SCH		1G14	●	●	●	●	●
		2		BUF	2G04			●	●	
				UBF	2GU04			●	●	
				OC	2G06			●	●	
			SCH		2G14			●	*	
		3		BUF	3G04			●		
				UBF	3GU04			●		
				OC	3G06			●		
			SCH		3G14			●		
NON-INVERTING	1	1		OC	1G07			●	●	●
			SCH		1G17			●	●	●
				BUF	1G34			●		●
		2		OC	2G07			●	●	
			SCH		2G17			●		
				BUF	2G34			●	●	
		3		OC	3G07			●		
			SCH		3G17			●		
				BUF	3G34			●		

Explanatory notes [Input] SCH: Schmitt-Trigger Inputs
[Output] BUF: Buffered Output OC: Open-Collector Output 3S: 3-State Output

Status ●: Product available in technology indicated *: New product planned in technology indicated

LITTLE LOGIC BUFFER/DRIVER

Description	Curcuit	Output	Device	Technology				
				Advanced CMOS		Low-Voltage CMOS		Low-Power CMOS
				AHC	AHCT	LVC	AUC	AUP
NON-INVERTING	1	3S	1G125	●	●	●	●	●
		3S	1G126	●	●	●	●	●
	2	3S	2G125			●	●	
		3S	2G126			●	●	
		3S	2G241			●	●	
INVERTING	1	3S	1G240			●	●	●
	2	3S	2G240			●	●	

Explanatory notes [Output] 3S: 3-State Output R3S: Series Resistor and 3-State output OC: Open-Collector Output
Status ●: Product available in technology indicated *: New product planned in technology indicated

LITTLE LOGIC LATCH

Type	Curcuit	PRE · CLR	Output	Q · $\overline{Q}$	Device	Technology				
						Advanced CMOS		Low-Voltage CMOS		Low-Power CMOS
						AHC	AHCT	LVC	AUC	AUP
D	4		3S	Q	373			●		

Explanatory notes [Type] S-R: S-R Latch AD: Addressable Latch BIS: Bistable Latch
R-B: Read-Back Latch D: D-Type Transparent Latch

LITTLE LOGIC D-TYPE FLIP-FLOP

Trigger	Curcuit	Edge	PRE • CLR	Output	Q • $\overline{Q}$	Device	Technology				
							Advanced CMOS		Low-Voltage CMOS		Low-Power CMOS
							AHC	AHCT	LVC	AUC	AUP
POS	1	S	B	2S	B	1G74				●	●
		S		2S	Q	1G79			●	●	●
		S		2S	$\overline{Q}$	1G80			●	●	●
			C	2S	Q	1G175			●		
				3S	Q	1G374			●		
		S	B	2S	B	2G74			●		
		D		2S	Q	2G79			●	●	
		D		2S	$\overline{Q}$	2G80			●	●	

Explanatory notes [Trigger] POS: POSITIVE EDGE, NEG: NEGATIVE EDGE
[PRE • CLR] B: Preset and Clear, C: Clear only
[Edge] S: Single Edge Triggered, D: Dual Edge Triggered
[Output] 2S: Totem pole Output 3S: 3-State Output
[Q • $\overline{Q}$] B: Q • $\overline{Q}$-Output Q: Q-Output $\overline{Q}$: $\overline{Q}$-Output
Status ●: Product available in technology indicated *: New product planned in technology indicated

LITTLE LOGIC DATA SELECTOR/MULTIPLEXER

No. of Input/Output	Output	Curcuit	Device	Technology				
				Advanced CMOS		Low-Voltage CMOS		Low-Power CMOS
				AHC	AHCT	LVC	AUC	AUP
1/2	3S	1	1G18			●		
2/1	2S	1	2G157			●		

Explanatory notes [Output] 2S: Totem Pole Output 3S: 3-State Output OC: Open-Collector Output
Status ●: Product available in technology indicated *: New product planned in technology indicated

LITTLE LOGIC MONOSTABLE MULTIVIBRATOR

Curcuit	CLR	Retrigger	Device	Technology				
				Advanced CMOS		Low-Voltage CMOS		Low-Power CMOS
				AHC	AHCT	LVC	AUC	AUP
1	C	1	1G123			●		

Explanatory notes [CLR] C: With Clear
[Retrigger] R: With Retrigger

LITTLE LOGIC DECODER/DEMULTIPLEXER

No. of Input/Output	Output	Curcuit	Type	Technology				
				Advanced CMOS		Low-Voltage CMOS		Low-Power CMOS
				AHC	AHCT	LVC	AUC	AUP
1/1	2S	1	1G19			●	●	
2/3	2S	1	1G29			●		
2/4	2S	1	1G139			●		

Explanatory notes [Output] 2S: Totem Pole Output 3S: 3-State Output OC: Open-Collector Output
Status ●: Product available in technology indicated *: New product planned in technology indicated

LITTLE LOGIC ANALOG SWITCH

Description	Type	Technology				
		Advanced CMOS		Low-Voltage CMOS		Low-Power CMOS
		AHC	AHCT	LVC	AUC	AUP
DUAL ANALOG MULTIPLEXER/DEMULTIPLEXER	1G3157			●		
DUAL ANALOG MULTIPLEXER/DEMULTIPLEXER	2G53			●	●	
SINGLE BILATERAL ANALOG SWITCH	1G66			●	●	
DUAL BILATERAL ANALOG SWITCH	2G66			●	●	

Status ●: Product available in technology indicated *: New product planned in technology indicated

LITTLE LOGIC MULTIFUNCTION GATE

Description	Input	Type	Technology				
			Advanced CMOS		Low-Voltage CMOS		Low-Power CMOS
			AHC	AHCT	LVC	AUC	AUP
CONFIGURABLE MULTI-FUNCTION GATE AND gate/ AND with both inputs inverted NAND with inverted input OR with inverted input NOR gate / NOR with both inputs inverted XNOR	3	1G57			●		●
CONFIGURABLE MULTI-FUNCTION GATE AND with inverted input NAND gate, NAND with both inputs inverted OR gate / OR with both inputs inverted NOR with inverted input XOR gate	3	1G58			●		●
CONFIGURABLE MULTI-FUNCTION GATE 2-to-1 data selector AND gate OR gate with one inverted input NAND gate with one inverted input AND gate with one inverted input NOR gate with one inverted input OR gate Inverter Noninverted buffer	3	1G97			●		●
CONFIGURABLE MULTI-FUNCTION GATE 2-to-1 data selector with inverted output NAND gate NOR gate with one inverted input AND gate with one inverted input NAND gate with one inverted input OR gate with one inverted input NOR gate Noninverted buffer Inverter	3	1G98			●		●
ULTRA-CONFIGURABLE MULTI-FUNCTION GATE PRIMARY FUNCTION 3-state buffer 3-state inverter 3-state 2-in-1 data selector MUX 3-state 2-in-1 data selector MUX, inverted out 3-state 2-input AND 3-state 2-input AND, one input inverted 3-state 2-input AND, both inputs inverted 3-state 2-input NAND 3-state 2-input NAND, one input inverted 3-state 2-input NAND, both inputs inverted 3-state 2-input XOR 3-state 2-input XNOR COMPLEMENTARY FUNCTION 3-state 2-input NOR 3-state 2-input NOR, one input inverted 3-state 2-input NOR, both inputs inverted 3-state 2-input OR 3-state 2-input OR, one input inverted 3-state 2-input OR, both inputs inverted 3-state 2-input XOR, one input inverted	4	1G99			●		●

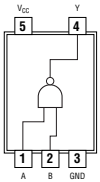
Status ●: Product available in technology indicated *: New product planned in technology indicated

PIN ASSIGNMENTS

1G / 2G / 3G

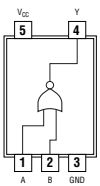
Pin Assignments

1G00
SINGLE 2-INPUT POSITIVE-NAND GATE
$Y = \overline{AB}$



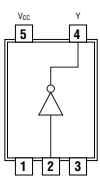
See page 91

1G02
SINGLE 2-INPUT POSITIVE-NOR GATE
$Y = \overline{A + B}$



See page 91

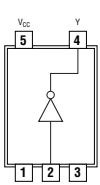
1G04
SINGLE INVERTER GATE
$Y = \overline{A}$



NC-No internal connection

See page 92

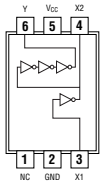
1GU04
SINGLE INVERTER
$Y = \overline{A}$



NC-No internal connection

See page 92

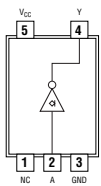
1GX04
CRYSTAL OSCILLATOR DRIVER



NC-No internal connection

See page 93

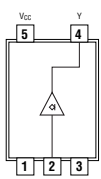
1G06
SINGLE INVERTER BUFFER/DRIVER WITH OPEN-DRAIN OUTPUT



NC-No internal connection

See page 94

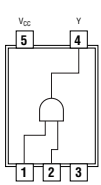
1G07
SINGLE BUFFER/DRIVER WITH OPEN-DRAIN OUTPUT



NC-No internal connection

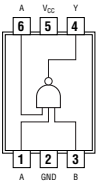
See page 94

1G08
SINGLE 2-INPUT POSITIVE-AND GATE
$Y = A \bullet B$



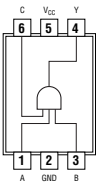
See page 95

1G10
SINGLE 3-INPUT POSITIVE-NAND GATE
$Y = \overline{A \bullet B \bullet C}$



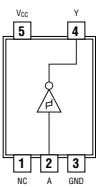
See page 95

1G11
SINGLE 3-INPUT POSITIVE-AND GATE
$Y = A \bullet B \bullet C$



See page 96

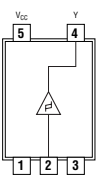
1G14
SINGLE SCHMITT-TRIGGER INVERTER GATE
$Y = \overline{A}$



NC-No internal connection

See page 96

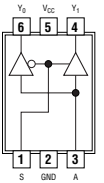
1G17
SINGLE SCHMITT-TRIGGER BUFFER
$Y = A$



NC-No internal connection

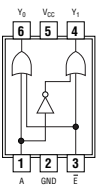
See page 97

1G18
1-OF-2 NONINVERTING DEMULTIPLEXER WITH 3-STATE DESELECTED OUTPUT



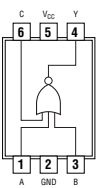
See page 97

1G19
1-OF-2 DECODER/DEMULTIPLEXER



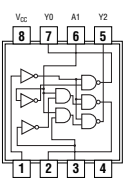
See page 98

1G27
3-INPUT POSITIVE-NOR GATE
$Y = \overline{A + B + C}$



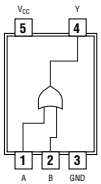
See page 98

1G29
2-OF-3 DECODER/DEMULTIPLEXER



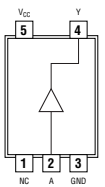
See page 99

1G32
SINGLE 2-INPUT POSITIVE-OR GATE
$Y = A + B$



See page 100

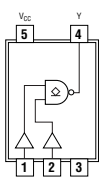
1G34
SINGLE BUFFER GATE
$Y = A$



NC-No internal connection

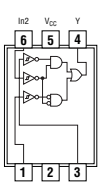
See page 100

1G38
SINGLE 2-INPUT NAND GATE WITH OPEN-DRAIN OUTPUT
$Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$



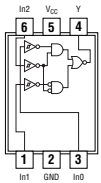
See page 101

1G57
CONFIGURABLE MULTIPLE-FUNCTION GATE



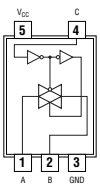
See page 101

1G58
CONFIGURABLE MULTIPLE-FUNCTION GATE



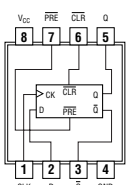
See page 102

1G66
SINGLE BILATERAL ANALOG SWITCH



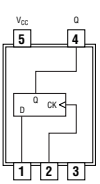
See page 102

1G74
SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET



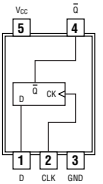
See page 103

1G79
SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP



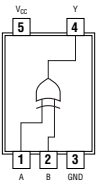
See page 104

1G80
SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP



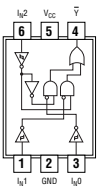
See page 105

1G86
SINGLE 2-INPUT EXCLUSIVE-OR GATE
Y = A = B



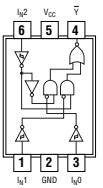
See page 106

1G97
CONFIGURABLE MULTIPLE-FUNCTION GATE



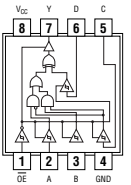
See page 106

1G98
CONFIGURABLE MULTIPLE-FUNCTION GATE



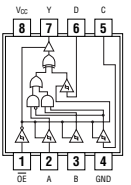
See page 107

1G99
SINGLE RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH SCHMITT-TRIGGER INPUTS



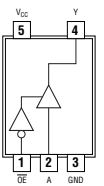
See page 108

1G123
SINGLE RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH SCHMITT-TRIGGER INPUTS



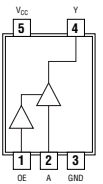
See page 109

1G125
SINGLE BUS BUFFER GATE WITH 3-STATE OUTPUT
Y = A



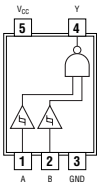
See page 110

1G126
SINGLE BUS BUFFER GATE WITH 3-STATE OUTPUT
Y = A



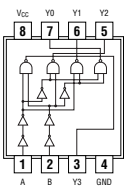
See page 110

1G132
SINGLE 2-INPUT NAND GATE WITH SCHMITT-TRIGGER INPUTS
$Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$



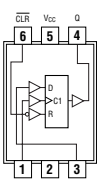
See page 111

1G139
2-TO-4 LINE DECODER



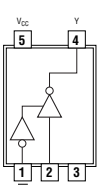
See page 112

1G175
SINGLE D-TYPE FLIP-FLOP WITH ASYNCHRONOUS CLEAR



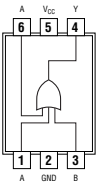
See page 113

1G240
SINGLE BUFFER/DRIVER WITH 3-STATE OUTPUT



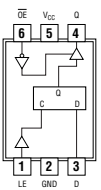
See page 114

1G332
SINGLE 3-INPUT POSITIVE-OR GATE
Y = A + B + C



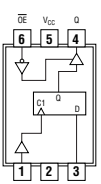
See page 114

1G373
SINGLE D-TYPE LATCH WITH 3-STATE OUTPUT



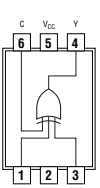
See page 115

1G374
SINGLE D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT



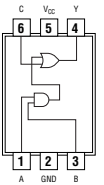
See page 116

1G386
SINGLE 3-INPUT EXCLUSIVE-XOR GATE
Y = A ⊕ B ⊕ C



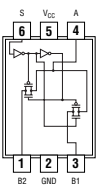
See page 117

1G0832
SINGLE 3-INPUT POSITIVE AND-OR GATE
$Y = (A \bullet B) + C$



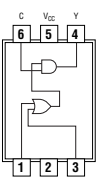
See page 117

1G3157
SINGLE-POLE, DOUBLE-THROW ANALOG SWITCH



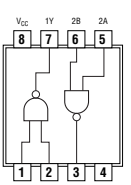
See page 118

1G3208
SINGLE 3-INPUT POSITIVE OR-AND GATE
$Y = (A + B) \bullet C$



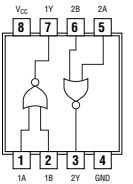
See page 119

2G00
DUAL 2-INPUT POSITIVE-NAND GATE
$Y = \overline{A \bullet B}$



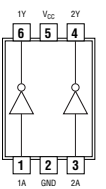
See page 120

2G02
DUAL 2-INPUT POSITIVE-NOR GATE
$Y = \overline{A + B}$



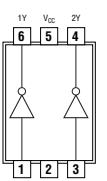
See page 120

2G04
DUAL INVERTER GATE
$Y = \overline{A}$



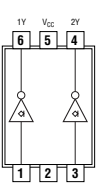
See page 121

2GU04
DUAL INVERTER GATE
$Y = \overline{A}$



See page 121

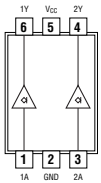
2G06
DUAL INVERTER BUFFER/DRIVER WITH OPEN-DRAIN OUTPUTS



See page 122

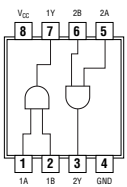
Pin Assignments

2G07
DUAL BUFFER/DRIVER
WITH OPEN-DRAIN OUTPUTS



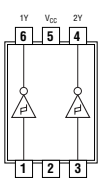
See page 122

2G08
DUAL 2-INPUT POSITIVE-AND GATE
Y = A • B



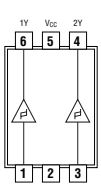
See page 123

2G14
DUAL INVERTER GATE
Y = $\overline{A}$



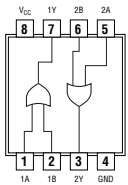
See page 123

2G17
DUAL SCHMITT-TRIGGER BUFFER
Y = A



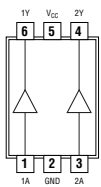
See page 124

2G32
DUAL 2-INPUT POSITIVE-OR GATE
Y = A + B



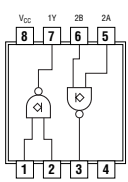
See page 124

2G34
DUAL INVERTER GATE
Y = A



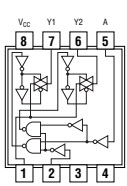
See page 125

2G38
SINGLE 2-INPUT NAND GATE WITH OPEN-DRAIN OUTPUT
Y = $\overline{A \bullet B}$ or Y = $\overline{A} + \overline{B}$



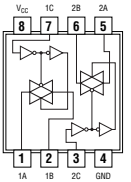
See page 125

2G53
SINGLE-POLE DOUBLE-THROW (SPDT) ANALOG SWITCH OR
2:1 ANALOG MULTIPLEXER/DEMULTIPLEXER



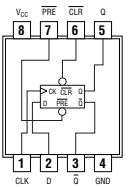
See page 126

2G66
DUAL BILATERAL ANALOG SWITCH



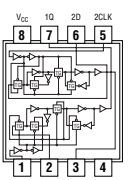
See page 126

2G74
SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET



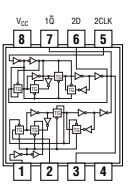
See page 127

2G79
DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP



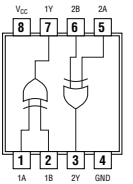
See page 128

2G80
DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP



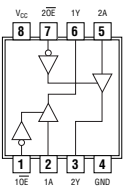
See page 129

2G86
DUAL 2-INPUT EXCLUSIVE-OR GATE
$Y = A \oplus B$



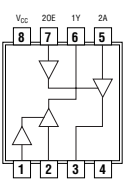
See page 130

2G125
DUAL BUS BUFFER GATE WITH 3-STATE OUTPUTS



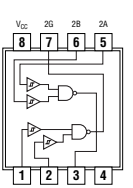
See page 130

2G126
DUAL BUS BUFFER GATE WITH 3-STATE OUTPUTS



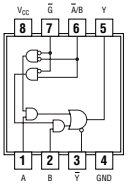
See page 131

2G132
SINGLE 2-INPUT NAND GATE WITH OPEN-DRAIN OUTPUT
$Y = A \bullet \overline{B}$ or $Y = \overline{A} + \overline{B}$



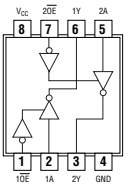
See page 131

2G157
SINGLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER



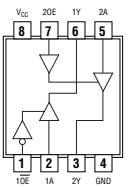
See page 132

2G240
DUAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS



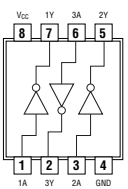
See page 133

2G241
DUAL BUFFER/DRIVER WITH 3-STATE OUTPUTS



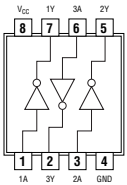
See page 133

3G04
TRIPLE INVERTER GATE
$Y = \overline{A}$



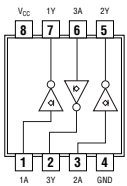
See page 134

3GU04
TRIPLE INVERTER GATE
$Y = \overline{A}$



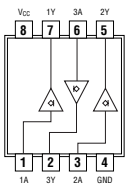
See page 134

3G06
TRIPLE INVERTER BUFFER/DRIVER WITH OPEN-DRAIN OUTPUTS



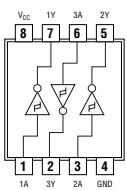
See page 135

3G07
TRIPLE BUFFER/DRIVER WITH OPEN-DRAIN OUTPUTS



See page 135

3G14
TRIPLE SCHMITT-TRIGGER INVERTER
$Y = \overline{A}$

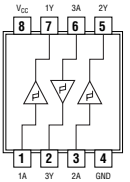


See page 136

3G17

TRIPLE SCHMITT-TRIGGER BUFFER

Y = A

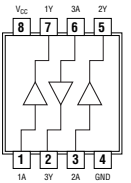


See page 136

3G34

TRIPLE BUFFER GATE

Y = A



See page 137

FUNCTION AND ELECTRICAL CHARACTERISTICS

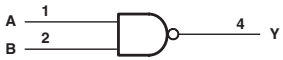
1G / 2G / 3G

1G00

SINGLE 2-INPUT POSITIVE-NAND GATE

● $Y = \overline{A \bullet B}$

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.0009	0.0009	0.0009	0.0009	mA
I_{OH}	MAX	-8	-8	-32	-24	-8	-4	-9	-8	-4	-3.1	-1.9	-1.1	mA
I_{OL}	MAX	8	8	32	24	8	4	9	8	4	3.1	1.9	1.1	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V
t_{PLH}	A or B	Y	MAX	8.5	9	4	4.7	5.5	9	2	2.2	5.2	6.8	9.8	18.8
t_{PHL}				8.5	9	4	4.7	5.5	9	2	2.2	5.2	6.8	9.8	18.8

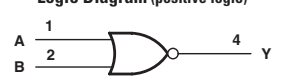
UNIT:ns

1G02

SINGLE 2-INPUT POSITIVE-NOR GATE

● $Y = \overline{A + B}$

Logic Diagram (positive logic)



FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.0009	0.0009	0.0009	0.0009	mA
I_{OH}	MAX	-8	-8	-32	-24	-8	-4	-9	-8	-4	-3.1	-1.9	-1.1	mA
I_{OL}	MAX	8	8	32	24	8	4	9	8	4	3.1	1.9	1.1	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V
t_{PLH}	A or B	Y	MAX	8.5	9	4	4.5	5.5	8	2.1	2.4	5	6.5	9.5	17.9
t_{PHL}				8.5	9	4	4.5	5.5	8	2.1	2.4	5	6.5	9.5	17.9

UNIT:ns

1G04

SINGLE INVERTER GATE

● $Y = \overline{A}$

Logic Diagram

5pin Package

4pin Package

FUNCTION TABLE

INPUT A	OUTPUT Y
H	L
L	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.0009	0.0009	0.0009	0.0009	mA
I_{OH}	MAX	-8	-8	-32	-24	-8	-4	-9	-8	-4	-3.1	-1.9	-1.1	mA
I_{OL}	MAX	8	8	32	24	8	4	9	8	4	3.1	1.9	1.1	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V
t_{PLH}	A	Y	MAX	8.5	8.5	3.7	4.2	5.2	7.5	1.9	2.2	4.5	5.6	7.9	15
t_{PHL}				8.5	8.5	3.7	4.2	5.2	7.5	1.9	2.2	4.5	5.6	7.9	15

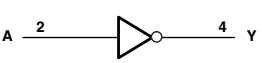
UNIT:ns

1GU04

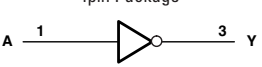
SINGLE INVERTER GATE

Logic Diagram

5pin Package



4pin Package



● $Y = \overline{A}$
● Unbuffered Output
● Supply Voltage Renge : 2V to 5.5V

FUNCTION TABLE

INPUT A	OUTPUT Y
H	L
L	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AHC	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-8	-32	-24	-8	-4	-9	-8	mA
I_{OL}	MAX	8	32	24	8	4	9	8	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
t_{PLH}	A	Y	MAX	8	3	3.7	4	5	2.1	2.4
t_{PHL}				8	3	3.7	4	5	2.1	2.4

UNIT:ns

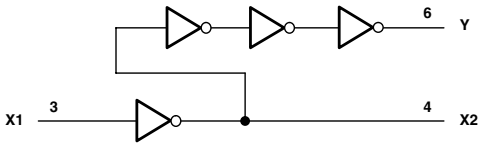
: **PREVIEW**

1GX04

CRYSTAL OSCILLATOR DRIVER

- One Unbuffered Inverter (1GU04)
- One Buffered Inverter (1G04)
- Suitable for Commonly Used Clock Frequencies
- Optimized for Use in Crystal Oscillator Applications

Logic Diagram



FUNCTION TABLE

OUTPUT	INPUTS	
X1	X2	Y
H	L	H
L	H	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-32	-24	-8	-4	mA
I_{OL}	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t_{PLH}	X1	X2	MAX	3	3.7	4	7
t_{PHL}				3	3.7	4	7
t_{PLH}	X1	Y*	MAX	5	7.8	7.4	18
t_{PHL}				5	7.8	7.4	18

UNIT : ns

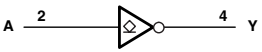
*X2 : no external load

1G06

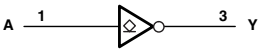
SINGLE INVERTER BUFFER/DRIVER WITH OPEN-DRAIN OUTPUT

Logic Diagram

5pin Package



4pin Package



FUNCTION TABLE

INPUT A	OUTPUT Y
H	L
L	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.0009	0.0009	0.0009	0.0009	mA
V_O	MAX	5.5	5.5	5.5	5.5	3.6	3.6	3.6	3.6	3.6	3.6	V
I_{OL}	MAX	32	24	8	4	9	8	4	3.1	1.9	1.1	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V
t_{PLH}	A	Y	MAX	3	4	4	6.5	1.8	2.5	4.9	4.5	6.7	14.1
t_{PHL}				3	4	4	6.5	1.8	2.5	4.9	4.5	6.7	14.1

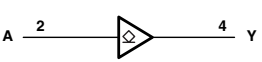
UNIT:ns

1G07

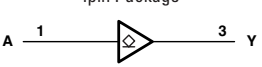
SINGLE BUFFER/DRIVER WITH OPEN-DRAIN OUTPUT

Logic Diagram

5pin Package



4pin Package



FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.0009	0.0009	0.0009	0.0009	mA
I_{OH}	MAX	5.5	5.5	5.5	5.5	3.6	3.6	3.6	3.6	3.6	3.6	V
I_{OL}	MAX	32	24	8	4	9	8	4	3.1	1.9	1.1	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V
t_{PLH}	A	Y	MAX	3.5	4.2	5.5	8.3	1.8	2.5	4.5	4.8	7.1	16.2
t_{PHL}				3.5	4.2	5.5	8.3	1.8	2.5	4.5	4.8	7.1	16.2

UNIT:ns

: **PREVIEW**

1G08

SINGLE 2-INPUT POSITIVE-AND GATE

● Y = A•B

Logic Diagram

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.0009	0.0009	0.0009	0.0009	mA
I_{OH}	MAX	-8	-8	-32	-24	-8	-4	-9	-8	-4	-3.1	-1.9	-1.1	mA
I_{OL}	MAX	8	8	32	24	8	4	9	8	4	3.1	1.9	1.1	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V
t_{PLH}	A or B	Y	MAX	9	9	4	4.5	5.5	8	2	2.4	4.7	6.1	9	17.2
t_{PHL}				9	9	4	4.5	5.5	8	2	2.4	4.7	6.1	9	17.2

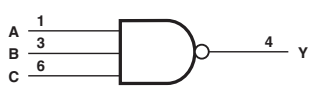
UNIT:ns

1G10

SINGLE 3-INPUT POSITIVE-NAND GATE

● $Y = \overline{A \bullet B \bullet C}$

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-32	-24	-8	-4	-9	-8	mA
I_{OL}	MAX	32	24	8	4	9	8	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
t_{PLH}	A, B or C	Y	MAX	3.6	5.0	6.5	18.0	TBD	TBD
t_{PHL}				3.6	5.0	6.5	18.0	TBD	TBD

UNIT:ns

1G11

SINGLE 3-INPUT POSITIVE-AND GATE

● Y = A•B•C

Logic Diagram

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-32	-24	-8	-4	-9	-8	mA
I_{OL}	MAX	32	24	8	4	9	8	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
t_{PLH}	A, B or C	Y	MAX	3.5	4.9	6.2	17.2	TBD	TBD
t_{PHL}				3.5	4.9	6.2	17.2	TBD	TBD

UNIT:ns

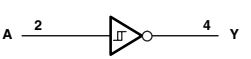
1G14

SINGLE SCHMITT-TRIGGER INVERTER GATE

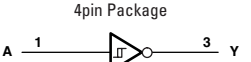
● $Y = \overline{A}$

Logic Diagram

5pin Package



4pin Package



FUNCTION TABLE

INPUT A	OUTPUT Y
H	L
L	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.0009	0.0009	0.0009	0.0009	mA
I_{OH}	MAX	-8	-8	-32	-24	-8	-4	-9	-8	-4	-3.1	-1.9	-1.1	mA
I_{OL}	MAX	8	8	32	24	8	4	9	8	4	3.1	1.9	1.1	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V
t_{PLH}	A	Y	MAX	12	9	5	5.5	6.5	11	2.5	2.5	5.6	6.8	9.5	16.7
t_{PHL}				12	9	5	5.5	6.5	11	2.5	2.5	5.6	6.8	9.5	16.7

UNIT:ns

: **PREVIEW**

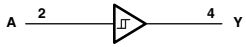
1G17

SINGLE SCHMITT-TRIGGER BUFFER

● Y = A

Logic Diagram

5pin Package



4pin Package

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.0009	0.0009	0.0009	0.0009	mA
I_{OH}	MAX	-32	-24	-8	-4	-9	-8	-4	-3.1	-1.9	-1.1	mA
I_{OL}	MAX	32	24	8	4	9	8	4	3.1	1.9	1.1	mA

SWITCHING CHARACTERISTICS

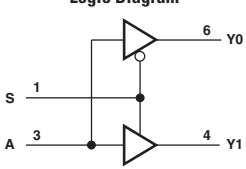
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V
t_{PLH}	A	Y	MAX	5	5.5	6.5	11	2.5	2.4	5.7	6.8	9	15.6
t_{PHL}				5	5.5	6.5	11	2.5	2.4	5.7	6.8	9	15.6

UNIT:ns

1G18

1-OF-2 NONINVERTING DEMULTIPLEXER WITH 3-STATE DESELECTED OUTPUT

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUTS	
S	A	Y0	Y1
L	L	L	Z
L	H	H	Z
H	L	Z	L
H	H	Z	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-32	-24	-8	-4	mA
I_{OL}	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

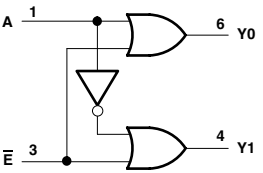
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t_{PLH}	A	Y	MAX	3.2	4.2	5	9.3
t_{PHL}				3.2	4.2	5	9.3
t_{PZL}	S	Y	MAX	3.4	4.6	5.6	10.2
t_{PZH}				3.4	4.6	5.6	10.2
t_{PLZ}	S	Y	MAX	3.3	4.9	5.3	12.7
t_{PHZ}				3.3	4.9	5.3	12.7

UNIT:ns

1G19

1-OF-2 DECODER/DEMULTIPLEXER

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUTS	
$\overline{E}$	A	Y0	Y1
L	L	L	H
L	H	H	L
H	X	H	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT	AUC 2.5V	AUC 1.8V
I_{CC}	MAX	0.01	0.01	0.01	0.01	mA	0.01	0.01
I_{OH}	MAX	-32	-24	-8	-4	mA	-9	-8
I_{OL}	MAX	32	24	8	4	mA	9	8

SWITCHING CHARACTERISTICS

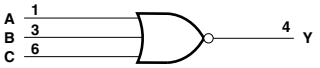
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
t_{PLH}	A or $\overline{E}$	Y	MAX	3.9	5.2	6.5	16.1	2.0	2.8
t_{PHL}				3.9	5.2	6.5	16.1	2.0	2.8

UNIT:ns

1G27

SINGLE 3-INPUT POSITIVE-NOR GATE

Logic Diagram



● $Y = \overline{A + B + C}$

FUNCTION TABLE

INPUTS			OUTPUT Y
A	B	C	
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-32	-24	-8	-4	mA
I_{OL}	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t_{PLH}	A, B or C	Y	MAX	3.6	5.4	7.1	20.5
t_{PHL}				3.6	5.4	7.1	20.5

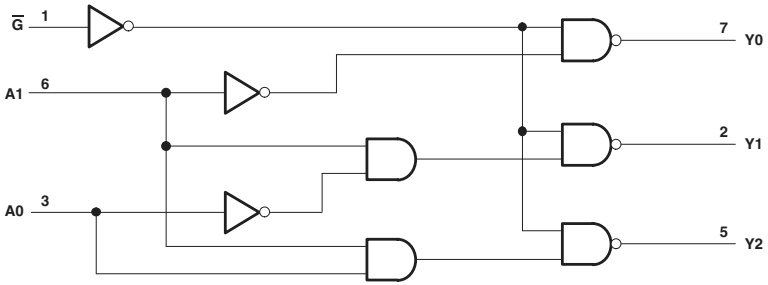
UNIT:ns

: **PREVIEW**

1G29

2-OF-3 DECODER/DEMULTIPLEXER

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUTS		
$\overline{G}$	A1	A0	Y0	Y1	Y2
L	L	X	L	H	H
L	H	L	H	L	H
L	H	H	H	H	L
H	X	X	H	H	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-32	-24	-8	-4	mA
I_{OL}	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t_{PLH}	A or $\overline{G}$	Y	MAX	5.1	6.1	7.5	15.8
t_{PHL}				5.1	6.1	7.5	15.8

UNIT : ns

1G32

SINGLE 2-INPUT POSITIVE-OR GATE

● Y = A + B

Logic Diagram

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.0009	0.0009	0.0009	0.0009	mA
I_{OH}	MAX	-8	-8	-32	-24	-8	-4	-9	-8	-4	-3.1	-1.9	-1.1	mA
I_{OL}	MAX	8	8	32	24	8	4	9	8	4	3.1	1.9	1.1	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V
t_{PLH}	A or B	Y	MAX	8.5	9	4	4.5	5.5	8	2.1	2.4	5	6.6	9.6	18.4
t_{PHL}				8.5	9	4	4.5	5.5	8	2.1	2.4	5	6.6	9.6	18.4

UNIT:ns

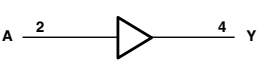
1G34

SINGLE BUFFER GATE

● Y = A

Logic Diagram

5pin Package



4pin Package

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V	UNIT
I_{CC}	MAX	0.001	0.001	0.001	0.001	0.009	0.009	0.009	0.009	mA
I_{OH}	MAX	-32	-24	-8	-4	-4	-3.1	-1.9	-1.1	mA
I_{OL}	MAX	32	24	8	4	4	3.1	1.9	1.1	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V
t_{PLH}	A	Y	MAX	3.2	4.1	4.4	8.6	4.8	5.8	8.3	15.4
t_{PHL}				3.2	4.1	4.4	8.6	4.8	5.8	8.3	15.4

UNIT : ns

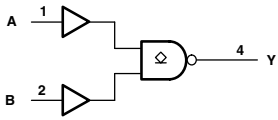
: **PREVIEW**

1G38

SINGLE 2-INPUT NAND GATE WITH OPEN-DRAIN OUTPUT

● $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	mA
V_O	MAX	5.5	5.5	5.5	5.5	mA
I_{OL}	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

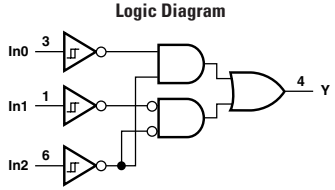
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t_{PLH}	A or B	Y	MAX	3.9	4.5	6	10
t_{PHL}				3.9	4.5	6	10

UNIT : ns

1G57

CONFIGURABLE MULTIPLE-FUNCTION GATE

Logic Diagram



FUNCTION SELECTION TABLE

2-input AND
2-input AND with both inputs inverted
2-input NAND with inverted input
2-input OR with inverted input
2-input NOR
2-input NOR with both inputs inverted
2-input XNOR

FUNCTION TABLE

INPUTS			OUTPUT
In2	In1	In0	Y
L	L	L	H
L	L	H	L
L	H	L	H
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	H
H	H	H	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	0.0009	0.0009	0.0009	0.0009	mA
I_{OH}	MAX	-32	-24	-8	-4	-4	-3.1	-1.9	-1.1	mA
I_{OL}	MAX	32	24	8	4	4	3.1	1.9	1.1	mA

SWITCHING CHARACTERISTICS

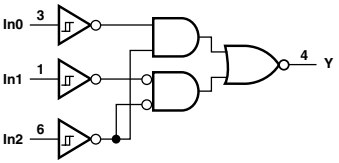
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V
t_{PLH}	Any In	Y	MAX	5.1	6.3	8.3	14.4	6.1	7.3	10	18.1
t_{PHL}				5.1	6.3	8.3	14.4	6.1	7.3	10	18.1

UNIT:ns

1G58

CONFIGURABLE MULTIPLE-FUNCTION GATE

Logic Diagram



FUNCTION SELECTION TABLE

2-input AND with inverted input
2-input NAND
2-input NAND with both inputs inverted
2-input OR
2-input OR with both inputs inverted
2-input NOR with inverted input
2-input XOR

FUNCTION TABLE

INPUTS			OUTPUT
In2	In1	In0	Y
L	L	L	L
L	L	H	H
L	H	L	L
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	L
H	H	H	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	0.0009	0.0009	0.0009	0.0009	mA
I_{OH}	MAX	-32	-24	-8	-4	-4	-3.1	-1.9	-1.1	mA
I_{OL}	MAX	32	24	8	4	4	3.1	1.9	1.1	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V
t_{PLH}	Any In	Y	MAX	5.1	6.3	8.3	14.4	6.3	7.6	10.2	19
t_{PHL}				5.1	6.3	8.3	14.4	6.3	7.6	10.2	19

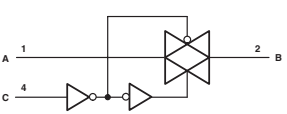
UNIT:ns

1G66

SINGLE BILATERAL ANALOG SWITCH

- High On-Off Outputs Voltage Ratio
- High Degree of Linearity

Logic Diagram



FUNCTION TABLE

CONTROL INPUT (C)	SWITCHI
L	OFF
H	ON

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA
R_{ON}	MAX	10	15	20	30	15	20	Ω
$R_{ON(P)}$	MAX	15	20	30	120	20	80	Ω

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
t_{PLH}	A or B	B or A	MAX	0.6	0.8	1.2	2	0.3	0.3
t_{PHL}				0.6	0.8	1.2	2	0.3	0.3
t_{PZH}	C	B or A	MAX	4.2	5	6.5	12	1.4	2.3
t_{PZL}				4.2	5	6.5	12	1.4	2.3
t_{PHZ}	C	B or A	MAX	5	6.5	6.9	10	1.5	2.9
t_{PLZ}				5	6.5	6.9	10	1.5	2.9

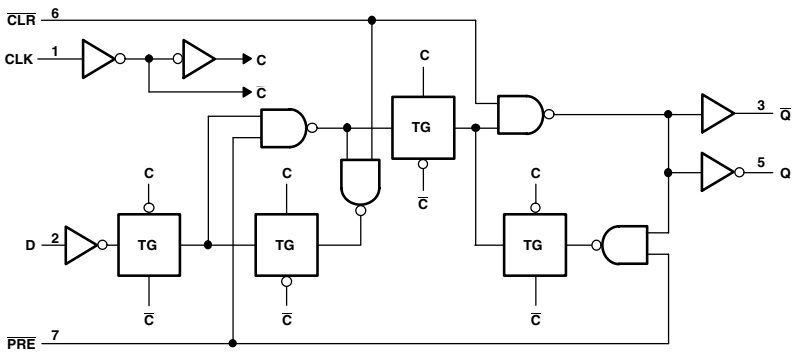
UNIT : ns

: PREVIEW

1G74

SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUTS	
PRE	CLR	CLK	D	Q	Q
L	H	X	X	H	L
X	L	X	X	L	H
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V	UNIT
I_{CC}	MAX	0.01	0.01	0.0009	0.0009	0.0009	0.0009	mA
I_{OH}	MAX	-9	-8	-4	-3.1	-1.9	-1.1	mA
I_{OL}	MAX	9	8	4	3.1	1.9	1.1	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

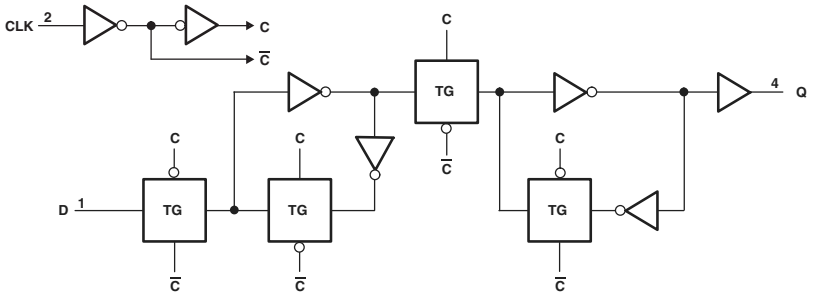
PARAMETER		INPUT	OUTPUT		MAX or MIN	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V
f_{max}					MIN	275	250	160	130	60	50
t_w	Pulse duration		CLK		MIN	1	1	2	2	2	2
			PRE or CLR	low	MIN	1	1	2	2	2	2
t_{su}	Setup time, before CLK↑		Data	high	MIN	0.4	0.5	0.5	0.5	1	1.3
				low	MIN	0.4	0.5	1	1	1	1.2
			PRE or CLR	inactive	MIN	0.4	0.7	0.5	0.5	0.5	0.5
t_h	Hold time, data after CLK↑				MIN	0.3	0.3	0	0	0	0
t_{PLH}		CLK	Q		MAX	1.8	2.4	5.3	7	10.4	21.8
t_{PHL}						1.8	2.4	5.3	7	10.4	21.8
t_{PLH}		CLK	$\overline{Q}$		MAX	1.8	2.4	5.2	6.7	9.9	20.3
t_{PHL}						1.8	2.4	5.2	6.7	9.9	20.3
t_{PLH}		PRE or CLR	Q or $\overline{Q}$		MAX	2.1	2.8	5.8	7.4	10.8	21.4
t_{PHL}						2.1	2.8	5.8	7.4	10.8	21.4

UNIT f_{max} : MHz other : ns

1G79

SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUT
CLK	D	Q
↑	H	H
↑	L	L
L	X	Q_0

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.0009	0.0009	0.0009	0.0009	mA
I_{OH}	MAX	-32	-24	-8	-4	-9	-8	-4	-3.1	-1.9	-1.1	mA
I_{OL}	MAX	32	24	8	4	9	8	4	3.1	1.9	1.1	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V
fmax			MIN	160	160	160	160	275	250	260	250	240	160
tw	CLK high or low		MIN	2.5	2.5	2.5	2.5	1.7	1.7	1.9	1.7	1.6	2.2
tsu	Before CLK ↑, Data high		MIN	1.2	1.3	1.4	2.2	0.7	0.5	0.6	0.7	0.9	1.4
	Before CLK ↑, Data low			1.2	1.3	1.4	2.6	0.7	0.5	1	1	1.1	1.8
th	Data after CLK ↑		MIN	0.5	1.0	0.4	0.3	0.1	0	0	0	0	0
t_{PLH}	CLK	Q	MAX	4.5	5	7	9.9	1.8	2.4	4.5	5.7	8	14.4
t_{PHL}				4.5	5	7	9.9	1.8	2.4	4.5	5.7	8	14.4

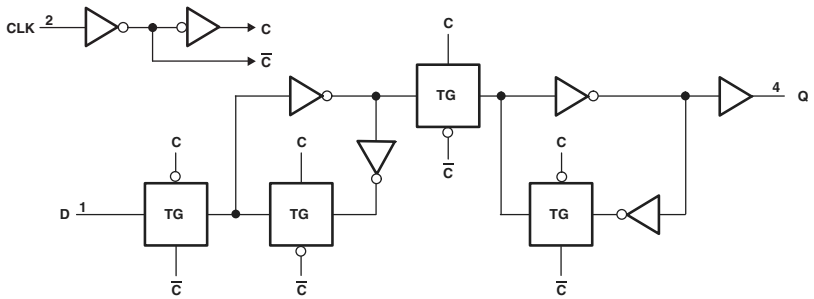
UNIT fmax : MHz other : ns

: **PREVIEW**

1G80

SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUT
CLK	D	Q̄
↑	H	L
↑	L	H
L	X	Q_0

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.0009	0.0009	0.0009	0.0009	mA
I_{OH}	MAX	-32	-24	-8	-4	-9	-8	-4	-3.1	-1.9	-1.1	mA
I_{OL}	MAX	32	24	8	4	9	8	4	3.1	1.9	1.1	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V
fmax			MIN	160	160	160	160	275	250	260	250	240	170
tw	CLK high or low		MIN	2.5	2.5	2.5	2.5	1.7	1.7	1.9	1.7	1.6	2.5
tsu	Before CLK↑, Data high		MIN	1.1	1.3	1.5	2.3	0.5	0.6	0.4	0.6	0.8	1.2
	Before CLK↑, Data low			1.1	1.3	1.5	2.5	0.5	0.6	0.7	0.8	1.1	2
th	Data after CLK↑		MIN	0.4	0.9	0.2	0	0.1	0.1	0	0	0	0
t_{PLH}	CLK	Q̄	MAX	4.5	5.2	7	9.9	1.8	2.4	4.9	6.3	7.3	17.7
t_{PHL}				4.5	5.2	7	9.9	1.8	2.4	4.9	6.3	7.3	17.7

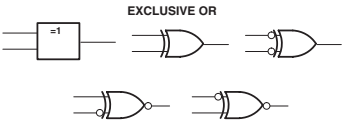
UNIT fmax : MHz other : ns

1G86

SINGLE 2-INPUT EXCLUSIVE-OR GATE

● $Y = A \oplus B$

Logic Diagram



An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-8	-8	-32	-24	-8	-4	-9	-8	mA
I_{OL}	MAX	8	8	32	24	8	4	9	8	mA

SWITCHING CHARACTERISTICS

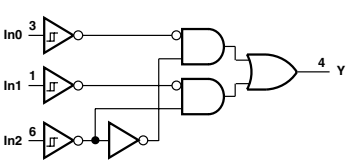
PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
t_{PLH}	A or B	Y	MAX	10	9	4	5	5.5	9.9	2	2.6
t_{PHL}				10	9	4	5	5.5	9.9	2	2.6

UNIT:ns

1G97

CONFIGURABLE MULTIPLE-FUNCTION GATE

Logic Diagram



FUNCTION SELECTION TABLE

2-to-1 data selector
2-input AND gate
2-input OR gate with one inverted input
2-input NAND gate with one inverted input
2-input AND gate with one inverted input
2-input NOR gate with one inverted input
2-input OR gate
Inverter
Noninverted buffer

FUNCTION TABLE

INPUTS			OUTPUT
In2	In1	In0	Y
L	L	L	L
L	L	H	L
L	H	L	H
L	H	H	H
H	L	L	L
H	L	H	H
H	H	L	L
H	H	H	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	0.0009	0.0009	0.0009	0.0009	mA
I_{OH}	MAX	-32	-24	-8	-4	-4	-3.1	-1.9	-1.1	mA
I_{OL}	MAX	32	24	8	4	4	3.1	1.9	1.1	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V
t_{PLH}	Any In	Y	MAX	5.1	6.3	8.3	14.4	6.4	7.8	10.5	19.2
t_{PHL}				5.1	6.3	8.3	14.4	6.4	7.8	10.5	19.2

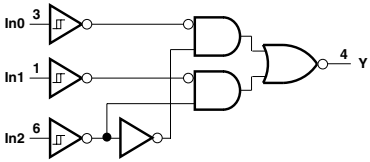
UNIT:ns

: **PREVIEW**

1G98

CONFIGURABLE MULTIPLE-FUNCTION GATE

Logic Diagram



FUNCTION SELECTION TABLE

2-to-1 data selector with inverted output
2-input NAND gate
2-input NOR gate with one inverted input
2-input AND gate with one inverted input
2-input NAND gate with one inverted input
2-input OR gate with one inverted input
2-input NOR gate
Noninverted buffer
Inverter

FUNCTION TABLE

INPUTS			OUTPUT
In2	In1	In0	Y
L	L	L	H
L	L	H	H
L	H	L	L
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	H
H	H	H	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	0.0009	0.0009	0.0009	0.0009	mA
I_{OH}	MAX	-32	-24	-8	-4	-4	-3.1	-1.9	-1.1	mA
I_{OL}	MAX	32	24	8	4	4	3.1	1.9	1.1	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V
t_{PLH}	Any In	Y	MAX	5.1	6.3	8.3	14.4	6	7.3	10.2	19
t_{PHL}				5.1	6.3	8.3	14.4	6	7.3	10.2	19

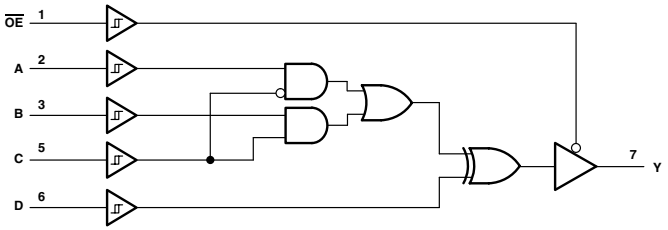
UNIT:ns

1G99

SINGLE RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH SCHMITT-TRIGGER INPUTS

- Offers Nine Different Logic Functions in a Single Package

Logic Diagram



FUNCTION TABLE

INPUTS					OUTPUT
$\overline{OE}$	D	C	B	A	Y
L	L	L	L	L	L
L	L	L	L	H	H
L	L	L	H	L	L
L	L	L	H	H	H
L	L	H	L	L	L
L	L	H	L	H	L
L	L	H	H	L	H
L	L	H	H	H	H
L	H	L	L	L	H
L	H	L	L	H	L
L	H	L	H	L	H
L	H	L	H	H	L
L	H	H	L	L	H
L	H	H	L	H	H
L	H	H	H	L	L
L	H	H	H	H	H
H	H or L	H or L	H or L	H or L	Z

PRIMARY FUNCTION

3-state buffer
3-state inverter
3-state 2-in-1 data selector MUX
3-state 2-in-1 data selector MUX, inverted out
3-state 2-input AND
3-state 2-input AND, one input inverted
3-state 2-input AND, both inputs inverted
3-state 2-input NAND
3-state 2-input NAND, one input inverted
3-state 2-input NAND, both inputs inverted
3-state 2-input XOR
3-state 2-input XNOR

COMPLEMENTARY FUNCTION

3-state 2-input NOR, both inputs inverted
3-state 2-input NOR, one input inverted
3-state 2-input NOR
3-state 2-input OR, both inputs inverted
3-state 2-input OR, one input inverted
3-state 2-input OR
3-state 2-input XOR, one input inverted

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	0.0009	0.0009	0.0009	0.0009	mA
I_{OH}	MAX	-32	-24	-8	-4	-4	-3.1	-1.9	-1.1	mA
I_{OL}	MAX	32	24	8	4	4	3.1	1.9	1.1	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V
t_{PLH}	A	Y	MAX	5.5	8.4	11.7	30.8	8.4	10.5	14.5	29.8
t_{PHL}				5.5	8.4	11.7	30.8	8.4	10.5	14.5	29.8
t_{PLH}	B	Y	MAX	5.4	8.2	11.3	28.9	8.4	10.5	14.5	29.8
t_{PHL}				5.4	8.2	11.3	28.9	8.4	10.5	14.5	29.8
t_{PLH}	C	Y	MAX	5.7	8.6	12.3	29.8	8.4	10.5	14.5	29.8
t_{PHL}				5.7	8.6	12.3	29.8	8.4	10.5	14.5	29.8
t_{PLH}	D	Y	MAX	5.2	7.6	10.7	25.7	8.4	10.5	14.5	29.8
t_{PHL}				5.2	7.6	10.7	25.7	8.4	10.5	14.5	29.8
t_{PZH}	$\overline{OE}$	Y	MAX	4.7	7	11.3	25.2	8.2	9.9	14.8	29.3
t_{PZL}				4.7	7	11.3	25.2	8.2	9.9	14.8	29.3
t_{PHZ}	$\overline{OE}$	Y	MAX	4.5	5.6	5.8	15	5.8	5.5	7.9	10
t_{PLZ}				4.5	5.6	5.8	15	5.8	5.5	7.9	10

UNIT : ns

: **PREVIEW**

1G123

SINGLE RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH SCHMITT-TRIGGER INPUTS

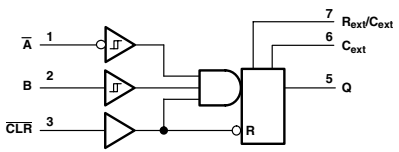
- Schmitt-Triggered Circuitry on $\overline{A}$ and B Inputs for Slow Input Transition Rates
- Edge Triggered From Active-High or Active-Low Gated Logic Inputs
- Retriggerable for Very Long Outputs Pulses, up to 100% Duty Cycle
- Overriding Clear Terminates Output Pulse
- Glitch-Free Power-Up Reset on Outputs

FUNCTION TABLE

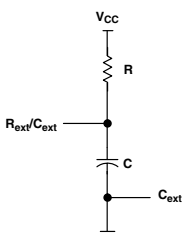
INPUTS			OUTPUT
$\overline{CLR}$	$\overline{A}$	B	Q
L	X	X	L
X	H	X	L(1)
X	X	L	L(1)
H	L	↑	⎍
H	↓	H	⎍
↑	L	H	⎍

(1) These outputs are based on the assumption that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the setup.

Logic Diagram



REQUIRED TIMING CIRCUIT



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I_{CC}	Quiescent	MAX	0.01	-	-	-	mA
I_{CC}	Active State	MAX	0.975	0.65	0.28	0.22	mA
I_{OH}		MAX	-32	-24	-8	-4	mA
I_{OL}		MAX	32	24	8	4	mA

TIMING REQUIREMENTS

PARAMETER		MAX or MIM	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t_wIN	$\overline{CLR}$	MAX	2.5	3	4	8
	$\overline{A}$ or B trigger	MAX	2.5	3	4	8

UNIT : ns

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t_{PLH}	$\overline{A}$ or B	Q	MAX	8.2	12.5	18.5	57
t_{PHL}				8.2	12.5	18.5	57
t_{PLH}	$\overline{CLR}$	Q	MAX	6	8.6	12.5	36.5
t_{PHL}				6	8.6	12.5	36.5
t_{PLH}	$\overline{CLR}$ trigger	Q	MAX	7.5	11.5	17	59
t_{PHL}				7.5	11.5	17	59

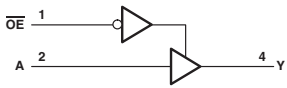
UNIT : ns

1G125

SINGLE BUS BUFFER GATE WITH 3-STATE OUTPUT

● Y = A

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.0009	0.0009	0.0009	0.0009	mA
I_{OH}	MAX	-8	-8	-32	-24	-8	-4	-9	-8	-4	-3.1	-1.9	-1.1	mA
I_{OL}	MAX	8	8	32	24	8	4	9	8	4	3.1	1.9	1.1	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V
t_{PLH}	A	Y	MAX	8.5	8.5	4	4.5	5.5	9	1.7	2.5	5.2	6.4	9.1	16.6
t_{PHL}				8.5	8.5	4	4.5	5.5	9	1.7	2.5	5.2	6.4	9.1	16.6
t_{PZH}	$\overline{OE}$	Y	MAX	8	8	5	5.3	6.6	10.1	1.9	2.6	6.4	7.8	11	20.2
t_{PZL}				8	8	5	5.3	6.6	10.1	1.9	2.6	6.4	7.8	11	20.2
t_{PHZ}	$\overline{OE}$	Y	MAX	10	10	4.2	5	5	9.2	1.7	3.1	5.6	5.4	7.5	14
t_{PLZ}				10	10	4.2	5	5	9.2	1.7	3.1	5.6	5.4	7.5	14

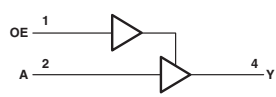
UNIT:ns

1G126

SINGLE BUS BUFFER GATE WITH 3-STATE OUTPUT

● Y = A

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUT
OE	A	Y
H	H	H
H	L	L
L	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.0009	0.0009	0.0009	0.0009	mA
I_{OH}	MAX	-8	-8	-32	-24	-8	-4	-9	-8	-4	-3.1	-1.9	-1.1	mA
I_{OL}	MAX	8	8	32	24	8	4	9	8	4	3.1	1.9	1.1	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V
t_{PLH}	A	Y	MAX	8.5	8.5	4	4.5	5.5	8	1.7	2.5	5.2	6.4	9.1	16.6
t_{PHL}				8.5	8.5	4	4.5	5.5	8	1.7	2.5	5.2	6.4	9.1	16.6
t_{PZH}	OE	Y	MAX	8	8	5	5.3	6.6	9.4	1.9	2.5	6.4	7.8	11	20.2
t_{PZL}				8	8	5	5.3	6.6	9.4	1.9	2.5	6.4	7.8	11	20.2
t_{PHZ}	OE	Y	MAX	10	10	4.2	5.5	5.5	9.8	2.1	3.1	5.6	5.4	7.5	14
t_{PLZ}				10	10	4.2	5.5	5.5	9.8	2.1	3.1	5.6	5.4	7.5	14

UNIT:ns

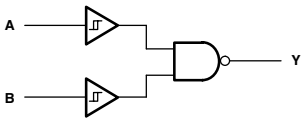
: **PREVIEW**

1G132

SINGLE 2-INPUT NAND GATE WITH SCHMITT-TRIGGER INPUTS

● $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-32	-24	-8	-4	mA
I_{OL}	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

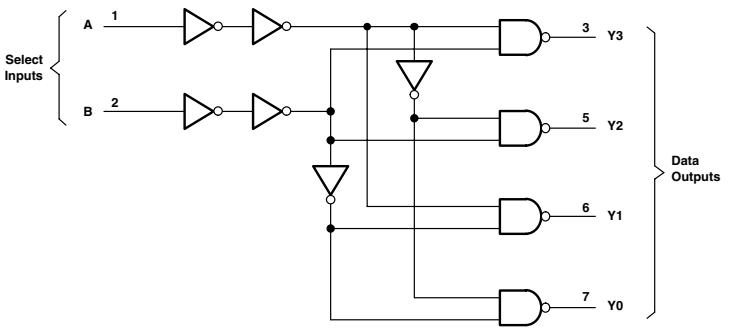
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t_{PLH}	A or B	Y	MAX	5	6	7.5	16
t_{PHL}				5	6	7.5	16

UNIT : ns

1G139

2-TO-4 LINE DECODER

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUTS			
B	A	Y0	Y1	Y2	Y3
L	L	L	H	H	H
L	H	H	L	H	H
H	L	H	H	L	H
H	H	H	H	H	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-32	-24	-8	-4	mA
I_{OL}	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t_{PLH}	A or B	Y	MAX	4.2	5.9	8.2	16.7
t_{PHL}				4.2	5.9	8.2	16.7

UNIT : ns

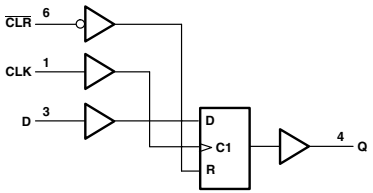
: **PREVIEW**

1G175

SINGLE D-TYPE FLIP-FLOP WITH ASYNCHRONOUS CLEAR

- Complementary Outputs (Q, $\overline{Q}$)
- Buffered Clock and Direct Clear Inputs
- Asynchronous Clear Function

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT
$\overline{CLR}$	CLK	D	Q
H	↑	L	L
H	↑	H	H
H	H or L	X	Q_O
L	X	X	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-32	-24	-8	-4	mA
I_{OL}	MAX	32	24	8	4	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

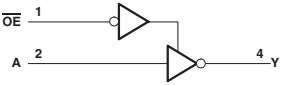
PARAMETER		INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
f_{max}				MIN	175	150	125	100
t_w	Pulse duration	$\overline{CLR}$	Low	MIN	2.5	2.8	3	5.6
		CLK	High or low	MIN	2.5	2.8	3	3.5
t_{su}	Setup time, before CLK ↑	Data		MIN	1.5	2	2.5	3
		$\overline{CLR}$ inactive		MIN	0.5	0.5	0	0
th	Hold time, data after CLK ↑			MIN	0.5	0.5	0	0
t_{PLH}		CLK	Q	MAX	4	5.7	7.1	13.4
t_{PHL}					4	5.7	7.1	13.4
t_{PLH}		$\overline{CLR}$	Q	MAX	4.1	5.8	7	12.9
t_{PHL}					4.1	5.8	7	12.9

UNIT f_{max} : MHz other : ns

1G240

SINGLE BUFFER/DRIVER WITH 3-STATE OUTPUT

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.0009	0.0009	0.0009	0.0009	mA
I_{OH}	MAX	-32	-24	-8	-4	-9	-8	-4	-3.1	-1.9	-1.1	mA
I_{OL}	MAX	32	24	8	4	9	8	4	3.1	1.9	1.1	mA

SWITCHING CHARACTERISTICS

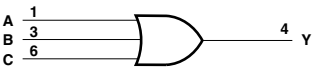
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	AUP 3.3V	AUP 2.5V	AUP 1.8V	AUP 1.1V
t_{PLH}	A	Y	MAX	4	4.5	5.5	8.6	1.7	2.5	5.2	6.3	9.1	17.3
t_{PHL}				4	4.5	5.5	8.6	1.7	2.5	5.2	6.3	9.1	17.3
t_{PZH}	$\overline{OE}$	Y	MAX	5.2	5.4	6.5	10.0	1.9	2.6	6.3	7.7	10.9	20.9
t_{PZL}				5.2	5.4	6.5	10.0	1.9	2.6	6.3	7.7	10.9	20.9
t_{PHZ}	$\overline{OE}$	Y	MAX	4.1	5.2	4.9	9.4	1.7	3.1	9.1	7.3	10.1	12.9
t_{PLZ}				4.1	5.2	4.9	9.4	1.7	3.1	9.1	7.3	10.1	12.9

UNIT:ns

1G332

SINGLE 3-INPUT POSITIVE-OR GATE

Logic Diagram



● $Y = A + B + C$

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
H	X	X	H
X	H	X	H
X	X	H	H
L	L	L	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-32	-24	-8	-4	mA
I_{OL}	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t_{PLH}	A, B or C	Y	MAX	3.5	4.8	6.2	17.2
t_{PHL}				3.5	4.8	6.2	17.2

UNIT:ns

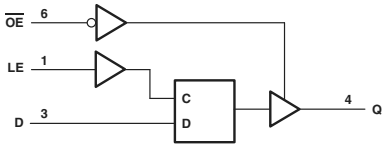
: **PREVIEW**

1G373

SINGLE D-TYPE LATCH WITH 3-STATE OUTPUT

- 3-State Outputs
- Buffered Control Inputs

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	L	L
L	H	H	H
L	L	X	Q_O
H	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-32	-24	-8	-4	mA
I_{OL}	MAX	32	24	8	4	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t_w	Pulse duration, LE high			MIN	3	3	3	3
t_{su}	Setup time, data before LE ↓			MIN	1.5	1.5	2	2.4
t_h	Hold time, data after LE ↓			MIN	1.5	1.5	1.5	2.5
t_{PLH}		D	Q	MAX	4	5.4	7.3	16
t_{PHL}					4	5.4	7.3	16
t_{PLH}		LE	Q	MAX	4	5.5	7.4	16.3
t_{PHL}					4	5.5	7.4	16.3
t_{PZH}		$\overline{OE}$	Q	MAX	3.7	5.1	6.3	13
t_{PZL}					3.7	5.1	6.3	13
t_{PHZ}		$\overline{OE}$	Q	MAX	4.6	6.5	5.9	17.4
t_{PLZ}					4.6	6.5	5.9	17.4

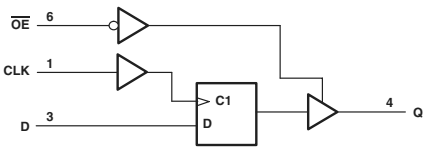
UNIT : ns

1G374

SINGLE D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT

- 3-State Outputs
- Buffered Control Inputs

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	L	L
L	↑	H	H
L	H or L	X	Q
H	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-32	-24	-8	-4	mA
I_{OL}	MAX	32	24	8	4	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
f_{max}				MIN	175	150	125	100
t_w	Pulse duration, CLK high or low			MIN	2.5	2.8	3	3.3
t_{su}	Setup time, data before CLK ↑			MIN	1.5	2	2.5	3.5
t_h	Hold time, data after CLK ↑			MIN	1.5	1.5	1.6	3.4
t_{PLH}		CLK	Q	MAX	4	6	8.2	18.3
t_{PHL}					4	6	8.2	18.3
t_{PZH}		$\overline{OE}$	Q	MAX	3.5	5	6.3	13
t_{PZL}					3.5	5	6.3	13
t_{PHZ}		$\overline{OE}$	Q	MAX	3.1	4.5	5.3	14
t_{PLZ}					3.1	4.5	5.3	14

UNIT f_{max} : MHz other : ns

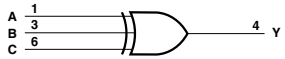
: **PREVIEW**

1G386

SINGLE 3-INPUT EXCLUSIVE-XOR GATE

- $Y = A \oplus B \oplus C$

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
L	L	L	L
L	L	H	H
L	H	L	H
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	L
H	H	H	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-32	-24	-8	-4	mA
I_{OL}	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t_{PLH}	A, B or C	Y	MAX	4	5	5.5	12
t_{PHL}				4	5	5.5	12

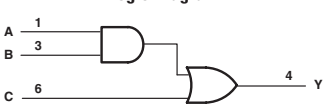
UNIT:ns

1G0832

SINGLE 3-INPUT POSITIVE AND-OR GATE

- $Y = (A \bullet B) + C$
- Can Be Used in Three Combinations
  - AND-OR Gate
  - AND Gate
  - OR Gate

Logic Diagram



FUNCTION SELECTION TABLE

2-Input AND Gate
2-Input OR Gate
Y = (A • B) + C

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
X	X	H	H
H	H	X	H
X	L	L	L
L	X	L	L

X = Valid H or L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-32	-24	-8	-4	mA
I_{OL}	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t_{PLH}	A, B, or C	Y	MAX	4	5.9	7.6	17.5
t_{PHL}				4	5.9	7.6	17.5

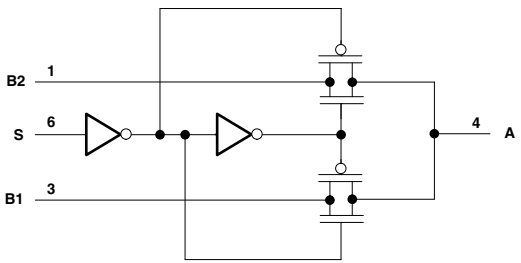
UNIT : ns

1G3157

SINGLE-POLE, DOUBLE-THROW ANALOG SWITCH

- Useful for Both Analog and Digital Apprications
- Specified Break-Before-Make Switching
- Rail-to-Rail Signal Handling
- High Degree of Linearity

Logic Diagram



FUNCTION TABLE

CONTROL INPUT S	ON CHANNEL
L	B1
H	B2

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	mA

ELECTRICAL CHARACTERISTICS

PARAMETER	MAX or MIN	LVC 5V		LVC 3.3V		LVC 2.5V		LVC 1.8V		UNIT
I_O		30	-30	24	-24	8	-8	4	-4	mA
R_{ON}	MAX	7	15	9	20	12	30	20	50	W

UNIT:ns

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t_{PLH}	A or Bn	Bn or A	MAX	0.3	0.8	1.2	2
t_{PHL}				0.3	0.8	1.2	2
t_{PZH}	S	Bn	MAX	5.7	7.6	14	24
t_{PZL}				5.7	7.6	14	24
t_{PHZ}	S	Bn	MAX	3.8	5.3	7.5	13
t_{PLZ}				3.8	5.3	7.5	13

UNIT:ns

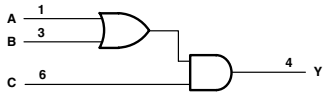
: **PREVIEW**

1G3208

SINGLE 3-INPUT POSITIVE OR-AND GATE

- Y = (A + B)•C
- Can Be Used in Three Combinations
  - OR-AND Gate
  - OR Gate
  - AND Gate

Logic Diagram



FUNCTION SELECTION TABLE

2-Input AND Gate
2-Input OR Gate
Y = (A + B) • C

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
H	X	H	H
X	H	H	H
X	X	L	L
L	L	H	L

X = Valid H or L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-32	-24	-8	-4	mA
I_{OL}	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t_{PLH}	A, B, or C	Y	MAX	4	5.9	7.6	17.5
t_{PHL}				4	5.9	7.6	17.5

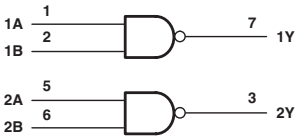
UNIT : ns

2G00

DUAL 2-INPUT POSITIVE-NAND GATE

● $Y = \overline{A \bullet B}$

Logic Diagram



FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	**B**	**Y**
H	H	L
L	X	H
X	L	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-32	-24	-8	-4	-9	-8	mA
I_{OL}	MAX	32	24	8	4	9	8	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
t_{PLH}	A or B	Y	MAX	3.3	4.3	4.8	8.6	1.7	2.1
t_{PHL}				3.3	4.3	4.8	8.6	1.7	2.1

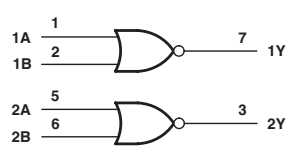
UNIT:ns

2G02

DUAL 2-INPUT POSITIVE-NOR GATE

● $Y = \overline{A + B}$

Logic Diagram



FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	**B**	**Y**
H	X	L
X	H	L
L	L	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-32	-24	-8	-4	-9	-8	mA
I_{OL}	MAX	32	24	8	4	9	8	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
t_{PLH}	A or B	Y	MAX	4.4	4.9	5.4	8.9	1.9	2.4
t_{PHL}				4.4	4.9	5.4	8.9	1.9	2.4

UNIT:ns

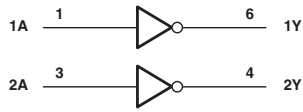
: **PREVIEW**

2G04

DUAL INVERTER GATE

● $Y = \overline{A}$

Logic Diagram



FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-32	-24	-8	-4	-9	-8	mA
I_{OL}	MAX	32	24	8	4	9	8	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
t_{PLH}	A	Y	MAX	3.2	4.1	4.4	8	1.5	2
t_{PHL}				3.2	4.1	4.4	8	1.5	2

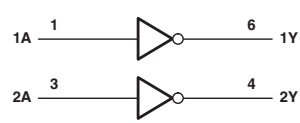
UNIT:ns

2GU04

DUAL INVERTER GATE

● $Y = \overline{A}$

Logic Diagram



FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-32	-24	-8	-4	-9	-8	mA
I_{OL}	MAX	32	24	8	4	9	8	mA

SWITCHING CHARACTERISTICS

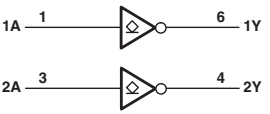
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
t_{PLH}	A	Y	MAX	3	3.7	4	5.5	2	2.7
t_{PHL}				3	3.7	4	5.5	2	2.7

UNIT:ns

2G06

DUAL INVERTER BUFFER/DRIVER WITH OPEN-DRAIN OUTPUTS

Logic Diagram



FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA
V_O	MAX	5.5	5.5	5.5	5.5	3.6	3.6	V
I_{OL}	MAX	32	24	8	4	9	8	mA

SWITCHING CHARACTERISTICS

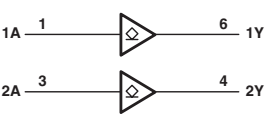
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
t_{PLH}	A	Y	MAX	2.9	3.4	3.9	7.2	1.2	2.5
t_{PHL}				2.9	3.4	3.9	7.2	1.8	2.3

UNIT:ns

2G07

DUAL BUFFER/DRIVER WITH OPEN-DRAIN OUTPUTS

Logic Diagram



FUNCTION TABLE
(each buffer/deiver)

INPUT A	OUTPUT Y
H	H
L	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA
V_O	MAX	5.5	5.5	5.5	5.5	3.6	3.6	V
I_{OL}	MAX	32	24	8	4	9	8	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
t_{PLH}	A	Y	MAX	2.9	3.7	4.4	8.6	1.2	2.5
t_{PHL}				2.9	3.7	4.4	8.6	1.8	2.3

UNIT:ns

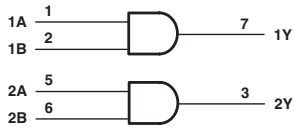
: **PREVIEW**

2G08

DUAL 2-INPUT POSITIVE-AND GATE

● Y = A•B

Logic Diagram



FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-32	-24	-8	-4	-9	-8	mA
I_{OL}	MAX	32	24	8	4	9	8	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
t_{PLH}	A or B	Y	MAX	3.8	4.7	5.1	9	1.6	2.1
t_{PHL}				3.8	4.7	5.1	9	1.6	2.1

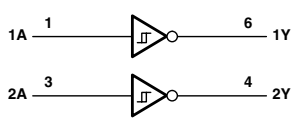
UNIT:ns

2G14

DUAL SCHMITT-TRIGGER INVERTER

● $Y = \overline{A}$

Logic Diagram



FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-32	-24	-8	-4	-9	-8	mA
I_{OL}	MAX	32	24	8	4	9	8	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
t_{PLH}	A	Y	MAX	4.3	5.4	5.7	9.5	TBD	TBD
t_{PHL}				4.3	5.4	5.7	9.5	TBD	TBD

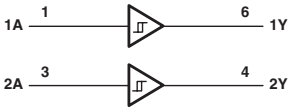
UNIT:ns

2G17

DUAL SCHMITT-TRIGGER BUFFER

● Y = A

Logic Diagram



FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	H
L	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-32	-24	-8	-4	mA
I_{OL}	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t_{PLH}	A	Y	MAX	4.3	5.4	5.7	9.3
t_{PHL}				4.3	5.4	5.7	9.3

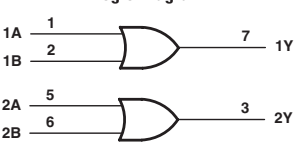
UNIT:ns

2G32

DUAL 2-INPUT POSITIVE-OR GATE

● Y = A + B

Logic Diagram



FUNCTION TABLE
(each gate)

INPUTS A	INPUTS B	OUTPUT Y
H	X	H
X	H	H
L	L	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-32	-24	-8	-4	-9	-8	mA
I_{OL}	MAX	32	24	8	4	9	8	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
t_{PLH}	A or B	Y	MAX	3.2	3.8	4.4	8	1.7	2.1
t_{PHL}				3.2	3.8	4.4	8	1.7	2.1

UNIT:ns

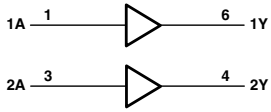
: **PREVIEW**

2G34

DUAL BUFFER GATE

● Y = A

Logic Diagram



FUNCTION TABLE
(each gate)

INPUT A	OUTPUT Y
H	H
L	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-32	-24	-8	-4	-9	-8	mA
I_{OL}	MAX	32	24	8	4	9	8	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
t_{PLH}	A	Y	MAX	3.2	4.1	4.4	8.6	1.8	2.4
t_{PHL}				3.2	4.1	4.4	8.6	1.8	2.4

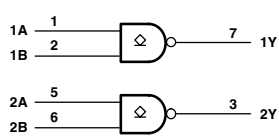
UNIT:ns

2G38

SINGLE 2-INPUT NAND GATE WITH OPEN-DRAIN OUTPUT

● $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$

Logic Diagram



FUNCTION TABLE
(each gate)

INPUTS A	INPUTS B	OUTPUT Y
L	L	H
L	H	H
H	L	H
H	H	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	mA
V_O	MAX	5.5	5.5	5.5	5.5	mA
I_{OL}	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t_{PLH}	A or B	Y	MAX	3.9	4.5	6	10
t_{PHL}				3.9	4.5	6	10

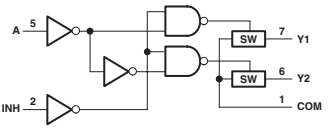
UNIT : ns

2G53

SINGLE-POLE DOUBLE-THROW (SPDT) ANALOG SWITCH 2:1 ANALOG MULTIPLEXER/DEMULTIPLEXER

- High On-Off Outputs Voltage Ratio
- High Degree of Linearity

Logic Diagram



FUNCTION TABLE

CONTROL INPUTS		ON CHANNEL
INH	A	
L	L	Y1
L	H	Y2
H	X	None

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I_{CC}	MAX	0.001	0.001	0.001	0.001	0.01	0.01	mA
R_{ON}	MAX	13	17	20	30	15	20	mA
$R_{ON(P)}$	MAX	15	20	30	120	20	80	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
t_{PLH}	COM or Y	Y or COM	MAX	0.6	0.8	1.2	2	0.2	0.4
t_{PHL}				0.6	0.8	1.2	2	0.2	0.4
t_{PZH}	INH	COM or Y	MAX	4.5	5.4	6.1	9	2.2	3.1
t_{PZL}				4.5	5.4	6.1	9	2.2	3.1
t_{PHZ}				8	8.1	8.3	10.9	2.2	3.4
t_{PLZ}				8	8.1	8.3	10.9	2.2	3.4
t_{PZH}	A	COM or Y	MAX	5.4	5.8	7.2	10.3	2.2	3.0
t_{PZL}				5.4	5.8	7.2	10.3	2.2	3.0
t_{PHZ}				5	7.2	7.9	9.4	2.3	3.0
t_{PLZ}				5	7.2	7.9	9.4	2.3	3.0

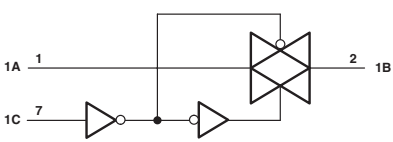
UNIT:ns

2G66

DUAL BILATERAL ANALOG SWITCH

- High On-Off Outputs Voltage Ratio
- High Degree of Linearity
- Rail-to-Rail Input/Output

Logic Diagram, each switch



One of Two Switches

FUNCTION TABLE
(each section)

CONTROL INPUT (C)	SWITCHI
L	OFF
H	ON

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA
R_{ON}	MAX	10	15	20	30	15	20	mA
$R_{ON(P)}$	MAX	15	20	30	120	20	80	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
t_{PLH}	A or B	B or A	MAX	0.6	0.8	1.2	2	0.7	0.7
t_{PHL}				0.6	0.8	1.2	2	0.7	0.7
t_{PZH}	C	A or B	MAX	3.9	4.4	5.6	10	2.3	2.7
t_{PZL}				3.9	4.4	5.6	10	2.3	2.7
t_{PHZ}	C	A or B	MAX	6.3	7.2	6.9	10.5	2	3.4
t_{PLZ}				6.3	7.2	6.9	10.5	2	3.4

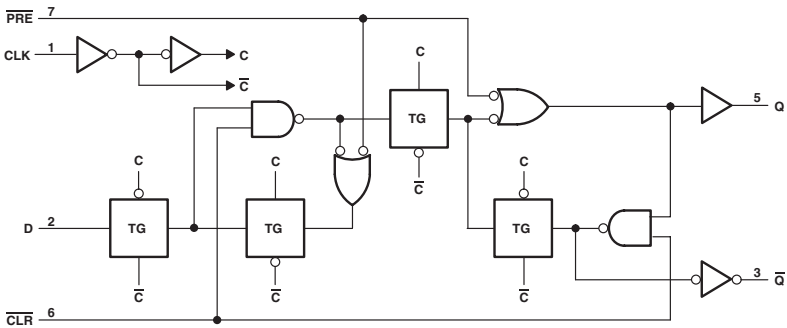
UNIT:ns

: **PREVIEW**

2G74

SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

† This configuration is nonstable; that is, it does not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-32	-16	-8	-4	mA
I_{OL}	MAX	32	16	8	4	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

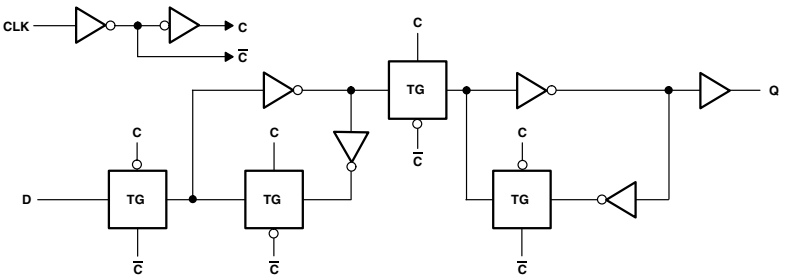
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
fmax			MIN	200	175	175	80
tw	CLK		MIN	2	2.7	2.7	6.2
	$\overline{PRE}$ or $\overline{CLR}$ low			2	2.7	2.7	6.2
tsu	Data		MIN	1.1	1.3	1.7	2.9
	$\overline{PRE}$ or $\overline{CLR}$ inactive			1	1.2	1.4	1.9
th			MIN	0.5	1.2	0.3	0
t_{PLH}	CLK	Q	MAX	4.1	5.9	7.1	13.4
t_{PHL}				4.1	5.9	7.1	13.4
t_{PLH}	CLK	$\overline{Q}$	MAX	4.4	6.2	7.7	14.4
t_{PHL}				4.4	6.2	7.7	14.4
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	MAX	4.1	5.9	7	12.9
t_{PHL}				4.1	5.9	7	12.9

UNIT:ns

2G79

DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUT
CLK	D	Q
↑	H	H
↑	L	L
L	X	Q_0

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I_{CC}	MAX	0.005	0.005	0.005	0.005	0.01	0.01	mA
I_{OH}	MAX	-32	-24	-8	-4	-9	-8	mA
I_{OL}	MAX	32	24	8	4	9	8	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
fmax			MIN	160	160	160	160	275	250
tw	CLK high or low		MIN	2.5	2.5	2.5	2.5	1	1
tsu	Before CLK ↑, Data high		MIN	0.9	1.1	1.4	2.2	0.5	0.6
	Before CLK ↑, Data low			0.9	1.1	1.4	2.2	0.5	0.6
th	Data after CLK ↑		MIN	0.5	0.7	0.8	1.4	0.1	0.1
t_{PLH}	CLK	Q	MAX	4.5	5.2	7.0	9.9	1.8	2.4
t_{PHL}				4.5	5.2	7.0	9.9	1.8	2.4

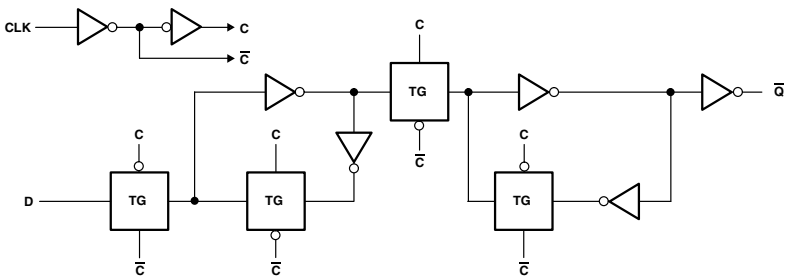
UNIT fmax : MHz other : ns

: **PREVIEW**

2G80

DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

Logic Diagram



FUNCTION TABLE

(each flip-flop)

INPUTS		OUTPUT
CLK	D	Q̄
↑	H	L
↑	L	H
L	X	$\bar{Q}_0$

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I_{CC}	MAX	0.005	0.005	0.005	0.005	0.01	0.01	mA
I_{OH}	MAX	-32	-24	-8	-4	-9	-8	mA
I_{OL}	MAX	32	24	8	4	9	8	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
fmax			MIN	160	160	160	160	275	250
tw	CLK high or low		MIN	2.5	2.5	2.5	2.5	1	1
tsu	Before CLK ↑, Data high		MIN	0.9	1.1	1.4	2.2	0.5	0.6
	Before CLK ↑, Data low			0.9	1.1	1.4	2.2	0.5	0.6
th	Data after CLK ↑		MIN	0.6	0.8	1.0	1.6	0.5	0.1
t_{PLH}	CLK	Q̄	MAX	4.5	5.2	7.0	13.9	1.8	2.4
t_{PHL}				4.5	5.2	7.0	13.9	1.8	2.4

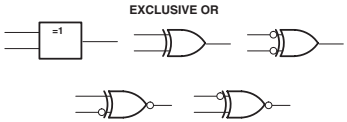
UNIT fmax : MHz other : ns

2G86

DUAL 2-INPUT EXCLUSIVE-OR GATE

● $Y = A \oplus B$

Logic Diagram



An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

FUNCTION TABLE
(each gate)

INPUTS A	INPUTS B	OUTPUT Y
L	L	L
L	H	H
H	L	H
H	H	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-32	-24	-8	-4	-9	-8	mA
I_{OL}	MAX	32	24	8	4	9	8	mA

SWITCHING CHARACTERISTICS

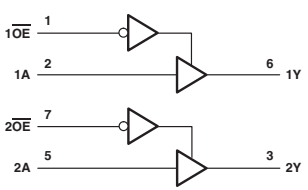
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
t_{PLH}	A or B	Y	MAX	3.6	4.7	5.7	9.9	2.0	2.6
t_{PHL}				3.6	4.7	5.7	9.9	2.0	2.6

UNIT:ns

2G125

DUAL BUS BUFFER GATE WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
(each buffer)

INPUTS $\overline{OE}$	INPUTS A	OUTPUT Y
L	H	H
L	L	L
H	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-32	-24	-8	-4	-9	-8	mA
I_{OL}	MAX	32	24	8	4	9	8	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
t_{PLH}	A	Y	MAX	3.7	4.3	4.8	9.1	1.8	2.6
t_{PHL}				3.7	4.3	4.8	9.1	1.8	2.6
t_{PZH}	$\overline{OE}$	Y	MAX	3.8	4.7	5.6	9.9	2.2	2.9
t_{PZL}				3.8	4.7	5.6	9.9	2.2	2.9
t_{PHZ}	$\overline{OE}$	Y	MAX	3.4	4.6	5.8	11.6	2	3.6
t_{PLZ}				3.4	4.6	5.8	11.6	2	3.6

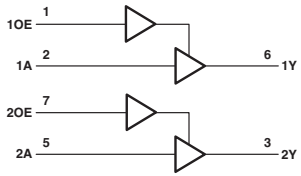
UNIT:ns

: **PREVIEW**

2G126

DUAL BUS BUFFER GATE WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
OE	A	Y
H	H	H
H	L	L
L	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-32	-24	-8	-4	-9	-8	mA
I_{OL}	MAX	32	24	8	4	9	8	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
t_{PLH}	A	Y	MAX	3.2	4	4.9	9.8	1.8	2.3
t_{PHL}				3.2	4	4.9	9.8	1.8	2.3
t_{PZH}	OE	Y	MAX	3.1	4.1	5	10	2.2	2.4
t_{PZL}				3.1	4.1	5	10	2.2	2.4
t_{PHZ}	OE	Y	MAX	3.3	4.4	5.7	12.6	1.8	3.3
t_{PLZ}				3.3	4.4	5.7	12.6	1.8	3.3

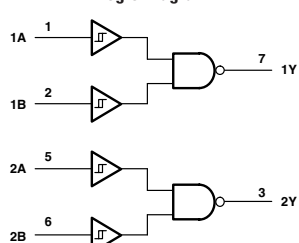
UNIT:ns

2G132

DUAL 2-INPUT NAND GATE WITH SCHMITT-TRIGGER INPUT

● $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$

Logic Diagram



FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-32	-24	-8	-4	mA
I_{OL}	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

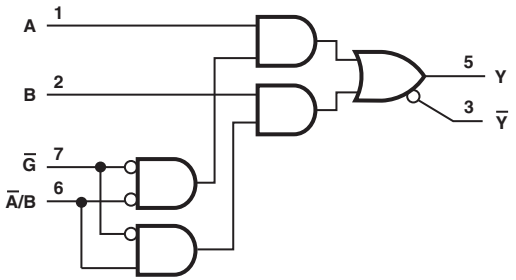
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t_{PLH}	A or B	Y	MAX	5	6	7.5	16
t_{PHL}				5	6	7.5	16

UNIT : ns

2G157

SINGLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{G}$	$\overline{A}$/B	A	B	Y	$\overline{Y}$
H	X	X	X	L	L
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-32	-24	-8	-4	mA
I_{OL}	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t_{PLH}	A or B	Y or $\overline{Y}$	MAX	4	6	8	14
t_{PHL}				4	6	8	14
t_{PLH}	$\overline{A}$/B	Y or $\overline{Y}$	MAX	4	6	9	16
t_{PHL}				4	6	9	16
t_{PLH}	$\overline{G}$	Y or $\overline{Y}$	MAX	4	6	8	14
t_{PHL}				4	6	8	14

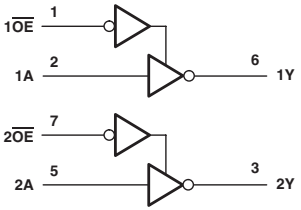
UNIT:ns

: **PREVIEW**

2G240

DUAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-32	-24	-8	-4	-9	-8	mA
I_{OL}	MAX	32	24	8	4	9	8	mA

SWITCHING CHARACTERISTICS

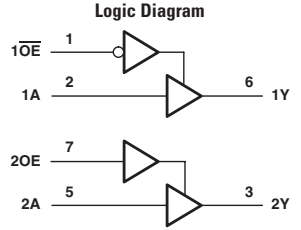
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
t_{PLH}	A	Y	MAX	4	4.6	5.5	11.3	1.7	2.5
t_{PHL}				4	4.6	5.5	11.3	1.7	2.5
t_{PZH}	$\overline{OE}$	Y	MAX	5	5.4	6.6	11.7	2.1	3.1
t_{PZL}				5	5.4	6.6	11.7	2.1	3.1
t_{PLZ}	$\overline{OE}$	Y	MAX	4.2	5.5	5.7	12.8	1.9	3.7
t_{PHZ}				4.2	5.5	5.7	12.8	1.9	3.7

UNIT:ns

2G241

DUAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUT
$1\overline{OE}$	1A	1Y
L	H	H
L	L	L
H	X	Z

INPUTS		OUTPUT
2OE	2A	2Y
H	H	H
H	L	L
L	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-32	-24	-8	-4	-9	-8	mA
I_{OL}	MAX	32	24	8	4	9	8	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
t_{PLH}	A	Y	MAX	3.7	4.3	4.8	8.8	1.8	2.5
t_{PHL}				3.7	4.3	4.8	8.8	1.8	2.5
t_{PZL}	$\overline{OE}$	Y	MAX	3.8	4.7	5.6	9.9	2	2.8
t_{PZH}				3.8	4.7	5.6	9.9	2	2.8
t_{PLZ}	$\overline{OE}$	Y	MAX	3.4	4.4	5.8	11.6	2.1	3.6
t_{PHZ}				3.4	4.4	5.8	11.6	2.1	3.6
t_{PZL}	OE	Y	MAX	3.3	4.1	4.7	8.8	2	2.8
t_{PZH}				3.3	4.1	4.7	8.8	2	2.8
t_{PLZ}	OE	Y	MAX	3.3	4.2	5.2	12.5	2.1	8.6
t_{PHZ}				3.3	4.2	5.2	12.5	2.1	8.6

UNIT:ns

3G04

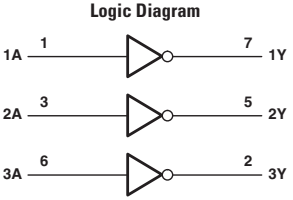
TRIPLE INVERTER GATE

● $Y = \overline{A}$

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-32	-24	-8	-4	mA
I_{OL}	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t_{PLH}	A	Y	MAX	3.2	4.1	4.4	7.9
t_{PHL}				3.2	4.1	4.4	7.9

UNIT:ns

3GU04

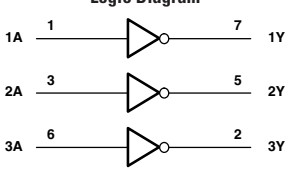
TRIPLE INVERTER GATE

● $Y = \overline{A}$

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-32	-24	-8	-4	mA
I_{OL}	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
tPLH	A	Y	MAX	3.2	3.9	4	9.2
tPHL				3.2	3.9	4	9.2

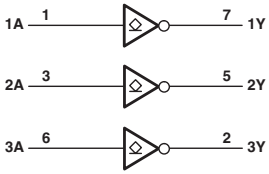
UNIT : ns

: **PREVIEW**

3G06

TRIPLE INVERTER BUFFER/DRIVER WITH OPEN-DRAIN OUTPUTS

Logic Diagram



FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	mA
V_O	MAX	5.5	5.5	5.5	5.5	mA
I_{OL}	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

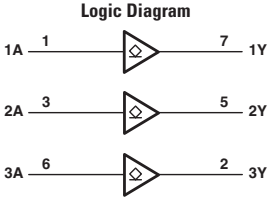
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t_{PLH}	A	Y	MAX	2.9	3.4	3.9	7.2
t_{PHL}				2.9	3.4	3.9	7.2

UNIT:ns

3G07

TRIPLE BUFFER/DRIVER WITH OPEN-DRAIN OUTPUTS

Logic Diagram



FUNCTION TABLE
(each buffer/driver)

INPUT A	OUTPUT Y
H	H
L	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	mA
V_O	MAX	5.5	5.5	5.5	5.5	mA
I_{OL}	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t_{PLH}	A	Y	MAX	2.9	3.7	4.3	7.8
t_{PHL}				2.9	3.7	4.3	7.8

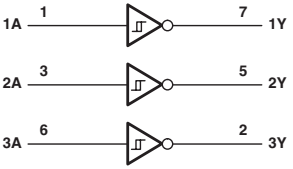
UNIT:ns

3G14

TRIPLE SCHMITT-TRIGGER INVERTER

● $Y = \overline{A}$

Logic Diagram



FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-32	-24	-8	-4	mA
I_{OL}	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t_{PLH}	A	Y	MAX	4.3	5.4	5.7	9.2
t_{PHL}				4.3	5.4	5.7	9.2

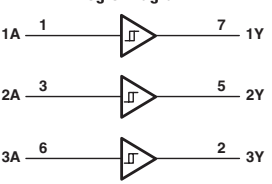
UNIT:ns

3G17

TRIPLE SCHMITT-TRIGGER BUFFER

● $Y = A$

Logic Diagram



FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-32	-24	-8	-4	mA
I_{OL}	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t_{PLH}	A	Y	MAX	4.1	5.4	6.2	9.2
t_{PHL}				4.1	5.4	6.2	9.2

UNIT:ns

: **PREVIEW**

3G34

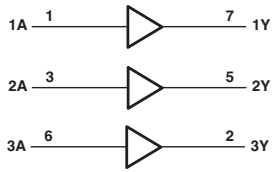
TRIPLE BUFFER GATE

● Y = A

FUNCTION TABLE
(each gate)

INPUT A	OUTPUT Y
H	H
L	L

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-32	-24	-8	-4	mA
I_{OL}	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t_{PLH}	A	Y	MAX	3.2	4.1	4.4	7.9
t_{PHL}				3.2	4.1	4.4	7.9

UNIT:ns

FUNCTION

Standard

GATE (AND / NAND / OR / NOR)

Description	No. of Input	Curcuit	Input	Output	Device	Technology																									
						Bipolar						CMOS		BiCMOS				Advanced CMOS				Low-Voltage CMOS					
						TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	AUC	
POS-AND	2	4			08	×	●	●	●	●	●	●/●	●/●					●/●/●	●/●/●	●	●	●A	●A	●		●	
				OC	09	×	●	●	●		×	×/-															
				OC	15		×	×	×																		
				BUF	1008				×A	●A																	
			SCH		7001							●/-															
		6		BUF	808				×	●B		×/-															
				BUF	1808				×	×																	
	3	3			11		●	×	●A	●	●	●/●	-/●					×/●/-	×/●/-			●A					
				BUF	1011				×																		
	4	2			21		●		●A	●	●	●/●	×/●					×/-/-	×/-/-			●A					
POS-NAND	2	2			8003				×	●																	
		4			00	●	●	●	●A	●	●	●/●	●/●					●/●/●	●/●/●	●	●	●A	●A	●		●	
				OC	01	×	×		×			×/-															
				OC	03	×	●	×	●B			●/●	-/●														
			SCH		24		×																				
				OC	26	×	●																				
				BUF	37	×	●	●	●A		×																
				OC	38	●	●	●	●B		●																
			SCH		132	×	●	●				●/●	-/●					×/-/-	×/-/-	●	●	●A					
				BUF	1000				×A	●A																	
				OC	1003				×A																		
			SCH	OC	7003							×/-															
				OC	39	×																					
		6		BUF	804				●A	●B		×/-															
				BUF	1804				×A	×																	
	3	3			10	●	●	●	●A	●	●	●/●	-/●					×/●/●	×/●/●			●A	●A	●			
				OC	12	×	×		×																		
				BUF	1010				×																		
	4	2	SCH		13	×	×											×/-/-	-/×/-								
			SCH		18		×																				
					20	×	●	●	●A	●	●	●/●	-/●					×/×/●	×/×/●			●A					
				OC	22	×	×	×	×																		
				BUF	40	×	×	×	×		×																
				BUF	140			●																			
				BUF	1020				×																		
		3	SCH		618		×																				
	8	1			30	×	●	×	●A	●	●	×/●	-/●					×/-/ ×	●/-/ ×								
	12	1		3S	134			×																			
	13	1			133			×	●			×/-															
POS- OR	2	4			32	●	●	●	●	●	●	●/●	●/●					●/●/●	●/●/●	●	●	●A	●A	●		●	
				BUF	1032				×	●A																	
			SCH		7032							●/-															
		6		BUF	832				●A	●B		×/-															
				BUF	1832				×A	×																	
	3	3			4075							×/●	-/●														
POS- NOR	2	4			02	●	●	●	●A	●	●	●/●	●/●					×/-/ ●	×/-/ ●	●	●	●A	●A			●	
				BUF	28	×	×		×																		
				OC	33	×	●		●A																		
					36						×	×/-															
				BUF	128	●																					
				BUF	1002				×A																		
			SCH		7002							●/-															
				BUF	1036					×A																	
		6		BUF	805				●A	●B		×/-															
				BUF	1805				×	×																	
	3	3			27	×	●		●A	●	●	●/●	-/●					×/-/ ×	×/-/ ×			●A					
	4	2			23	×																					
					25	●																					
					4002							×/●															
	5	2			260			●			●																

Explanatory notes [Input] SCH: Schmitt-Trigger Inputs

Explanatory notes [Output] BUF: Buffered Output OC: Open-Collector Output

●: Product available in technology indicated *: New product planned in technology indicated

×: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCxx / CD74HCTxx

BCT: SN74BCTxx / SN64BCTxx

AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

GATE (EX-OR / EX-NOR / INVERTER / NONINVERTER / etc.)

Description	No. of Input	Curcuit	Input	Output	Device	Technology																					
						Bipolar						CMOS		BiCMOS				Advanced CMOS				Low-Voltage CMOS					
						TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	AUC
EX-OR	2	4			86	×	●A	●	●	●A	●	●/●	-/●					●/●/●	×/●/●	●	●	●A	●A			
				OC	136	×	●		×	×																	
					386		×					×/-															
EX-NOR	2	4		OC	266		●					●/-															
					810				×	×								×/-/-	×/-/-							
				OC	811				×	×																	
					7266							×/●															
EX-OR/NOR	2	4			135			×																			
INVERTING	1	6			04	●	●	●	●B	●	●	●/●	●/●					●/●/●	●/●/●	●	●	●A	●A	●		●
				OC	05	●	●	●	●A			●/-						-/-/ ●	-/-/ ●	●		●A				
				OC	06	●	●															●A	●A			●
			SCH		14	●	●					●/●	-/●					×/●/●	×/●/●	●	●	●A	●A	●		●
				OC	16	●	×																			
			SCH		19		●																			
				BUF	1004		×		●	●A																
				OC	1005		×		●																	
					4049							−/●														
					U04							●/●								●		●A	●A			●
		8	SCH		619		×																			
NON-INVERTING	1	4			425	×																				
					426	×																				
		6		OC	07	●	●															●A	●A			●
				OC	17	●																				●
					34				×	×								×/-/-	×/-/-							●
				OC	35				●A																	
				BUF	1034				●	●A																
				OC	1035				●																	
					4050							−/●														
OTHER	1	6			63		×																			
	2	6			31		●																			
	4	2			50	×																				
					51	×	●	●			×	×/-						×/-/-	×/-/-							
					60	×																				
	8	1			53	×																				
					55		×																			
					4078							×/-														
	10	1			54	×	×																			
	11	1			64			×			×							×/-/-	×/-/-							
				OC	65			×																		
	12	3		BUF	800													×/-/-	×/-/-							
				BUF	802													×/-/-	×/-/-							
	-	6			7006							×/-														
					7008							×/-														
					7074							×/-														
					7075							×/-														
					7076							×/-														

Explanatory notes [Input] SCH: Schmitt-Trigger Inputs

Explanatory notes [Output] BUF: Buffered Output OC: Open-Collector Output

Status ●: Product available in technology indicated *: New product planned in technology indicated

×: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCxx / CD74HCTxx

BCT: SN74BCTxx / SN64BCTxx

AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

BUFFER / DRIVER (NON-INVERTING)

Description	No. of Output	Output	Device	Technology																					
				Bipolar						CMOS		BiCMOS				Advanced CMOS									
				TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LV-AT	LVC	ALVC	AVC	AUC
NON-INVERTING	4	3S	125	×	●A				●	●/●	●/●	●A/●A	●	H●				●	●	●A	●	●A	●		●
		3S	126	×	●A				●	●/●	-/●	●A/●A	●	H●				●	●	●A		●A	●		●
	6	3S	365	×	●A					●/●	-/●														
		3S	367	×A	●A					●/●	-/●							●	●	●A					
	8	3S	241		●	●	●C	●A	●	●/●	×/●	●/-	●A	H●		×/●/-	×/●/●					-			
		3S	244		●	●	●C ●C1	●A	●	●/●	●/●	●/●	●A	●B H●A		●/●/●	●/●/●	●	●	●A	●	●A H●A Z●A	● H●		● H●
		3S	455									×/-													
		3S	465		●		×																		
		3S	467		×		×																		
		3S	541		●		● ●1		●	●/●	●/●	●A/-	●B	H●		-/●	-/●	●	●	●A	●	●A			
		3S	656													×/-/-	×/-/-								
		3S	747				×																		
		OC	757					●				●/●													
		OC	760				●	●				●/-													
		3S	1241																						
		3S	1244				●A																		
		R3S	2241									●/-	●												
		R3S	2244						×			●/-	●A									●A			
		R3S	2541				●																		
		3S	25241									×/-													
		3S	25244									●/●													
		OC	25757									×/-													
		OC	25760									×/-													
	10	3S	827										●			×/-/-	×/-/-					●A			
		R3S	2827									●C/-	×												
		3S	29827				●					●B/-													
	11	R3S	5400										●A												
	12	3S	5402										●A												
		R3S	16903																				H●		
	16	3S	16241										●A	H●			×					H×A			
		3S	16244										●A H●	●B H●A	H●	●	●	●	●			●A H●A Z●A	●A H●	●	● H●
		3S	16541										●A	H●			●	●	●			H●A	×		
		R3S	162241											H●											
		R3S	162244										●	●A H●	H●							●A H●A	H●		
		R3S	162541											H●									×		
	18	3S	16825										●				●						H●		
		R3S	162825										●												
		3S	16835											H●									● H●	●	
		R3S	162835																				● H● F●		
	20	3S	16827										●		H●		●						H●	●	*
		3S	162827										●A		H●								H●		
	32	3S	32244											● H●	H●							● H●A Z●A	H●		● H●
		R3S	322244																			H●A			

Explanatory notes [Output] 3S: 3-State Output R3S: Series Resistor and 3-State Output OC: Open-Collector Output

Status ●: Product available in technology indicated *: New product planned in technology indicated

×: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCxx / CD74HCTxx

BCT: SN74BCTxx / SN64BCTxx

AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

BUFFER / DRIVER (INVERTING, INVERTING AND NON-INVERTING, ADDRESS DRIVERS)

Description	No. of Output	Output	Device	Technology																				
				Bipolar						CMOS		BiCMOS				Advanced CMOS								
				TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LV-AT	LVC	ALVC	AVC	AUC
INVERTING	6	3S	366	×	×					×/●															
		3S	368	×A	●A					●/●	-/●														
		3S	436			×																			
		3S	437	×																					
	8	3S	231				×	×																	
		3S	240		●	●	●A ●A1	●A	●	●/●	●/●	●/-	●A	●A H●		●/●/●	●/●/●	●	●	●A		●A Z●A			● H●
		3S	456									×/-													
		3S	466		×		×																		
		3S	468		×		×																		
		3S	540		●		● ●1		×	●/●	●/●	●A/-	●	H●		-/-/ ●	-/-/ ●	●	●	●A		●A			
		3S	655													×/-/-	×/-/-								
		3S	746				×																		
		OC	756				×	●				●/-													
		OC	763					×																	
		3S	1240				×																		
		R3S	2240				×					●/-	●A												
		R3S	2540				×																		
		3S	25240									×/-													
		OC	25756									×/-													
	10	3S	828													×/-/-	×/-/-					●A			
		R3S	2828									×/-													
		3S	29828				×					×B/-													
	11	R3S	5401										●												
	12	R3S	5403										●												
	16	3S	16240										●A	● H●	H●	×	●	●	●			H●A Z●A	H●		●
		3S	16540										●A				×	●	●			H●A	×		
		R3S	162240											● H●									-		
		R3S	162540																				×		
	20	3S	16828														×						×		
	32	3S	32240											●								Z●A			
INVERTING AND NON-INVERTING	8	3S	230				×	×																	
		OC	762					×																	
ADDRESS DRIVERS	1-2	3S	16830																				H*		
		R3S	162830																				H● HS●		
	1-4	3S	16344																				H●		
		3S	16831																				H●		
		3S	16832																				H●		
		R3S	162344																				H●		
		R3S	162831																				● H●		
		R3S	162832																				H●		

Explanatory notes [Output] 3S: 3-State Output R3S: Series Resistor and 3-State Output OC: Open-Collector Output

Status ●: Product available in technology indicated *: New product planned in technology indicated

×: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCxx / CD74HCTxx

BCT: SN74BCTxx / SN64BCTxx

AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

BUS TRANSCEIVER (NON-INVERTING)

Description	No. of Output	Output	Device	Technology																					
				Bipolar						CMOS		BiCMOS				Advanced CMOS									
				TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LV-AT	LVC	ALVC	AVC	AUC
NON-INVERTING	4	3S	226			×																			
		3S	440		×																				
		OC	441		×																				
		3S	442		●																				
		3S	443		×																				
		3S	444		×																				
		OC	448		×																				
		3S	449		×																				
		3S	243		●		●A	×	×	-/●	-/●														
		3S	1243																						
	8	3S	245		●		●A ●A1	●	●	●/●	●/●	●/●	●B H●	●B H●A		●/●/●	●/●/●	●	●	●A	●	●A H●A Z●A	● H●	● H●	● H●
		3S	470													×/-/-	×/-/-								
		3S	472													×/-/-	×/-/-								
		3S	474													×/-/-	×/-/-								
		3S	543						●			●/-	●A	● H●		×/-/-	●/-/-					●A			
		OC	615				×																		
		OC	621		×		●A ●A1	×	×																
		3S	623		●		●A	×	×	●/-	●/-	●/-	●			×/-/ ●	●/-/ ●								
		3SOC	639		×		●A	×																	
		OC	641		● ●1		●A ●A1	●																	
		3S	645		● ●1		●A ●A1	●		●/-	●/-														
		3S	646		●		●A ●A1	●		●/●	●/●	●/-	● ●A	H●		×/-/ ●	×/-/ ●					●A			
		OC	647		×		×																		
		3S	652		●		●A ×A1	●		●/●	●/●	●/-	● ●A	H●		×/-/ ●	●/-/ ●					●A			
		3SOC	654		×		●																		
		3S	657						●			×/-	●A			×/-/-	×/-/-								
		3S	659							X/-	X/-														
		3S	665							X/-	X/-														
		3S	852					×								×/-/-	×/-/-								
		3S	856					×								×/-/-	×/-/-								
		3S	877					×								×/-/-	×/-/-								
		3S	899									×/-													
		3S	1245				●A																		
		3S	1645				●A																		
		3S	2245									●/-	● R●	H●								R●A			
		3S	2623				×																		
		3S	2645					×																	
		3S	2952									×/-	●A	H●								●A			
		3S	25245									●/●	●H												
		3S	25543									×/-													
		3S	25621									×/-													
		3S	25623									×/-													
		3S	25641									×/-													
		3S	25646									×/-													
		3S	25647									×/-													
		3S	25652									×/-													
		3S	25654									×/-													
	8+1P	3SOC	833										●			×/-/-	×/-/-								
		3SOC	853										●			×/-/-	×/-/-								
		3SOC	29833				×					×/-													
		3SOC	29853				×					×/-													
	9	3S	863										●			×/-/-	×/-/-					●A			
		3S	29863				●					●B/-													
	9 x 4	3S	16409																				H● HR●		
	10	3S	861										●			×/-/-	×/-/-					●A			
		3S	29861				×					×B/-													

Explanatory notes **[No. of Output] +P: With Parity Bit**

[Output] 3S: 3-State Output R3S: Series Resistor and 3-State Output

[Output] OC: Open-Collector Output 3SOC: 3-State Output / Open-Collector Output

Status **●: Product available in technology indicated *: New product planned in technology indicated**

×: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCxx / CD74HCTxx

BCT: SN74BCTxx / SN64BCTxx

AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

BUS TRANSCEIVER (NON-INVERTING)

Description	No. of Output	Output	Device	Technology																					
				Bipolar						CMOS		BiCMOS				Advanced CMOS									
				TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LV-AT	LVC	ALVC	AVC	AUC
NON-INVERTING	12/24	3S	16268																				×		
		3S	16269																				H● HR●A	●	
		3S	16270																				H●		
		3S	16271																				H●		
		3S	16272																				×		
		3S	162268																				H●		
		3S	162269																						
	16/32	3S	162280																				HG●		
	16	3S	16245										●A H●	●B H●A	H● HR●	●	●	*	●			●A H●A HR●A R●A Z●A	H● HR●	●	●
		3S	16334																				● H●	●	
		3S	16470										●				×								
		3S	16543										●	● H●	*	×	●					H●A	H●		
		3S	16623										●			×	●								
		3S	16646										●	● H●		×	●					●A H●A	H●	●	*
		3S	16652										●	H●	*	●	●					H●A	×		*
		3S	16952										●	● H●			●					H●A	H●		
		R3S	162245										● H●	●A H●	H●							R×			
		R3S	162334																				● H●		
	16X3	3S	32316										H●												
	18X3	3S	32318										H●												
	16+2P	3S	16657										●				●								
		3S	16833										●				×								
		3S	16853										●				×								
	18	3S	16472													×									
		3S	16474														×								
		3S	16500										●B	H●									H●		
		3S	16501										●	H●									H●		*
		3S	16525																				H●		
		3S	16600										●									-	H●		
		3S	16601										●		H●							-	H● HR●		
		3S	16834														×						●	●	
		3S	16863										●				●						H●		
		3S	16901																			H●	H●		
		R3S	162500										●												
		R3S	162501										●												
		R3S	162525																				H●		
		R3S	162600																						
		R3S	162601										●										H●		
		R3S	162834																				● F●		
	18/36	3S	16282																				H●		
		R3S	162262																				HG●		
	20	3S	16836																				H*	*	
		3S	16851														●								
		R3S	162836																				● H●		
	32	3S	32543										H●												
		3S	32952										×												
	36	3S	32245										H●	H●								● H●A R●A HR●A Z●A	H●		●
		3S	32500										×												
		3S	32501										H●										H●		

Explanatory notes [No. of Output] +P: With Parity Bit

[Output] 3S: 3-State Output R3S: Series Resistor and 3-State Output

[Output] OC: Open-Collector Output 3SOC: 3-State Output / Open-Collector Output

Status ●: Product available in technology indicated *: New product planned in technology indicated

×: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCxx / CD74HCTxx

BCT: SN74BCTxx / SN64BCTxx

AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

BUS TRANSCEIVER (INVERTING, NON-INVERTING / INVERTING)

Description	No. of Output	Output	Device	Technology																					
				Bipolar						CMOS		BiCMOS				Advanced CMOS									
				TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LV-AT	LVC	ALVC	AVC	AUC
INVERTING	4	3S	242		×		×	×	×	×/-	×/-														
		3S	446		×																				
		3S	1242				×																		
		R3S	2242				×																		
	8	3S	544						×			×/-				×/-/-	×/-/-								
		3S	471													×/-/-	×/-/-								
		3S	473													×/-/-	×/-/-								
		3S	475													×/-/-	×/-/-								
		OC	614				×																		
		3S	620		×		●A	×	×	×/-	×/-/-	×/-	●			×/-/-	×/-/-								
		OC	622		×		×	×	×																
		3SOC	638		×		●A ●A1	●A																	
		3S	640		● ●1		●B ●B1	●		●/●	×/●	●/-	●			×/-/-	×/-/-								
		OC	642		● ●1		×A ●A1	×				×/-														
		3S	648		●		●A	●		×/-	×/-	×/-				×/-/-	×/-/-								
		OC	649		×		×																		
		3S	651		×		●A	×		×/-	×/-	×/-	●			×/-/-	×/-/ ●								
		3SOC	653		×		●																		
		3S	658							×/-	×/-														
		3S	664							×/-	×/-														
		3S	1640				×																		
		3S	2620				×																		
		3S	2640					×				×/-													
		3S	2953									×/-													
		3S	25620									×/-													
		3S	25622									×/-													
		3S	25640									×/-													
		3S	25642									●/-													
		3S	25648									×/-													
		3S	25649									×/-													
		3S	25651									×/-													
		3S	25653									×/-													
	8+1P	3SOC	834													×/-/-	×/-/-								
		3SOC	854													×/-/-	×/-/-								
		3SOC	29834				×					×/-													
		3SOC	29854				●					●/-													
	9	3S	864													×/-/-	×/-/-								
		3S	29864				×					●B/-													
	10	3S	862													×/-/-	×/-/-								
		3S	29862				×					×B/-													
	16	3S	16471																						
		3S	16544														×								
		3S	16620													×	×								
		3S	16640										●			×	×								
		3S	16648														×								
		3S	16651														●								
		3S	16862																						
		3S	16953														×								
	18	3S	16475														×								
		3S	16524																				H●		
		3S	16864														×								

Description	No. of Output	Output	Device	Technology																					
				Bipolar						CMOS		BiCMOS				Advanced CMOS									
				TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LV-AT	LVC	ALVC	AVC	AUC
NON-INVERTING /INVERTING	8	3S	643		×		×	×		×/-	×/-					×/-/-	×/-/-								
		OC	644		×		×	×																	
		OC	758				×	×																	
		OC	759					×																	
		3S	7340							×/-															

Explanatory notes [No. of Output] +P: With Parity Bit

[Output] 3S: 3-State Output R3S: Series Resistor and 3-State Output

[Output] OC: Open-Collector Output 3SOC: 3-State Output / Open-Collector Output

Status ●: Product available in technology indicated *: New product planned in technology indicated

×: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCxx / CD74HCTxx

BCT: SN74BCTxx / SN64BCTxx

AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

J/K FLIP-FLOP

Trigger	Curcuit	PRE • CLR	Output	Q • $\overline{Q}$	Device	Technology: Bipolar TTL	Bipolar LS	Bipolar S	Bipolar ALS	Bipolar AS	Bipolar F	CMOS HC	CMOS HCT	BiCMOS BCT	BiCMOS ABT	BiCMOS LVT	BiCMOS ALVT	Advanced CMOS AC	Advanced CMOS ACT	Advanced CMOS AHC	Advanced CMOS AHCT	Advanced CMOS LV	Advanced CMOS LV-AT	Advanced CMOS LVC	Advanced CMOS ALVC	Advanced CMOS AVC	Advanced CMOS AUC
POS	1	B	2S	B	72	×																					
	2	B	2S	B	70	×																					
		B	2S	B	73	×	●A					×/●	-/●														
		B	2S	B	109	×	●A		●A	●A	●	●/●	-/●					×/-/ ●	×/-/ ●								
		B	2S	B	110	×																					
		B	2S	B	111	×																					
	4	B	2S	Q	376	×																					
NEG	2	B	2S	B	76	×	×					×/-/-															
		B	2S	B	78		×					×/-/-															
		B	2S	B	107	●	●A					×/●	-/●														
		B	2S	B	112		●A	●A	●A		●	●/●	-/●					×/-/ ●	×/-/ ●					●A			
		B	2S	B	113		×	×	×		×	×/-/-															
		B	2S	B	114		×	×	×		×	×/-/-															
	4	B	2S	Q	276	×																					

D-TYPE FLIP-FLOP

Trigger	Curcuit	PRE • CLR	Output	Q • $\overline{Q}$	Device	Technology: Bipolar TTL	Bipolar LS	Bipolar S	Bipolar ALS	Bipolar AS	Bipolar F	CMOS HC	CMOS HCT	BiCMOS BCT	BiCMOS ABT	BiCMOS LVT	BiCMOS ALVT	Advanced CMOS AC	Advanced CMOS ACT	Advanced CMOS AHC	Advanced CMOS AHCT	Advanced CMOS LV	Advanced CMOS LV-AT	Advanced CMOS LVC	Advanced CMOS ALVC	Advanced CMOS AVC	Advanced CMOS AUC
POS	2	B	2S	B	74	×A	●A	●	●A	●A	●	●/●	●/●					●/●/●	●/●/●	●	●	●A		●A	*		●
	4	C	2S	B	171		×																				
		C	2S	B	175	×	●	●	●	●B	●	●/●	-/●					×/-/ ●	×/-/ ●			●A					
			2S	B	379		×				×	×/-						×/-/-	×/-/-								
	6	C	2S	Q	174	×	●	●	●	●	●A	●/●	-/●					×/-/ ●	×/-/ ●	●	●	●A					
			2S	Q	378		●				×	×/-						×/-/-	×/-/-								
	8	C	2S	Q	273	×	●		●		×	●/●	●/●		●	H●		×/-/ ●	×/-/ ●	●	●	●A					
			3S	Q	374		●	●	●A	●	●	●/●	●/●	●/-	●A	H●		×/●/●	●/●/●	●	●	●A		●A	H●		*
			2S	Q	377		●			●A	●/●	●/●		●A				×/-/-	×/-/-								
			3S	Q	478													×/-/-	×/-/-								
			3S	$\overline{Q}$	534				●A	×	×	×/●	×/●	×/-	●A			×/●/●	×/●/-								
			3S	$\overline{Q}$	564				●B		×	×/●	×/●	×/-				×/●/-	×/●/-								
			3S	Q	574				●B	●	●	●/●	●/●	●/-	●A	● H●		×/●/●	×/●/●	●	●	●A		●A			
			3S	Q	575				●A	×																	
			3S	$\overline{Q}$	576				●B	●																	
			3S	$\overline{Q}$	577				●A	×																	
			3S	Q	825					●A								×/-/-	×/-/-								
			3S	Q	826					×								×/-/-	×/-/-								
		C	3S	Q	874				●B	●								×/-/-	×/-/-								
		P	3S	$\overline{Q}$	876				●A	●																	
		C	3S	Q	878				×	×																	
		C	3S	$\overline{Q}$	879				×A	×																	
			3S	Q	4374					●B																	
			3S	Q	29825				×	×				●/-													
			3S	Q	29826				×	×				×/-													
	9	C	3S	Q	823					●A					●			×/-/-	×/-/-					●A			
		C	3S	$\overline{Q}$	824					×A								×/-/-	×/-/-								
		C	3S	Q	29823				×	×				×/-													
		C	3S	$\overline{Q}$	29824				×	×				×/-													
	10		3S	Q	821					●A					●A			×/-/-	×/-/-					●A			
			3S	$\overline{Q}$	822					×								×/-/-	×/-/-								
			3S	Q	1821					×																	
			3S	Q	29821				●	×				●/-													
			3S	$\overline{Q}$	29822				×	×				×/-													
	10X2		3S	Q	16820																				H●		
			3S	Q	162820																				H●		
	16		3S	Q	16374										●A	H●	H●	●	●	●	●			● ●A H●A	H●	●	● H●
			3S	$\overline{Q}$	16534														×								
			3S	Q	162374											H●									H●		
	18	C	3S	Q	16823										● H●			×	●						H●		
		C	3S	Q	162823										●A												
	20		3S	Q	16721												*								H●		
			3S	Q	16821										●		H●		×						H●		
			3S	Q	162721																				H●		
			3S	Q	162821																				×		
	22		3S	Q	16722																					●	
	32		3S	Q	32374											H●	H●							●A H●A	H●		● H●
			3S	Q	322374											H●											

Explanatory notes [Trigger] POS: Positive edge NEG: Negative Edge

[PRE · CLR] B: Preset and Clear C: Clear Only

[Output] 2S: Totem pole Output 3S: 3-State Output

[Q·$\overline{Q}$] B: $\overline{Q}$··Output Q: Q-Output $\overline{Q}$: $\overline{Q}$-Output

Status ●: Product available in technology indicated *: New product planned in technology indicated

×: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCxx / CD74HCTxx

BCT: SN74BCTxx / SN64BCTxx

AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

LATCH

Type	Curcuit	Output	PRE • CLR	Q • $\overline{Q}$	Device	Technology																							
						Bipolar						CMOS		BiCMOS				Advanced CMOS											
						TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LV-AT	LVC	ALVC	AVC	AUC
S-R	4	2S		Q	279	×	●A																						
AD	8	2S		Q	259	×	●B		●			●/●	-/●					×/-/-	×/-/-										
	8	2S		$\overline{Q}$	4724							×/-																	
BIS	4	2S		Q	75	×	●					×/●	×/●					×/-/-											
	4	2S		Q	77							×/-																	
	4	2S		Q	375		●					×/-																	
	8	2S		Q	100	×																							
R/B	8	3S		Q	990				●																				
	8	3S		$\overline{Q}$	991				×																				
	8	3S	B	Q	666				●																				
	8	3S	C	Q	996				●																				
	8	3S	B	$\overline{Q}$	667				●																				
	9	3S	C	Q	992				●																				
	9	3S	C	$\overline{Q}$	993				×																				
	10	3S		Q	994				●																				
	10	3S		$\overline{Q}$	995				×																				
D	8	2S	C	Q	116	×																							
	8	3S		Q	373		●	●	●A	●	●	●/●	●/●	●/-	●	H●		×/●/●	●/●/●	●	●	●A	●	●A	H●				
	8	3S		Q	2373						●																		
	8	3S		$\overline{Q}$	533				●A	●A	×	×/●	×/●	×/-	●A			×/●/-	×/●/-										
	8	3S		Q	573				●C	●A	●	●/●	●/●	●/-	●A	● H●		×/●/●	×/●/●	●	●	●A	●	●A					
	8	3S		$\overline{Q}$	563				●B		×	●/●	×/●	×/-				×/●/●	×/●/-										
	8	3S		$\overline{Q}$	580				●B	×																			
	8	3S	C	Q	873				●B	×A								×/-/-	×/-/-										
	8	3S	P	Q	880				×A	×																			
	8	3S	B	Q	845				×	×								×/-/-	×/-/-										
	8	3S	B	Q	29845				×	×				×/-															
	8	3S	B	$\overline{Q}$	846				×	×								×/-/-	×/-/-										
	8	3S	B	$\overline{Q}$	29846				×	×				×/-															
	9	3S	B	Q	843				●	×					●			×/-/-	×/-/-										
	9	3S	B	Q	1843																								
	9	3S	B	Q	29843				×	×				●/-															
	9	3S	B	$\overline{Q}$	844				×	×								×/-/-	×/-/-										
	9	3S	B	$\overline{Q}$	29844				×	×				×/-															
	10	3S		Q	841				●	×A					●A			×/-/-	×/-/-					●A					
	10	3S		Q	29841				×	×				×/-															
	10	3S		$\overline{Q}$	842				×	×								×/-/-	×/-/-										
	10	3S		$\overline{Q}$	29842					×				×/-															
	12/24	3S		Q	16260										H●										H●				
	12/24	3S		Q	162260										H●										H●				
	16	3S		Q	16373										●A	H●	H●	●	●	●	●	●		●A H●A	H●		●	●
	16	3S		$\overline{Q}$	16533														×										
	16	3S		Q	162373											H●									H●				
	18	3S	B	Q	16843										●				×						×				
	20	3S		Q	16841										●				●						H●				
	20	3S		Q	162841										●										H●				
	32	3S		Q	32373											H●	H●							● H●A		*	*

Explanatory notes [Type] S-R: S-R Latch AD: Addressable Latch BIS: Bistable Latch

[Type] R-B: Read-Back Latch D: D-Type Transparent Latch

[PRE・CLR] B: Preset and Clear C: Clear Only

[Output] 2S: Totem pole Output 3S: 3-State Output

[Q·$\overline{Q}$] B: $\overline{Q}$-Output Q: Q-Output $\overline{Q}$: $\overline{Q}$-Output

Status ●: Product available in technology indicated *: New product planned in technology indicated

×: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCxx / CD74HCTxx

SHIFT REGISTER

Input Type	Output Type	No. of Bit	CLR	Shift	Output	Device	Technology																				
							Bipolar						CMOS		BiCMOS				Advanced CMOS								
							TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	AUC
S/P	S/P	4		R	2S	178	×																				
			C	R	2S	179	×																				
				R	2S	195	×	×	×		×		×/●														
				B	2S	95	×	×			×																
				B	2S	295		×C																			
			C	R	3S	395		×A																			
			C	B	2S	194	×	●A	×		●		×/●	-/●					×/-/-	×/-/-							
		5	C	R	2S	96	×	×																			
			C	R	3S	322		×					×/-														
			C	B	2S	198	×																				
		8	C	B	3S	299		●	×	●	×	●	-/●	-/●	×/-				×/-/ ●	×/-/ ●							
			C	B	3S	323		×		●	×	×			×/-				×/-/ ●	×/-/-							
			C	B	2S	199	×																				
S/P	S	8		R	2S	165	×	●A		●			●/●	-/●									●A				
			C	R	2S	166	×	●A		●		×	●/●	-/●									●A				
S	S/P	8	C	R	2S	164	×	●		●A			●/●	-/●					-/-/ ●	-/-/ ●			●A				
S	P	10	C		2S	898													×/-/-	×/-/-							
S	S	8		R	2S	91	×	×																			
P	S	4	C	R	2S	94	×																				
		16		R	3S	674		●																			

SHIFT REGISTER WITH LATCH

Input Type	Output Type	No. of Bit	CLR	Shift	Output	Device	Technology																				
							Bipolar						CMOS		BiCMOS				Advanced CMOS								
							TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	AUC
S/P	S/P	4	C	B	3S	671		×																			
		4	C	B	3S	672		×																			
		8	C	R	2S	598		●																			
S	S/P	8	C	R	3S	595		●					●/-								●	●	●A				
		8	C	R	OC	599		×																			
		8	C	R	OC	596		●																			
		8	C	R	2S	594		●					●/-								●	●	●A				
		16	C	B	3S	673		●																			
S/P	S	8	C	R	2S	597		●					-/●	-/●													

Explanatory notes [Input/Output Type] S: Serial P: Parallel S/P: Alternative Serial/Parallel
[CLR] C: With Clear
[Shift] R: Right-Shift B: Alternative Shift Right/Left
[Output] 2S: Totem-Pole Output 3S: 3-State Output

Status ●: Product available in technology indicated *: New product planned in technology indicated
×: Discontinued ■: Not recommended for new designs
HC: SN74HCxx / CD74HCxx
HCT: SN74HCxx / CD74HCTxx
BCT: SN74BCTxx / SN64BCTxx
AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx
ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

REGISTER (ETC)

Descriotion	Device	Technology																					
		Bipolar						CMOS		BiCMOS				Advanced CMOS									
		TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	AUC
REGISTER FILES 8W x 2B	172	×																				
REGISTER FILES 4W x 4B	170	×	×																			
REGISTER FILES 4W x 4B	670		●					-/●	-/●													
REGISTER FILES 16W x 5B	870				●	×								×/-/-	×/-/-							
REGISTER FILES 16W x 5B	858													×/-/-	×/-/-							
REGISTER FILES 16W x 6B	871				×	×																
REGISTER FILES 32W x 4B	859													×/-/-	×/-/-							
MUX WITH STRAGE	298	×	●			●A		×/-														
MUX WITH STRAGE	398		×																			
4BIT BUS-BUFFER REGISTER	173	×	●A					×/●	-/●													
8BIT STORAGE REGISTER	396		×																			
8BIT DIAGNOTICCS/PIPELINE REGISTER	818													×/-/-	×/-/-							
	819													×/-/-	×/-/-							
	29818				×					×/-												

Status ●: Product available in technology indicated *: New product planned in technology indicated
×: Discontinued ■: Not recommended for new designs
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HCT: SN74HCxx / CD74HCTxx
BCT: SN74BCTxx / SN64BCTxx
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ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

MONOSTABLE MULTIVIBRATOR

Curcuit	CLR	Retrigger	Device	Technology																			
				Bipolar						CMOS		BiCMOS				Advanced CMOS							
				TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	AUC
1			121	●																			
	C	R	122	×	●																		
	C	R	422		×																		
2	C	R	123	●	●					-/●	-/●							●A	●A	●A			
	C		221	●	●					-/●	-/●									●A			
	C	R	423		●					-/●	-/●												
	C	R	4538							-/●	-/●												

Explanatory notes [CLR] C: With Clear
[Retrigger] R: With Retrigger

Status ●: Product available in technology indicated *: New product planned in technology indicated
×: Discontinued ■: Not recommended for new designs
HC: SN74HCxx / CD74HCxx
HCT: SN74HCxx / CD74HCTxx
BCT: SN74BCTxx / SN64BCTxx
AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx
ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

DECADE/BINARY COUNTER

DEC • BIN	ASYN • SYN	No. of Bit	UP/DOWN Mode	CLR	LOAD	ETC	Device	Technology																				
								Bipolar						CMOS		BiCMOS				Advanced CMOS								
								TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	AUC
DEC	A	4		A			68		×																			
					9		90	×	●																			
							290	×	×																			
				A		D	390	×	●					×/●	-/●													
				A	A		176	×																				
				A	A		196	×	×	×																		
				A	9	D	490	×	×					×/-														
							560				×																	
	S			S	S		162	×	×A	×	×B	×	×	×/-						×/-/-	×/-/-							
				A	S		160	×	×A		×B	×	×	×/-						×/-/-	×/-/-							
				A	S		690		×																			
				S	S		692		×																			
		4			S		568				×		×							×/-/-	×/-/-							
			Y		S		168			×	×	×	×							×/-/-	×/-/-							
					S		668		×																			
				A			190	×	×		×		×A	×/●						×/-/-	×/-/-							
				A	S		696		×																			
				S	S		698		×																			
				A	A		192	×	×		×			×/●						×/-/-	×/-/-							
		8		A		J	4017							×/●														
BIN	A	4		A			69		×																			
							93	×	●					-/●	-/●													
							293	×	●																			
				A		D	393	×	●					●/●	-/●										●A			
				A	A		177	×																				
				A	A		197	×	×	×																		
		7		A			4024							×/●	-/●													
		12		A			4040							●/●	-/●										●A			
		14		A			4020							●/●	-/●													
				A			4060							●/●	-/●													
				A			4061							×/-														
	S						561					●A																
				S	S		163	×	●A	●	●B	●	●A	●/●	-/●					×/-/●	×/-/●				●A			
				S	S		693		×																			
				A	S		161	×	●A		●B	●	●A	●/●	-/●					×/-/●	×/-/●				●A			
				A	S		691		×																			
						D	4518							-/●														
		4			S		669		●																			
			Y	S	S		699		×																			
					S		169		●B	×	●B	●A	●							×/-/-	×/-/-							
					A		191	×	●		●A			●/●	-/●					×/-/-	×/-/-							
				A	S		697		●																			
				A	A		193	×	●		●A		×A	●/●	-/●					×/-/-	×/-/-							
				A	A		569				●A		×							×/-/-	×/-/-							
	S			A	S		461													×/-/-	×/-/-							
				S	S		463													×/-/-	×/-/-							
				A	A	R	590		●					●A/-						×/-/-	×/-/-							
				A	A	R	591		×																			
				A	A	R	592		●											×/-/-	×/-/-							
				A	A	R	593		●											×/-/-	×/-/-							
		8		A		J	4022							×/-														
							4520							-/●	-/●													
				A		J	7022							×/-														
							40103							-/●	-/●													
			Y		S		469													×/-/-	×/-/-							
							579													×/-/-	×/-/-							
				S	S		869				●	●								×/-/-	×/-/-							
				A	S		867				●A	●								×/-/-	×/-/-							
OTH	A	1				12	92	×	●																			

Explanatory notes **[DEC·BIN] DEC: Decoder BIN: Binary Counter OHE: Other**
[ASYN·SYN] ASYN: Asynchronous SYN: Synchronous
[Up/Down] Y: Up/Down
[CLR] A: With Asynchronous Clear S: With Synchronous Clear
[LOAD] A: With Asynchronous Clear S: With Synchronous Clear 9: Preset 9
[ETC] D: 2-Curcuit R: With Series Register J: Johnson Counter 12: Devide By-Twelve Counter

Status **●: Product available in technology indicated *: New product planned in technology indicated**
×: Discontinued ■: Not recommended for new designs
HC: SN74HCxx / CD74HCxx
HCT: SN74HCxx / CD74HCTxx
BCT: SN74BCTxx / SN64BCTxx
AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx
ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

RATE MULTIPLIER/FREQUENCY DIVIDERS

Descriotion	Device	Technology																				
		Bipolar						CMOS		BiCMOS				Advanced CMOS								
		TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	AUC
FREQUENCY DIVIDERS	56		×																			
FREQUENCY DIVIDERS	57		×																			
6BIT BINARY RATE MULTIPLIER	97	●																				
DECADE RATE MULTILIER	167	×																				
PROGRAMABLE FREQUENCY DIVIDER/DIGITAL TIMERS	292		●																			
	294		●																			

Status ●: Product available in technology indicated *: New product planned in technology indicated
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BCT: SN74BCTxx / SN64BCTxx
AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx
ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

DATA SELECTOR/MULTIPLEXER

No. of Input/output	Output	Curcuit	ETC	Device	Technology																				
					Bipolar						CMOS		BiCMOS				Advanced CMOS								
					TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	AUC
16/1	2S	1		150	●												×/-/-	×/-/-							
	3S	1		250					●A								×/-/-	×/-/-							
	3S	1		850					×																
	3S	1		851					×																
	2S	1		4067							×/●	-/●													
8/1	2S	1		151	×A	●	●	●	●	●B	●/●	-/●					×/-/ ●	×/-/ ●							
	2S	1		152							×/-														
	3S	1		251	×	●	×	●	×	●B	●/●	-/●					×/-/ ●	×/-/ ×							
	3S	1		354		×					×/●	-/●													
	3S	1		356		×					×/-	-/●													
	3S	1		4051							-/●	-/●									●A				
	3S	1		4351							-/●	-/●													
	3S	1		4851							●/-														
	OC	1		355		×																			
	OC	1		357		×																			
4/1	2S	2		352		×		×	×	×	×/-						×/-/-	×/-/-							
	3S	2		153	×	●	×	●	●	●	●/●	-/●					×/-/ ●	×/-/ ●							
	3S	2		253		●		●	●A	●	●/●	-/●					×/-/ ●	×/-/ ●							
	3S	2		353		×		×	×	×	×/-						×/-/-	×/-/-							
	3S	2		4052							-/●	-/●									●A				
	3S	2		4352							-/●														
	3S	4		16460										H●								×			
	3S	4		162460										H●											
2/1	2S	1		157	×	●	●	●A	●	●A	●/●	●/●					×/-/ ●	×/-/ ●	●	●	●A	●A			
	2S	1		158		●	×	●	●	×A	●/●	-/●					×/-/ ●	×/-/ ●	●	●		-			
	2S	4	S	399		●																			
	3S	1		257		●B	●	●A	●	●	●/●	●/●					●/-/ ●	●/-/ ●				●A			
	3S	1		258		●B	×	●A	●	●	●/×	-/●					×/-/-	×/-/ ●				-			
	3S	4		4053							-/●	-/●									●A				
	3S	6	U	857				●	×																
	3S	8	S	604		×					×/-														
	OC	8	S	605		×																			
	3S	8	S	606		×																			
	OC	8	S	607		×																			
16	3S	16	AD	16254														×							

Explanatory notes [Output] 2S: Totem pole Output 3S: 3-State Output OC: Open-Collector Output
[ETC] S: Storage Register

Status ●: Product available in technology indicated *: New product planned in technology indicated
×: Discontinued ■: Not recommended for new designs
HC: SN74HCxx / CD74HCxx
HCT: SN74HCxx / CD74HCTxx
BCT: SN74BCTxx / SN64BCTxx

DECODER / DEMULTIPLEXER

No. of Input/output	Output	Curcuit	ETC	Device	Technology																						
					Bipolar						CMOS		BiCMOS				Advanced CMOS										
					TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LV-AT	LVC	ALVC	AVC	AUC
4/16	2S	1	AD	4514							×/●	×/●														
	2S	1	AD	4515							×/●	-/●														
	3S	1		154	●						×/●	-/●					×/-/-	×/-/-								
	OC	1		159	●																					
4/10	2S	1	BD	42	×A	●					●/●	-/●														
	2S	1	BD	43	×																					
	2S	1	BD	44	×																					
3/8	2S	1		238							×/●	-/●					×/-/ ●	×/-/ ●								
	2S	1		138		●	●A	●A	●	●	●/●	●/●					●/-/ ●	×/-/ ●	●	●	●A		●A			
	2S	1	AD	237							×/●	-/●														
	2S	1	AD	137		×		●A	×		×/●	-/●											*			
	2S	1	AD	131				×	×																	
2/4	2S	2		139		●A	●A	●	×	×	●/●	●/●					×/-/ ●	●/-/ ●	●	●	●A		●A			
	2S	2		239							×/-/-						×/-/-	×/-/-								
	2S	2		155	×	●A																				
	OC	2		156	×	●		●																		

Explanatory notes [Output] 2S: Totem pole Output 3S: 3-State Output OC: Open-Collector Output
[ETC] AD: Adress Latch BD: BCD TO DECIMAL

Status ●: Product available in technology indicated *: New product planned in technology indicated
×: Discontinued ■: Not recommended for new designs
HC: SN74HCxx / CD74HCxx
HCT: SN74HCxx / CD74HCTxx
BCT: SN74BCTxx / SN64BCTxx
AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx
ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

CODE CONVERTER / PRIORITY ENCODER / REGISTER

Descriotion	Device	Technology																								
		Bipolar						CMOS		BiCMOS				Advanced CMOS												
		TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LV-AT	LVC	ALVC	AVC	AUC			
CODE CONVERTER	184	×																								
CODE CONVERTER	185	×																								
10-4 PRIORITY ENCODER	147	×	×					-/●	-/●																	
8-3 PRIORITY ENCODER	148	×	●				×	●/-																		
8-3 PRIORITY ENCODER	348		●									×														
4BIT CASCADABLE PRIORITY REGISTER	278	×																								

Status ●: Product available in technology indicated *: New product planned in technology indicated
×: Discontinued ■: Not recommended for new designs
HC: SN74HCxx / CD74HCxx
HCT: SN74HCxx / CD74HCTxx
BCT: SN74BCTxx / SN64BCTxx
AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx
ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

Display Decoder / Driver

Function	V_{OH} (V)	Device	Technology																						
			Bipolar						CMOS		BiCMOS				Advanced CMOS										
			TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	AUC
D	30	45	●																				
D	60	141	×																				
D	15	145	●	●																			
D	7	445		×																			
7	30	46	×																				
7	15	47	●A	●																			
7	5.5	48	×	×																			
7	5.5	49		×																			
7	30	246	×																				
7	15	247	×	●																			
7	7	347																					
7	7	447																					
7	5.5	248		×																			
7	5.5	249		×																			
B	7	142	×																				
B	7	143	×																				
B	7	144	×																				

Explanatory notes [Function] D: BCD TO DECIMAL, 7: BCD TO 7-SEGMENT, B: COUNTER/LATCH/DECODER/DRIVER
[VOH] Off-Stage Output Voltage (V)

Status ●: Product available in technology indicated *: New product planned in technology indicated
×: Discontinued ■: Not recommended for new designs
HC: SN74HCxx / CD74HCxx
HCT: SN74HCxx / CD74HCTxx
BCT: SN74BCTxx / SN64BCTxx
AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx
ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

COMPARATOR

No. of Bit	Input	P=Q	$\overline{P=Q}$	P>Q	P<Q	Output	Device	Technology																			
								Bipolar						CMOS		BiCMOS				Advanced CMOS							
								TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	AUC
4	S	Y	N	Y	Y	2S	85	×	●	●		×		×A/●	-/●												
6	S	N	Y	N	N	2S	29806				×																
8	20	Y	N	N	N	OC	518				●		×														
8	20	N	Y	N	N	2S	520				●		×							×/-/-	×/-/-						
8	20	N	Y	N	N	OC	522				×																
8	20	N	Y	Y	N	2S	682		●					●/-													
8	20	N	Y	Y	N	OC	683		×																		
8	S	Y	N	N	N	OC	519				×		×														
8	S	N	Y	N	N	2S	521				●		●							×/-/-	×/-/-						
8	S	N	Y	Y	N	2S	684		●					●/-													
8	S	N	Y	Y	N	OC	685		×																		
8	S	N	Y	Y	N	2S	686		×																		
8	S	N	Y	Y	N	OC	687		×																		
8	S	N	Y	N	N	2S	688		●		●			●/●	-/●												
8	S	N	Y	N	N	OC	689		×		×																
8	S	Y	N	Y	Y	2S	860													×/-/-	×/-/-						
8	S	N	N	Y	Y	2S	865													×/-/-	×/-/-						
8	LP	N	N	Y	Y	2S	885					●								×/-/-	×/-/-						
8	LPQ	Y	N	Y	Y	OC	866					×A															
9	-	N	Y	N	N	2S	29809				×																

Explanatory notes [Input] S: Standard 20: 20-kW Pullup Resistors LP: P-Port Latch LPQ: L,P-port Latch
[P=Q, $\overline{P=Q}$, P>Q, P<Q] Y: Yes N: No
[Output] 2S: Totem Pole Output, OC: Open-Collector Output

Status ●: Product available in technology indicated *: New product planned in technology indicated
×: Discontinued ■: Not recommended for new designs
HC: SN74HCxx / CD74HCxx
HCT: SN74HCxx / CD74HCTxx
BCT: SN74BCTxx / SN64BCTxx

ADRESS COMPARATOR / FUSE-PROGRAMMABLE IDENTITY COMPARATOR

Descriotion	No. of Bit	ETC	Device	Technology																										
				Bipolar							CMOS		BiCMOS				Advanced CMOS													
				TTL	LS	S	ALS	AS	F		HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	AUC					
A	16-4	OE	677				×A				×/-						×/-/-	×/-/-												
A	16-4	L	678				×				×/-						×/-/-	×/-/-												
A	12-4	OE	679				●				×/-																			
A	12-4	L	680				×				×/-																			
F	16		526				×																							
F	12		528				×																							
F	8		527				×																							

Explanatory notes [Function] A: Adress Comparator F: Fuse-Programmable Identity Comparators
[ETC] OE: Output-With Enable L: Output-With Latch

Status ●: Product available in technology indicated *: New product planned in technology indicated
×: Discontinued ■: Not recommended for new designs
HC: SN74HCxx / CD74HCxx
HCT: SN74HCxx / CD74HCTxx
BCT: SN74BCTxx / SN64BCTxx
AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx
ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

PARITY GENERATOR / CHECKER

No. of Bit	Device	Technology																												
		Bipolar							CMOS		BiCMOS				Advanced CMOS															
		TTL	LS	S	ALS	AS	F		HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	AUC							
8	180	×							×/-																					
9	280		●	●	●	●	●B		×/●	-/●					×/-/●	×/-/●														
9	286					●	×								×/-/-	●/-/-														

Status ●: Product available in technology indicated *: New product planned in technology indicated
×: Discontinued ■: Not recommended for new designs
HC: SN74HCxx / CD74HCxx
HCT: SN74HCxx / CD74HCTxx
BCT: SN74BCTxx / SN64BCTxx
AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx
ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

VOLTAGE CONTROLLED OSCILLATOR (VCO)

Curcuit	Fmax (MHz)	COMP'L Z OUT	ENABLE	RANGE INPUT	Rext	PLL	Device	Technology																								
								Bipolar							CMOS		BiCMOS				Advanced CMOS												
								TTL	LS	S	ALS	AS	F		HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	AUC				
1	20	Y	Y	Y			624		●																							
	20	Y	Y	Y	Y		628		●																							
	24				Y	Y	7046								-/●A	-/●A																
2	20						627		×																							
	20		Y	Y			629		●																							
	20	Y					625		×																							
	20	Y	Y				626		×																							
	60		Y	Y			124			●																						
	24				Y	Y	4046								-/●A	-/●A																

Status ●: Product available in technology indicated *: New product planned in technology indicated
×: Discontinued ■: Not recommended for new designs
HC: SN74HCxx / CD74HCxx
HCT: SN74HCxx / CD74HCTxx
BCT: SN74BCTxx / SN64BCTxx
AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx
ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

ACCUMULATORS / ARITHMETIC LOGIC UNIT (ALU) / LOOK-AHEAD CARRY GENERATOR

Descriotion	Device	Technology																						
		Bipolar						CMOS		BiCMOS				Advanced CMOS										
		TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	AUC
4BIT PARALLEL BINARY ACCUMULATORS	281			×																		
4BIT PARALLEL BINARY ACCUMULATORS	681		×																			
4BIT ALU/FUNCTION GENERATORS	181	×	●	×		●A								×/-/-	×/-/-							
4BIT ALU/FUNCTION GENERATORS	381		×	×			×															
4BIT ALU/FUNCTION GENERATORS	881					×A								×/-/-	×/-/-							
4BIT ALU WITH RIPPLE CARRY	382		×				×															
LOOK AHEAD CARRY GENERATORS	264					×																
LOOK AHEAD CARRY GENERATORS	182	×		×		×																
LOOK AHEAD CARRY GENERATORS	282					×																
LOOK AHEAD CARRY GENERATORS	882					×A								×/-/-	×/-/-							
QUAD SERIAL ADDER/SUBTRACTOR	385		×																			

Status ●: Product available in technology indicated *: New product planned in technology indicated
×: Discontinued ■: Not recommended for new designs
HC: SN74HCxx / CD74HCxx
HCT: SN74HCxx / CD74HCTxx
BCT: SN74BCTxx / SN64BCTxx
AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx
ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

ADDER

Descriotion	Device	Technology																						
		Bipolar						CMOS		BiCMOS				Advanced CMOS										
		TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	AUC
4BIT BINARY FULL ADDER	83	×	×																			
4BIT BINARY FULL ADDER	283	×	●	●			●	-/●	-/●					-/-/●	-/-/●							
DUAL CARRY SAVE FULL ADDER	183		×																			
GATED FULL ADDER	80	×																				
2BIT BINARY FULL ADDER	82	×																				

Status ●: Product available in technology indicated *: New product planned in technology indicated
×: Discontinued ■: Not recommended for new designs
HC: SN74HCxx / CD74HCxx
HCT: SN74HCxx / CD74HCTxx
BCT: SN74BCTxx / SN64BCTxx
AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx
ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

MULTIPLIER

Descriotion	Device	Technology																						
		Bipolar						CMOS		BiCMOS				Advanced CMOS										
		TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	AUC
2-4 PARALLEL BINARY MULTIPLIERS	261		×																			
4-4 PARALLEL BINARY MULTIPLIERS	284	×																				
4-4 PARALLEL BINARY MULTIPLIERS	285	×																				
2'S COMPLEMENT MULTIPLIERS	384		×																			

Status ●: Product available in technology indicated *: New product planned in technology indicated
×: Discontinued ■: Not recommended for new designs
HC: SN74HCxx / CD74HCxx
HCT: SN74HCxx / CD74HCTxx
BCT: SN74BCTxx / SN64BCTxx
AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx
ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

MEMORY

Descriotion	Device	Technology																				
		Bipolar						CMOS		BiCMOS				Advanced CMOS								
		TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	AUC
MEMORY REFRESH CONTROLLERS	600		×																			
MEMORY REFRESH CONTROLLERS	601		×																			
MEMORY REFRESH CONTROLLERS	603		×																			
MEMORY CYCLE CONTROLLER	608		×																			
MEMMORY MAPPERS	612		×																			
MEMMORY MAPPERS	613		×																			
MEMMORY MAPPERS WITH LATCH	610		×																			
MEMMORY MAPPERS WITH LATCH	611		×																			
MULTI-MODE LATCH	412			×																		
3-8 MEMORY DECIDER	2414									●/-												

Status ●: Product available in technology indicated *: New product planned in technology indicated
×: Discontinued ■: Not recommended for new designs
HC: SN74HCxx / CD74HCxx
HCT: SN74HCxx / CD74HCTxx
BCT: SN74BCTxx / SN64BCTxx
AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx
ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

CLOCK GENERATOR CIRCUIT

Descriotion	Device	Technology																				
		Bipolar						CMOS		BiCMOS				Advanced CMOS								
		TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	AUC
QUAD COMPLEMENTARY-OUTPUT LOGIC	265	×																				
DUAL PULSE SYNCHRONIZERS/DRIVERS	120	×																				
CRYSTAL-CONTOROLLED OSCILLATORS	320		×																			
CRYSTAL-CONTOROLLED OSCILLATORS	321		×																			
DIGITAL PHASE-LOCK LOOP	297		●					-/●	-/●						-/-/●							

Status ●: Product available in technology indicated *: New product planned in technology indicated
×: Discontinued ■: Not recommended for new designs
HC: SN74HCxx / CD74HCxx
HCT: SN74HCxx / CD74HCTxx
BCT: SN74BCTxx / SN64BCTxx
AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx
ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

SWITCH, SHIFTER, ERROR DETECTION CORRECTION CIRCUIT, HARD DISK DRIVER

Descriotion	Device	Technology																				
		Bipolar						CMOS		BiCMOS				Advanced CMOS								
		TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	AUC
QUAD BILATERAL SWITCHES	4016							-/●														
	4066							●/●	-/●							●		●A				
ANALOG SWITCHES WITH LEVEL TRANSLATION	4316							-/●	-/●													
4BIT SHIFTERS	350			×			×															
8BIT PARALLEL ERROR DETECTION CORRECTION CIRCUIT	636		×																			
	637		×																			
16BIT PARALLEL ERROR DETECTION CORRECTION CIRCUIT	616				×																	
	617																					
	630		×																			
	631		×																			
32BIT PARALLEL ERROR DETECTION CORRECTION CIRCUIT	632				×	×																
	633				×																	
	634				×	×																
	635				×																	
HARD DISK DRIVER	1250				×																	

Status ●: Product available in technology indicated *: New product planned in technology indicated
×: Discontinued ■: Not recommended for new designs
HC: SN74HCxx / CD74HCxx
HCT: SN74HCxx / CD74HCTxx
BCT: SN74BCTxx / SN64BCTxx
AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx
ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

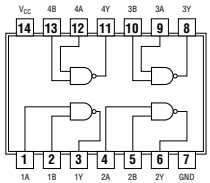
PIN ASSIGNMENTS

Standard

00
QUADRUPLE 2-INPUT POSITIVE-NAND GATES

positive logic:

$Y = \overline{A \cdot B}$

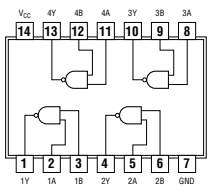


See page 231

01
QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

positive logic:

$Y = \overline{A \cdot B}$

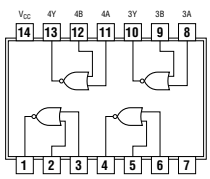


See page 232

02
QUADRUPLE 2-INPUT POSITIVE-NOR GATES

positive logic:

$Y = \overline{A + B}$

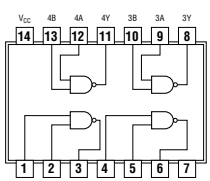


See page 233

03
QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

positive logic:

$Y = \overline{A \cdot B}$

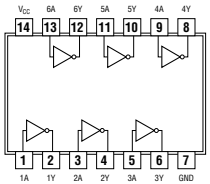


See page 234

04
HEX INVERTERS

positive logic:

$Y = \overline{A}$

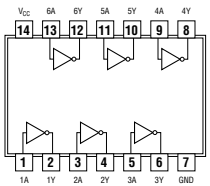


See page 235

U04
HEX INVERTERS

positive logic:

$Y = \overline{\overline{A}}$

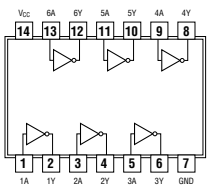


See page 236

05
HEX INVERTERS WITH OPEN-DRAIN OUTPUTS

positive logic:

$Y = \overline{A}$

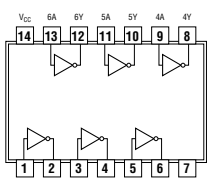


See page 236

06
HEX INVERTER BUFFERS/DRIVERS WITH OPEN-DRAIN OUTPUTS

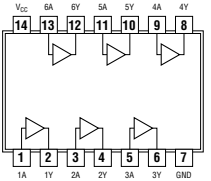
positive logic:

$Y = \overline{A}$



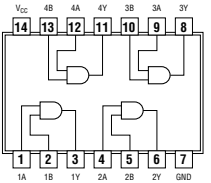
See page 237

07
HEX BUFFERS/DRIVERS WITH OPEN-DRAIN OUTPUTS
positive logic:
$Y = \overline{A}$



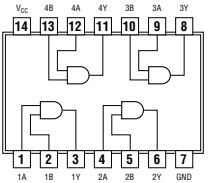
See page 237

08
QUADRUPLE 2-INPUT POSITIVE-AND GATES
positive logic:
$Y = A \bullet B$



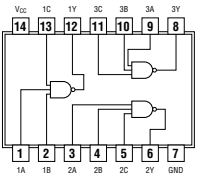
See page 238

09
QUADRUPLE 2-INPUT POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS
positive logic:
$Y = A \bullet B$



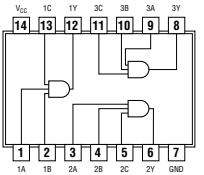
See page 239

10
TRIPLE 3-INPUT POSITIVE-NAND GATES
positive logic:
$Y = \overline{A \bullet B \bullet C}$



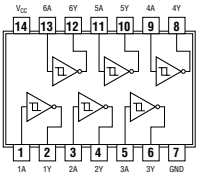
See page 240

11
TRIPLE 3-INPUT POSITIVE-AND GATES
positive logic:
$Y = A \bullet B \bullet C$



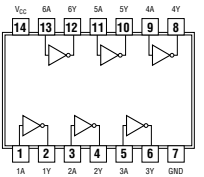
See page 241

14
HEX SCHMITT-TRIGGER INVERTERS
positive logic:
$Y = \overline{A}$



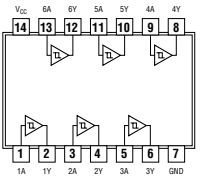
See page 242

16
HEX INVERTER BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS
positive logic:
$Y = \overline{A}$



See page 243

17
HEX SCHMITT-TRIGGER BUFFER
positive logic:
$Y = A$

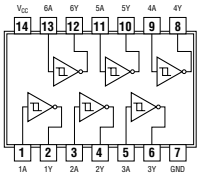


See page 243

19
HEX SCHMITT-TRIGGER INVERTERS

positive logic:

$Y = \overline{A}$

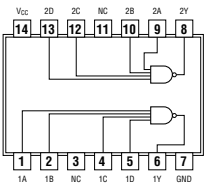


See page 244

20
DUAL 4-INPUT POSITIVE-NAND GATES

positive logic:

$Y = \overline{A \bullet B \bullet C \bullet D}$



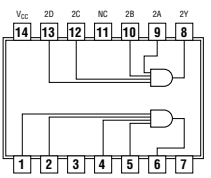
NC-No internal connection

See page 245

21
DUAL 4-INPUT POSITIVE-AND GATES

positive logic:

$Y = A \bullet B \bullet C \bullet D$



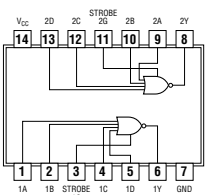
NC-No internal connection

See page 246

25
DUAL 4-INPUT POSITIVE-NOR GATES WITH STROBE

positive logic:

$Y = G\,\overline{(A + B + C + D)}$

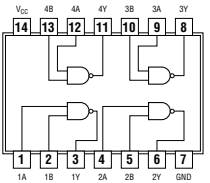


See page 246

26
QUADRUPLE 2-INPUT HIGH-VOLTAGE INTERFACE POSITIVE-NAND GATES

positive logic:

$Y = \overline{AB}$

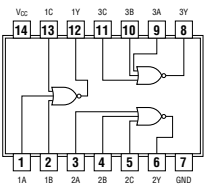


See page 247

27
TRIPLE 3-INPUT POSITIVE-NOR GATES

positive logic:

$Y = \overline{A + B + C}$

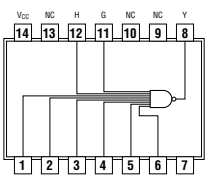


See page 247

30
8-INPUT POSITIVE-NAND GATES

positive logic:

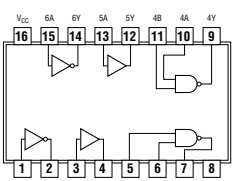
$Y = \overline{A \bullet B \bullet C \bullet D \bullet E \bullet F \bullet G \bullet H}$



NC-No internal connection

See page 248

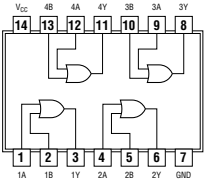
31
DELAY ELEMENTS



See page 248

32
QUADRUPLE 2-INPUT POSITIVE-OR GATES

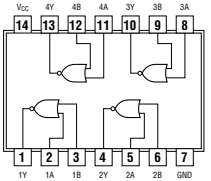
positive logic:
$Y = A + B$



See page 249

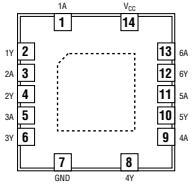
33
QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS WITH OPEN-COLLECTOR OUTPUTS

positive logic:
$Y = \overline{A + B}$



See page 250

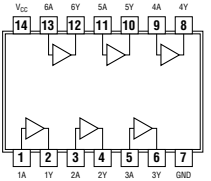
34
HEX BUFFER GATE



See page 250

35
HEX NONINVERTERS WITH OPEN-COLLECTOR OUTPUTS

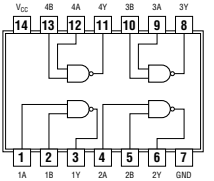
positive logic:
$Y = A$



See page 251

37
QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS

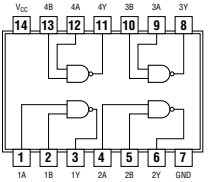
positive logic:
$Y = \overline{A \cdot B}$



See page 252

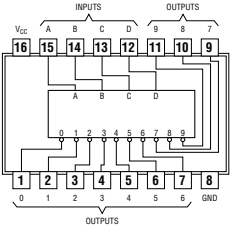
38
QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS WITH OPEN-COLLECTOR OUTPUTS

positive logic:
$Y = \overline{A \cdot B}$



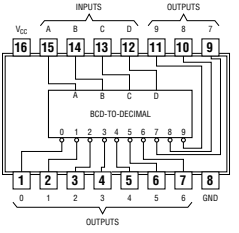
See page 253

42
4-LINE-TO-10-LINE DECODERS (1 of 10)



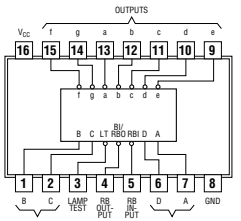
See page 254

45
BCD-TO-DECIMAL DECODERS/DRIVERS



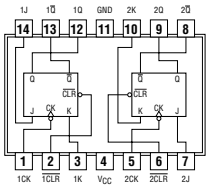
See page 256

47
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS



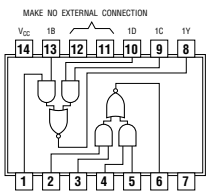
See page 258

73
DUAL J-K FLIP-FLOPS WITH CLEAR

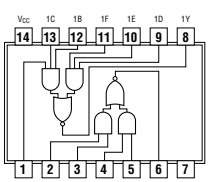


See page 262

51
AND-OR-INVERT GATES
`51, `S51 DUAL 2-WIDE 2-INPUT
positive logic:
$Y = \overline{AB + CD}$

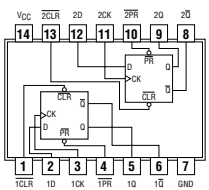


AND-OR-INVERT GATES
`LS51 2-WIDE 3-INPUT, 2-WIDE 2-INPUT
positive logic:
1Y = (1A 1B 1C) + (1D 1E 1F)
2Y = (2A 2B) + (2C 2D)



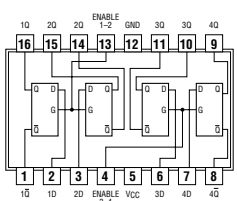
See page 260

74
DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET



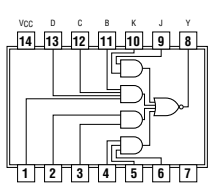
See page 264

75
4-BIT BISTABLE LATCHES



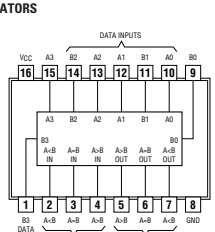
See page 266

64
4-2-3-2 INPUT AND-OR INVERT GATES
positive logic:
$Y = \overline{ABCD + EF + GHI + JK}$



See page 261

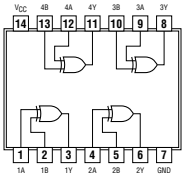
85
4-BIT MAGNITUDE COMPARATORS



See page 267

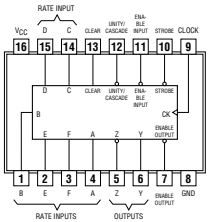
86
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

positive logic:
$Y = A = B$ or $Y = \overline{A}B + A\overline{B}$



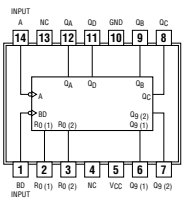
See page 268

97
SYNCHRONOUS 6-BIT BINARY RATE MULTIPLIERS



See page 272

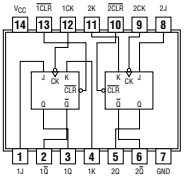
90
DECADE COUNTER



NC-No internal connection

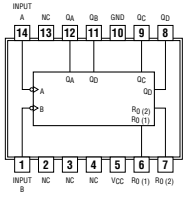
See page 269

107
DUAL J-K FLIP-FLOPS WITH CLEAR



See page 274

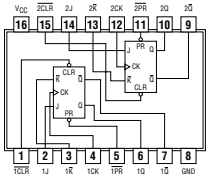
92
DIVIDE-BY-TWELVE DECODE COUNTERS



NC-No internal connection

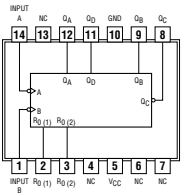
See page 270

109
DUAL J-$\overline{K}$ POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET



See page 276

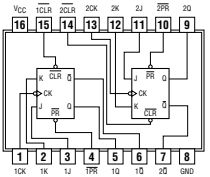
93
4-BIT BINARY COUNTERS



NC-No internal connection

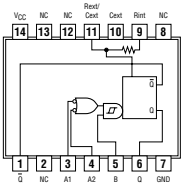
See page 271

112
DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET



See page 278

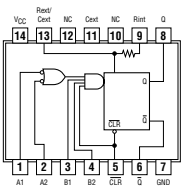
121
MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS



NC-No internal connection

See page 280

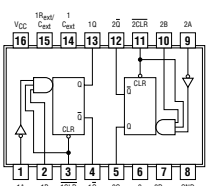
122
RETRIGGERABLE MONOSTABLE MULTIVIBRATORS



NC-No internal connection

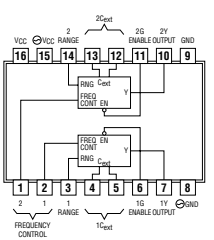
See page 281

123
DUAL RETRIGGERABLE MONOSTABLE MULTIVIBARATORS WITH SCHMITT-TRIGGER INPUTS



See page 282

124
DUAL VOLTAGE-CONTROLLED OSCILLATORS

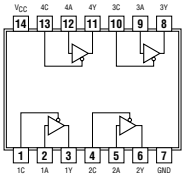


See page 283

125
QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

positive logic:

$Y = A$

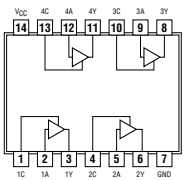


See page 284

126
QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

positive logic:

$Y = A$

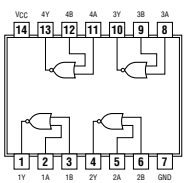


See page 285

128
SN54128...75-Ω LINE DRIVER
SN74128...50-Ω LINE DRIVER

positive logic:

$Y = \overline{A + B}$

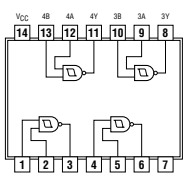


See page 286

132
QUADRUPLE POSITIVE-NAND GATES WITH SCHMITT TRIGGER INPUTS

positive logic:

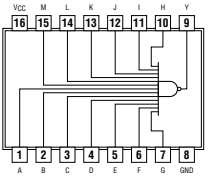
$Y = \overline{A \cdot B}$



See page 286

133
13-INPUT POSITIVE-NAND GATES

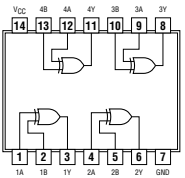
positive logic:
$Y = \overline{A \bullet B \bullet C \bullet D \bullet E \bullet F \bullet G \bullet H \bullet I \bullet J \bullet K \bullet L \bullet M}$



See page 287

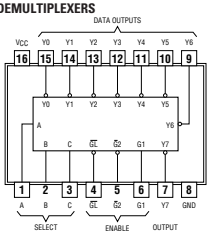
136
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES WITH OPEN COLLECTOR OUTPUTS

positive logic:
$Y = A \bullet \overline{B} = \overline{A}B + A\overline{B}$



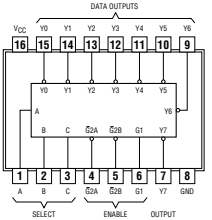
See page 287

137
3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS WITH ADDRESS LATCHES



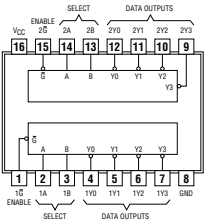
See page 288

138
3-LINE TO 8-LINE DECODERS/DEMULTIPLEXRS



See page 290

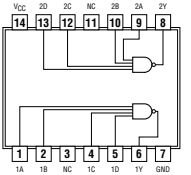
139
DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS



See page 292

140
DUAL 4-INPUT POSITIVE-NAND 50-Ω LINE DRIVERS

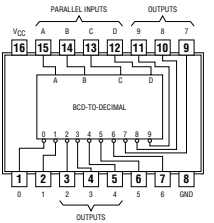
positive logic:
$Y = \overline{ABCD}$



NC-No internal connection

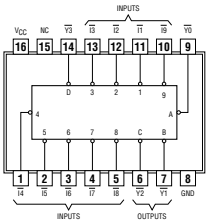
See page 294

145
BCD-TO-DECIMAL DECODERS/DRIVERS



See page 295

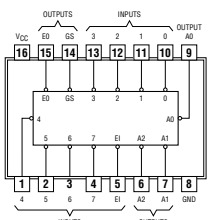
147
10-LINE TO 4-LINE BCD PRIORITY ENCODER



NC-No internal connection

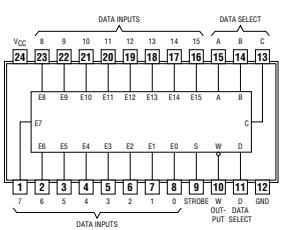
See page 296

148
8-LINE TO 3-LINE PRIORITY ENCODERS



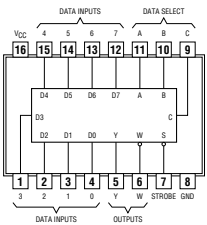
See page 298

150
16-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER



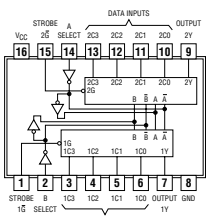
See page 300

151
8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS



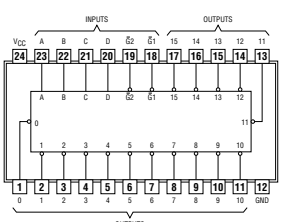
See page 302

153
DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS



See page 304

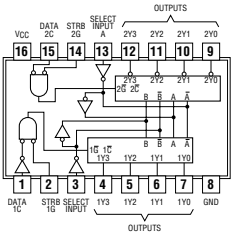
154
4-LINE TO 16-LINE DECODERS/DEMULTIPLEXERS



See page 306

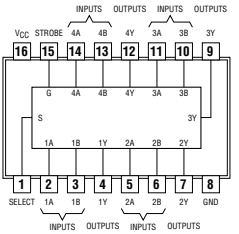
155
DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

156
DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS WITH OPEN-COLLECTOR OUTPUTS



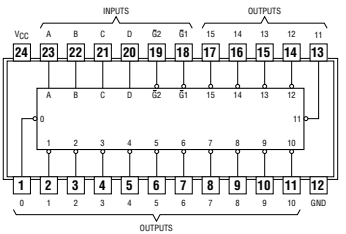
See page 308, 310

157
158
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS



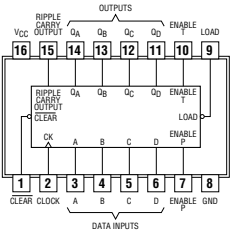
See page 312, 314

159
4-LINE TO 16-LINE DECODERS/DEMULTIPLEXERS WITH OPEN-COLLECTOR OUTPUTS



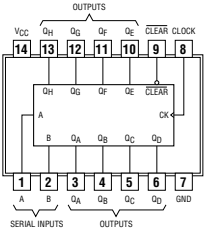
See page 316

161
163
4-BIT SYNCHRONOUS BINARY COUNTERS



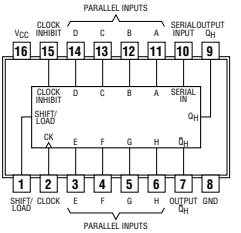
See page 318, 320

164
8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS



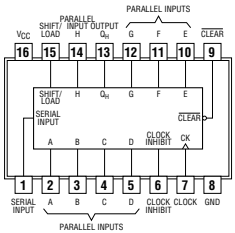
See page 322

165
PARALLEL-LOAD 8-BIT SHIFT REGISTERS



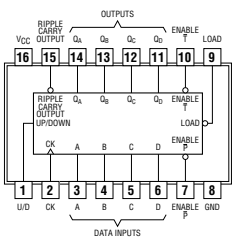
See page 324

166
8-BIT PARALLEL-LOAD SHIFT REGISTERS



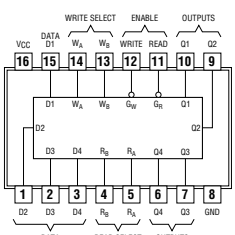
See page 326

169
SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS



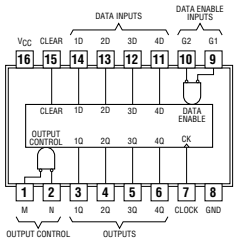
See page 328

170
4-BY-4-REGISTER FILES WITH OPEN-COLLECTOR OUTPUTS



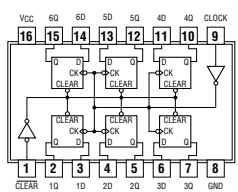
See page 330

173
4-BIT D-TYPE REGISTERS WITH 3-STATE OUTPUTS



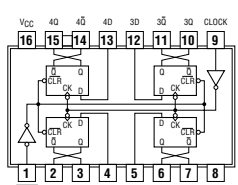
See page 332

174
HEX D-TYPE FLIP-FLOPS WITH CLEAR



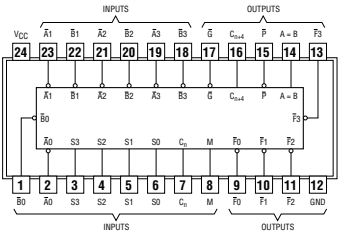
See page 334

175
QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR



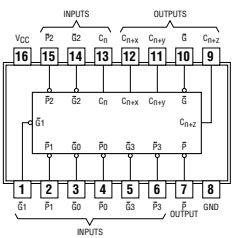
See page 335

181
ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS



See page 336

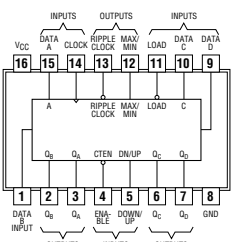
182
LOOK-AHEAD CARRY GENERATOR



See page 338

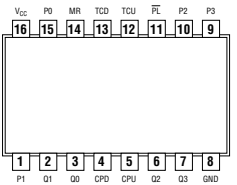
190
SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS

191
4-BIT SYNCHRONOUS UP/DOWN BINARY COUNTERS



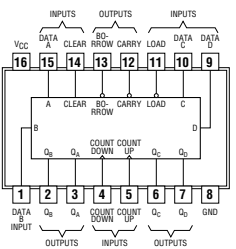
See page 340, 342

192
PRESETTABLE SYNCHRONOUS 4-BIT UP/DOWN COUNTERS



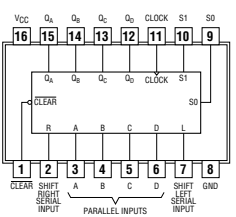
See page 344

193
4-BIT SYNCHRONOUS UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)



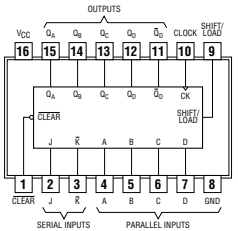
See page 346

194
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS



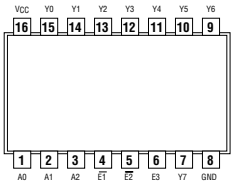
See page 348

195
4-BIT PARALLEL-ACCESS SHIFT REGISTERS



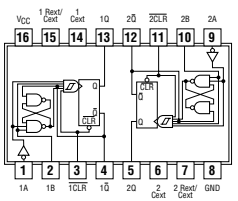
See page 350

238
3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS



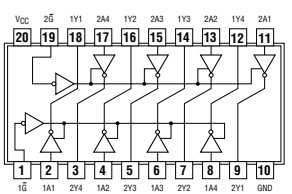
See page 356

221
DUAL MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS



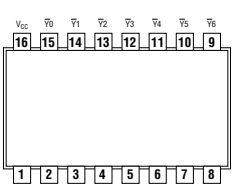
See page 352

240
OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS



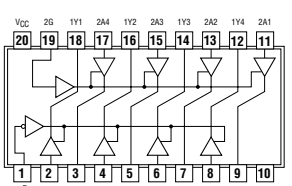
See page 358

237
3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS WITH ADDRESS LATCHES



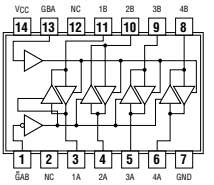
See page 354

241
OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS



See page 360

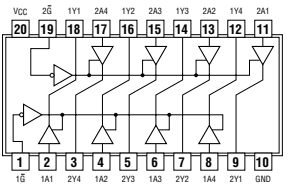
243
QUADRUPLE BUS TRANSCEIVERS WITH 3-STATE OUTPUTS



NC-No internal connection

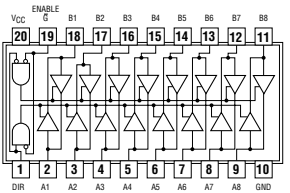
See page 362

244
OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS



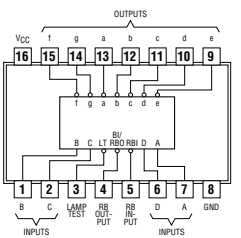
See page 364

245
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS



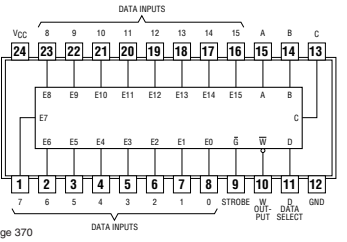
See page 366

247
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS



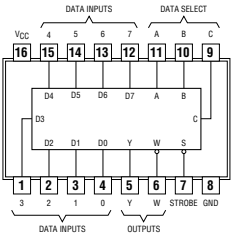
See page 368

250
1-OF-16 DATA GENERATORS/MULTIPLEXERS WITH 3-STATE OUTPUTS



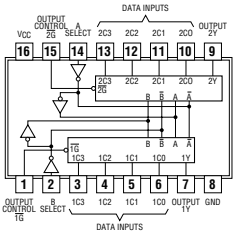
See page 370

251
DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS



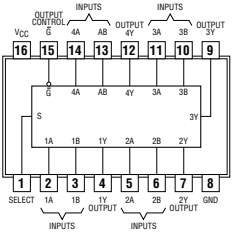
See page 372

253
DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS



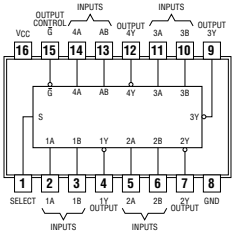
See page 374

257
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS



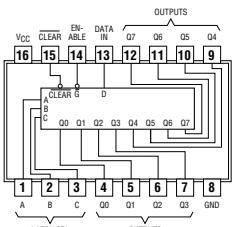
See page 376

258
QUADRUPLE 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS



See page 378

259
8-BIT ADDRESSABLE LATCHES

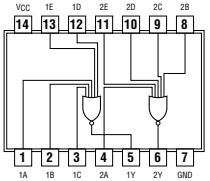


See page 380

260
DUAL 5-INPUT POSITIVE-NOR GATES

positive logic:

$Y = A + B + C + D + E$



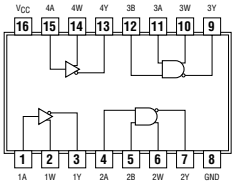
See page 382

265
QUADRUPLE COMPLEMENTARY-OUTPUT ELEMENTS

positive logic:

$Y = \overline{A}$, $W = A$

$Y = AB$, $W = \overline{AB}$

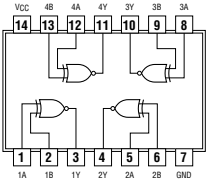


See page 382

266
QUADRUPLE 2-INPUT EXCLUSIVE-NOR GATES WITH OPEN-DRAIN OUTPUTS

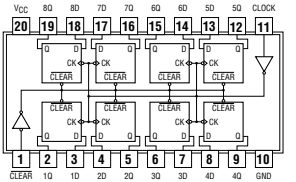
positive logic:

$Y = \overline{A = B}$



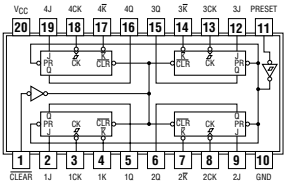
See page 383

273
OCTAL D-TYPE FLIP-FLOPS WITH CLEAR



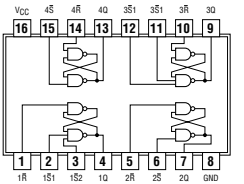
See page 384

276
QUADRUPLE J-$\overline{K}$ FLIP-FLORS



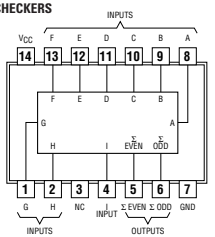
See page 386

279
QUADRUPLE $\overline{S}$-$\overline{R}$ LATCHES



See page 387

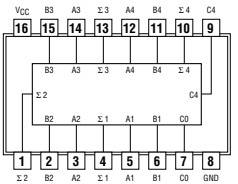
280
9-BIT PARITY GENERATORS/CHECKERS



NC-No internal connection

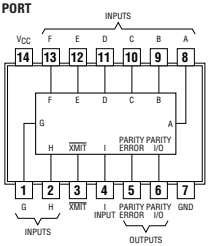
See page 388

283
4-BIT BINARY FULL ADDERS WITH FAST CARRY



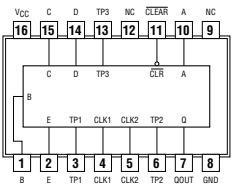
See page 390

286
9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS WITH BUS DRIVER PARITY I/O PORT



See page 392

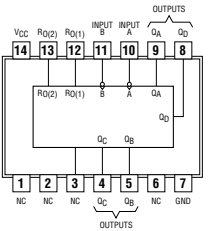
292
PROGRAMMABLE FREQUENCY DIVIDERS/DIGITAL TIMERS



NC-No internal connection

See page 394

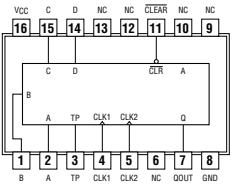
293
4-BIT BINARY COUNTERS



NC-No internal connection

See page 396

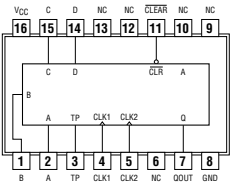
294
PROGRAMMABLE FREQUENCY DIVIDERS/DIGITAL TIMERS



NC-No internal connection

See page 398

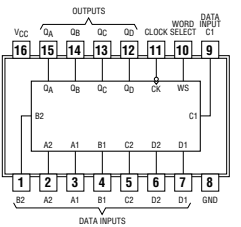
297
DIGITAL PHASE-LOCKED-LOOP FILTERS



NC-No internal connection

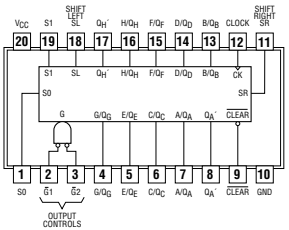
See page 400

298
QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE



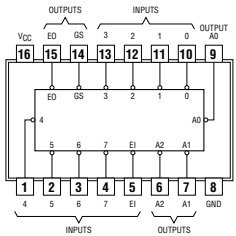
See page 402

299
8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS



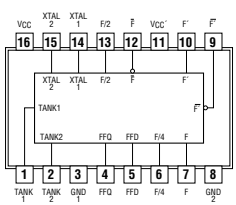
See page 404

348
8-LINE TO 3-LINE PRIORITY ENCODERS WITH 3-STATE OUTPUTS



See page 410

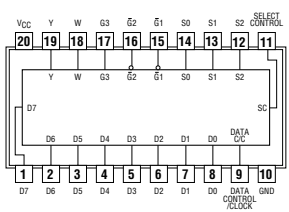
321
CRYSTAL-CONTROLLED OSCILLATORS



See page 406

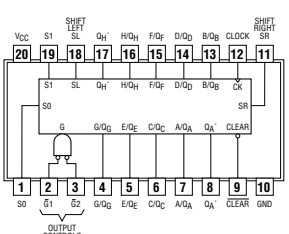
354
8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS/TRANSPARENT/ REGISTERS WITH 3-STATE OUTPUTS

356
8-INPUT MULTIPLEXER/REGISTERS 3-STATE



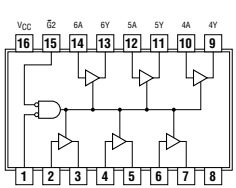
See page 412, 414

323
8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH SYNCHRONOUS CLEAR AND 3-STATE OUTPUTS



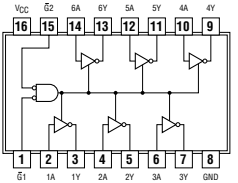
See page 408

365
HEX BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS



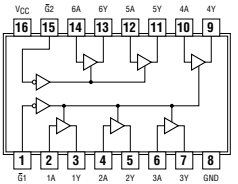
See page 416

366
HEX BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS



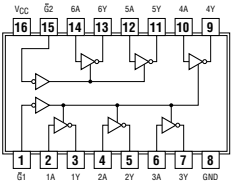
See page 417

367
HEX BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS



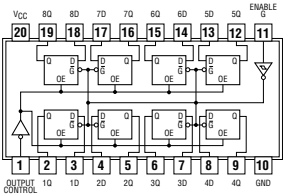
See page 418

368
HEX INVERTING BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS



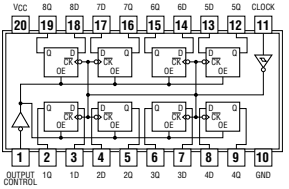
See page 419

373
OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS



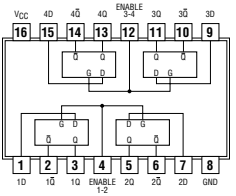
See page 420

374
OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS



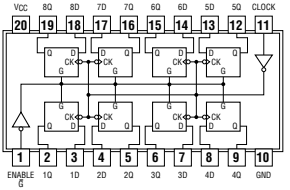
See page 422

375
4-BIT BISTABLE LATCHES



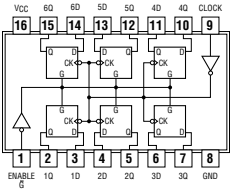
See page 424

377
OCTAL D-TYPE FLIP-FLOPS WITH CLOCK ENABLE



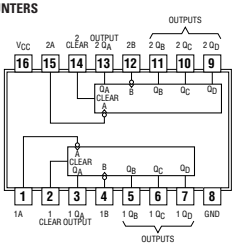
See page 425

378
HEX D-TYPE FLIP-FLOPS WITH CLOCK ENABLE



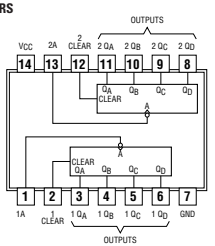
See page 426

390
DUAL 4-BIT DECADE COUNTERS



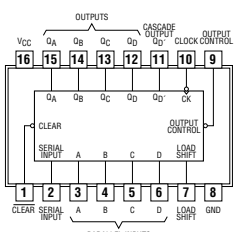
See page 427

393
DUAL 4-BIT BINARY COUNTERS



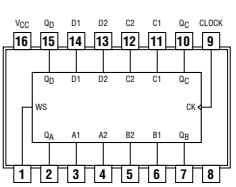
See page 428

395
CASCADABLE SHIFT REGISTERS



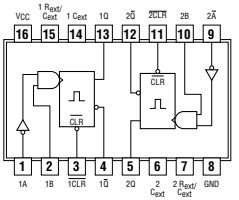
See page 429

399
QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE



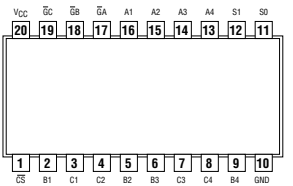
See page 430

423
RETRIGGERABLE MONOSTABLE MULTIVIBRATORS
positive logic:
Y = A



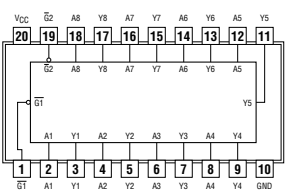
See page 431

442
QUADRUPLE TRIDIRECTIONAL BUS TRANSCEIVERS



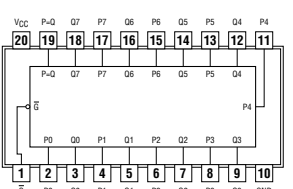
See page 432

465
OCTAL BUFFERS WITH 3-STATE OUTPUTS



See page 433

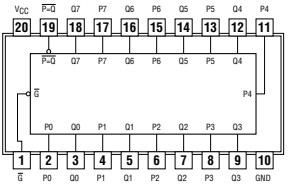
518
OCTAL BINARY/BCD IDENTITY COMPARATORS WITH ENABLE



See page 433

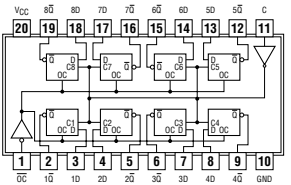
520
OCTAL BINARY/BCD IDENTITY COMPARATORS WITH ENABLE

521
8-BIT IDENTITY COMPARATORS WITH OPEN-COLLECTOR OUTPUTS



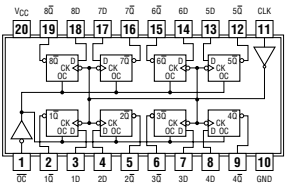
See page 434, 435

533
OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS



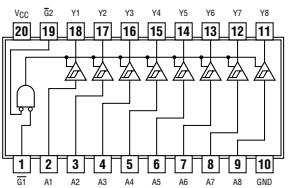
See page 436

534
OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS



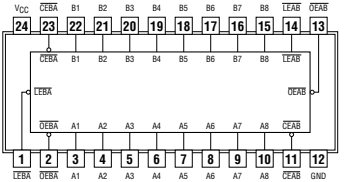
See page 437

540
541
OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS



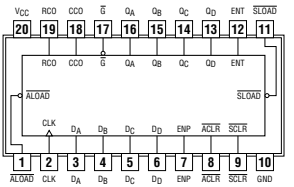
See page 438, 439

543
OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS



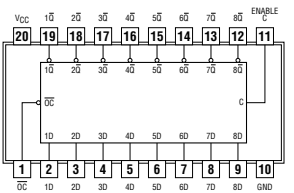
See page 440

561
SYNCHRONOUS 4-BIT COUNTERS WITH 3-STATE OUTPUTS



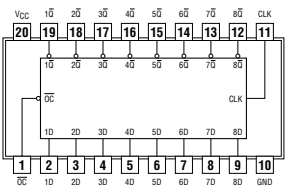
See page 442

563
OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS



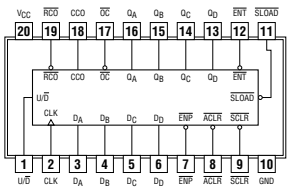
See page 444

564
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS



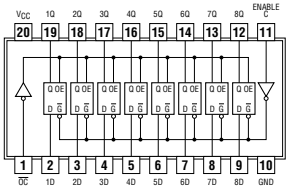
See page 445

569
SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS WITH 3-STATE OUTPUTS



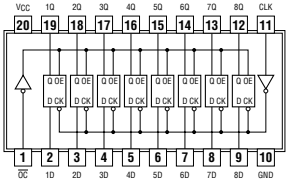
See page 446

573
OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS



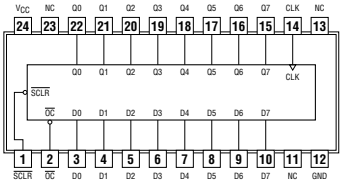
See page 448

574
OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS



See page 450

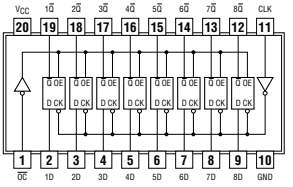
575
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS



NC-No internal connection

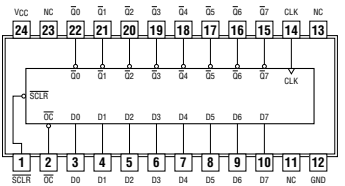
See page 452

576
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS



See page 453

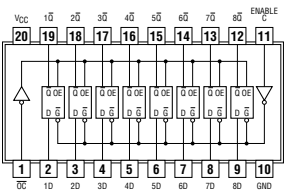
577
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS



NC-No internal connection

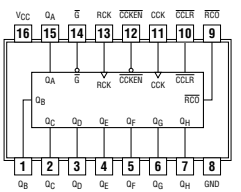
See page 454

580
OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS



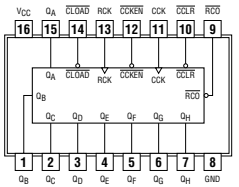
See page 455

590
8-BIT BINARY COUNTERS WITH 3-STATE OUTPUT REGISTERS



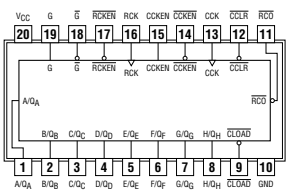
See page 456

592
8-BIT BINARY COUNTERS WITH INPUT REGISTERS



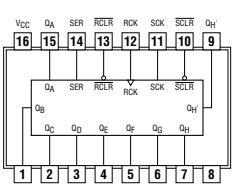
See page 458

593
8-BIT BINARY COUNTERS WITH INPUT REGISTERS



See page 460

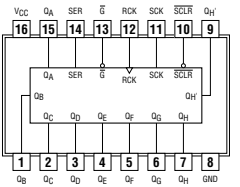
594
8-BIT SHIFT REGISTERS WITH OUTPUT REGISTERS



See page 462

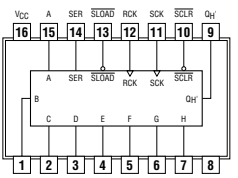
595
8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUT REGISTERS

596
8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES



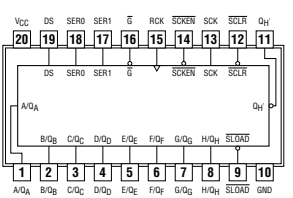
See page 464, 466

597
SERIAL-OUT SHIFT REGISTERS WITH INPUT LATCHES



See page 468

598
8-BIT SHIFT REGISTERS WITH INPUT LATCHES

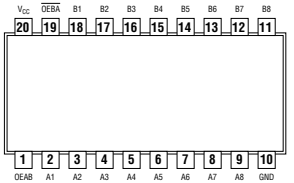


See page 470

620
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

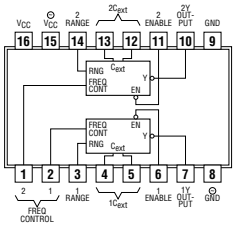
621
OCTAL BUS TRANSCEIVERS

623
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS



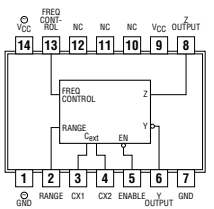
See page 472, 473, 474

629
DUAL VOLTAGE-CONTROLLED OSCILLATORS



See page 477

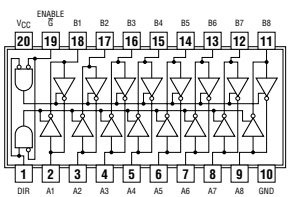
624
VOLTAGE-CONTROLLED OSCILLATORS



NC-No internal connection

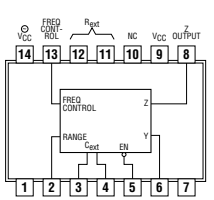
See page 475

638
OCTAL BUS TRANSCEIVERS



See page 478

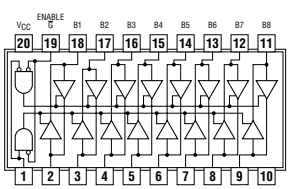
628
VOLTAGE-CONTROLLED OSCILLATORS



NC-No internal connection

See page 476

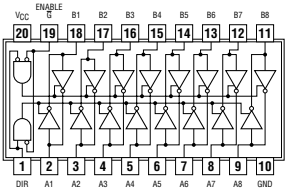
639
OCTAL BUS TRANSCEIVERS



See page 479

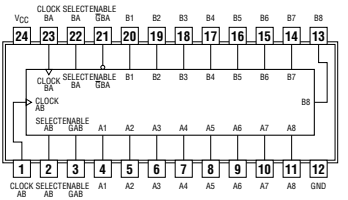
640
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

642
OCTAL BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS



See page 480, 482

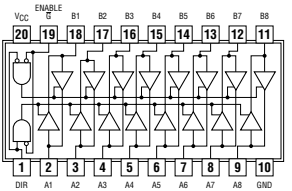
651
652
653
654
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS



See page 490, 492, 494, 496

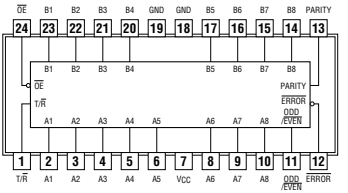
641
OCTAL BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

645
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS



See page 481, 483

657
OCTAL BUS TRANSCEIVERS WITH PARITY GENERATORS/CHECKERS AND 3-STATE OUTPUTS

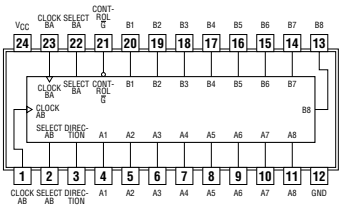


See page 498

646
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

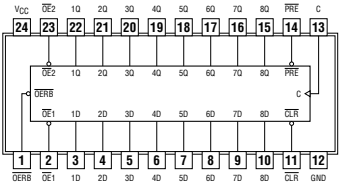
647
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH OPEN-COLLECTOR OUTPUTS

648
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS



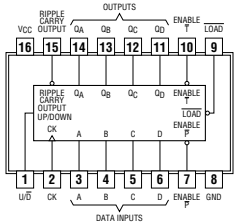
See page 484, 486, 488

666
667
8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES WITH 3-STATE OUTPUTS



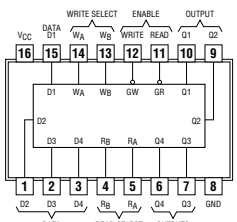
See page 500, 501

669
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS



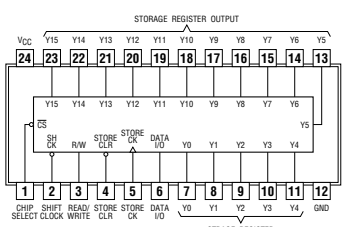
See page 502

670
4-BY-4 REGISTER FILES WITH 3-STATE OUTPUTS



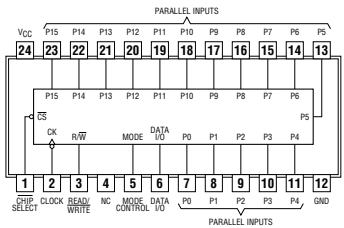
See page 504

673
16-BIT SHIFT REGISTERS



See page 506

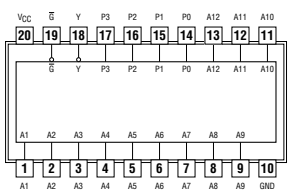
674
16-BIT SHIFT REGISTERS



NC-No internal connection

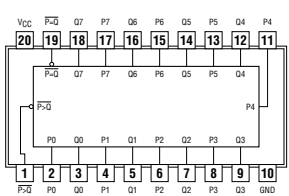
See page 508

679
12-BIT ADDRESS COMPARATOR



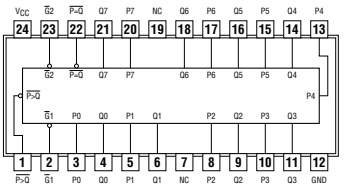
See page 510

682
684
8-BIT MAGNITUDE COMPARATORS



See page 512, 514

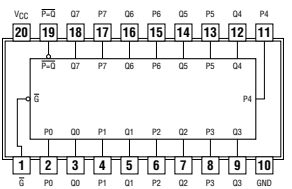
686
8-BIT MAGNITUDE/IDENTITY COMPARATORS



NC-No internal connection

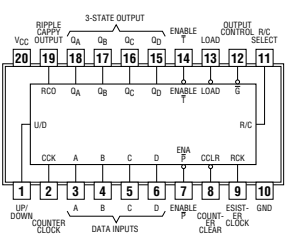
See page 516

688
8-BIT IDENTITY COMPARATORS



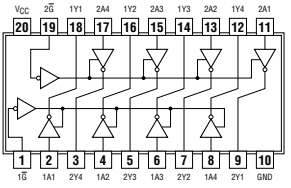
See page 518

697
699
SYNCHRONOUS UP/DOWN COUNTERS WITH OUTPUT REGISTERS AND MULTIPLEXED 3-STATE OUTPUTS



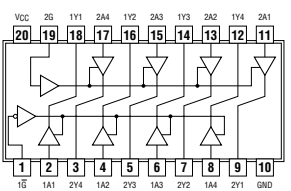
See page 520, 522

756
OCTAL BUFFER/DRIVER WITH OPEN-COLLECTOR OUTPUTS



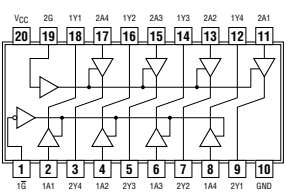
See page 524

757
OCTAL BUFFER/DRIVER WITH OPEN-COLLECTOR OUTPUTS



See page 525

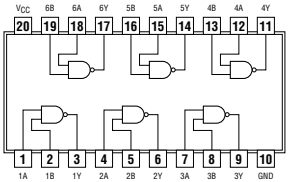
760
OCTAL BUFFERS/DRIVERS WITH OPEN-COLLECTOR OUTPUTS



See page 526

804
HEX 2-INPUT NAND DRIVERS

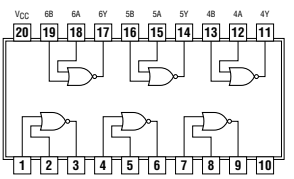
positive logic:
$Y = \overline{A \cdot B}$



See page 527

805
HEX 2-INPUT NOR DRIVERS

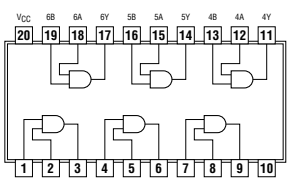
positive logic:
$Y = \overline{A + B}$



See page 528

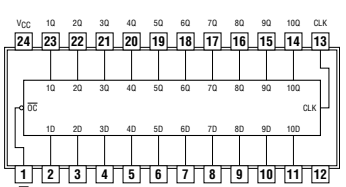
808
HEX 2-INPUT AND DRIVERS

positive logic:
$Y = A + B$



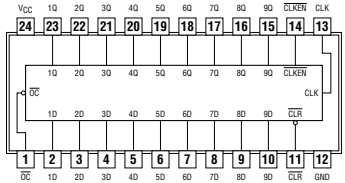
See page 528

821
10-BIT BUS-INTERFACE FLIP FLOPS WITH 3-STATE OUTPUTS



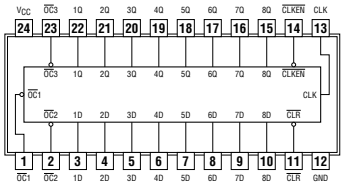
See page 529

823
9-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS



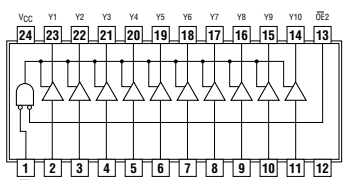
See page 530

825
8-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS



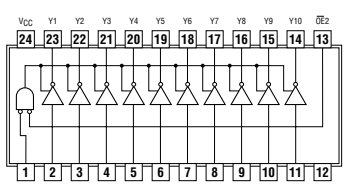
See page 531

827
10-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS



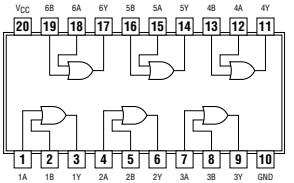
See page 532

828
10-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS



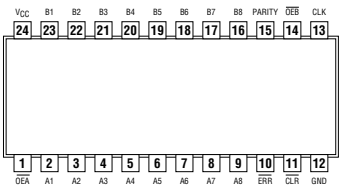
See page 532

832
HEX 2-INPUT OR DRIVERS
positive logic:
Y = A + B



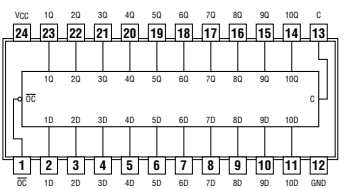
See page 533

833
8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS



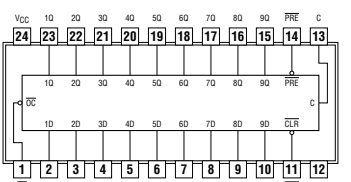
See page 534

841
10-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS



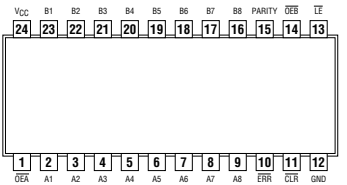
See page 536

843
9-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS



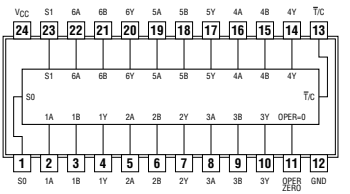
See page 537

853
8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS



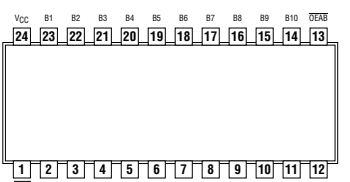
See page 538

857
HEX 2-TO-1 UNIVERSAL MULTIPLEXERS WITH 3-STATE OUTPUTS



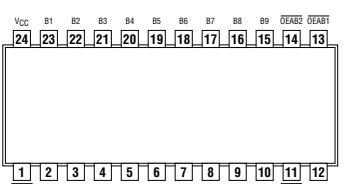
See page 540

861
10-BIT TRANSCEIVERS WITH 3-STATE OUTPUTS



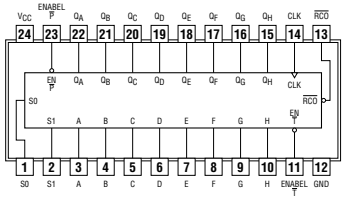
See page 542

863
9-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS



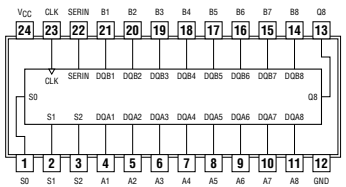
See page 543

867
869
SYNCHRONOUS 8-BIT UP/DOWN COUNTERS



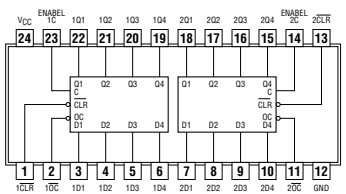
See page 544, 546

870
DUAL 16-BY 4-BIT REGISTER FILES



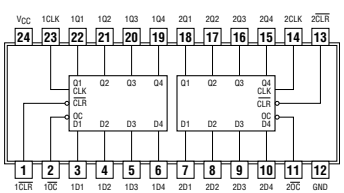
See page 548

873
DUAL 4-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS



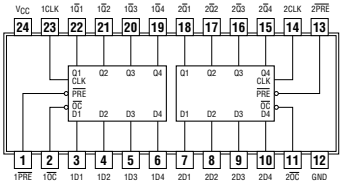
See page 550

874
DUAL 4-BIT D-TYPE EDGE-TRIGGERD FLIP-FLOPS WITH 3-STATE OUTPUTS



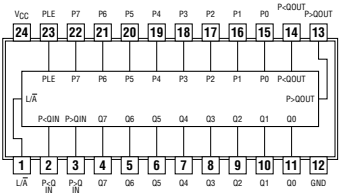
See page 551

876
DUAL 4-BIT D-TYPE EDGE-TRIGGERD FLIP-FLOPS WITH 3-STATE OUTPUTS



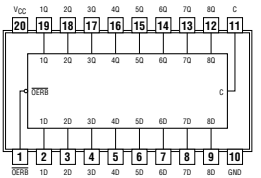
See page 552

885
8-BIT MAGNITUDE COMPARATORS



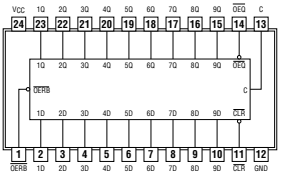
See page 554

990
8-BIT D-TYPE TRANSPARENT READ-BACK LATCH



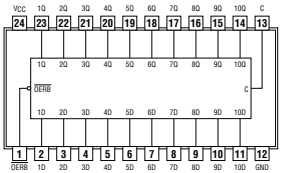
See page 556

992
9-BIT D-TYPE TRANSPARENT READ-BACK LATCH WITH 3-STATE OUTPUTS



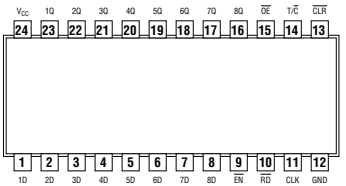
See page 557

994
10-BIT D-TYPE TRANSPARENT READ-BACK LATCH



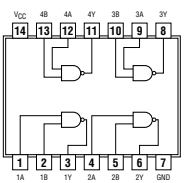
See page 558

996
8-BIT D-TYPE EDGE-TRIGGERED READ-BACK LATCHES



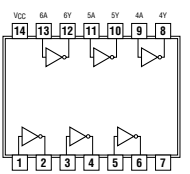
See page 559

1000
QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS/DRIVERS



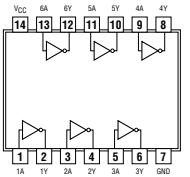
See page 560

1004
HEX INVERTING DRIVERS



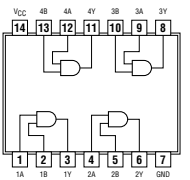
See page 560

1005
HEX INVERTING BUFFERS WITH OPEN-COLLECTOR OUTPUTS



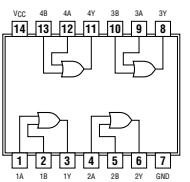
See page 561

1008
QUADRUPLE 2-INPUT POSITIVE-AND BUFFER/DRIVER



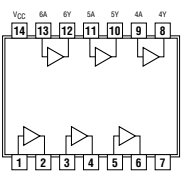
See page 561

1032
QUADRUPLE 2-INPUT POSITIVE-OR BUFFERS/DRIVERS
positive logic:
Y = A + B



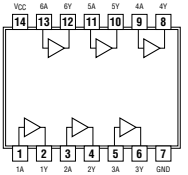
See page 562

1034
HEX DRIVERS



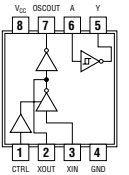
See page 562

1035
HEX NONINVERTING BUFFERS WITH OPEN-COLLECTOR OUTPUTS



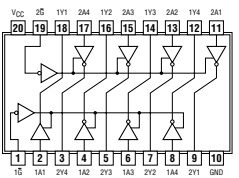
See page 563

1404
OSCILLATOR DRIVER FOR CRYSTAL OSCILLATOR OR CERAMIC RESONATOR



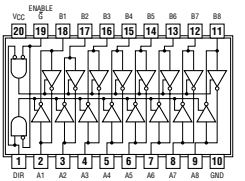
See page 565

1240
OCTAL BUFFER AND LINE DRIVER WITH 3-STATE OUTPUTS



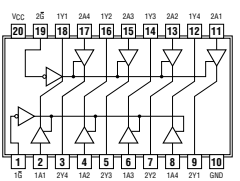
See page 563

1640
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS



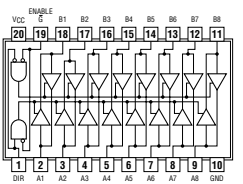
See page 566

1244
OCTAL BUFFERS AND DRIVERS WITH 3-STATE OUTPUTS



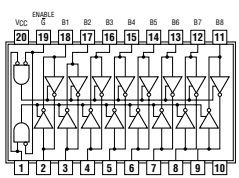
See page 564

1645
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS



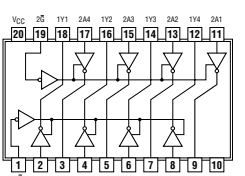
See page 567

1245
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS



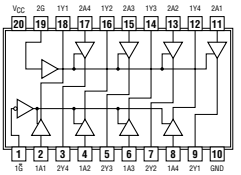
See page 564

2240
OCTAL BUFFERS AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS



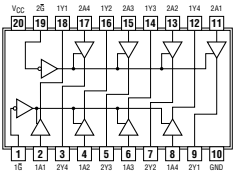
See page 568

2241
OCTAL BUFFERS AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS



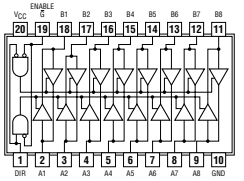
See page 569

2244
OCTAL BUFFERS AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS



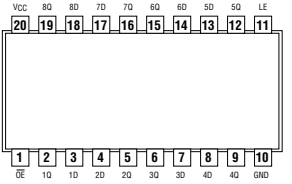
See page 570

2245
OCTAL TRANSCEIVER AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS



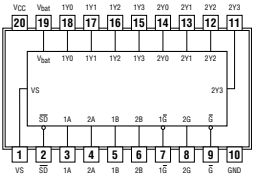
See page 571

2373
25-Ω OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS



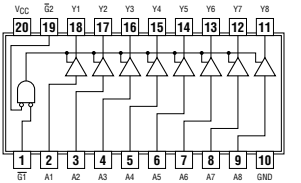
See page 572

2414
MEMORY DECODER WITH ON-CHIP SUPPLY VOLTAGE MONITOR



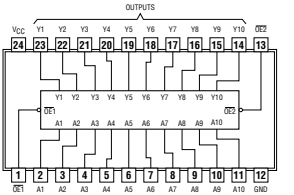
See page 573

2541
OCTAL LINE DRIVER/MOS DRIVER WITH 3-STATE OUTPUTS



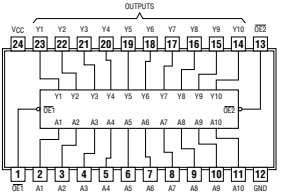
See page 574

2827
10-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS



See page 574

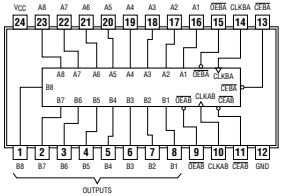
2828
10-BIT BUS/MOS MEMORY DRIVERS WITH 3-STATE INVERTING



See page 575

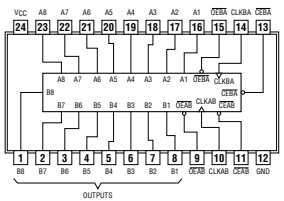
Pin Assignments

2952
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS



See page 576

2953
OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

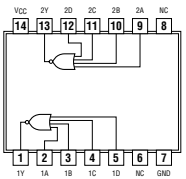


See page 578

4002
DUAL 4-INPUT POSITIVE-NOR GATES

positive logic:

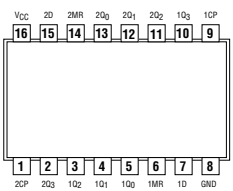
$Y = \overline{A + B + C + D}$



NC-No internal connection

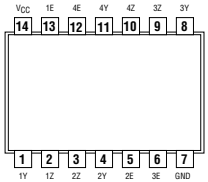
See page 579

4015
DUAL 4-STAGE STATIC SHIFT REGISTER



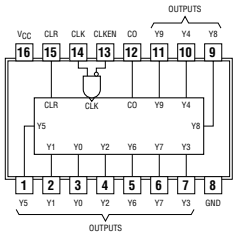
See page 580

4016
QUAD BILATERAL SWITCH



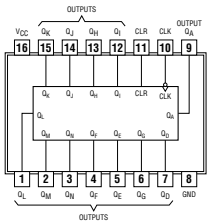
See page 581

4017
DECADE COUNTERS/DIVIDER



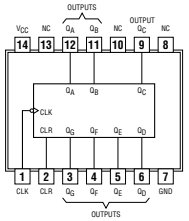
See page 582

4020
14-STAGE BINARY COUNTERS



See page 583

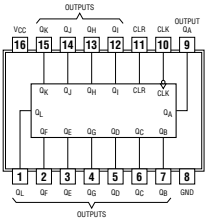
4024
7-STAGE BINARY COUNTERS



NC-No internal connection

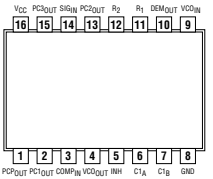
See page 584

4040
12-STAGE BINARY COUNTERS



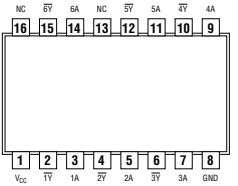
See page 585

4046
PHASE-LOCKED-LOOP WITH VCO



See page 586

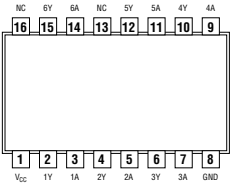
4049
HEX INVERTING BUFFERS



NC-No internal connection

See page 588

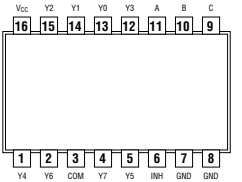
4050
HEX NON-INVERTING BUFFERS



NC-No internal connection

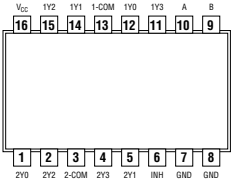
See page 588

4051
8-CHANNEL ANALOG MULTIPLEXERS/DEMULTIPLEXERS



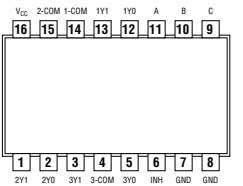
See page 589

4052
DUAL 4-CHANNEL ANALOG MULTIPLEXERS/DEMULTIPLEXERS



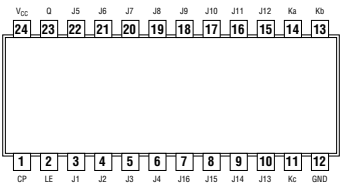
See page 590

4053
TRIPLE 2-CHANNEL ANALOG MULTIPLEXERS/DEMULTIPLEXERS



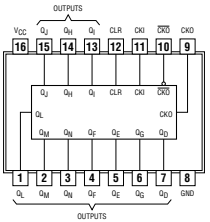
See page 591

4059
CMOS PROGRAMMABLE DIVIDE-BY-N COUNTER



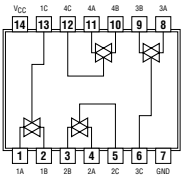
See page 592

4060
ASYNCHRONOUS 14-STAGE BINARY COUNTERS AND OSCILLATORS



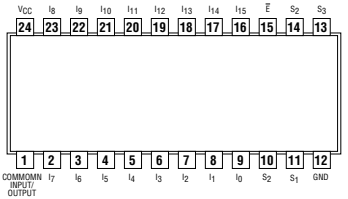
See page 593

4066
QUADRUPLE BILATERAL SWITCHES



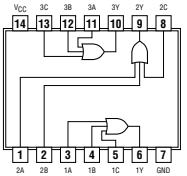
See page 594

4067
16-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER



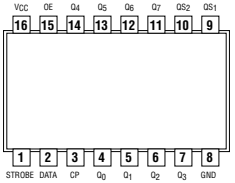
See page 595

4075
TRIPLE 3-INPUT OR GATES
positive logic:
Y = A + B + C



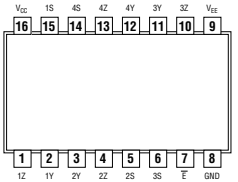
See page 596

4094
8-STAGE SHIFT AND STORE BUS REGISTER, THREE-STATE



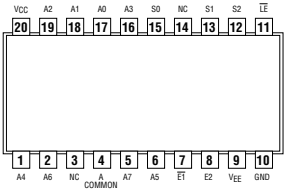
See page 597

4316
QUAD ANALOG SWITCH WITH LEVEL TRANSLATION



See page 598

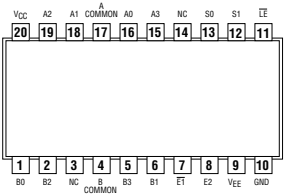
4351
ANALOG MULTIPLEXERS/DEMULTIPLEXERS WITH LATCH



NC-No internal connection

See page 599

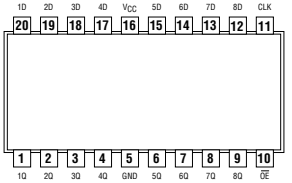
4352
ANALOG MULTIPLEXERS/DEMULTIPLEXERS WITH LATCH



NC-No internal connection

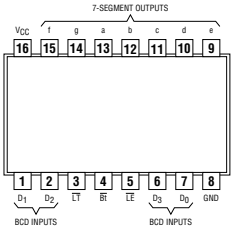
See page 600

4374
OCTAL EDGE-TRIGGERED D-TYPE DUAL-RANK FLIP-FLOP WITH 3-STAE OUTPUTS



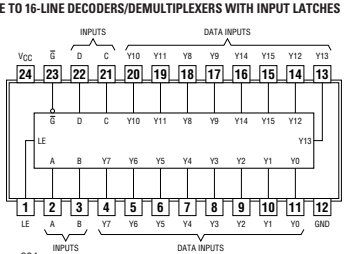
See page 601

4511
BCD-TO-7 SEGMENT LATCH/DECODER/DRIVERS



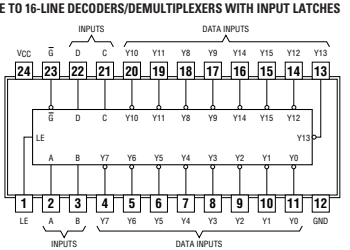
See page 602

4514
4-LINE TO 16-LINE DECODERS/DEMULTIPLEXERS WITH INPUT LATCHES



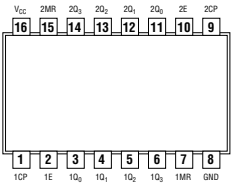
See page 604

4515
4-LINE TO 16-LINE DECODERS/DEMULTIPLEXERS WITH INPUT LATCHES



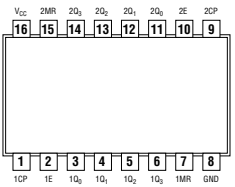
See page 605

4518
DUAL SYNCHRONOUS COUNTERS



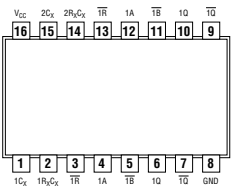
See page 606

4520
DUAL SYNCHRONOUS COUNTERS



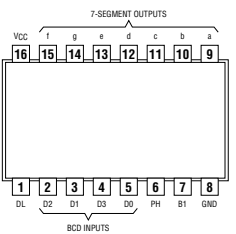
See page 607

4538
DUAL RETRIGGERABLE PRECISION MONO STABLE MULTIVIBRATOR



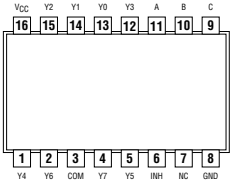
See page 608

4543
BCD-TO-7 SEGMENT LATCH/DECODER/DRIVERS



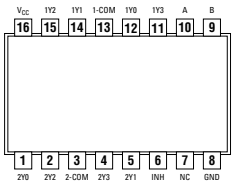
See page 610

4851
8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER WITH INJECTION-CURRENT EFFECT CONTROL



See page 612

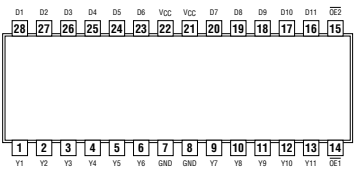
4852
DUAL 4-TO-1 CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER WITH INJECTION-CURRENT EFFECT CONTROL



NC-No internal connection

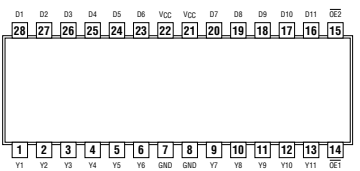
See page 612

5400
11-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS



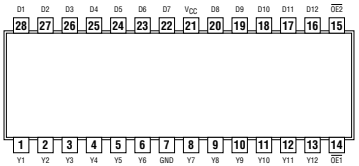
See page 614

5401
11-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS



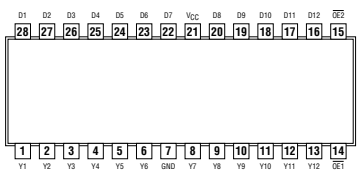
See page 614

5402
12-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS



See page 615

5403
12-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS

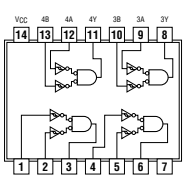


See page 615

7001
QUADRUPLE POSITIVE-AND GATES WITH SCHMITT-TRIGGER INPUTS

positive logic:

$Y = A \bullet B$

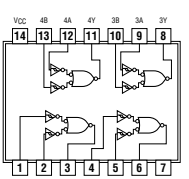


See page 616

7002
QUADRUPLE POSITIVE-NOR GATES WITH SCHMITT-TRIGGER INPUTS

positive logic:

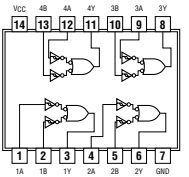
$Y = \overline{A} + \overline{B}$



See page 616

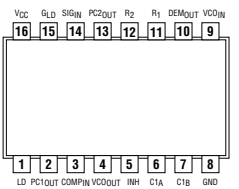
7032
QUADRUPLE POSITIVE-OR GATES WITH SCHMITT-TRIGGER INPUTS

positive logic:
$Y = A + B$



See page 617

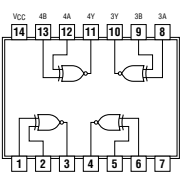
7046
PHASE-LOCKED LOOP WITH VCO AND LOCK DETECTOR



See page 618

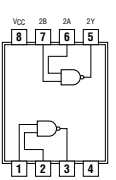
7266
QUAD 2-INPUT EXCLUSIVE-NOR GATES

positive logic:
$Y = \overline{A} = \overline{B}$



See page 619

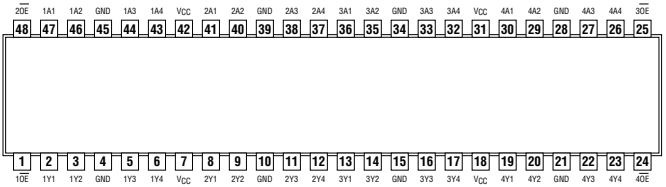
8003
DUAL 2-INPUT POSITIVE-NAND GATES



See page 619

16240

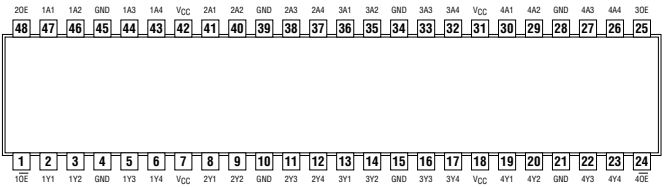
16-BIT BUS BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS



See page 620

16241

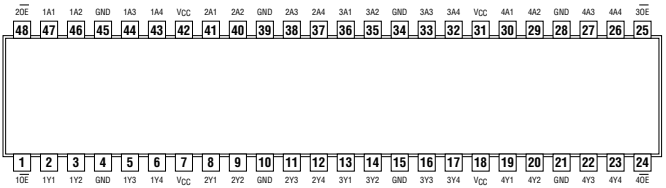
16-BIT BUS BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS



See page 622

16244

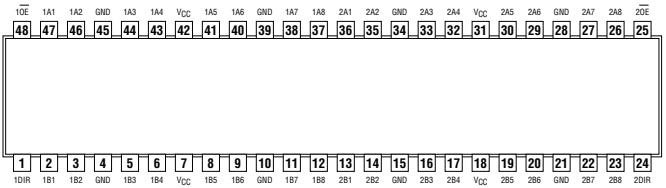
16-BIT BUS BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS



See page 624

16245

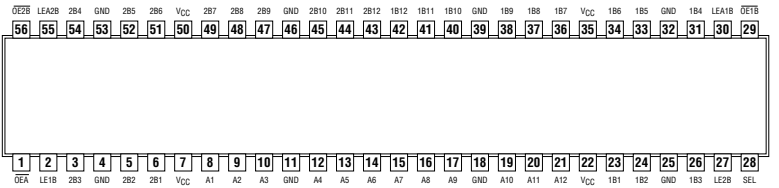
16-BIT BUS TRANSCEIVER
WITH 3-STATE OUTPUTS



See page 626

16260

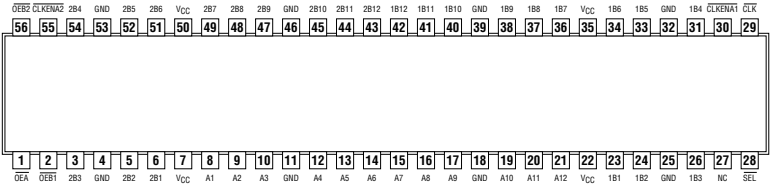
12-BIT TO 24-BIT MULTIPLEXES D-TYPE LATCH
WITH 3-STATE OUTPUTS



See page 628

16269

12-BIT TO 24-BIT REGISTERED BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

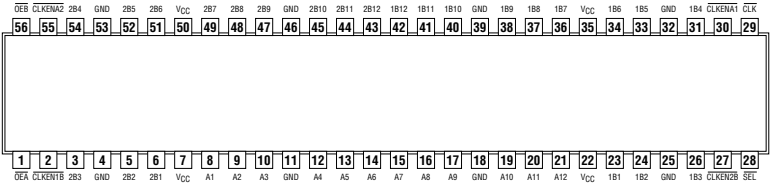


NC-No internal connection

See page 630

16270

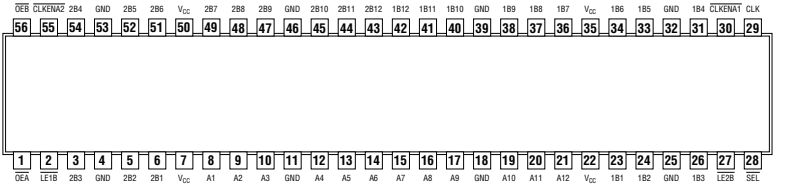
12-BIT TO 24-BIT REGISTERED BUS EXCHANGER
WITH 3-STATE OUTPUTS



See page 632

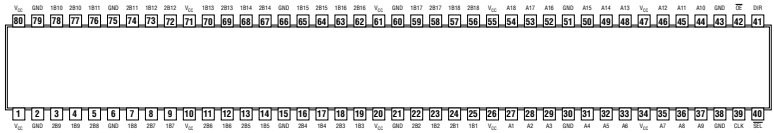
16271

12-BIT TO 24-BIT MULTIPLEXED BUS EXCHANGER
WITH 3-STATE OUTPUTS



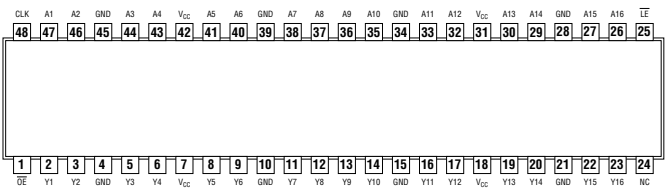
See page 634

16282
18-BIT TO 36-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS



See page 636

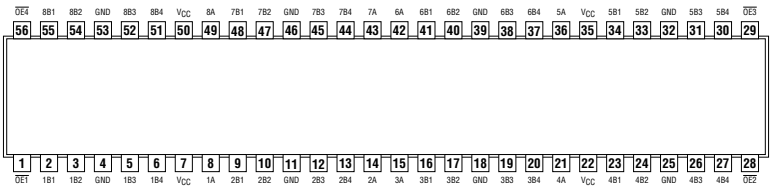
16334
16-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS



NC-No internal connection

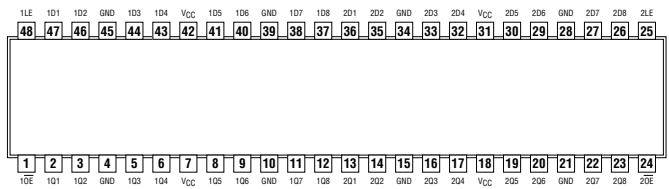
See page 638

16344
1-BIT TO 4-BIT ADDRESS DRIVER WITH 3-STATE OUTPUTS



See page 640

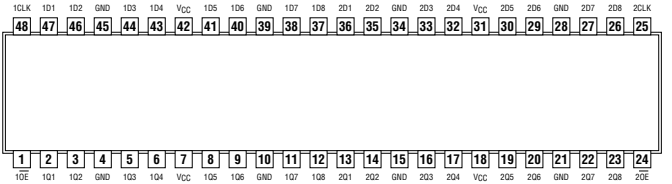
16373
16-BIT TRANSPARENT LATCHES WITH 3-STATE OUTPUTS



See page 642

16374

16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH 3-STATE OUTPUTS



See page 644

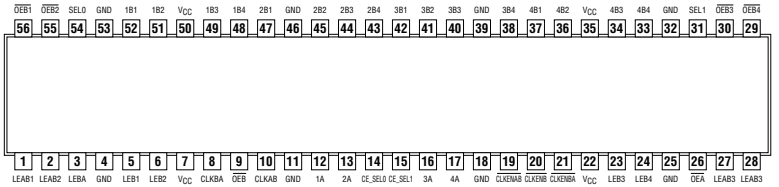
16409

9-BIT, 4-PORT UNIVERSAL BUS EXCHANGER
WITH 3-STATE OUTPUTS

See page 646

16460

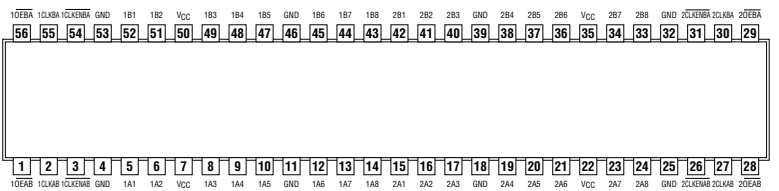
4-TO-1 MULTIPLEXED/DEMULTIPLEXED TRANSCEIVERS
WITH 3-STATE OUTPUTS



See page 648

16470

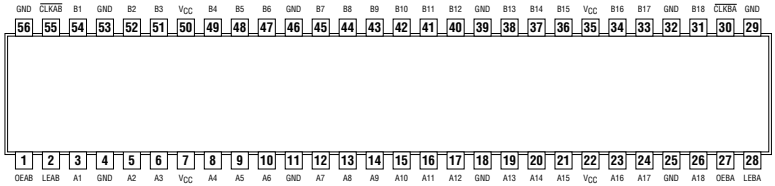
16-BIT REGISTERED TRANSCEIVERS
WITH 3-STATE OUTPUTS



See page 650

16500

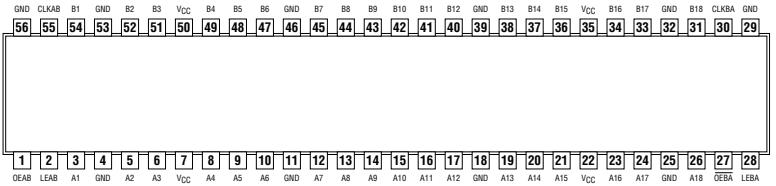
18-BIT UNIVERSAL BUS TRANSCEIVER
WITH 3-STATE OUTPUTS



See page 652

16501

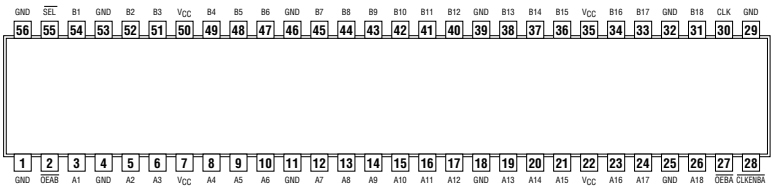
18-BIT UNIVERSAL BUS TRANSCEIVER
WITH 3-STATE OUTPUTS



See page 654

16524

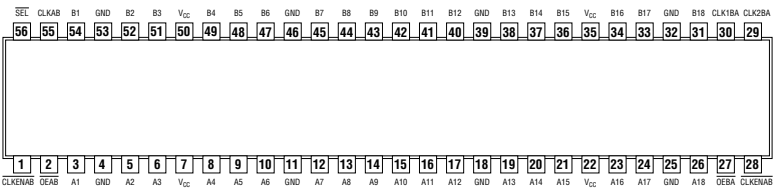
18-BIT REGISTERED BUS TRANSCEIVER
WITH 3-STATE OUTPUTS



See page 656

16525

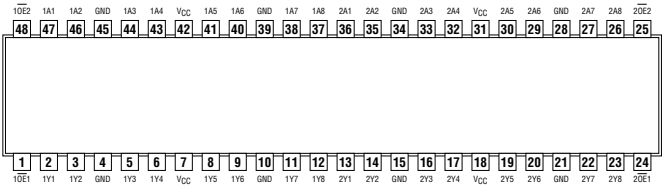
18-BIT REGISTERED BUS TRANSCEIVER
WITH 3-STATE OUTPUTS



See page 658

16540

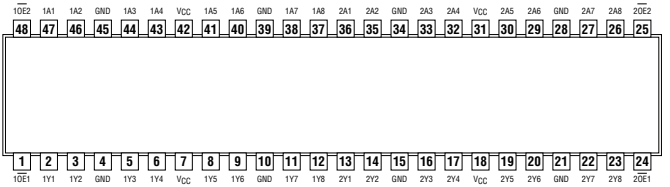
16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS



See page 660

16541

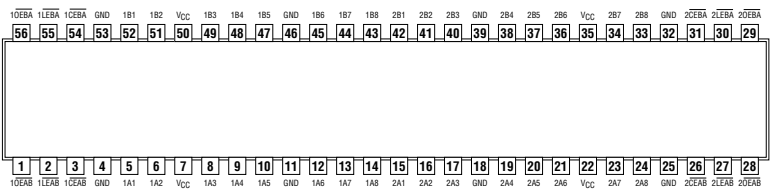
16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS



See page 661

16543

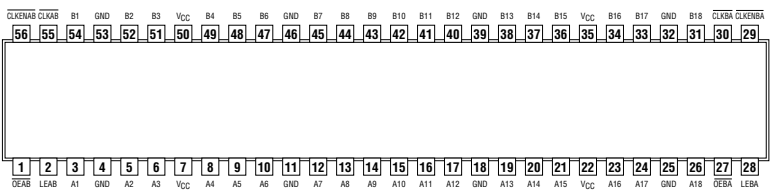
16-BIT REGISTERED TRANSCEIVERS
WITH 3-STATE OUTPUTS



See page 662

16600

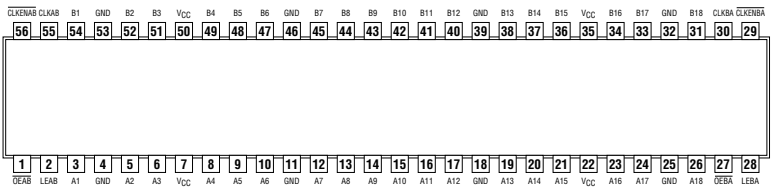
18-BIT UNIVERSAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS



See page 664

16601

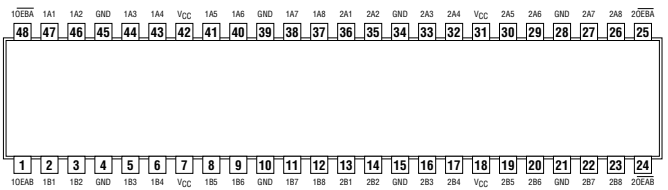
18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS



See page 666

16620

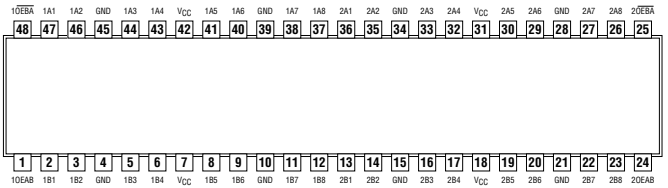
16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS



See page 668

16623

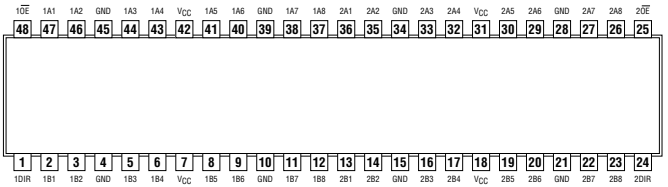
16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS



See page 670

16640

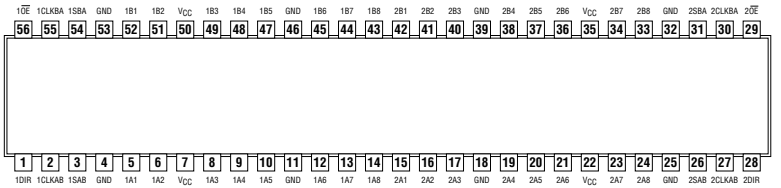
16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS



See page 671

16646

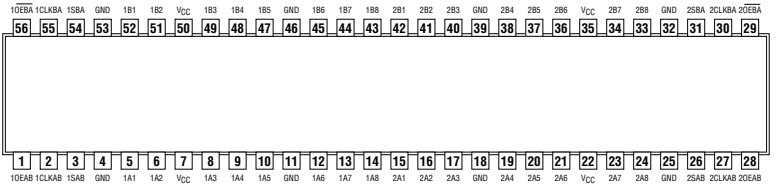
16-BIT BUS TRANSCEIVERS AND REGISTERS
WITH 3-STATE OUTPUTS



See page 672

16651

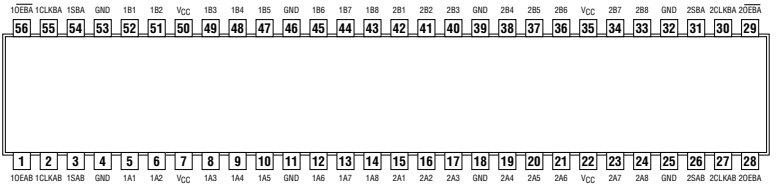
16-BIT BUS TRANSCEIVERS AND REGISTERS
WITH 3-STATE OUTPUTS



See page 674

16652

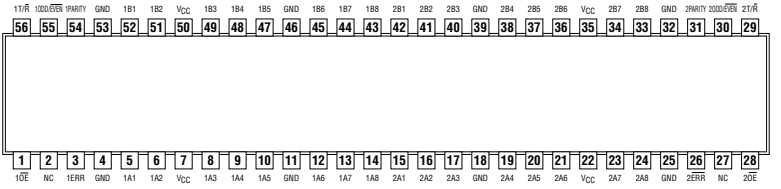
16-BIT BUS TRANSCEIVERS AND REGISTERS
WITH 3-STATE OUTPUTS



See page 676

16657

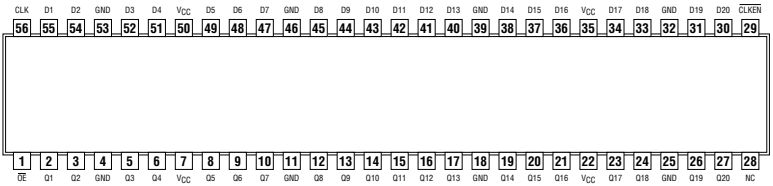
16-BIT TRANSCEIVERS
WITH PARITY GENERATORS/CHECKERS AND 3-STATE OUTPUTS



See page 678

NC-No internal connection

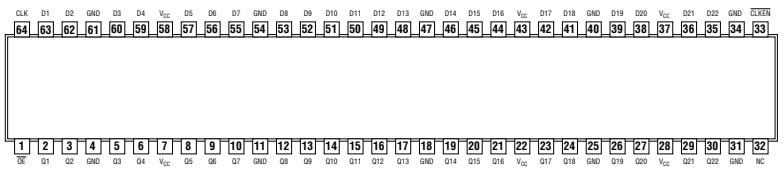
16721
20-BIT FLIP-FLOP
WITH 3-STATE OUTPUTS



NC-No internal connection

See page 680

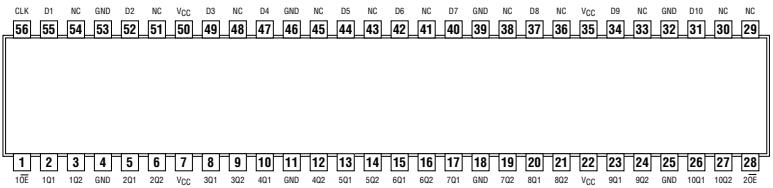
16722
22-BIT FLIP-FLOP WITH 3-STATE OUTPUTS



NC-No internal connection

See page 681

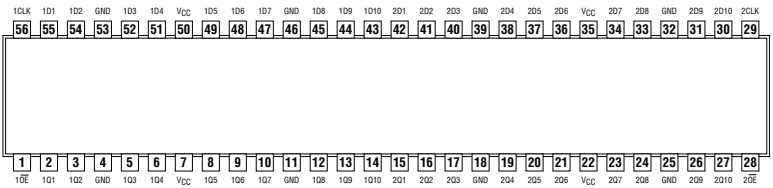
16820
10-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH DUAL OUTPUTS



NC-No internal connection

See page 682

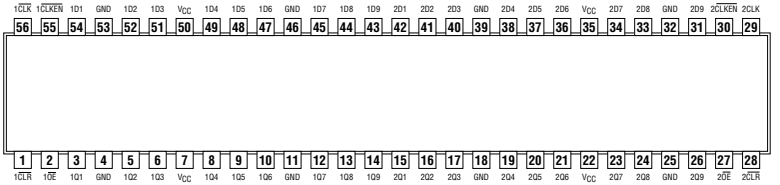
16821
20-BIT BUS INTERFACE FLIP-FLOPS
WITH 3-STATE OUTPUTS



See page 683

16823

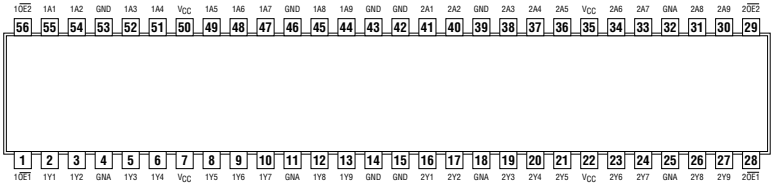
18-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH DUAL OUTPUTS



See page 684

16825

18-BIT BUS BUFFERS/DRIVERS WITH 3-STATE OUTPUTS



See page 685

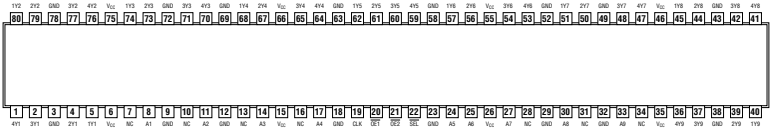
16827

20-BIT BUS BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

See page 686

16831

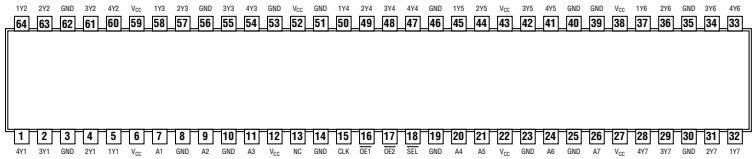
1-TO-4 ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS



NC–No internal connection

See page 688

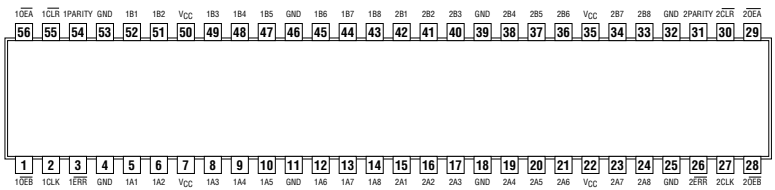
16832
1-TO-4 ADDRESS REGISTER/DRIVER
WITH 3-STATE OUTPUTS



NC-No internal connection

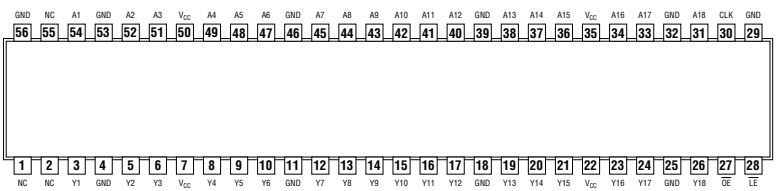
See page 689

16833
DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS



See page 690

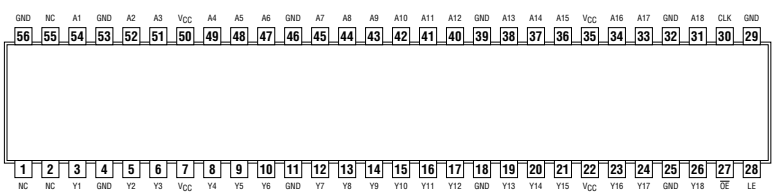
16834
16-BIT UNIVERSAL BUS DRIVER
WITH 3-STATE OUTPUTS



NC-No internal connection

See page 692

16835
3.3-V ABT 18-BIT UNIVERSAL BUS DRIVER
WITH 3-STATE OUTPUTS

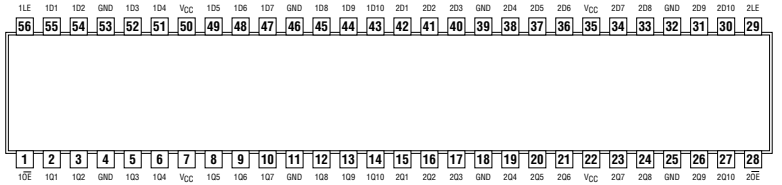


NC-No internal connection

See page 693

16841

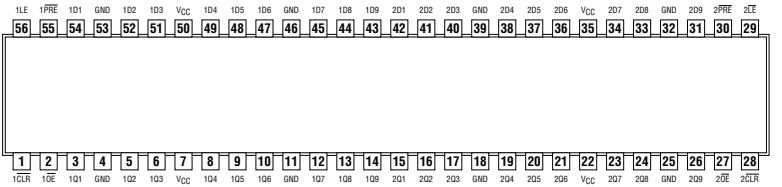
20-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS



See page 694

16843

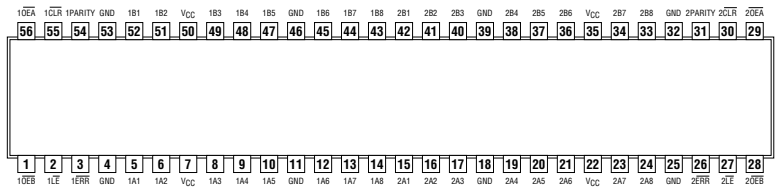
18-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS



See page 695

16853

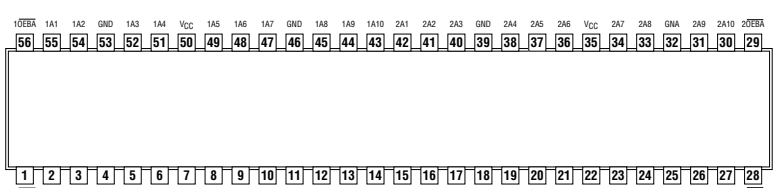
DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS



See page 696

16861

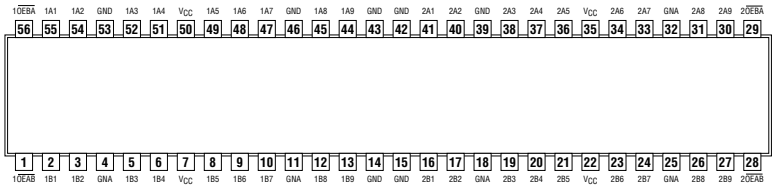
20-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS



See page 698

16863

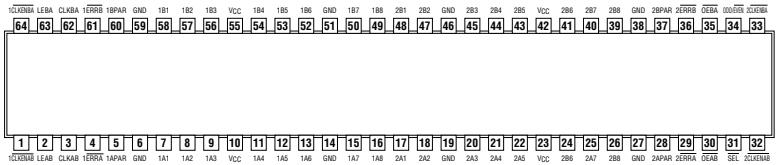
18-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS



See page 699

16901

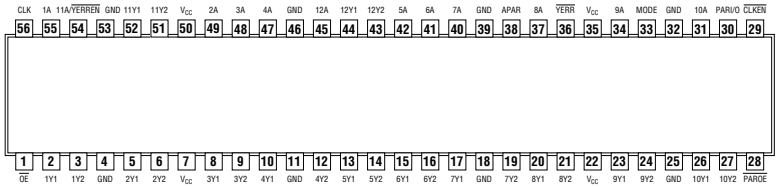
18-BIT UNIVERSAL BUS TRANSCEIVER
WITH PARITY GENERATORS/CHECKERS



See page 700

16903

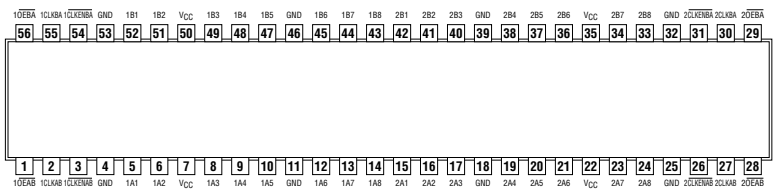
3.3-V 12-BIT UNIVERSAL BUS DRIVER
WITH PARITY CHECKER AND DUAL 3-STATE OUTPUTS



See page 702

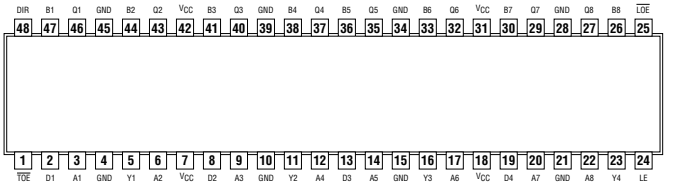
16952

16-BIT REGISTERED TRANSCEIVERS
WITH 3-STATE OUTPUTS



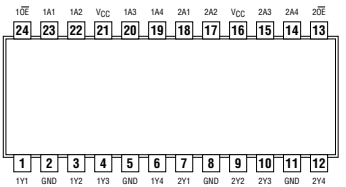
See page 704

16973
8-BIT BUS TRANSCEIVER AND TRANSPARENT D-TYPE LATCH WITH FOUR INDEPENDENT BUFFERS



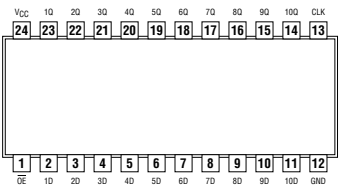
See page 706

25244
25-Ω OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS



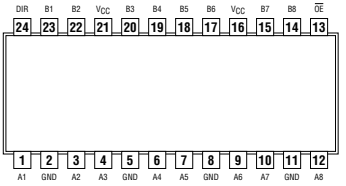
See page 708

29821
10-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS



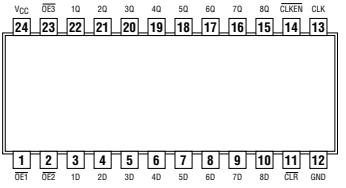
See page 711

25245
25-Ω OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS



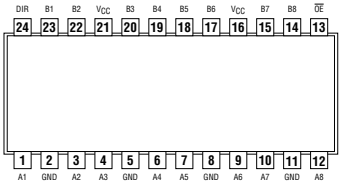
See page 709

29825
8-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS



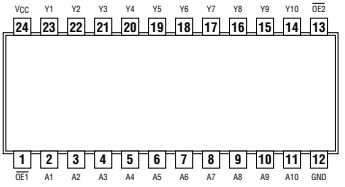
See page 712

25642
25-Ω OCTAL BUS TRANSCEIVER



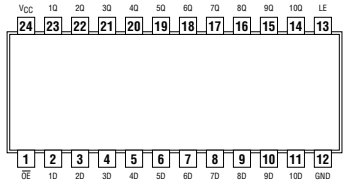
See page 710

29827
29828
10-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS



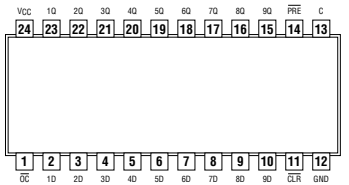
See page 713, 714

29841
10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS



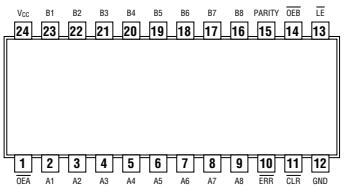
See page 715

29843
9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS



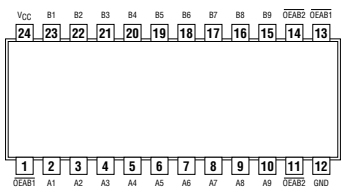
See page 716

29854
8-BIT TO 9-BIT PARITY BUS TRANSCEIVER



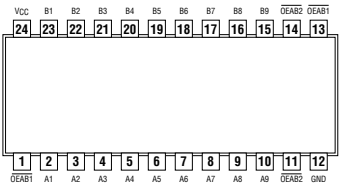
See page 718

29863
9-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS



See page 720

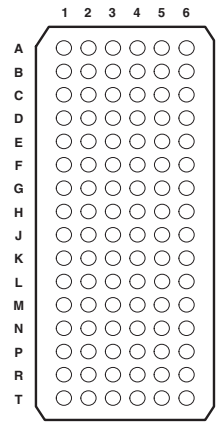
29864
9-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS



See page 721

32240
32-BIT BUFFER/DRIVER

GKE PACKAGE
(TOP VIEW)



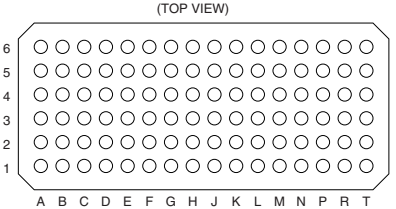
terminal assignments

	1	2	3	4	5	6
A	1Y2	1Y1	$1\overline{OE}$	$2\overline{OE}$	1A1	1A2
B	1Y4	1Y3	GND	GND	1A3	1A4
C	2Y2	2Y1	$1V_{CC}$	$1V_{CC}$	2A1	2A2
D	2Y2	2Y3	GND	GND	2A3	2A4
E	3Y2	3Y1	GND	GND	3A1	3A2
F	3Y4	3Y3	$1V_{CC}$	$1V_{CC}$	3A3	3A4
G	4Y2	4Y1	GND	GND	4A1	4A2
H	4Y3	4Y4	$4\overline{OE}$	$3\overline{OE}$	4A4	4A3
J	5Y2	5Y1	$5\overline{OE}$	$6\overline{OE}$	5A1	5A2
K	5Y4	5Y3	GND	GND	5A3	5A4
L	6Y2	6Y1	$2V_{CC}$	$2V_{CC}$	6A1	6A2
M	6Y4	6Y3	GND	GND	6A3	6A4
N	7Y2	7Y1	GND	GND	7A1	7A2
P	7Y4	7Y3	$2V_{CC}$	$2V_{CC}$	7A3	7A4
R	8Y2	8Y1	GND	GND	8A1	8A2
T	8Y3	8Y4	$8\overline{OE}$	$7\overline{OE}$	8A4	8A3

See page 722

32244
32-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS

GKE PACKAGE
(TOP VIEW)

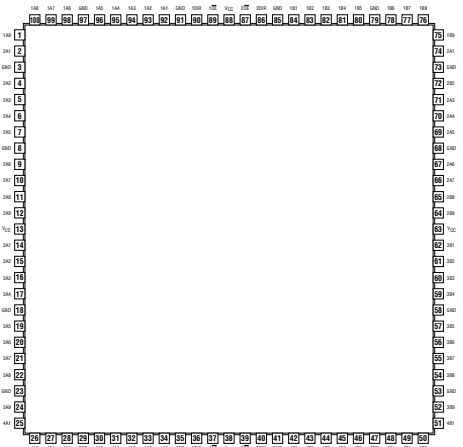


6	1A2	1A4	2A2	2A4	3A2	3A4	4A2	4A3	5A2	5A4	6A2	6A4	7A2	7A4	8A2	8A3
5	1A1	1A3	2A1	2A3	3A1	3A3	4A1	4A4	5A1	5A3	6A1	6A3	7A1	7A3	8A1	8A4
4	$2\overline{OE}$	GND	V_{CC}	GND	GND	V_{CC}	GND	$3\overline{OE}$	$6\overline{OE}$	GND	V_{CC}	GND	GND	V_{CC}	GND	$7\overline{OE}$
3	$1\overline{OE}$	GND	V_{CC}	GND	GND	V_{CC}	GND	$4\overline{OE}$	5DIR	GND	V_{CC}	GND	GND	V_{CC}	GND	8DIR
2	1Y1	1Y3	2Y1	2Y3	3Y1	3Y3	4Y1	4Y4	5Y1	5Y3	6Y1	6Y3	7Y1	7Y3	8Y1	8Y4
1	1Y2	1Y4	2Y2	2Y4	3Y2	3Y4	4Y2	4Y3	5Y2	5Y4	6Y2	6Y4	7Y2	7Y4	8Y2	8Y3
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T

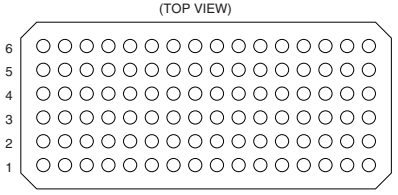
See page 724

32245

32-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS



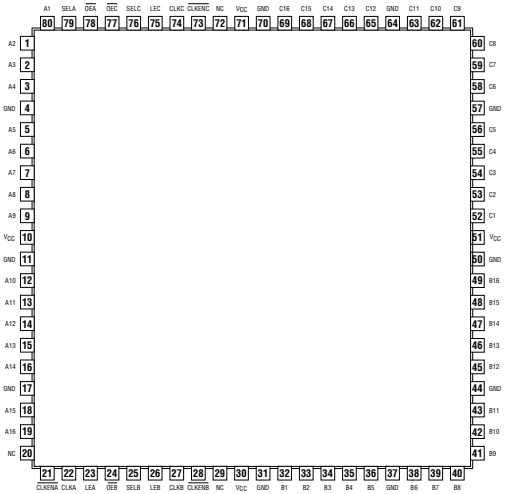
GKE PACKAGE
(TOP VIEW)



6	1A2	1A4	1A6	1A8	2A2	2A4	2A6	2A7	3A2	3A4	3A6	3A8	4A2	4A4	4A6	4A7
5	1A1	1A3	1A5	1A7	2A1	2A3	2A5	2A8	3A1	3A3	3A5	3A7	4A1	4A3	4A5	4A8
4	$1\overline{OE}$	GND	V_{CC}	GND	GND	V_{CC}	GND	$2\overline{OE}$	$3\overline{OE}$	GND	V_{CC}	GND	GND	V_{CC}	GND	$4\overline{OE}$
3	1DIR	GND	V_{CC}	GND	GND	V_{CC}	GND	2DIR	3DIR	GND	V_{CC}	GND	GND	V_{CC}	GND	4DIR
2	1B1	1B3	1B5	1B7	2B1	2B3	2B5	2B8	3B1	3B3	3B5	3B7	4B1	4B3	4B5	4B8
1	1B2	1B4	1B6	1B8	2B2	2B4	2B6	2B7	3B2	3B4	3B6	3B8	4B2	4B4	4B6	4B7
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T

See page 726

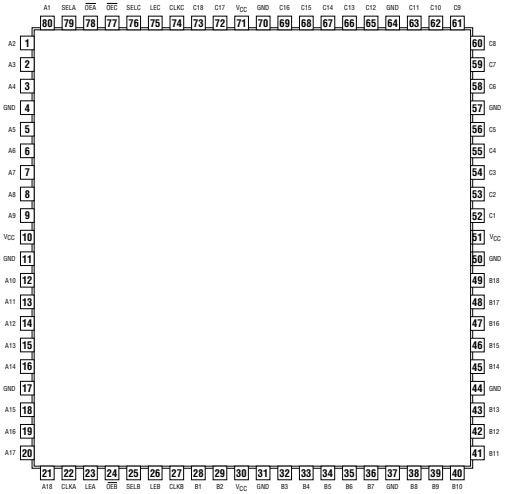
32316
16-BIT TRI-PORT UNIVERSAL BUS EXCHANGERS



NC-No internal connection

See page 728

32318
18-BIT TRI-PORT UNIVERSAL BUS EXCHANGERS

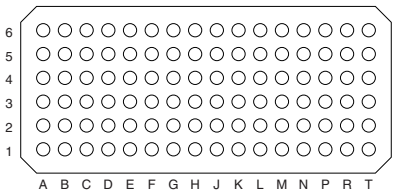


See page 730

32373

32-BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

GKE PACKAGE
(TOP VIEW)



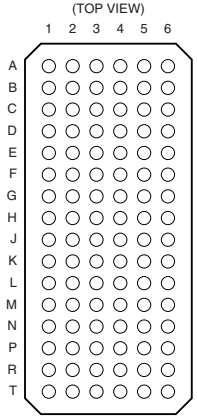
6	1D2	1D4	1D6	1D8	2D2	2D4	2D6	2D7	3D2	3D4	3D6	3D8	4D2	4D4	4D6	4D7
5	1D1	1D3	1D5	1D7	2D1	2D3	2D5	2D8	3D1	3D3	3D5	3D7	4D1	4D3	4D5	4D8
4	1LE	GND	V_{CC}	GND	GND	V_{CC}	GND	2LE	3LE	GND	V_{CC}	GND	GND	V_{CC}	GND	4LE
3	$1\overline{OE}$	GND	V_{CC}	GND	GND	V_{CC}	GND	$2\overline{OE}$	$3\overline{OE}$	GND	V_{CC}	GND	GND	V_{CC}	GND	$4\overline{OE}$
2	1Q1	1Q3	1Q5	1Q7	2Q1	2Q3	2Q5	2Q8	3Q1	3Q3	3Q5	3Q7	4Q1	4Q3	4Q5	4Q8
1	1Q2	1Q4	1Q6	1Q8	2Q2	2Q4	2Q6	2Q7	3Q2	3Q4	3Q6	3Q8	4Q2	4Q4	4Q6	4Q7
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T

See page 732

32374

32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

GKE PACKAGE
(TOP VIEW)



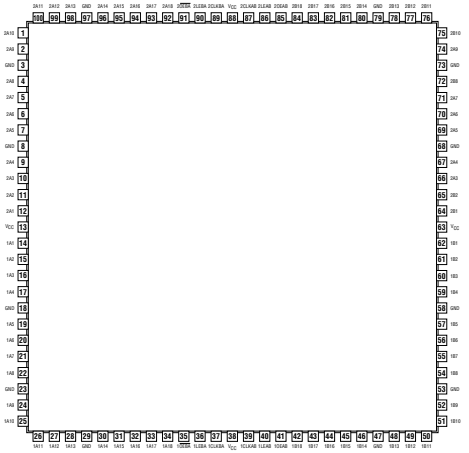
terminal assignments

	1	2	3	4	5	6
A	1Q2	1Q1	$1\overline{OE}$	1CLK	1D1	1D2
B	1Q4	1Q3	GND	GND	1D3	1D4
C	1Q6	1Q5	V_{CC}	V_{CC}	1D5	1D6
D	1Q8	1Q7	GND	GND	1D7	1D8
E	2Q2	2Q1	GND	GND	2D1	2D2
F	2Q4	2Q3	V_{CC}	V_{CC}	2D3	2D4
G	2Q6	2Q5	GND	GND	2D5	2D6
H	2Q8	2Q7	$2\overline{OE}$	2CLK	2D7	2D8
J	3Q2	3Q1	$3\overline{OE}$	3CLK	3D1	3D2
K	3Q4	3Q3	GND	GND	3D3	3D4
L	3Q6	3Q5	V_{CC}	V_{CC}	3D5	3D6
M	3Q8	3Q7	GND	GND	3D7	3D8
N	4Q2	4Q1	GND	GND	4D1	4D2
P	4Q4	4Q3	V_{CC}	V_{CC}	4D3	4D4
R	4Q6	4Q5	GND	GND	4D5	4D6
T	4Q7	4Q8	$4\overline{OE}$	4CLK	4D8	4D7

See page 734

32501

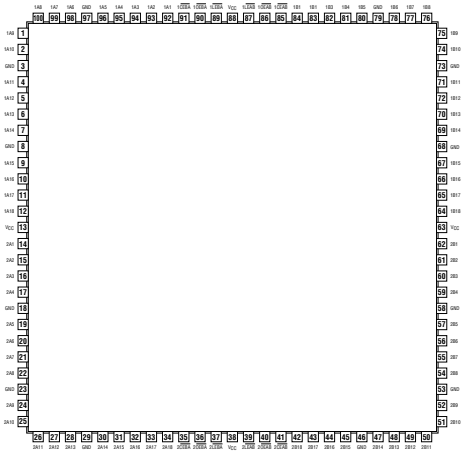
36-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS



See page 736

32543

36-BIT REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

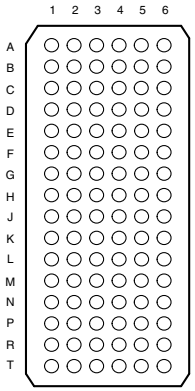


See page 738

32973

16-BIT BUS TRANSCEIVER AND TRANSPARENT D-TYPE LATCH WITH EIGHT INDEPENDENT BUFFERS

GKE PACKAGE
(TOP VIEW)



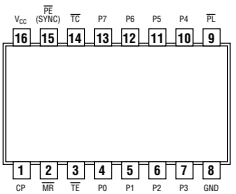
terminal assignments

	1	2	3	4	5	6
A	1A1	D1	$1\overline{TOE}$	1DIR	1B1	1Q1
B	1A2	Y1	GND	GND	1B2	1Q2
C	1A3	D2	V_{CC}	V_{CC}	1B3	1Q3
D	1A4	Y2	GND	GND	1B4	1Q4
E	1A5	D3	GND	GND	1B5	1Q5
F	1A6	Y3	V_{CC}	V_{CC}	1B6	1Q6
G	1A7	D4	GND	GND	1B7	1Q7
H	1A8	Y4	1LE	$1\overline{LOE}$	1B8	1Q8
J	2A1	D5	$2\overline{TOE}$	2DIR	2B1	2Q1
K	2A2	Y5	GND	GND	2B2	2Q2
L	2A3	D6	V_{CC}	V_{CC}	2B3	2Q3
M	2A4	Y6	GND	GND	2B4	2Q4
N	2A5	D7	GND	GND	2B5	2Q5
P	2A6	Y7	V_{CC}	V_{CC}	2B6	2Q6
R	2A7	D8	GND	GND	2B7	2Q7
T	2A8	Y8	2LE	$2\overline{LOE}$	2B8	2Q8

See page 740

40103

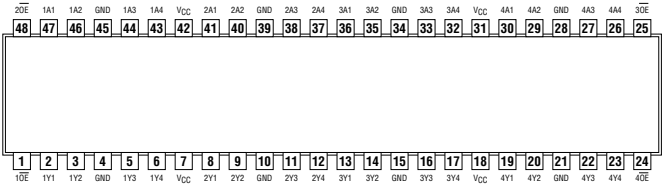
8-STAGE SYNCHRONOUS DOWN COUNTERS



See page 742

162240

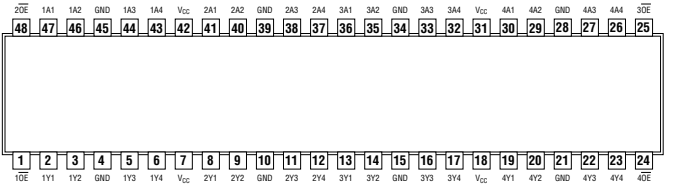
3.3-V ABT 16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS



See page 744

162241

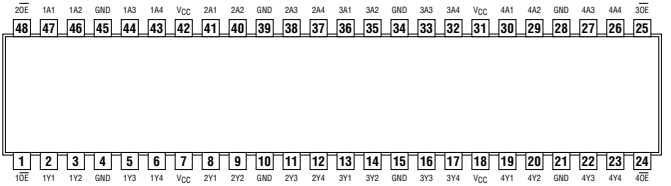
3.3-V ABT 16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS



See page 745

162244

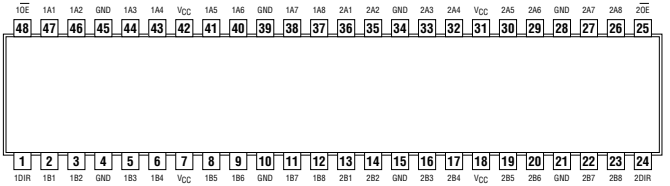
16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS



See page 746

162245

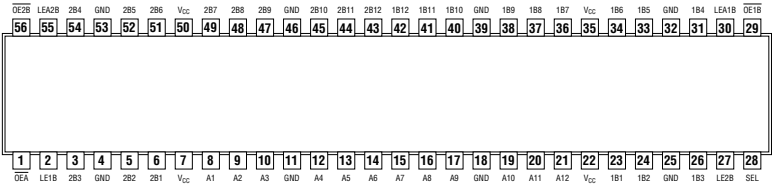
16-BIT TRANSCEIVER
WITH 3-STATE OUTPUTS



See page 747

162260

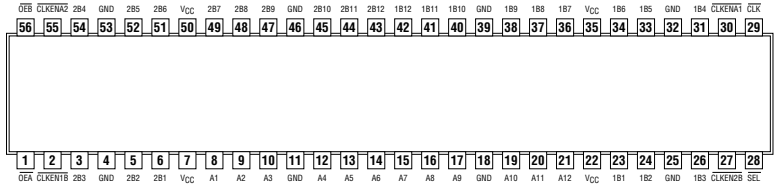
12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCH
WITH 3-STATE OUTPUTS



See page 748

162268

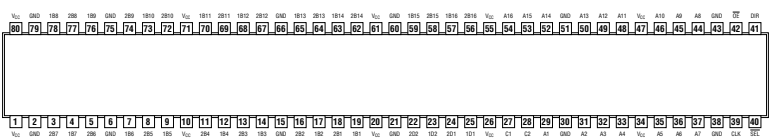
12-BIT TO 24-BIT REGISTERED BUS EXCHANGER
WITH 3-STATE OUTPUTS



See page 750

162280

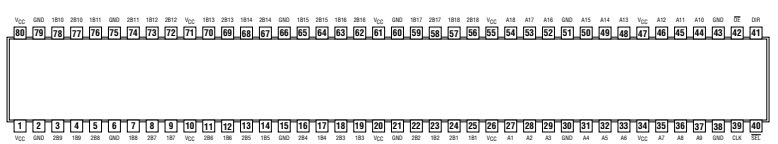
16-BIT TO 32-BIT REGISTERED BUS EXCHANGER
WITH BYTE MASKS AND 3-STATE OUTPUTS



See page 752

162282

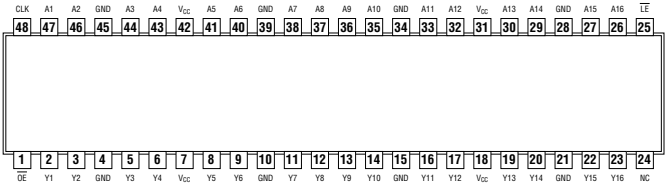
18-BIT TO 36-BIT REGISTERED BUS EXCHANGER
WITH 3-STATE OUTPUTS



See page 754

162334

16-BIT UNIVERSAL BUS DRIVER
WITH 3-STATE OUTPUTS

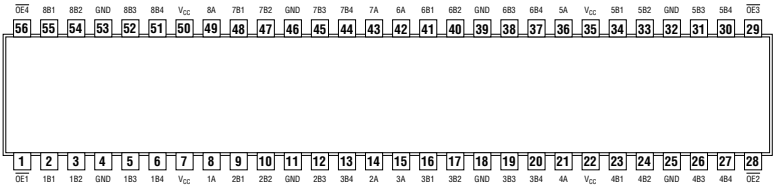


NC-No internal connection

See page 756

162344

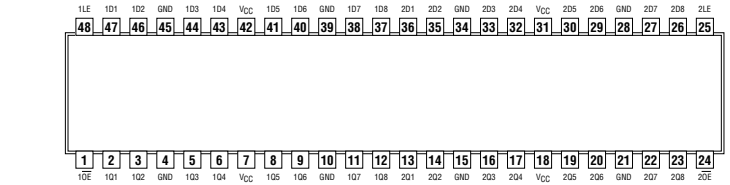
1-BIT TO 4-BIT ADDRESS DRIVER
WITH 3-STATE OUTPUTS



See page 758

162373

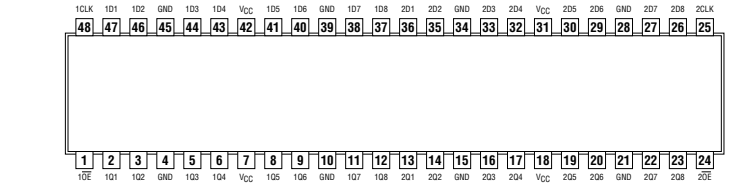
3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES
WITH 3-STATE OUTPUTS



See page 760

162374

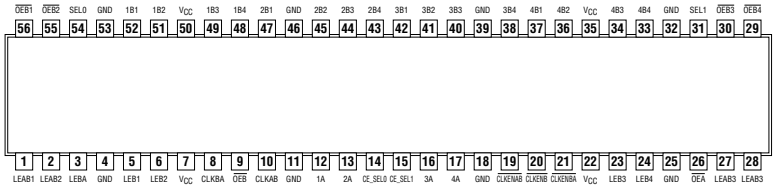
3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH 3-STATE OUTPUTS



See page 761

162460

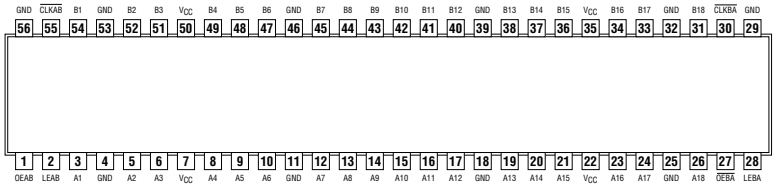
4-TO-1 MULTIPLEXED/DEMULTIPLEXED REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS



See page 762

162500

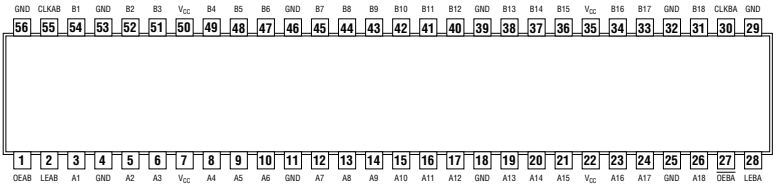
18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS



See page 764

162501

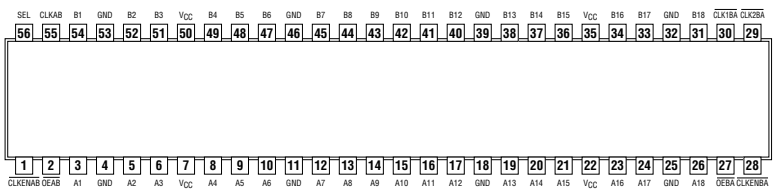
18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS



See page 766

162525

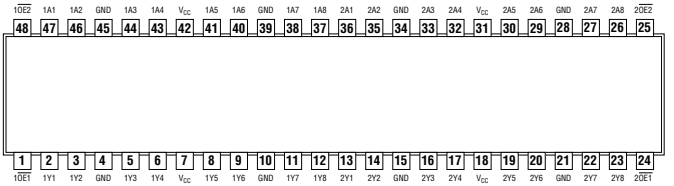
18-BIT REGISTERED BUS TRANSCEIVER WITH 3-STATE OUTPUTS



See page 768

162541

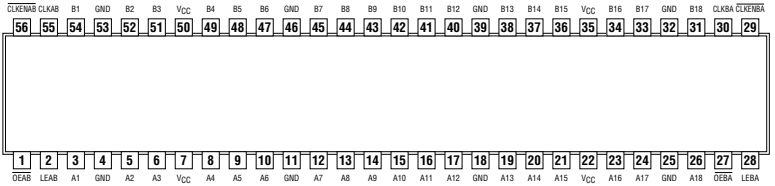
3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS



See page 770

162601

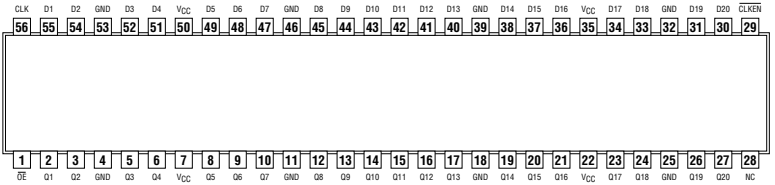
18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS



See page 772

162721

3.3-V 20-BIT FLIP-FLOP WITH 3-STATE OUTPUTS

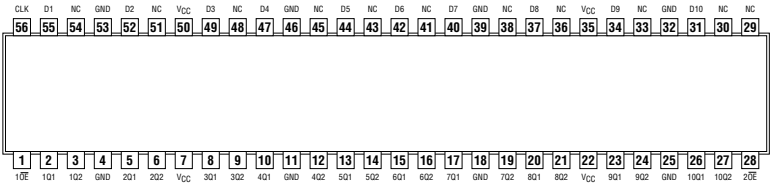


See page 774

NC-No internal connection

162820

3.3-V 10-BIT FLIP-FLOP WITH DUAL OUTPUTS AND 3-STATE OUTPUTS

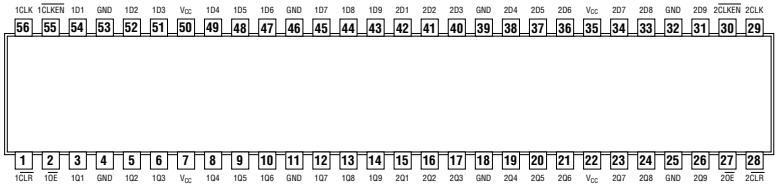


See page 775

NC-No internal connection

162823

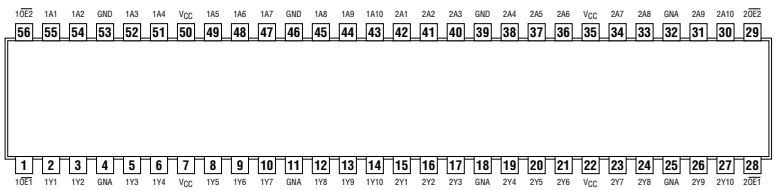
18-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS



See page 776

162825

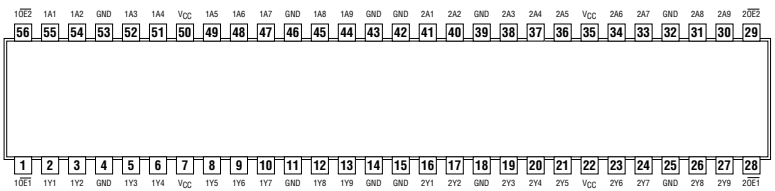
18-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS



See page 777

162827

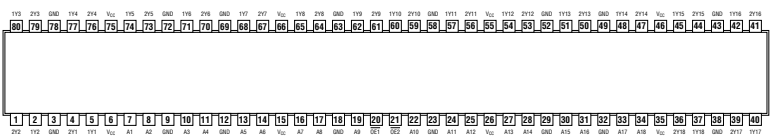
20-BIT BUS BUFFERS/DRIVERS WITH 3-STATE OUTPUTS



See page 778

162830

1-BIT TO 2-BIT ADDRESS DRIVER WITH 3-STATE OUTPUTS



See page 779

162831

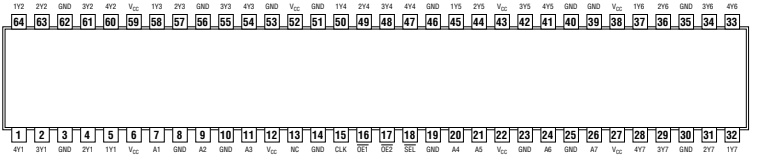
1-BIT TO 4-BIT ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS

NC-No internal connection

See page 780

162832

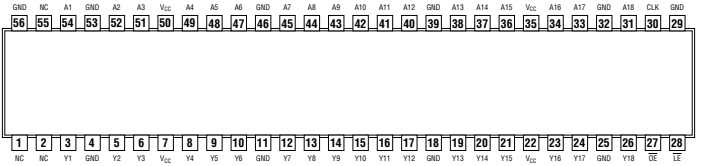
1-BIT TO 4-BIT ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS



See page 781

162834
162835

18-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

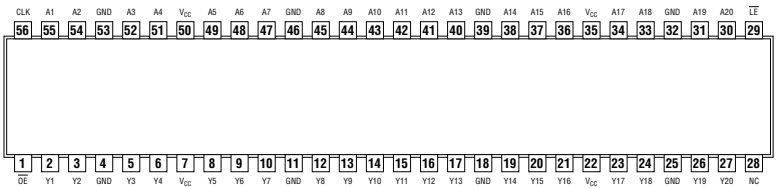


NC-No internal connection

See page 782, 783

162836

20-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS



NC-No internal connection

See page 784

162841

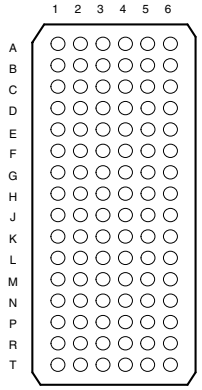
20-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

See page 785

322244

32-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

GKE PACKAGE
(TOP VIEW)



terminal assignments

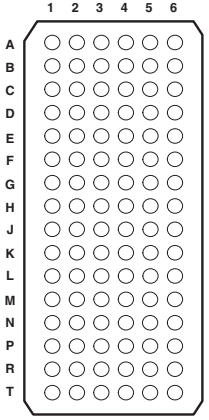
	1	2	3	4	5	6
A	1Y2	1Y1	$1\overline{OE}$	$2\overline{OE}$	1A1	1A2
B	1Y4	1Y3	GND	GND	1A3	1A4
C	2Y2	2Y1	V_{CC}	V_{CC}	2A1	2A2
D	2Y4	2Y3	GND	GND	2A3	2A4
E	3Y2	3Y1	GND	GND	3A1	3A2
F	3Y4	3Y3	V_{CC}	V_{CC}	3A3	3A4
G	4Y2	4Y1	GND	GND	4A1	4A2
H	4Y3	4Y4	$4\overline{OE}$	$3\overline{OE}$	4A4	4A3
J	5Y2	5Y1	$5\overline{OE}$	$6\overline{OE}$	5A1	5A2
K	5Y4	5Y3	GND	GND	5A3	5A4
L	6Y2	6Y1	V_{CC}	V_{CC}	6A1	6A2
M	6Y4	6Y3	GND	GND	6A3	6A4
N	7Y2	7Y1	GND	GND	7A1	7A2
P	7Y4	7Y3	V_{CC}	V_{CC}	7A3	7A4
R	8Y2	8Y1	GND	GND	8A1	8A2
T	8Y3	8Y4	$8\overline{OE}$	$7\overline{OE}$	8A4	8A3

See page 786

322374

3.3-V ABT 32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

GKE PACKAGE
(TOP VIEW)



terminal assignments

	1	2	3	4	5	6
A	1Q2	1Q1	$1\overline{OE}$	1CLK	1D1	1D2
B	1Q4	1Q3	GND	GND	1D3	1D4
C	1Q6	1Q5	V_{CC}	V_{CC}	1D5	1D6
D	1Q8	1Q7	GND	GND	1D7	1D8
E	2Q2	2Q1	GND	GND	2D1	2D2
F	2Q4	2Q3	V_{CC}	V_{CC}	2D3	2D4
G	2Q6	2Q6	GND	GND	2D5	2D6
H	2Q7	2Q8	$2\overline{OE}$	2CLK	2D8	2D7
J	3Q2	3Q1	$3\overline{OE}$	3CLK	3D1	3D2
K	3Q4	3Q3	GND	GND	3D3	3D4
L	3Q6	3Q5	V_{CC}	V_{CC}	3D5	3D6
M	3Q8	3Q7	GND	GND	3D7	3D8
N	4Q2	4Q1	GND	GND	4D1	4D2
P	4Q4	4Q3	V_{CC}	V_{CC}	4D3	4D4
R	4Q6	4Q5	GND	GND	4D5	4D6
T	4Q7	4Q8	$4\overline{OE}$	4CLK	4D8	4D7

See page 787

FUNCTION AND ELECTRICAL CHARACTERISTICS

Standard

00

QUADRUPLE 2-INPUT POSITIVE-NAND GATES

- $Y = \overline{A \bullet B}$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram (SN74)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC	CD74 AC	UNIT
I_{CC}	MAX	22	4.4	36	3	17.4	10.2	0.02	0.04	0.02	0.04	0.04	0.02	0.08	mA
I_{OH}	MAX	-0.4	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-4	-24	-24	-24	mA
I_{OL}	MAX	16	8	20	8	20	20	4	4	4	4	24	24	24	mA

PARAMETER	MAX or MIN	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	ALVC 3V	AUC 1.8V	AUC 2.3V	UNIT
I_{CC}	MAX	0.04	0.02	0.08	0.02	0.02	-	0.02	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-24	-24	-24	-8	-8	-6	-12	-24	-24	-8	-9	mA
I_{OL}	MAX	24	24	24	8	8	6	12	24	24	8	9	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT
t_{PLH}	A or B	Y	MAX	22	15	4.5	11	4.5	6	23	27	25
t_{PHL}	A or B	Y	MAX	15	15	5	8	4	5.3	23	27	25

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HCT	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT
t_{PLH}	A or B	Y	MAX	30	7.4	8.5	7.3	12.3	9.5	10.8	8.5	9
t_{PHL}	A or B	Y	MAX	30	6.8	7	7.3	8.8	8	13.2	8.5	9

PARAMETER	INPUT	OUTPUT	MAX or MIN	LV 3V	LV 5V	LVC 3V	ALVC 3V	AUC 1.8V	AUC 2.3V
t_{PLH}	A or B	Y	MAX	13	8.5	4.3	3	2.4	2
t_{PHL}	A or B	Y	MAX	13	8.5	4.3	3	2.4	2

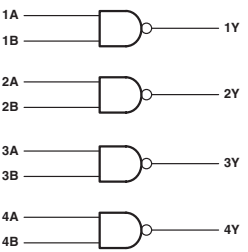
UNIT:ns

01

QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

● $Y = \overline{A \bullet B}$

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	HC	UNIT
I_{CC}	MAX	22	4.4	3	0.02	mA
V_{OH}	MAX	5.5	5.5	5.5	Vcc	V
I_{OL}	MAX	16	8	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	HC
t_{PLH}	A or B	Y	MAX	55	32	54	31
t_{PHL}	A or B	Y	MAX	15	28	28	25

UNIT:ns

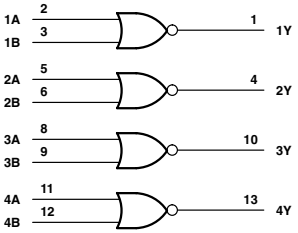
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

02

QUADRUPLE 2-INPUT POSITIVE-NOR GATES

- $Y = \overline{A + B}$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram (SN74)



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	UNIT
I_{CC}	MAX	27	5.4	45	4	20.1	13	0.02	0.04	0.02	0.04	mA
I_{OH}	MAX	-0.4	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-4	mA
I_{OL}	MAX	16	8	20	8	20	20	4	4	4	4	mA

PARAMETER	MAX or MIN	AC 11	CD74 AC	ACT 11	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	AUC 1.8V	AUC 2.3V	UNIT
I_{CC}	MAX	0.04	0.08	0.04	0.08	0.02	0.02	-	0.02	0.01	0.01	0.01	mA
I_{OH}	MAX	-24	-24	-24	-24	-8	-8	-6	-12	-24	-8	-9	mA
I_{OL}	MAX	24	24	24	24	8	8	6	12	24	8	9	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT
t_{PLH}	A or B	Y	MAX	22	15	5.5	12	4.5	6.5	23	27	25	32
t_{PHL}	A or B	Y	MAX	15	15	5.5	10	4.5	5.3	23	27	25	32

PARAMETER	INPUT	OUTPUT	MAX or MIN	AC 11	CD74 AC	ACT 11	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V
t_{PLH}	A or B	Y	MAX	6.9	11.5	10.6	12.2	8.5	8.5	13	8.5	4.4
t_{PHL}	A or B	Y	MAX	6.4	11.5	8.7	12.2	8.5	8.5	13	8.5	4.4

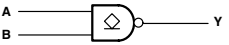
PARAMETER	INPUT	OUTPUT	MAX or MIN	AUC 1.8V	AUC 2.3V
t_{PLH}	A or B	Y	MAX	2.4	2
t_{PHL}	A or B	Y	MAX	2.4	2

UNIT: ns

03

QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

Logic Diagram (SN74)



● $Y = \overline{A \bullet B}$

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	22	4.4	36	4	0.02	0.04	0.04	mA
V_{OH}	MAX	5.5	8	5.5	8	V_{CC}	V_{CC}	V_{CC}	V
I_{OL}	MAX	16	0.1	20	0.1	4	4	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	SN74 HC	CD74 HC	CD74 HCT
t_{PLH}	A or B	Y	MAX	45	32	7.5	50	31	30	36
t_{PHL}	A or B	Y	MAX	15	28	7	13	25	30	36

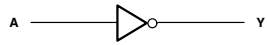
UNIT: ns

: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

04

HEX INVERTERS

Logic Diagram (SN74)



- $Y = \overline{A}$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC	UNIT
I_{CC}	MAX	33	6.6	54	4.2	26.3	15.3	0.02	0.04	0.02	0.04	0.04	0.02	mA
I_{OH}	MAX	-0.4	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-4	-24	-24	mA
I_{OL}	MAX	16	8	20	8	20	20	4	4	4	4	24	24	mA

PARAMETER	MAX or MIN	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	ALVC 3V	AUC 1.8V	AUC 2.3V	UNIT
I_{CC}	MAX	0.08	0.04	0.02	0.08	0.02	0.02	-	0.02	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-24	-24	-24	-24	-8	-8	-6	-12	-24	-24	-8	-9	mA
I_{OL}	MAX	24	24	24	24	8	8	6	12	24	24	8	9	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT
t_{PLH}	A or B	Y	MAX	22	15	4.5	11	5	6	24	26	25
t_{PHL}	A or B	Y	MAX	15	15	5	8	4	5.3	24	26	25

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HCT	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT
t_{PLH}	A or B	Y	MAX	29	7.1	7.5	6.5	9.7	9	9.3	8.5	8.5
t_{PHL}	A or B	Y	MAX	29	6	7	6.5	9.6	8.5	9.3	8.5	8.5

PARAMETER	INPUT	OUTPUT	MAX or MIN	LV 3V	LV 5V	LVC 3V	ALVC 3V	AUC 1.8V	AUC 2.3V
t_{PLH}	A or B	Y	MAX	12	8.5	4.5	2.8	2.5	2.0
t_{PHL}	A or B	Y	MAX	12	8.5	4.5	2.8	2.5	2.0

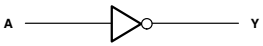
UNIT: ns

U04

HEX INVERTERS

- Y = $\overline{A}$
- Unbuffered Output

Logic Diagram (SN74)



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	CD74 HC	AHC	LV 3V	LV 5V	LVC 3V	AUC 1.8V	AUC 2.3V	UNIT
I_{CC}	MAX	0.02	0.04	0.02	-	0.02	0.01	0.01	0.01	mA
I_{OH}	MAX	-4	-4	-8	-6	-12	-24	-8	-9	mA
I_{OL}	MAX	4	4	8	6	12	24	8	9	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	AHC	LV 3V	LV 5V	LVC 3V	AUC 1.8V	AUC 2.3V
t_{PLH}	A or B	Y	MAX	20	21	8	13	8	3.8	2.0	1.7
t_{PHL}	A or B	Y	MAX	20	21	8	13	8	3.8	2.0	1.7

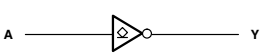
UNIT: ns

05

HEX INVERTERS WITH OPEN-DRAIN OUTPUTS

- Y = $\overline{A}$

Logic Diagram (SN74)



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	SN74 HC	CD74 AC	CD74 ACT	AHC	LV 3V	LV 5V	UNIT
I_{CC}	MAX	33	6.6	54	4.2	0.02	0.08	0.08	0.02	-	0.02	mA
I_{OH}	MAX	0.25	0.1	0.25	-	-	-24	-24	-	-	-	mA
V_{OH}	MAX	5.5	5.5	5.5	5.5	5.5	5.5	5.5	Vcc	5.5	5.5	V
I_{OL}	MAX	16	8	20	8	4	24	24	8	6	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	SN74 HC	CD74 AC	CD74 ACT	AHC	LV 3V	LV 5V
t_{PLH}	A or B	Y	MAX	55	32	7.5	54	29	-	-	-	12	8.5
t_{PHL}	A or B	Y	MAX	15	28	7	14	21	-	-	-	12	8.5
t_{PLZ}	A	Y	MAX	-	-	-	-	-	8.2	9.3	8.5	-	-
t_{PZL}	A	Y	MAX	-	-	-	-	-	6.5	10.8	8.5	-	-

UNIT: ns

: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

06

HEX INVERTER BUFFERS/DRIVERS WITH OPEN-DRAIN OUTPUTS

Logic Diagram

● $Y = \overline{A}$

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	LV 3V	LV 5V	LVC 3V	AUC 1.8V	AUC 2.5V	UNIT
I_{CC}	MAX	51	60	-	0.02	0.01	0.01	0.01	mA
I_{OH}	MAX	0.25	0.25	-	±0.0025	-	-	-	mA
V_{OH}	MAX	30	30	5.5	5.5	5.5	3.6	3.6	V
I_{OL}	MAX	40	40	8	16	24	8	9	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	LV 3V	LV 5V	LVC 3V	AUC 1.8V	AUC 2.5V
t_{PLH}	A or B	Y	MAX	15	15	12	8.5	3.7	2.8	1.3
t_{PHL}	A or B	Y	MAX	23	20	12	8.5	3.7	2.8	1.3

UNIT: ns

07

HEX BUFFERS/DRIVERS WITH OPEN-DRAIN OUTPUTS

Logic Diagram

● $Y = A$

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	LV 3V	LV 5V	LVC 3V	AUC 1.8V	AUC 2.5V	UNIT
I_{CC}	MAX	41	45	-	0.02	0.01	0.01	0.01	mA
I_{OH}	MAX	0.25	0.25	-	±0.0025	-	-	-	mA
V_{OH}	MAX	30	30	5.5	5.5	5.5	3.6	3.6	V
I_{OL}	MAX	40	40	8	16	24	8	9	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	LV 3V	LV 5V	LVC 3V	AUC 1.8V	AUC 2.5V
t_{PLH}	A or B	Y	MAX	15	10	12	8.5	2.9	2.3	1.3
t_{PHL}	A or B	Y	MAX	26	30	12	8.5	2.9	2.3	1.3

UNIT: ns

08

QUADRUPLE 2-INPUT POSITIVE-AND GATES

Logic Diagram (SN74)

- Y = A•B
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	UNIT
I_{CC}	MAX	33	8.8	57	4	24	12.9	0.02	0.04	0.02	0.04	0.04	mA
I_{OH}	MAX	-0.8	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-4	-24	mA
I_{OL}	MAX	16	8	20	8	20	20	4	4	4	4	24	mA

PARAMETER	MAX or MIN	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3.3V	ALVC 3V	AUC 1.8V	AUC 2.3V	UNIT
I_{CC}	MAX	0.02	0.08	0.04	0.02	0.08	0.02	0.02	-	0.02	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-24	-24	-24	-24	-24	-8	-8	-6	-12	-24	-24	-8	-9	mA
I_{OL}	MAX	24	24	24	24	24	8	8	6	12	24	24	8	9	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT
t_{PLH}	A or B	Y	MAX	27	15	7	14	5.5	6.6	25	27	30
t_{PHL}	A or B	Y	MAX	19	20	7.5	10	5.5	6.3	25	27	30

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HCT	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT
t_{PLH}	A or B	Y	MAX	38	6.9	8.5	8.7	9	10	12.9	9	9
t_{PHL}	A or B	Y	MAX	38	6.5	7.5	8.7	8.2	10	12.9	9	9

PARAMETER	INPUT	OUTPUT	MAX or MIN	LV 3V	LV 5V	LVC 3.3V	ALVC 3V	AUC 1.8V	AUC 2.3V
t_{PLH}	A or B	Y	MAX	14	9	4.1	2.9	2.3	1.8
t_{PHL}	A or B	Y	MAX	14	9	4.1	2.9	2.3	1.8

UNIT: ns

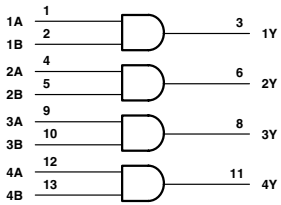
: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

09

QUADRUPLE 2-INPUT POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

● Y = A•B

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	F	SN74 HC	UNIT
I_{CC}	MAX	33	8.8	57	4.2	26.3	15.3	mA
I_{OH}	MAX	-	0.1	0.25	0.1	-	-	mA
V_{OH}	MAX	5.5	5.5	5.5	5.5	5.5	V_{CC}	mA
I_{OL}	MAX	16	8	20	8	20	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	F	SN74 HC
t_{PLH}	A or B	Y	MAX	32	35	10	54	9.6	31
t_{PHL}	A or B	Y	MAX	24	35	10	15	4.8	25

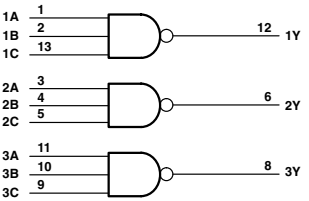
UNIT: ns

10

TRIPLE 3-INPUT POSITIVE-NAND GATES

- $Y = \overline{A \bullet B \bullet C}$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram (SN74)



FUNCTION TABLE (each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC	CD74 AC	UNIT
I_{CC}	MAX	16.5	3.3	27	2.2	13	7.7	0.02	0.04	0.02	0.04	0.04	0.02	0.08	mA
I_{OH}	MAX	-0.4	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-4	-24	-24	-24	mA
I_{OL}	MAX	16	8	20	8	20	20	4	4	4	4	24	24	24	mA

PARAMETER	MAX or MIN	ACT 11	SN74 ACT	CD74 ACT	LV 3V	LV 5V	LVC 3V	ALVC 3V	UNIT
I_{CC}	MAX	0.04	0.04	0.08	-	0.02	0.01	0.01	mA
I_{OH}	MAX	-24	-24	-24	-6	-12	-24	-24	mA
I_{OL}	MAX	24	24	24	6	12	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT
t_{PLH}	A, B or C	Y	MAX	22	15	4.5	11	4.5	6	24	30	19	36
t_{PHL}	A, B or C	Y	MAX	15	15	5	10	4.5	5.3	24	30	19	36

PARAMETER	INPUT	OUTPUT	MAX or MIN	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	LV 3V	LV 5V	LVC 3V	ALVC 3V
t_{PLH}	A, B or C	Y	MAX	6.7	8	12.2	8.9	10	13.5	13.5	9	4.9	3
t_{PHL}	A, B or C	Y	MAX	7	6.5	12.2	8.2	9.5	13.5	13.5	9	4.9	3

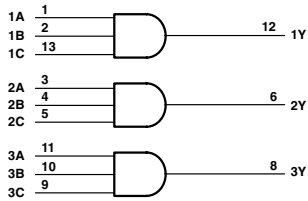
UNIT: ns

: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

TRIPLE 3-INPUT POSITIVE-AND GATES

- Y = A•B•C
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram (SN74)



FUNCTION TABLE (each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC	UNIT
I_{CC}	MAX	6.6	42	3	18	9.7	0.02	0.04	0.02	0.04	0.04	0.02	mA
I_{OH}	MAX	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-4	-24	-24	mA
I_{OL}	MAX	8	20	8	20	20	4	4	4	4	24	24	mA

PARAMETER	MAX or MIN	ACT 11	SN74 ACT	LV 3V	LV 5V	UNIT
I_{CC}	MAX	0.04	0.02	-	0.02	mA
I_{OH}	MAX	-24	-24	-6	-12	mA
I_{OL}	MAX	24	24	6	12	mA

SWITCHING CHARACTERISTICS

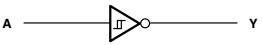
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT
t_{PLH}	A, B or C	Y	MAX	15	7	13	6	6.6	25	30	21	42
t_{PHL}	A, B or C	Y	MAX	20	7.5	10	5.5	6.5	25	30	21	42

PARAMETER	INPUT	OUTPUT	MAX or MIN	AC 11	SN74 AC	ACT 11	SN74 ACT	LV 3V	LV 5V
t_{PLH}	A, B or C	Y	MAX	6.5	8.5	9.6	10.5	14	9
t_{PHL}	A, B or C	Y	MAX	6.9	7.5	8.7	10.5	14	9

UNIT: ns

HEX SCHMITT-TRIGGER INVERTERS

Logic Diagram (SN74)



- $Y = \overline{A}$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 AC	CD74 AC	SN74 ACT	CD74 ACT	AHC	AHCT	UNIT
I_{CC}	MAX	60	21	0.02	0.04	0.02	0.04	0.02	0.08	0.02	0.08	0.02	0.02	mA
I_{OH}	MAX	-0.8	-0.4	-4	-4	-4	-4	-24	-24	-24	-24	-8	-8	mA
I_{OL}	MAX	16	8	4	4	4	4	24	24	24	24	8	8	mA

PARAMETER	MAX or MIN	LV 3V	LV 5V	LVC 3V	ALVC 3V	AUC 1.8V	AUC 2.5V	UNIT
I_{CC}	MAX	-	0.02	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-6	-12	-24	-24	-8	-9	mA
I_{OL}	MAX	6	12	24	24	8	9	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 AC	CD74 AC	SN74 ACT	CD74 ACT
t_{PLH}	A or B	Y	MAX	22	22	31	41	40	57	11	10.5	12.5	14.5
t_{PHL}	A or B	Y	MAX	22	22	31	41	40	57	9.5	10.5	11	9.5

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LV 3V	LV 5V	LVC 3V	ALVC 3V	AUC 1.8V	AUC 2.5V
t_{PLH}	A or B	Y	MAX	12	9	18.5	12	6.4	3.4	3.5	2.7
t_{PHL}	A or B	Y	MAX	12	9	18.5	12	6.4	3.4	3.5	2.7

UNIT: ns

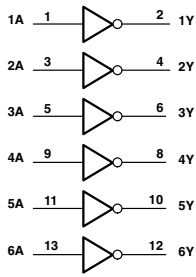
: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

16

HEX INVERTER BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

● $Y = \overline{A}$

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	UNIT
I_{CC}	MAX	51	mA
V_{OH}	MAX	15	V
I_{OL}	MAX	40	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL
t_{PLH}	A	Y	MAX	15
t_{PHL}	A	Y	MAX	23

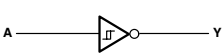
UNIT: ns

17

HEX SCHMITT-TRIGGER BUFFER

● $Y = A$

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	AUC 1.8V	AUC 2.5V	UNIT
I_{CC}	MAX	41	0.01	0.01	mA
I_{OH}	MAX	0.25	-8	-9	mA
I_{OL}	MAX	40	8	9	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	AUC 1.8V	AUC 2.5V
t_{PLH}	A	Y	MAX	15	2.4	1.9
t_{PHL}	A	Y	MAX	26	2.4	1.9

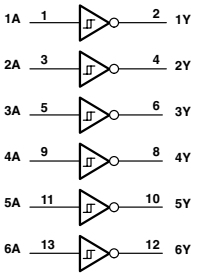
UNIT: ns

19

HEX SCHMITT-TRIGGER INVERTERS

- $Y = \overline{A}$
- P-N-P Input Reduce System Loading (I_{IL} = -0.05mA MAX)
- Excellent Noise Immunity with Typical Hysteresis of 0.8V

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	UNIT
I_{CC}	MAX	30	mA
I_{OH}	MAX	-0.4	mA
I_{OL}	MAX	8	mA

SWITCHING CHARACTERISTICS

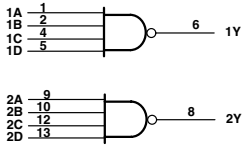
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
t_{PLH}	A or B	Y	MAX	20
t_{PHL}	A or B	Y	MAX	30

UNIT: ns

: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

DUAL 4-INPUT POSITIVE-NAND GATES

Logic Diagram (SN74)



- $Y = \overline{A \bullet B \bullet C \bullet D}$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

FUNCTION TABLE (each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	11	2.2	18	1.5	8.7	5.1	0.02	0.04	0.04	mA
I_{OH}	MAX	-0.4	-0.4	-1	-0.4	-2	-1	-4	-4	-4	mA
I_{OL}	MAX	16	8	20	8	20	20	4	4	4	mA

PARAMETER	MAX or MIN	AC 11	CD74 AC	ACT 11	CD74 ACT	LV 3V	LV 5V	UNIT
I_{CC}	MAX	0.04	0.08	0.04	0.08	-	0.02	mA
I_{OH}	MAX	-24	-24	-24	-24	-6	-12	mA
I_{OL}	MAX	24	24	24	24	6	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT
t_{PLH}	A, B, C or D	Y	MAX	22	15	4.5	11	5	6	28	30	42
t_{PHL}	A, B, C or D	Y	MAX	15	15	5	10	4.5	5.3	28	30	42

PARAMETER	INPUT	OUTPUT	MAX or MIN	AC 11	CD74 AC	ACT 11	CD74 ACT	LV 3V	LV 5V
t_{PLH}	A, B, C or D	Y	MAX	6.7	12.2	9.1	13.5	11.5	8
t_{PHL}	A, B, C or D	Y	MAX	7.3	12.2	9.2	13.5	11.5	8

UNIT: ns

21

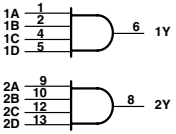
DUAL 4-INPUT POSITIVE-AND GATES

- Y = A•B•C•D
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

FUNCTION TABLE (each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	H
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L

Logic Diagram (SN74)



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	ACT 11	LV 3V	LV 5V	UNIT
I_{CC}	MAX	4.4	2.3	12	7.3	0.02	0.04	0.04	0.04	0.04	-	0.02	mA
I_{OH}	MAX	-0.4	-0.4	-2	-1	-4	-4	-4	-24	-24	-6	-12	mA
I_{OL}	MAX	8	8	20	20	4	4	4	24	24	6	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	ACT 11
t_{PLH}	A, B, C or D	Y	MAX	15	15	6	5.3	28	33	41	8.8	9.8
t_{PHL}	A, B, C or D	Y	MAX	20	10	6	5.5	28	33	41	6.9	8.9

PARAMETER	INPUT	OUTPUT	MAX or MIN	LV 3V	LV 5V
t_{PLH}	A, B, C or D	Y	MAX	12	8
t_{PHL}	A, B, C or D	Y	MAX	12	8

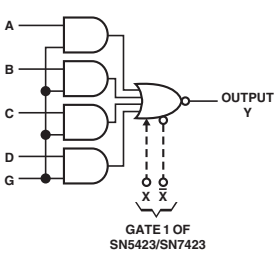
UNIT: ns

25

DUAL 4-INPUT POSITIVE-NOR GATES WITH STROBE

- $Y = \overline{G\,(A + B + C + D)}$

Logic Diagram (SN74)



FUNCTION TABLE (each gate)

INPUTS					OUTPUT
A	B	C	D	G	Y
H	X	X	X	H	L
X	H	X	X	H	L
X	X	H	X	H	L
X	X	X	H	H	L
L	L	L	L	X	H
X	X	X	X	L	H

Expander inputs are open.
H = high level, L = low level, X = irrelevant

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	UNIT
I_{CC}	MAX	19	mA
I_{OH}	MAX	-0.8	mA
I_{OL}	MAX	16	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL
t_{PLH}	A or B	Y	MAX	22
t_{PHL}	A or B	Y	MAX	15

UNIT: ns

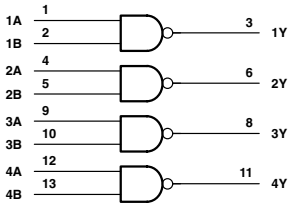
: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

26

QUADRUPLE 2-INPUT HIGH-VOLTAGE INTERFACE POSITIVE-NAND GATES

- $Y = \overline{AB}$

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	UNIT
I_{CC}	MAX	22	4.4	mA
V_{OH}	MAX	15	15	V
I_{OL}	MAX	16	8	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS
t_{PLH}	A or B	Y	MAX	24	32
t_{PHL}	A or B	Y	MAX	17	28

UNIT: ns

27

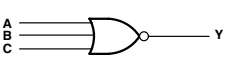
TRIPLE 3-INPUT POSITIVE-NOR GATES

- $Y = \overline{A + B + C}$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

FUNCTION TABLE (each gate)

INPUTS			OUTPUT
A	B	C	Y
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

Logic Diagram (SN74)



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	ACT 11	LV 3V	LV 5V	UNIT
I_{CC}	MAX	26	6.8	4	17.1	12	0.02	0.04	0.04	0.04	0.04	-	0.02	mA
I_{OH}	MAX	-0.8	-0.4	-0.4	-2	-1	-4	-4	-4	-24	-24	-6	-12	mA
I_{OL}	MAX	16	8	8	20	20	4	4	4	24	24	6	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11
t_{PLH}	A, B or C	Y	MAX	15	15	15	5.5	5.5	23	29	35	7.7
t_{PHL}	A, B or C	Y	MAX	11	15	9	4.5	4.5	23	29	35	8.1

PARAMETER	INPUT	OUTPUT	MAX or MIN	ACT 11	LV 3V	LV 5V
t_{PLH}	A, B or C	Y	MAX	10.1	14	9
t_{PHL}	A, B or C	Y	MAX	9.4	14	9

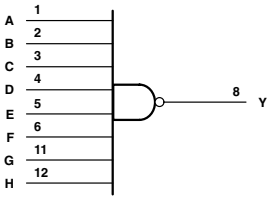
UNIT: ns

30

8-INPUT POSITIVE-NAND GATES

- $Y = \overline{A \bullet B \bullet C \bullet D \bullet E \bullet F \bullet G \bullet H}$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram (SN74)



FUNCTION TABLE

INPUTS A–H	OUTPUT Y
All inputs H	L
One or more inputs L	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	ACT 11	UNIT
I_{CC}	MAX	6	1.1	10	0.9	4.9	4	0.02	0.04	0.04	0.04	0.04	mA
I_{OH}	MAX	-0.4	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-24	-24	mA
I_{OL}	MAX	16	8	20	8	20	20	4	4	4	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	ACT 11
t_{PLH}	A thru H	Y	MAX	22	15	6	10	5	5.5	33	39	42	7.2	8.5
t_{PHL}	A thru H	Y	MAX	15	20	7	12	4.5	5	33	39	42	7.4	8.7

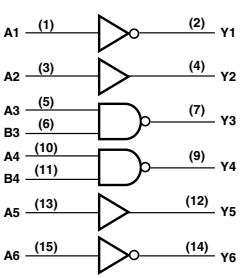
UNIT: ns

31

DELAY ELEMENTS

- Delay Elements for Generating Delay Line
- Inverting and Non-inverting Elements
- Buffer NAND Elements Rated at I_{OL} of 12/24mA
- P-N-P Inputs Reduce Fan-In (I_{IL} = -0.2mA MAX)
- Worst Case MIN/MAX Delays Guaranteed Across Temperature and V_{CC} Range

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	UNIT
I_{CC}		MAX	20	mA
I_{OH}	Y3, Y4 outputs	MAX	-1.2	mA
	All other outputs	MAX	-0.4	mA
I_{OL}	Y3, Y4 outputs	MAX	24	mA
	All other outputs	MAX	8	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
t_{PLH}	A1, A6	Y1, Y6	MAX	65
t_{PHL}				45
t_{PLH}	A2, A5	Y2, Y5	MAX	80
t_{PHL}				95
t_{PLH}	A3, B3	Y3, Y4	MAX	15
t_{PHL}	A4, Y4			15

UNIT: ns

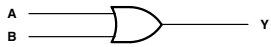
: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

32

QUADRUPLE 2-INPUT POSITIVE-OR GATES

● Y = A + B

Logic Diagram (SN74)



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	UNIT
I_{CC}	MAX	38	9.8	68	4.9	26.6	15.5	0.02	0.04	0.02	0.04	0.04	mA
I_{OH}	MAX	-0.8	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-4	-24	mA
I_{OL}	MAX	16	8	20	8	20	20	4	4	4	4	24	mA

PARAMETER	MAX or MIN	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	ALVC 3V	AUC 1.8V	AUC 2.3V	UNIT
I_{CC}	MAX	0.02	0.08	0.04	0.02	0.08	0.02	0.02	0.02	0.02	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-24	-24	-24	-24	-24	-8	-8	-6	-12	-24	-24	-8	-9	mA
I_{OL}	MAX	24	24	24	24	24	8	8	6	12	24	24	8	9	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT
t_{PLH}	A or B	Y	MAX	15	22	7	14	5.8	6.6	25	27	30
t_{PHL}	A or B	Y	MAX	22	22	7	12	5.8	-	25	27	30

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HCT	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT
t_{PLH}	A or B	Y	MAX	36	6.7	8.5	9.5	9	10	12.1	8.5	9
t_{PHL}	A or B	Y	MAX	36	5.9	7.5	9.5	8	10	12.1	8.5	9

PARAMETER	INPUT	OUTPUT	MAX or MIN	LV 3V	LV 5V	LVC 3V	ALVC 3V	AUC 1.8V	AUC 2.3V
t_{PLH}	A or B	Y	MAX	13	8.5	3.8	2.8	2.5	2.1
t_{PHL}	A or B	Y	MAX	13	8.5	3.8	2.8	2.5	2.1

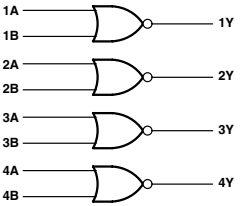
UNIT: ns

33

QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS WITH OPEN-COLLECTOR OUTPUTS

● $Y = \overline{A + B}$

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	UNIT
I_{CC}	MAX	16.5	13.8	9	mA
V_{OH}	MAX	5.5	5.5	5.5	V
I_{OL}	MAX	48	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS
t_{PLH}	A or B	Y	MAX	15	32	33
t_{PHL}	A or B	Y	MAX	18	28	12

UNIT: ns

34

HEX BUFFER GATE

● Y = A

Logic Diagram

FUNCTION TABLE (each gate)

INPUT A	OUTPUT Y
H	H
L	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AUC 1.8V	AUC 2.5V	UNIT
I_{CC}	MAX	0.01	0.01	mA
I_{OH}	MAX	-8	-9	mA
I_{OL}	MAX	8	9	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AUC 1.8V	AUC 2.5V
t_{PLH}	A	Y	MAX	2.4	1.8
t_{PHL}				2.4	1.8

UNIT: ns

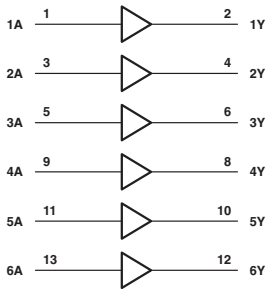
: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

35

HEX NONINVERTERS WITH OPEN-COLLECTOR OUTPUTS

● Y = A

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	UNIT
I_{CC}	MAX	63	mA
V_{OH}	MAX	5.5	V
I_{OL}	MAX	8	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
t_{PLH}	A	Y	MAX	50
t_{PHL}	A	Y	MAX	14

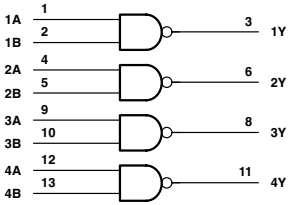
UNIT: ns

37

QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS

● $Y = \overline{A \bullet B}$

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	F	UNIT
I_{CC}	MAX	54	12	80	7.8	33	mA
I_{OH}	MAX	-1.2	-1.2	-3	-2.6	-15	mA
I_{OL}	MAX	48	24	60	24	64	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	F
t_{PLH}	A or B	Y	MAX	22	24	6.5	8	6.5
t_{PHL}	A or B	Y	MAX	15	24	6.5	7	5

UNIT: ns

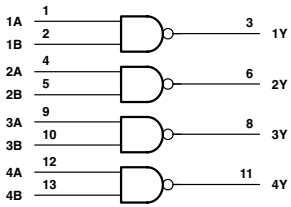
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

38

QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS WITH OPEN-COLLECTOR OUTPUTS

● $Y = \overline{A \bullet B}$

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	F	UNIT
I_{CC}	MAX	54	12	80	7.8	30	mA
V_{OH}	MAX	5.5	5.5	5.5	5.5	4.5	V
I_{OL}	MAX	48	24	60	24	64	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	F
t_{PLH}	A or B	Y	MAX	22	32	10	33	13
t_{PHL}	A or B	Y	MAX	18	28	10	12	5.5

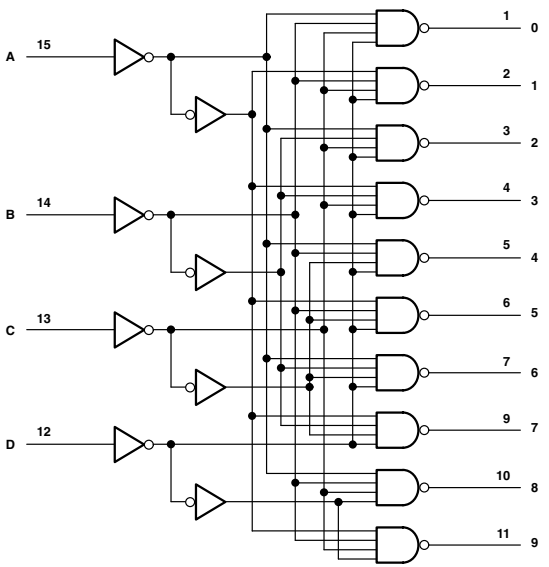
UNIT: ns

42

4-LINE-TO-10-LINE DECODERS (1 of 10)

- All Outputs Are High for Invalid Input Conditions
- Also for Applications as
  - 3-Line to 8-Line Decoders
  - 4-Line to 16-Line Decoders
- Full Decoding of Valid Input Logic Ensures That All Inputs Remain Off for All Invalid Input Conditions

Logic Diagram (SN74)



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE (SN74)

No.	INPUTS				OUTPUTS								
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	56	13	0.08	0.16	0.16	mA
I_{OH}	MAX	-0.8	-0.4	-4	-4	-4	mA
I_{OL}	MAX	16	8	4	4	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INTPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT
t_{PLH} 2Level · Logic	A, B, C or D	0-9	MAX	25	25	38	45	53
t_{PHL} 2Level · Logic		0-9		25	25	38	45	53
t_{PLH} 3Level · Logic	A, B, C or D	0-9	MAX	30	30	38	45	53
t_{PHL} 3Level · Logic		0-9		30	30	38	45	53

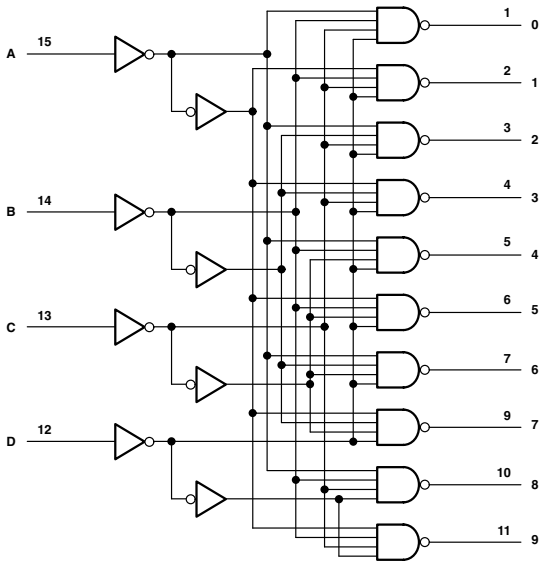
UNIT: ns

45

BCD-TO-DECIMAL DECODERS/DRIVERS

- 80-mA Sink-Current Capability
- All Outputs Are Off for Invalid BCD Input Conditions

Logic Diagram (SN74)



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

No.	INPUTS				OUTPUTS								
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING C

PARAMETER	MAX or MIN	TTL	UNIT
I_{CC}	MAX	70	mA
V_O (on)	MAX	0.9	V
I_{OL}	MAX	80	mA

SWITCHING CHARACTERISTICS

PARAMETER	MAX or MIN	TTL
t_{PLH}	MAX	25
t_{PHL}		25

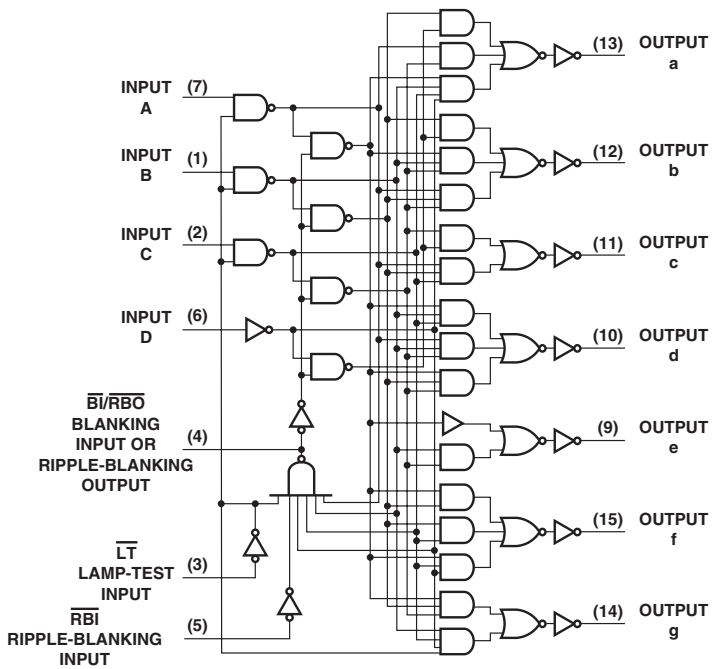
UNIT: ns

47

BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

- Open-Collector Outputs
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

No.	INPUTS						OUTPUTS						
	$\overline{LT}$	$\overline{RBI}$	D	C	B	A	$\overline{BI}/\overline{RBO}$†	a	b	c	d	e	f	g
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON
6	H	X	L	H	H	L	H	OFF	OFF	ON	ON	ON	ON	ON
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON
9	H	X	H	L	L	H	H	ON	ON	ON	OFF	OFF	ON	ON
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON

H = high level, L = low level, irrelevant

NOTES: 1. The blanking input ($\overline{BI}$) must be open held at high logic level when output functions 0 through 15 are desired. The ripple-blanking input ($\overline{RBI}$) must be open or high it blanking of a decimal zero is not desired.

2. When a low logic level is applied directly to the blanking input ($\overline{BI}$), all segment outputs are off regardless of the level of any other input.

3. When ripple-blanking input ($\overline{RBI}$) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go off and the ripple-blanking input/ripple blanking output ($\overline{BI}/\overline{RBI}$) is open or held high and a low is applied to the lamp-test input, all segment outputs are on.

† $\overline{BI}/\overline{RBO}$ is wire AND logic serving as blanking input ($\overline{BI}$) and/or ripple-blanking output ($\overline{RBI}$).

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	UNIT
I_{CC}	MAX	103	13	mA
I_{OH}	MAX	-0.2	-0.05	mA
I_{OL}	MAX	8	3.2	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS
t_{off}	A	A to g	MAX	100	100
t_{on}	A	A to g	MAX	100	100
t_{off}	$\overline{RBI}$	A to g	MAX	100	100
t_{on}	$\overline{RBI}$	A to g	MAX	100	100

UNIT: ns

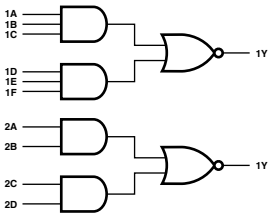
51

AND-OR-INVERT GATES

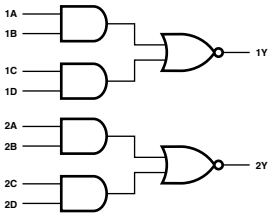
- '51, 'S51: $Y = \overline{AB + CD}$
- 'F51, 'LS51: $1Y = \overline{(1A \bullet 1B \bullet 1C) + (1D \bullet 1E \bullet 1F)}$
- 'HC51: $2Y = \overline{(2A \bullet 2B) + (2C \bullet 2D)}$

Logic Diagram

LS51



S51



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	F	SN74 HC	UNIT
I_{CC}	MAX	14	2.8	22	7.5	0.08	mA
I_{OH}	MAX	-0.4	-0.4	-1	-1	-4	mA
I_{OL}	MAX	16	8	20	20	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	F	SN74 HC
t_{PLH}	Any	Y	MAX	22	20	5.5	6.5	35
t_{PHL}	Any	Y	MAX	15	20	5.5	4.5	35

UNIT: ns

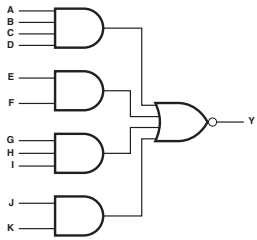
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

64

4-2-3-2 INPUT AND-OR INVERT GATES

● $Y = \overline{ABCD + EF + GHI + JK}$

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	S	F	UNIT
I_{CC}	MAX	16	4.7	mA
I_{OH}	MAX	-1	-1	mA
I_{OL}	MAX	20	20	mA

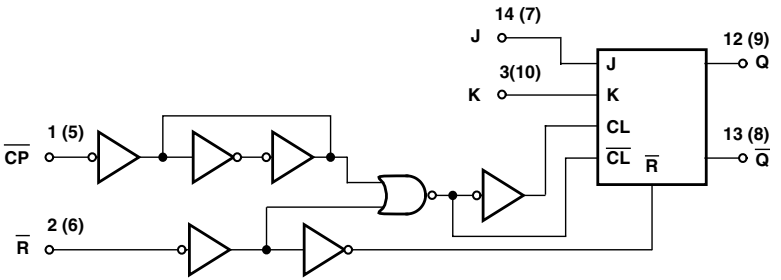
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	S	F
t_{PLH}	Any	Y	MAX	5.5	7
t_{PHL}	Any	Y	MAX	5.5	5.5

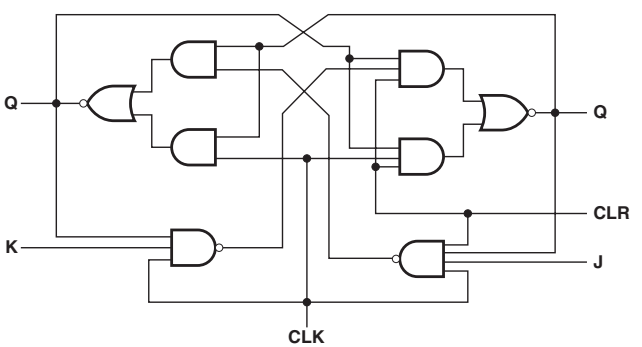
UNIT: ns

DUAL J-K FLIP-FLOPS WITH CLEAR

Logic Diagram



CD74HC/HCT73



SN74LS73

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE (SN74)

INPUTS				OUTPUTS	
$\overline{CLEAR}$	CLOCK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\overline{Q_0}$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\overline{Q_0}$

TRUTH TABLE (CD74)

INPUTS				OUTPUTS	
$\overline{R}$	$\overline{CP}$	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	No Change	
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	H	X	X	No Change	

NOTE:
H = High Level (Steady State)
L = Low Level (Steady State)
X = Irrelevant
↓ = High-to-Low Transition

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	20	6	0.04	0.08	0.08	mA
I_{OH}	MAX	16	8	4	4	4	mA
I_{OL}	MAX	-0.4	-0.4	-4	-4	-4	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT
fmax				MIN	15	30	25	20	20
tw	CLOCK"L"			MIN	20	-	20	-	-
	CLOCK"H"				47	20	20	-	-
	$\overline{CP}$ Pulse Wide				-	-	-	24	24
	$\overline{CLEAR}$ "L"				25	20	20	24	27
tsu	CLK			MIN	0 ↑	20 ↓	25 ↓	-	-
	J,K to $\overline{CP}$				-	-	-	24	24
th	CLK			MIN	0 ↓	0 ↓	0 ↓	-	-
	J,K to $\overline{CP}$				-	-	-	3	3
t_{PLH}		$\overline{CLEAR}$	$\overline{Q}$	MAX	25	20	39	44	51
t_{PHL}					-	20	39	44	51
t_{PLH}		$\overline{CLEAR}$	Q	MAX	-	20	39	44	51
t_{PHL}					40	20	39	44	51
t_{PLH}		CLOCK	Q or $\overline{Q}$	MAX	25	20	32	-	-
t_{PHL}					40	20	32	-	-
t_{PLH}		$\overline{CP}$	Q	MAX	-	-	-	48	57
t_{PHL}					-	-	-	48	57
t_{PLH}		$\overline{CP}$	$\overline{Q}$	MAX	-	-	-	48	54
t_{PHL}					-	-	-	48	54

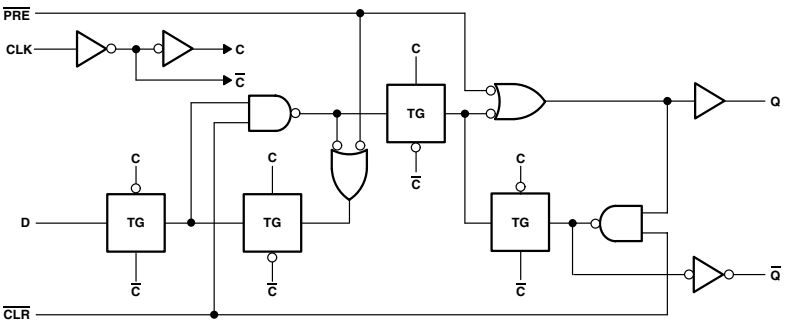
UNIT fmax : MHz, other : ns

74

DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram (SN74)



FUNCTION TABLE (SN74)

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLOCK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q_0}$

† This configuration is unstable; that is, it does not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC	UNIT
I_{CC}	MAX	15	8	25	4	16	16	0.04	0.08	0.04	0.08	0.04	0.02	mA
I_{OH}	MAX	-0.4	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-4	-24	-24	mA
I_{OL}	MAX	16	8	20	8	20	20	4	4	4	4	24	24	mA

PARAMETER	MAX or MIN	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	AUC 1.8V	AUC 2.5V	UNIT
I_{CC}	MAX	0.08	0.04	0.02	0.08	0.02	0.02	-	0.02	0.01	0.01	0.01	mA
I_{OH}	MAX	-24	-24	-24	-24	-8	-8	-6	-12	-24	-8	-9	mA
I_{OL}	MAX	24	24	24	24	8	8	6	12	24	8	9	mA

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC
fmax				MIN	15	25	75	34	105	100	25	20
tw	CLOCK"H"			MIN	30	25	6	14.5	4	4	20	24
	CLOCK"L"			MIN	37	-	7.3	14.5	5.5	5	20	24
	$\overline{PRE}$, $\overline{CLR}$ "L"			MIN	30	25	7	15	4	4	25	24
tsu	DATA			MIN	20	20	3	15	4.5	3	25	18
	$\overline{PRE}$, $\overline{CLR}$ INACTIVE			MIN	20	-	-	10	2	2	6	-
th				MIN	5	5	2	0	0	1	0	3
t_{PLH}		$\overline{PRE}$	Q or $\overline{Q}$	MAX	25	25	6	13	7.5	7.1	58	60
t_{PHL}					40	40	13.5	15	10.5	10.5	58	60
t_{PLH}		$\overline{CLR}$	Q or $\overline{Q}$	MAX	25	25	6	13	7.5	7.1	58	60
t_{PHL}					40	40	13.5	15	10.5	10.5	58	60
t_{PLH}		CLOCK	Q or $\overline{Q}$	MAX	25	25	9	16	8	7.8	44	53
t_{PHL}					40	40	9	18	9	9.2	44	53

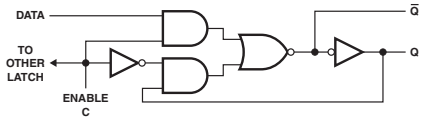
PARAMETER		INPUT	OUTPUT	MAX or MIN	SN74 HCT	CD74 HCT	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT
fmax				MIN	22	16	125	125	110	100	125	85
tw	CLOCK"H"			MIN	23	27	4	5	4.5	5	6	5.7
	CLOCK"L"			MIN	23	27	4	5	4.5	5	6	5.7
	$\overline{PRE}$, $\overline{CLR}$ "L"			MIN	20	24	4	5	4	5	6	5
tsu	DATA			MIN	15	18	3.5	3	3.5	4.5	3.5	4
	$\overline{PRE}$, $\overline{CLR}$ INACTIVE			MIN	0	-	1	0	-	2	0	-
th				MIN	0	3	0	0.5	0	0	1	0
t_{PLH}		$\overline{PRE}$	Q or $\overline{Q}$	MAX	44	60	7.1	10	10.5	9.6	10.5	11.5
t_{PHL}					44	60	9	10.5	11.5	12.5	11.5	12.5
t_{PLH}		$\overline{CLR}$	Q or $\overline{Q}$	MAX	44	60	7.1	10	10.5	9.6	10.5	11.5
t_{PHL}					44	60	9	10.5	11.5	12.5	11.5	12.5
t_{PLH}		CLOCK	Q or $\overline{Q}$	MAX	35	53	8.2	10.5	10	9.4	13.0	9.5
t_{PHL}					35	53	7.5	10.5	10	8.8	11.5	9.5

PARAMETER		INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LV 3V	LV 5V	LVC 3V	AUC 1.8V	AUC 2.5V
fmax				MIN	75	65	45	75	100	300	350
tw	CLOCK"H"			MIN	5	5	7	5	3.3	0.5	0.5
	CLOCK"L"			MIN	5	5	7	5	3.3	0.5	0.5
	$\overline{PRE}$, $\overline{CLR}$ "L"			MIN	5	5	7	5	3.3	1.5	1.5
tsu	DATA			MIN	5	5	7	5	3	0.6	0.7
	$\overline{PRE}$, $\overline{CLR}$ INACTIVE			MIN	3	3.5	5	3	2	0.2	0.3
th				MIN	0.5	0	0.5	0.5	0	0.3	0.3
t_{PLH}		$\overline{PRE}$	Q or $\overline{Q}$	MAX	11	13	18	11	5.4	3.1	2.5
t_{PHL}					11	13	18	11	5.4	3.1	2.5
t_{PLH}		$\overline{CLR}$	Q or $\overline{Q}$	MAX	11	13	18	11	5.4	3	2.4
t_{PHL}					11	13	18	11	5.4	3	2.4
t_{PLH}		CLOCK	Q or $\overline{Q}$	MAX	10.5	10	17.5	10.5	5.2	2.8	2.2
t_{PHL}					10.5	10	17.5	10.5	5.2	2.8	2.2

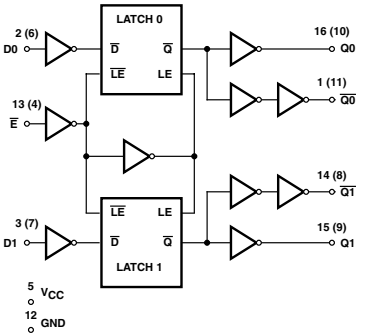
UNIT fmax : MHz, other : ns

4-BIT BISTABLE LATCHES

Logic Diagram



SN74LS75



CD74HC/HCT75

FUNCTION TABLE (SN74)

INPUTS		OUTPUTS	
D	C	Q	Q̄
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q_0}$

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	53	12	0.04	0.08	0.08	mA
I_{OH}	MAX	-0.4	-0.4	-4	-4	-4	mA
I_{OL}	MAX	16	8	4	4	4	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

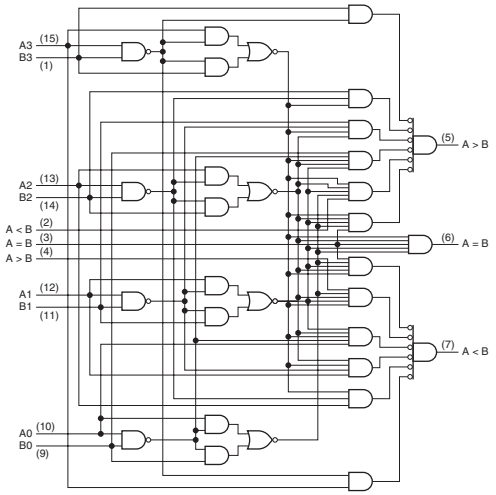
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT
tw			MIN	20	20	20	24	24
tsu			MIN	20	20	25	18	18
th			MIN	5	5	5	3	3
t_{PLH}	D	Q	MAX	30	27	30	33	42
t_{PHL}				25	17	30	33	42
t_{PLH}	D	$\overline{Q}$	MAX	40	20	30	39	42
t_{PHL}				15	15	30	39	42
t_{PLH}	G	Q	MAX	30	27	33	39	42
t_{PHL}				15	25	33	39	42
t_{PLH}	G	$\overline{Q}$	MAX	30	30	33	39	45
t_{PHL}				15	15	33	39	45

UNIT: ns

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

4-BIT MAGNITUDE COMPARATORS

Logic Diagram (SN74)



FUNCTION TABLE (SN74)

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A>B	A<B	A=B	A>B	A<B	A=B
A3>B3	X	X	X	X	X	X	H	L	L
A3<B3	X	X	X	X	X	X	L	H	L
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2<B2	X	X	X	X	X	L	H	L
A3=B3	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	H	L	L	H	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	H	L	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	H	H	L	L	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	L	H	H	L
A3=B3	A2=B2	A1=B1	A0=B0	X	X	H	L	L	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	88	20	115	0.08	0.16	0.16	mA
I_{OH}	MAX	-0.4	-0.4	-1	-4	-4	-4	mA
I_{OL}	MAX	16	8	20	4	4	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	Number of Gate Levels	MAX or MIN	TTL	LS	S	SN74 HC	CD74 HC	CD74 HCT
t_{PLH}	Any A or B data input	A < B, A > B	3	MAX	26	36	16	58	59	56
		A = B	4	MAX	35	45	18	50	53	60
t_{PHL}	Any A or B data input	A < B, A > B	3	MAX	30	30	16.5	58	59	56
		A = B	4	MAX	30	45	16.5	50	53	60
t_{PLH}	A < B, A = B	A > B	1	MAX	11	22	7.5	44	42	45
t_{PHL}	A < B, A = B	A > B	1		17	17	8.5	44	42	45
t_{PLH}	A = B	A = B	2	MAX	20	20	10.5	37	-	-
t_{PHL}	A = B	A = B	2		17	26	7.5	37	-	-
t_{PLH}	A > B, A = B	A < B	1	MAX	11	22	7.5	44	42	45
t_{PHL}	A > B, A = B	A < B	1		17	17	8.5	44	42	45

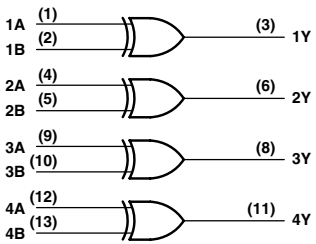
UNIT: ns

86

QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

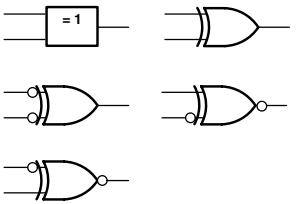
- $Y = A \oplus B$ or $Y = \overline{A}B + A\overline{B}$
- 74AC11xxx : Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram (SN74)



An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

Exclusive OR



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	SN74 AC	CD74 AC	ACT 11	UNIT
I_{CC}	MAX	50	10	75	5.9	38	28	0.02	0.04	0.04	0.04	0.02	0.08	0.04	mA
I_{OH}	MAX	16	8	20	8	20	20	4	4	4	24	24	24	24	mA
I_{OL}	MAX	-0.8	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-24	-24	-24	-24	mA

PARAMETER	MAX or MIN	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	UNIT
I_{CC}	MAX	0.04	0.08	0.02	0.02	-	0.02	0.01	mA
I_{OH}	MAX	24	24	-10	8	6	12	24	mA
I_{OL}	MAX	-24	-24	10	-8	-6	-12	-24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11
t_{PLH} Input Low	A or B	Y	MAX	23	23	10.5	17	7.5	6.5	25	36	48	7.6
t_{PHL} Input Low		Y	MAX	17	17	10	12	6.5	6.5	25	36	48	6.8
t_{PLH} Input High	A or B	Y	MAX	30	30	10.5	17	6.5	8	25	36	48	7.6
t_{PHL} Input High		Y	MAX	22	22	10	10	7	7.5	25	36	48	6.8

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V
t_{PLH} Input Low	A or B	Y	MAX	9	10.8	9.6	10	14.6	10	10	16.5	10	4.6
t_{PHL} Input Low		Y	MAX	9.5	10.8	9	10.5	14.6	10	10	16.5	10	4.6
t_{PLH} Input High	A or B	Y	MAX	9	10.8	9.6	10	14.6	10	10	16.5	10	4.6
t_{PHL} Input High		Y	MAX	9.5	10.8	9	10.5	14.6	10	10	16.5	10	4.6

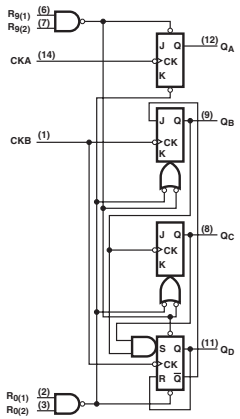
UNIT: ns

: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

90

DECADE COUNTER

Logic Diagram



FUNCTION TABLE

BCD COUNT SEQUENCE

Count	OUTPUTS			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BI-QUINARY

Count	OUTPUTS			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

RESET/COUNT

RESET INPUTS				OUTPUTS			
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	Count			
L	X	L	X	Count			
L	X	X	L	Count			
X	L	L	X	Count			

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	UNIT
I_{CC}	MAX	39	15	mA
I_{OH}	MAX	-0.8	-0.4	mA
I_{OL}	MAX	16	8	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS
fmax		A	QA	MIN	32	32
		B	QB		16	16
tw	A			MIN	15	15
	B				30	30
	RESET				15	30
tsu	RESET INACTIVE			MIN	25	25
t_{PLH}		A	QA	MAX	16	16
t_{PHL}					18	18
t_{PLH}		A	QD	MAX	48	48
t_{PHL}					50	50
t_{PLH}		B	QB	MAX	16	16
t_{PHL}					21	21
t_{PLH}		B	QC	MAX	32	32
t_{PHL}					35	35
t_{PLH}		B	QC	MAX	32	32
t_{PHL}					35	35
t_{PHL}		Set to 0	Any	MAX	40	40
t_{PLH}		Set to 9	QA, QD	MAX	30	30
t_{PHL}			QB, QC		40	40

UNIT fmax : MHz, other : ns

DIVIDE-BY-TWELVE DECODE COUNTERS

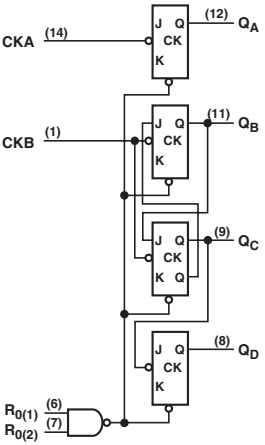
FUNCTION TABLE
COUNT SEQUENCE

COUNT	OUTPUTS			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

RESET/COUNT

RESET INPUTS		OUTPUTS
$R0_{(1)}$	$R0_{(2)}$	Q_D Q_C Q_B Q_A
H	H	L L L L
L	X	COUNT
X	L	COUNT

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	UNIT
I_{CC}	MAX	39	15	mA
I_{OH}	MAX	-0.8	-0.4	mA
I_{OL}	MAX	16	8	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

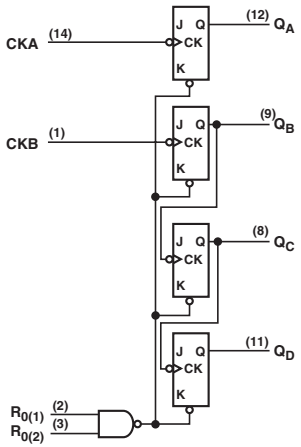
PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS
fmax		A	QA	MIN	32	32
		B	QB		16	16
tw	A			MIN	15	15
	B				30	30
	RESET				15	30
tsu	RESET INACTIVE			MIN	25	25
t_{PLH}		A	QA	MAX	16	16
t_{PHL}					18	18
t_{PLH}		A	QD	MAX	48	48
t_{PHL}					50	50
t_{PLH}		B	QB	MAX	16	16
t_{PHL}					21	21
t_{PLH}		B	QC	MAX	16	16
t_{PHL}					21	21
t_{PLH}		B	QD	MAX	32	32
t_{PHL}					35	35
t_{PHL}		Set to 0	Any	MAX	40	40

UNIT fmax : MHz, other : ns

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

4-BIT BINARY COUNTERS

Logic Diagram (SN74)



FUNCTION TABLE (SN74)
COUNT SEQUENCE

COUNT	OUTPUTS			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

RESET/COUNT

RESET INPUTS		OUTPUTS
R0(1)	R0(2)	Q_D Q_C Q_B Q_A
H	H	L L L L
L	X	COUNT
X	L	COUNT

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	39	15	0.16	0.16	mA
I_{OH}	MAX	-0.8	-0.4	-4	-4	mA
I_{OL}	MAX	16	8	4	4	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	CD74 HC	CD74 HCT
fmax		A (CD74:$\overline{CP0}$)	QA (CD74:Q_0)	MIN	32	32	20	20
		B (CD:74$\overline{CP1}$)	QB (CD74:Q_1)		16	16	20	20
tw	A ($\overline{CP0}$)			MIN	15	15	24	24
	B ($\overline{CP1}$)				30	30	24	24
	RESET				15	30	24	24
tsu	RESET INACTIVE			MIN	25	25	-	-
t_{PLH}		CKA ($\overline{CP0}$)	QA (Q_0)	MAX	16	16	38	51
t_{PHL}					18	18	38	51
t_{PLH}		CKA ($\overline{CP0}$)	QD (Q_3)	MAX	70	70	-	-
t_{PHL}					70	70	-	-
t_{PLH}		CKB ($\overline{CP1}$)	QB (Q_1)	MAX	16	16	41	51
t_{PHL}					21	21	41	51
t_{PLH}		CKB ($\overline{CP1}$)	QC (Q_2)	MAX	32	32	56	69
t_{PHL}					35	35	56	69
t_{PLH}		CKB ($\overline{CP1}$)	QD (Q_3)	MAX	51	51	74	87
t_{PHL}					51	51	74	87
t_{PHL}		Set to 0	ANY	MAX	40	40	-	-

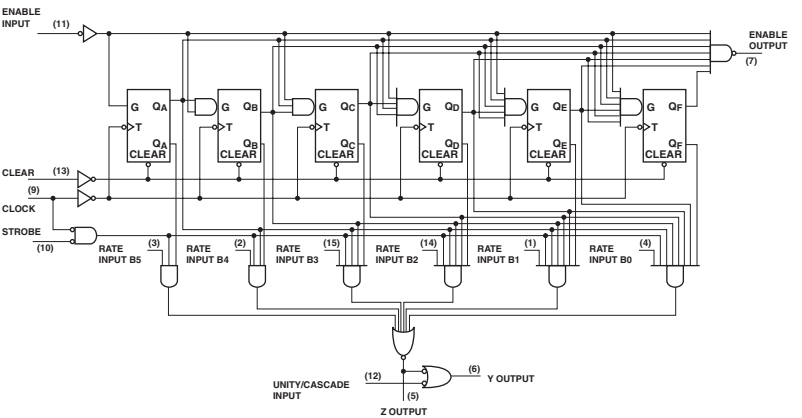
UNIT fmax : MHz, other : ns

97

SYNCHRONOUS 6-BIT BINARY RATE MULTIPLIERS

- Perform Fixed-Rate or Variable-Rate Frequency Division
- Typical Maximum Clock Frequency: 32MHz

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS					OUTPUTS		
					LOGI LEVEL OR NUMBER OF PULSES		
CLEAR	ENABLE	STROBE	BINARY RATE B_5 B_4 B_3 B_2 B_1 B_0	NUMBER OF CLOCK PULSES	UNITY/ CASCADE	Y	Z	ENABLE
H	X	H	X X X X X X	X	H	L	H	H
L	L	L	L L L L L L	64	H	L	H	1
L	L	L	L L L L L H	64	H	1	1	1
L	L	L	L L L L H L	64	H	2	2	1
L	L	L	L L L H L L	64	H	4	4	1
L	L	L	L L H L L L	64	H	8	8	1
L	L	L	L H L L L L	64	H	16	16	1
L	L	L	H L L L L L	64	H	32	32	1
L	L	L	H H H H H H	64	H	63	63	1
L	L	L	H H H H H H	64	L	H	63	1
L	L	L	H L H L L L	64	H	40	40	1

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

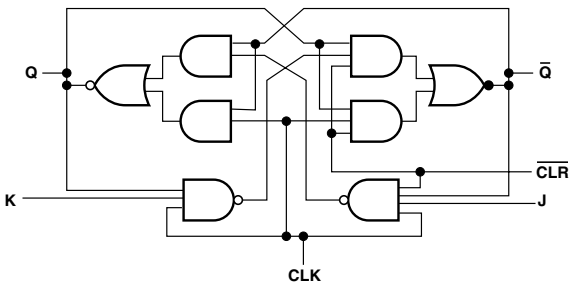
PARAMETER	MAX or MIN	TTL	UNIT
I_{CC}	MAX	120	mA
I_{OH}	MAX	16	mA
I_{OL}	MAX	-0.4	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

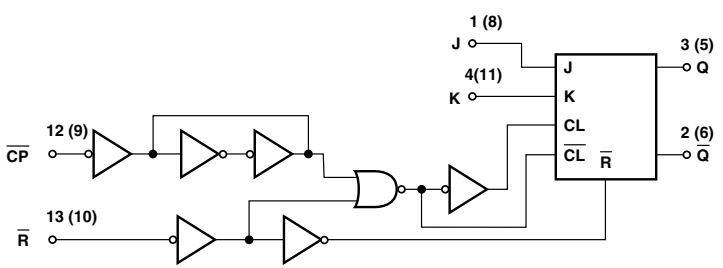
PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL
fmax		A	QA	MIN	25
tw	CLK			MIN	20
	CLR			MIN	15
tsu	Positive			MIN	25
	Negative			MIN	0
th	Positive			MIN	0
	Negative			MIN	20
t_{PLH}		ENABLE	ENABLE	MAX	20
t_{PHL}				MAX	21
t_{PLH}		STRB	Z	MAX	18
t_{PHL}				MAX	23
t_{PLH}		CLK	Y	MAX	39
t_{PHL}				MAX	30
t_{PLH}		CLK	Z	MAX	18
t_{PHL}				MAX	26
t_{PLH}		RATE	Z	MAX	10
t_{PHL}				MAX	14
t_{PLH}		UNITY /CAS	Y	MAX	14
t_{PHL}				MAX	10
t_{PLH}		STRB	Y	MAX	30
t_{PHL}				MAX	33
t_{PLH}		CLK	ENABLE	MAX	30
t_{PHL}				MAX	33
t_{PLH}		CLR	Y	MAX	36
t_{PHL}			Z	MAX	23
t_{PLH}		RATE	Y	MAX	23
t_{PHL}				MAX	23

UNIT fmax : MHz, other : ns

Logic Diagram
SN74LS



Logic Diagram
CD74HC/HCT



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLES
(SN74LS107A)

INPUTS				OUTPUTS	
$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_O	$\overline{Q_O}$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_O	$\overline{Q_O}$

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	20	6	0.04	0.08	0.08	mA
I_{OH}	MAX	-0.4	-0.4	-4	-4	-4	mA
I_{OL}	MAX	16	8	4	4	4	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

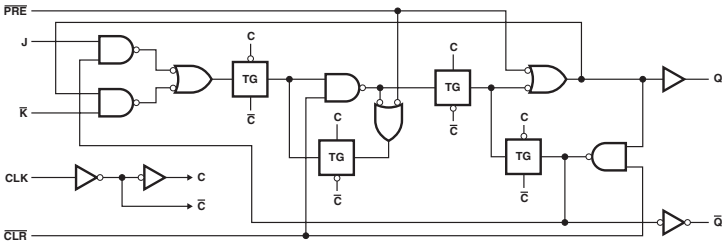
PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT
fmax				MIN	15	30	25	20	19
tw	CLK H			MIN	20	20	20	-	-
	CLK L			MIN	47	-	20	-	-
	$\overline{CP}$			MIN	-	-	-	24	27
	$\overline{CLR}$ L (or $\overline{R}$)			MIN	25	25	20	24	36
tsu	J, K			MIN	0	20	25	30	30
	$\overline{CLR}$ INACTIVE			MIN	0	25	25	-	-
th				MIN	0	0	0	3	5
t_{PLH}		$\overline{CLR}$ (or $\overline{R}$)	$\overline{Q}$	MAX	25	20	39	47	57
t_{PHL}			Q	MAX	40	20	39	47	57
t_{PLH}		CLK	$\overline{Q}$	MAX	25	20	32	-	-
t_{PHL}			Q	MAX	40	20	32	-	-
t_{PLH}		$\overline{CP}$	Q	MAX	-	-	-	51	65
t_{PHL}				MAX	-	-	-	51	65
t_{PLH}		$\overline{CP}$	$\overline{Q}$	MAX	-	-	-	51	60
t_{PHL}				MAX	-	-	-	51	60

UNIT fmax : MHz, other : ns

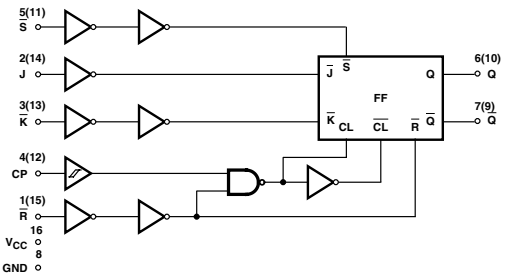
109

DUAL J-$\overline{K}$ POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

Logic Diagram
SN74, CD74AC/ACT



Logic Diagram
CD74HC/HCT



FUNCTION TABLE
(SN74, CD74AC/ACT)

INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLOCK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	$\overline{Q_0}$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q_0}$

† The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH}. Furthermore, this configuration is nonstable; that is, it will not persist when either $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	UNIT
I_{CC}	MAX	15	8	4	17	17	0.04	0.08	0.08	0.08	0.08	mA
I_{OH}	MAX	-0.8	-0.4	-0.4	-2	-1	-4	-4	-4	-24	-24	mA
I_{OL}	MAX	16	4	8	20	20	4	4	4	24	24	mA

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

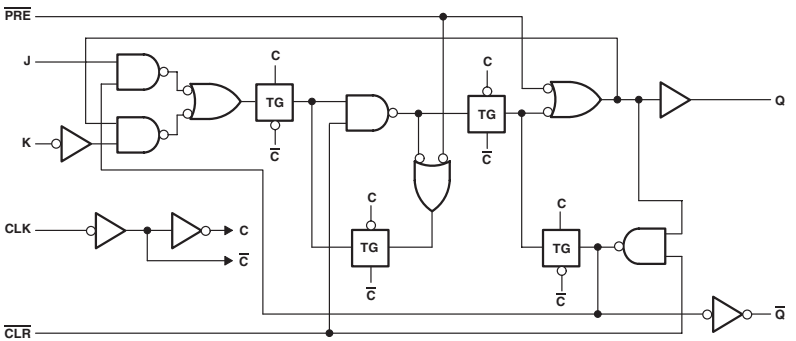
PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT
fmax				MIN	25	25	34	105	90	25	20	18
tw	CLK H			MIN	20	25	14.5	4	4	20	-	-
	CLK L			MIN	20	-	14.5	5.5	5	20	-	-
	$\overline{CP}$			MIN	-	-	-	-	-	-	24	27
	$\overline{PRE}$ L			MIN	20	25	15	4	4	25	-	-
	$\overline{CLR}$ L			MIN	20	25	15	4	4	25	-	-
	$\overline{R}$			MIN	-	-	-	-	-	-	24	27
tsu	J, $\overline{K}$			MIN	10	25	15	5.5	3	25	-	-
	$\overline{PRE}$, $\overline{CLR}$			MIN	10	-	10	2	2	6	-	-
	J, K to $\overline{CP}$			MIN	-	-	-	-	-	-	24	27
th				MIN	6	5	0	0	1	0	3	3
t_{PLH}		$\overline{PRE}$	Q	MAX	15	25	13	8	8	58	-	-
t_{PHL}			$\overline{Q}$	MAX	35	40	15	10.5	10.5	58	-	-
t_{PLH}		$\overline{CLR}$	$\overline{Q}$	MAX	15	25	13	8	8	58	-	-
t_{PHL}			Q	MAX	25	40	15	10.5	10.5	58	-	-
t_{PLH}		CLK	$\overline{Q}$,Q	MAX	16	25	16	9	8	44	-	-
t_{PHL}				MAX	28	40	18	9	9.2	44	-	-
t_{PLH}		$\overline{CP}$	Q	MAX	-	-	-	-	-	-	53	60
t_{PHL}				MAX	-	-	-	-	-	-	53	60
t_{PLH}		$\overline{CP}$	$\overline{Q}$	MAX	-	-	-	-	-	-	53	60
t_{PHL}				MAX	-	-	-	-	-	-	53	60
t_{PLH}		$\overline{R}$	Q	MAX	-	-	-	-	-	-	56	68
t_{PHL}				MAX	-	-	-	-	-	-	56	68
t_{PLH}		$\overline{R}$	$\overline{Q}$	MAX	-	-	-	-	-	-	51	56
t_{PHL}				MAX	-	-	-	-	-	-	51	56

PARAMETER		INPUT	OUTPUT	MAX or MIN	CD74 AC	CD74 ACT
fmax				MIN	100	100
tw	CLK H			MIN	5	5
	CLK L			MIN	5	5
	$\overline{CP}$			MIN	-	-
	$\overline{PRE}$ L			MIN	4.5	5.5
	$\overline{CLR}$ L			MIN	4.5	5.5
	$\overline{R}$			MIN	-	-
tsu	J, $\overline{K}$			MIN	5.5	5.5
	$\overline{PRE}$, $\overline{CLR}$			MIN	-	5.5
	J, K to $\overline{CP}$			MIN	-	-
th				MIN	0	0
t_{PLH}		$\overline{PRE}$	Q	MAX	12.2	12.2
t_{PHL}			$\overline{Q}$	MAX	12.2	12.2
t_{PLH}		$\overline{CLR}$	$\overline{Q}$	MAX	12.2	12.2
t_{PHL}			Q	MAX	12.2	12.2
t_{PLH}		CLK	$\overline{Q}$,Q	MAX	10.3	10.3
t_{PHL}				MAX	10.3	10.3
t_{PLH}		$\overline{CP}$	Q	MAX	-	-
t_{PHL}				MAX	-	-
t_{PLH}		$\overline{CP}$	$\overline{Q}$	MAX	-	-
t_{PHL}				MAX	-	-
t_{PLH}		$\overline{R}$	Q	MAX	-	-
t_{PHL}				MAX	-	-
t_{PLH}		$\overline{R}$	$\overline{Q}$	MAX	-	-
t_{PHL}				MAX	-	-

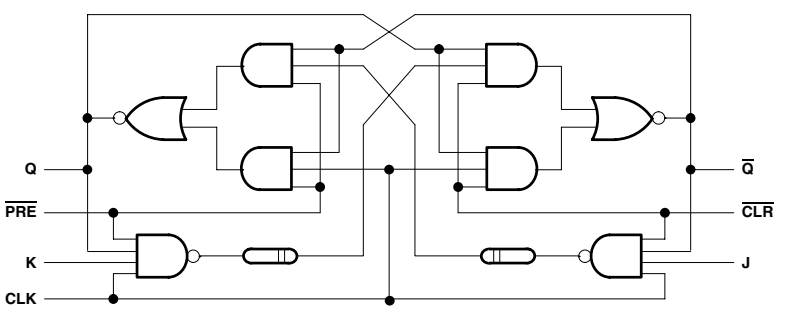
UNIT fmax : MHz, other : ns

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

Logic Diagram (SN74HC112)



Logic Diagram (SN74LVC112A)



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE (SN74)

INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↓	L	L	Q_0	$\overline{Q_0}$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q_0	$\overline{Q_0}$

†The output levels in this configuration may not meet the minimum levels for V_{OH}. Furthermore, this configuration is nonstable; that is, it does not persist when either $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	LVC 3V	UNIT
I_{CC}	MAX	6	25	4.5	19	0.04	0.08	0.08	0.08	0.08	0.01	mA
I_{OH}	MAX	-0.4	-1	-0.4	-1	-4	-4	-4	-24	-24	-24	mA
I_{OL}	MAX	8	20	8	20	4	4	4	24	24	24	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	LS	S	ALS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	LVC 3V
fmax				MIN	30	80	30	100	20	20	20	100	100	150
tw	$\overline{PRE}$, $\overline{CLR}$			MIN	25	8	10	5	25	24	27	4.5	4.5	-
	CLK H			MIN	20	6	16.5	5	25	-	-	4.5	4.5	3.3
	CLK L			MIN	-	6.5	16.5	5	25	-	-	4.5	4.5	3.3
	$\overline{CP}$			MIN	-	-	-	-	-	24	30		-	-
tsu	DATA			MIN	20	7	22	5	25	24	24	4	4	2.3
	$\overline{PRE}$ INACTIVE			MIN	25	-	20	5	25	-	-	-	-	1.1
	$\overline{CLR}$ INACTIVE			MIN	20	-	20	5	25	-	-	-	-	1.1
th				MIN	0	0	0	0	0	0	3	0	0	0.7
t_{PLH}		$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	MAX	20	7	15	7.5	41	-	-	10.3	10.3	4.8
t_{PHL}				MAX	20	7	18	7.5	41	-	-	12.2	12.2	4.8
t_{PLH}		CLK	Q or $\overline{Q}$	MAX	20	7	15	7.5	31	-	-	10.3	10.3	5.9
t_{PHL}				MAX	20	7	19	7.5	31	-	-	12.2	12.2	5.9
t_{PLH}		$\overline{CP}$	Q or $\overline{Q}$	MAX	-	-	-	-	-	53	53	-	-	-
t_{PHL}				MAX	-	-	-	-	-	53	53	-	-	-
t_{PLH}		$\overline{S}$	Q or $\overline{Q}$	MAX	-	-	-	-	-	47	48	-	-	-
t_{PHL}				MAX	-	-	-	-	-	47	48	-	-	-
t_{PLH}		$\overline{R}$	Q or $\overline{Q}$	MAX	-	-	-	-	-	54	56	-	-	-
t_{PHL}				MAX	-	-	-	-	-	54	56	-	-	-

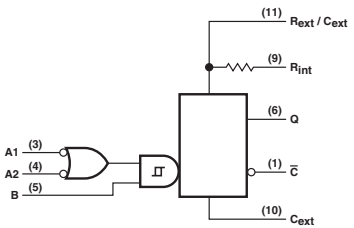
UNIT fmax : MHz, other : ns

121

MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

- Internal Timing Resistors (2kΩ)
- Programmable Output Pulse Width with Rext/Cext: 40ns to 28s

Logic Diagram



R_{int} = 2 kΩ NOM

NOTES: 1. An external capacitor may be connected between C_{ext} (positive) and R_{ext}/C_{ext}.
2. To use the internal timing resistor, connect R_{int} to V_{CC}. For improved pulse width accuracy and repetability, connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} open-circuited.

FUNCTION TABLE

INPUTS			OUTPUTS	
A1	A2	B	Q	$\overline{Q}$
L	X	H	L	H
X	L	H	L†	H†
X	X	L	L†	H†
H	H	X	L†	H†
H	↓	H	⎍	⎍
↓	H	H	⎍	⎍
↓	↓	H	⎍	⎍
L	X	↑	⎍	⎍
X	L	↑	⎍	⎍

See explanation of function table on page

† These lines of the functional tables assume that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the set up.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	UNIT
I_{CC}	MAX	40	mA
I_{OH}	MAX	-0.4	mA
I_{OL}	MAX	16	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL
tw (out)	Pulse width obtained with zero timing capacitance		MIN	50
t_{PLH}	A	Q	MAX	70
t_{PHL}	B			80
t_{PLH}	A	$\overline{Q}$	MAX	55
t_{PHL}	B			65

UNIT: NS

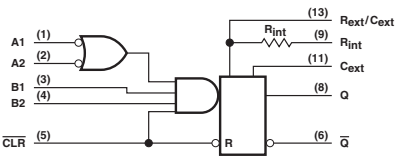
: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

122

RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

- Retriggerable for Very Long Output Pulse, Up to 100% Duty Cycle
- Internal Timing Resistors (5kΩ)

Logic Diagram



R_{int} is nominally 10 kΩ for '122 and 'LS122

FUNCTION TABLE

INPUTS					OUTPUTS	
$\overline{CLEAR}$	A1	A2	B	B2	Q	$\overline{Q}$
L	X	X	X	X	L	H
X	H	H	X	X	L†	H†
X	X	X	L	X	L†	H†
X	X	X	X	L	L†	H†
H	L	X	↑	H	⎍	⎍⎍
H	L	X	H	↑	⎍	⎍⎍
H	X	L	↑	H	⎍	⎍⎍
H	X	L	H	↑	⎍	⎍⎍
H	H	↓	H	H	⎍	⎍⎍
H	↓	↓	H	H	⎍	⎍⎍
H	↓	H	H	H	⎍	⎍⎍
↑	L	X	H	H	⎍	⎍⎍
↑	X	L	H	H	⎍	⎍⎍

See explanation of function table on page

† These lines of the functional tables assume that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the set up.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	UNIT
I_{CC}	MAX	66	11	mA
I_{OH}	MAX	-0.8	-0.4	mA
I_{OL}	MAX	16	8	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS
tw			MIN	40	40
t_{PLH}	A	Q	MAX	33	33
	B			28	44
t_{PHL}	A	$\overline{Q}$	MAX	40	45
	B			36	56
t_{PLH}	CLEAR	Q	MAX	27	27
t_{PHL}		$\overline{Q}$		40	45

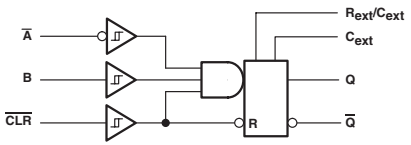
UNIT: NS

123

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBARATORS WITH SCHMITT-TRIGGER INPUTS

- Retriggerable for Very Long Output Pulse, Up to 100% Duty Cycle

Logic Diagram (SN74)



FUNCTION TABLE (SN74)

INPUTS			OUTPUTS	
$\overline{CLEAR}$	$\overline{A}$ (A)	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L†	H†
X	X	L	L†	H†
H	L	↑	⎍	⎍
H	↓	H	⎍	⎍
↑	L	H	⎍	⎍

See explanation of function table on page

† These lines of the functional tables assume that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the set up.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	CD74 HC	CD74 HCT	AHC	AHCT	LV 3V	LV 5V	UNIT
I_{CC}	MAX	66	20	0.16	0.16	0.65	0.975	0.28	0.65	mA
I_{OH}	MAX	-0.8	-0.4	-4	-4	-8	-8	-6	-12	mA
I_{OL}	MAX	16	8	4	4	8	8	6	12	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	CD74 HC	CD74 HCT	AHC	AHCT	LV 3V	LV 5V
tw			MIN	40	40	30	30	5	5	5	5
t_{PLH}	$\overline{A}$ (A)	Q	MAX	33	33	90	90	16	12	27.5	16
	B			28	44	90	90	16	12	27.5	16
t_{PHL}	$\overline{A}$ (A)	$\overline{Q}$	MAX	40	45	96	102	16	12	27.5	16
	B			36	56	96	102	16	12	27.5	16
t_{PLH}	$\overline{CLEAR}$ (R)	Q	MAX	40	45	65	72	13	14	22	13
t_{PHL}		$\overline{Q}$		27	27	65	72	13	14	22	13

UNIT: NS

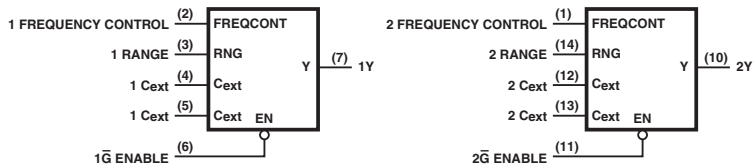
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

124

DUAL VOLTAGE-CONTROLLED OSCILLATORS

- Frequency Spectrum: 1Hz to 60MHz
- Typical fmax: 85MHz
- Typical Power Dissipation: 525mW

Block Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OF

PARAMETER	MAX or MIN	S	UNIT
I_{CC}	MAX	150	mA
I_{OH}	MAX	-1	mA
I_{OL}	MAX	20	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERIS

PARAMETER	MAX or MIN	S
fo	MIN	60

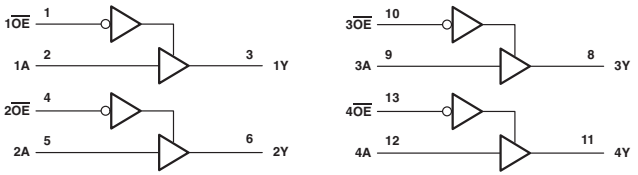
UNIT: NS

125

QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

● Y = A

Logic Diagram (SN74)



FUNCTION TABLE (SN74)
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	SN64 BCT	ABT	UNIT
I_{CC}	MAX	54	20	40	0.08	0.16	0.08	0.16	49	49	30	mA
I_{OH}	MAX	-5.2	-2.6	-15	-6	-6	-6	-6	-15	-15	-32	mA
I_{OL}	MAX	16	24	64	6	6	6	6	64	64	60	mA

PARAMETER	MAX or MIN	LVT 3V	LVTH 3V	AHC	AHCT	LV 3V	LV 5V	LV-AT	LVC 3V	ALVC 3V	AUC 1.8V	AUC 2.3V	UNIT
I_{CC}	MAX	7	7	0.04	0.02	0.02	0.02	0.02	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-32	-32	-8	-8	-8	-16	-16	-24	-24	-8	-9	mA
I_{OL}	MAX	64	64	8	8	8	16	16	24	24	8	9	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	SN64 BCT	ABT
t_{PLH}	A	Y	MAX	13	15	6.5	30	30	33	38	5.7	6	4.9
t_{PHL}			MAX	18	18	8	30	30	33	38	7.7	8	4.9
t_{PZH}	$\overline{G}$	Y	MAX	17	20	8.5	30	38	35	38	10.3	11.1	5.9
t_{PZL}			MAX	25	25	9	30	38	35	38	11.7	12.8	6.8
t_{PHZ}			MAX	8	20	6	30	38	33	42	8.9	9.4	6.2
t_{PLZ}			MAX	12	20	6	30	38	33	42	8.6	9.9	6.2

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVT 3V	LVTH 3V	AHC	AHCT	LV 3V	LV 5V	LV-AT	LVC 3V	ALVC 3V	AUC 1.8V	AUC 2.3V
t_{PLH}	A	Y	MAX	4.0	3.5	8.5	8.5	13	8.5	10.5	4.8	2.8	2.6	2.1
t_{PHL}			MAX	3.9	3.9	8.5	8.5	13	8.5	10.5	4.8	2.8	2.6	2.1
t_{PZH}	$\overline{G}$	Y	MAX	4.7	4	8	8	13	8	9.5	5.4	3.5	2.8	2.3
t_{PZL}			MAX	4.7	4	8	8	13	8	9.5	5.4	3.5	2.8	2.3
t_{PHZ}			MAX	5.1	4.5	10	10	15	10	9	4.6	4	3.4	2.3
t_{PLZ}			MAX	4.5	4.5	10	10	15	10	9	4.6	4	3.4	2.3

UNIT: NS

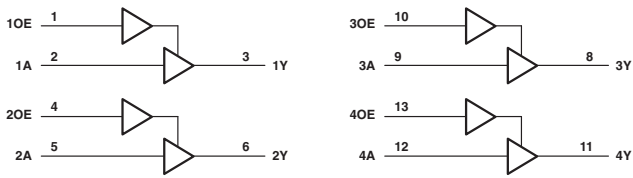
: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

126

QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

● Y = A

Logic Diagram (SN74)



FUNCTION TABLE (SN74)
(each buffer)

INPUTS		OUTPUT
OE	A	Y
H	H	H
H	L	L
L	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	F	SN74 HC	CD74 HC	CD74 HCT	SN74 BCT	SN64 BCT	ABT	UNIT
I_{CC}	MAX	62	22	48	0.08	0.16	0.16	51	51	30	mA
I_{OH}	MAX	-5.2	-2.6	-15	-6	-6	-6	-15	-15	-32	mA
I_{OL}	MAX	16	24	64	6	6	6	64	64	64	mA

PARAMETER	MAX or MIN	LVTH 3V	AHC	AHCT	LV 3V	LV 5V	LVC 3V	ALVC 3V	AUC 1.8V	AUC 2.3V	UNIT
I_{CC}	MAX	7	0.04	0.02	0.02	0.02	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-32	-8	-8	-8	-16	-24	-24	-8	-9	mA
I_{OL}	MAX	64	8	8	8	16	24	24	8	9	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	F	SN74 HC	CD74 HC	CD74 HCT	SN74 BCT	SN64 BCT	ABT
t_{PLH}	A	Y	MAX	13	15	7	30	30	36	6.3	6.3	6.3
t_{PHL}			MAX	18	18	8.5	30	30	36	7.4	7.4	5.7
t_{PZH}	G	Y	MAX	18	25	8.5	30	38	38	7.9	7.9	6.5
t_{PZL}			MAX	25	35	8.5	30	38	38	10.5	10.5	6.5
t_{PHZ}			MAX	16	25	7.5	30	38	42	10	10	6.8
t_{PLZ}			MAX	18	25	8	30	38	42	12.3	12.3	6.7

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTH 3V	AHC	AHCT	LV 3V	LV 5V	LVC 3V	ALVC 3V	AUC 1.8V	AUC 2.3V
t_{PLH}	A	Y	MAX	3.8	8.5	8.5	13	8.5	4.7	3.1	2.6	2.1
t_{PHL}			MAX	3.9	8.5	8.5	13	8.5	4.7	3.1	2.6	2.1
t_{PZH}	G	Y	MAX	5.4	8	8	13	8	5.7	3.3	2.7	2.2
t_{PZL}			MAX	5.2	8	8	13	8	5.7	3.3	2.7	2.2
t_{PHZ}			MAX	3.8	10	10	15	10	6	3.7	3.3	2.2
t_{PLZ}			MAX	5.5	10	10	15	10	6	3.7	3.3	2.2

UNIT: ns

128

50-Ω LINE DRIVERS

● $Y = \overline{A + B}$

Logic Diagram

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	UNIT
I_{CC}	MAX	57	mA
I_{OH}	MAX	-42.4	mA
I_{OL}	MAX	48	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL
t_{PLH}	A, B	Y	MAX	9
t_{PHL}	A, B	Y	MAX	12

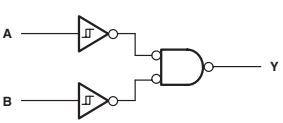
UNIT: ns

132

QUADRUPLE POSITIVE-NAND GATES WITH SCHMITT TRIGGER INPUTS

● $Y = \overline{A \bullet B}$

Logic Diagram (SN74)



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	SN74 HC	CD74 HC	CD74 HCT	AHC	AHCT	LV 3V	LV 5V	UNIT
I_{CC}	MAX	40	14	68	0.02	0.04	0.04	0.02	0.02	0.02	0.02	mA
I_{OH}	MAX	-0.8	-0.4	-1	-4	-4	-4	-8	-8	-6	-12	mA
I_{OL}	MAX	16	8	20	4	4	4	8	8	6	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	SN74 HC	CD74 HC	CD74 HCT	AHC	AHCT
t_{PLH}	A, B	Y	MAX	22	22	10.5	31	38	50	11	10
t_{PHL}	A, B	Y	MAX	22	22	13	31	38	50	11	8

PARAMETER	INPUT	OUTPUT	MAX or MIN	LV 3V	LV 5V
t_{PLH}	A, B	Y	MAX	17.5	11
t_{PHL}	A, B	Y	MAX	17.5	11

UNIT: ns

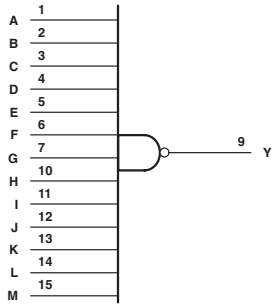
: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

133

13-INPUT POSITIVE-NAND GATES

● $Y = \overline{A \bullet B \bullet C \bullet D \bullet E \bullet F \bullet G \bullet H \bullet I \bullet J \bullet K \bullet L \bullet M}$

Logic Diagram



FUNCTION TABLE

INPUTS A–H	OUTPUT Y
All inputs H	L
One or more inputs L	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIOI

PARAMETER	MAX or MIN	S	ALS	SN74 HC	UNIT
I_{CC}	MAX	10	0.34	0.02	mA
I_{OH}	MAX	-1	-0.4	-4	mA
I_{OL}	MAX	20	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	S	ALS	SN74 HC
t_{PLH}	A to M	Y	MAX	6	11	38
t_{PHL}	A to M	Y	MAX	7	25	38

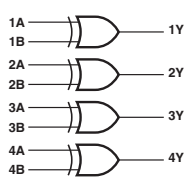
UNIT: ns

136

QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES WITH OPEN COLLECTOR OUTPUTS

● $Y = A \oplus B = \overline{A}B + A\overline{B}$

Logic Diagram



FUNCTION TABLE

INPUTS A	INPUTS B	OUTPUT Y
L	L	L
L	H	H
H	L	H
H	H	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	AS	UNIT
I_{CC}	MAX	50	10	5.9	31	mA
V_{OH}	MAX	5.5	5.5	5.5	5.5	V
I_{OL}	MAX	16	8	8	20	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	AS
t_{PLH}	A or B	Y (Other Output = L)	MAX	18	30	50	12.5
t_{PHL}	A or B	Y (Other Output = L)	MAX	50	30	15	7.1
t_{PLH}	A or B	Y (Other Output = L)	MAX	22	30	50	11.4
t_{PHL}	A or B	Y (Other Output = L)	MAX	55	30	15	10.7

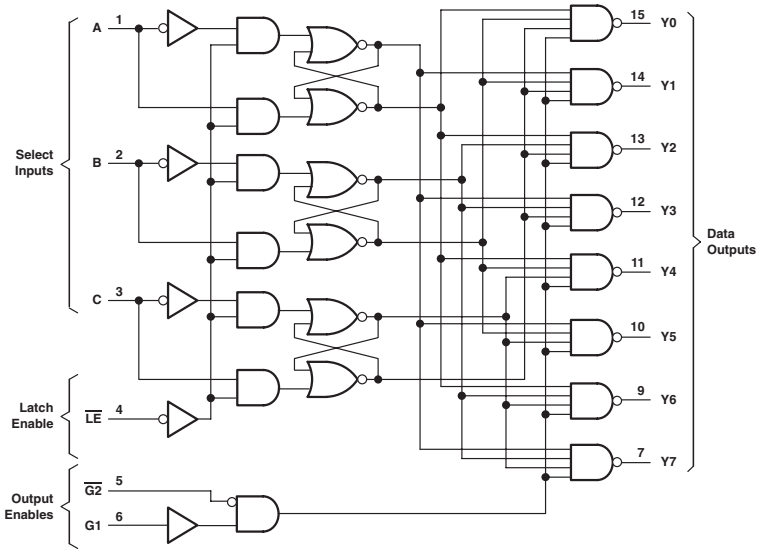
UNIT: ns

137

3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS WITH ADDRESS LATCHES

- Incorporates Two Output Enables To Simplify Cascading

Logic Diagram (SN74ALS)



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE (SN74)

INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{LE}$	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Depends upon the address previously applied while LE was at a logic low.							

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	LVC 3V	UNIT
I_{CC}	MAX	18	11	24	0.08	0.16	0.08	0.16	0.01	mA
I_{OH}	MAX	-0.4	-0.4	-2	-4	-4	-4	-4	-24	mA
I_{OL}	MAX	8	8	20	4	4	4	4	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	LVC 3V
t_{PLH}	SELECT	Y (CD74: $\overline{Y}$)	MAX	24	20	12.5	48	54	48	57	-
t_{PHL}			MAX	38	20	12.5	48	54	48	57	-
t_{PLH}	$\overline{G2}$	Y (CD74: $\overline{Y}$)	MAX	21	12	8	36	44	36	56	-
t_{PHL}			MAX	27	15	8.5	36	44	36	56	-
t_{PLH}	G1	Y (CD74: $\overline{Y}$)	MAX	21	17	10	36	44	36	53	-
t_{PHL}			MAX	27	15	9	36	44	36	53	-
t_{PLH}	$\overline{LE}$ (CD74: LE)	Y (CD74: $\overline{Y}$)	MAX	27	22	13.5	48	57	52	66	-
t_{PHL}			MAX	38	20	14	48	57	52	66	-

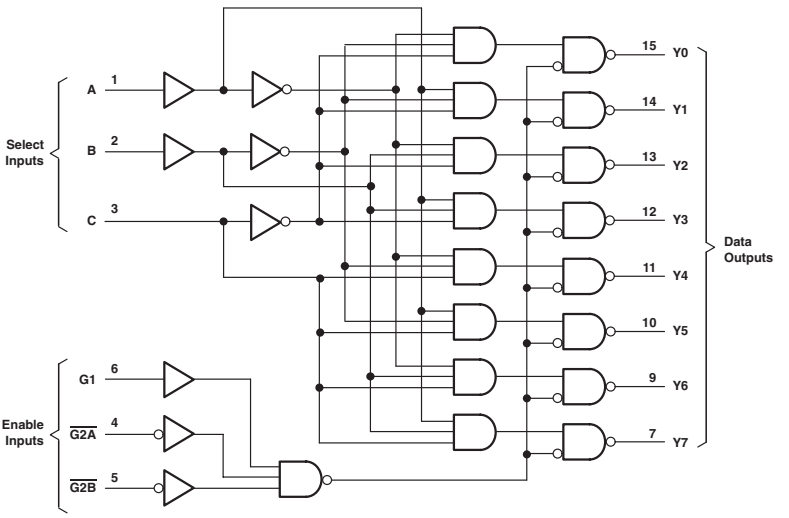
UNIT:ns LVC:Preview

138

3-LINE TO 8-LINE DECODERS/DEMULTIPLEXRS

- 3 Enable Inputs to Simplify Cascading and /or Data Reception
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram (SN74, CD74AC/ACT)



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE (SN74)

ENABLE INPUTS			SELECT INPUTS			OUTPUTS							
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	UNIT
I_{CC}	MAX	10	74	10	20	20	0.08	0.16	0.08	0.16	mA
I_{OH}	MAX	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-4	mA
I_{OL}	MAX	8	20	8	20	20	4	4	4	4	mA

PARAMETER	MAX or MIN	AC 11	CD74 AC	ACT 11	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LV-AT	LVC 3V	UNIT
I_{CC}	MAX	0.04	0.16	0.04	0.16	0.04	0.04	0.02	0.02	0.01	0.01	mA
I_{OH}	MAX	-24	-24	-24	-24	-8	-8	-6	-12	-8	-24	mA
I_{OL}	MAX	24	24	24	24	8	8	6	12	8	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT
t_{PLH}	A, B, C	Y (CD74:$\overline{Y}$)	MAX	27	12	22	10	8.5	45	45	45	53
t_{PHL}			MAX	39	12	18	9.5	9	45	45	45	53
t_{PLH}	$\overline{G2}$	Y (CD74:$\overline{Y}$)	MAX	26	11	17	7.5	8	39	53	42	53
t_{PHL}			MAX	38	11	17	8.5	7.5	39	53	42	53
t_{PLH}	G1	Y (CD74:$\overline{Y}$)	MAX	26	11	17	10	9	39	53	42	53
t_{PHL}			MAX	38	11	17	10	8.5	39	53	42	53

PARAMETER	INPUT	OUTPUT	MAX or MIN	AC 11	CD74 AC	ACT 11	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LV-AT	LVC 3V
t_{PLH}	A, B, C	Y (CD74:$\overline{Y}$)	MAX	8.1	11	9.8	12	11.5	13	18	11.5	14	6.7
t_{PHL}			MAX	8.8	11	9.7	12	11.5	13	18	11.5	14	6.7
t_{PLH}	$\overline{G2}$	Y (CD74:$\overline{Y}$)	MAX	8.3	10	8.9	10.5	11.5	12	17	11.5	13	6.5
t_{PHL}			MAX	8.3	10	8.9	10.5	11.5	12	17	11.5	13	6.5
t_{PLH}	G1	Y (CD74:$\overline{Y}$)	MAX	7.5	11	9.3	11	11.5	11.5	18.5	11.5	12	5.8
t_{PHL}			MAX	7.7	11	9.8	11	11.5	11.5	18.5	11.5	12	5.8

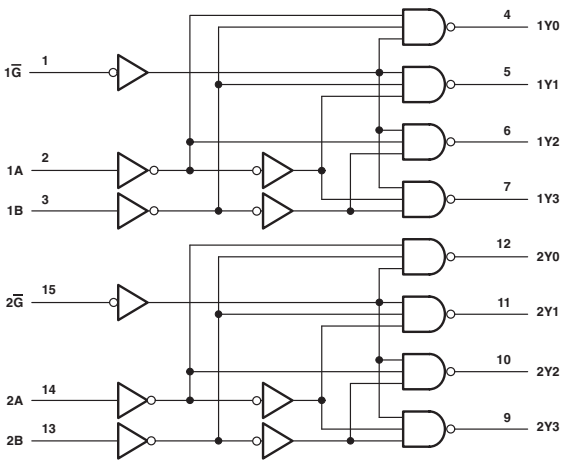
UNIT: ns

139

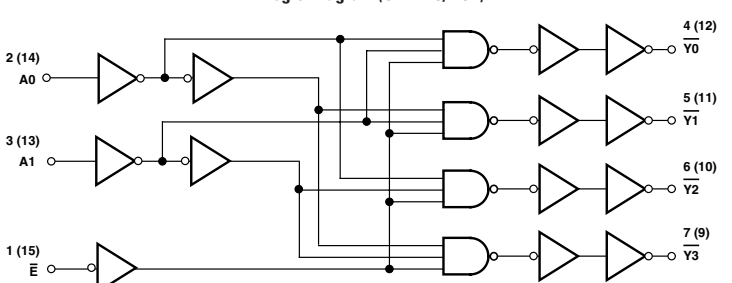
DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

- Incorporate Two Enable Inputs to Simplify Cascading and /or Data Reception
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram (SN74, CD74AC/ACT)



Logic Diagram (CD74HC/HCT)



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE (SN74)

INPUTS			OUTPUTS			
ENABLE	SELECT					
$\overline{G}$	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	CD74 AC	ACT 11	UNIT
I_{CC}	MAX	11	90	13	0.08	0.16	0.08	0.16	0.16	0.08	mA
I_{OH}	MAX	-0.4	-1	-0.4	-4	-4	-4	-4	-24	-24	mA
I_{OL}	MAX	8	20	8	4	4	4	4	24	24	mA

PARAMETER	MAX or MIN	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	UNIT
I_{CC}	MAX	0.16	0.04	0.02	-	0.02	0.01	mA
I_{OH}	MAX	-24	-8	-8	-6	-12	-24	mA
I_{OL}	MAX	24	8	8	6	12	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	CD74 AC	ACT 11
t_{PLH}	SELECT	Y (CD74: $\overline{Y}$)	MAX	29	12	14	44	44	43	51	10.5	8.5
t_{PHL}	SELECT	Y (CD74: $\overline{Y}$)	MAX	38	12	14	44	44	43	51	10.5	8.5
t_{PLH}	$\overline{G}$ (CD74: E)	Y (CD74: $\overline{Y}$)	MAX	24	8	14	44	41	43	51	10.5	7.9
t_{PHL}	$\overline{G}$ (CD74: E)	Y (CD74: $\overline{Y}$)	MAX	32	10	15	44	41	43	51	10.5	7.5

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V
t_{PLH}	SELECT	Y (CD74: $\overline{Y}$)	MAX	11.5	10.5	10.5	16.5	10.5	6.2
t_{PHL}	SELECT	Y (CD74: $\overline{Y}$)	MAX	11.5	10.5	10.5	16.5	10.5	6.2
t_{PLH}	$\overline{G}$ (CD74: E)	Y (CD74: $\overline{Y}$)	MAX	12	9.5	9.5	14.5	9.5	4.7
t_{PHL}	$\overline{G}$ (CD74: E)	Y (CD74: $\overline{Y}$)	MAX	12	9.5	9.5	14.5	9.5	4.7

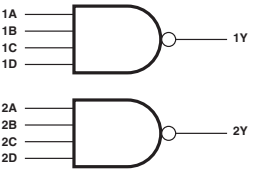
UNIT: ns

140

DUAL 4-INPUT POSITIVE-NAND 50-Ω LINE DRIVERS

● $Y = \overline{ABCD}$

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	S	UNIT
I_{CC}	MAX	44	mA
I_{OH}	MAX	-40	mA
I_{OL}	MAX	60	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	S
t_{PLH}	A, B, C, D	Y	MAX	6.5
t_{PHL}			MAX	6.5

UNIT: ns

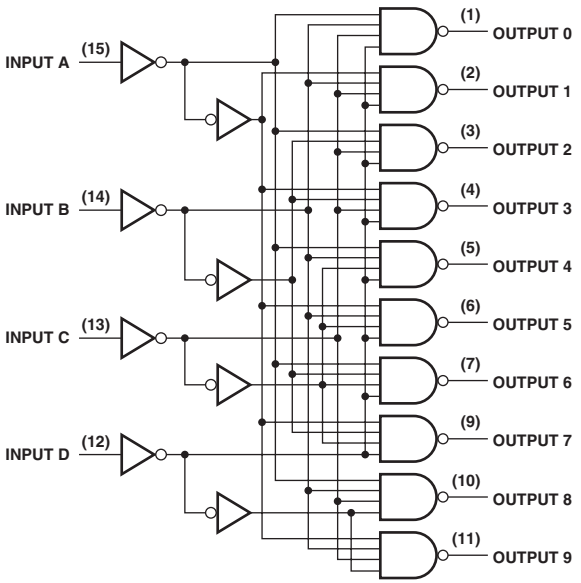
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

145

BCD-TO-DECIMAL DECODERS/DRIVERS

- Sink-Current Capability: 80mA
- Low Power Dissipation (SN74LS): 35mW (typ)

Logic Diagram



FUNCTION TABLE

No.	INPUTS				OUTPUTS									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERAT

PARAMETER	MAX or MIN	TTL	LS	UNIT
I_{CC}	MAX	70	13	mA
Vo (OFF)	MAX	15	15	mA

SWITCHING CHARACTERISTICS

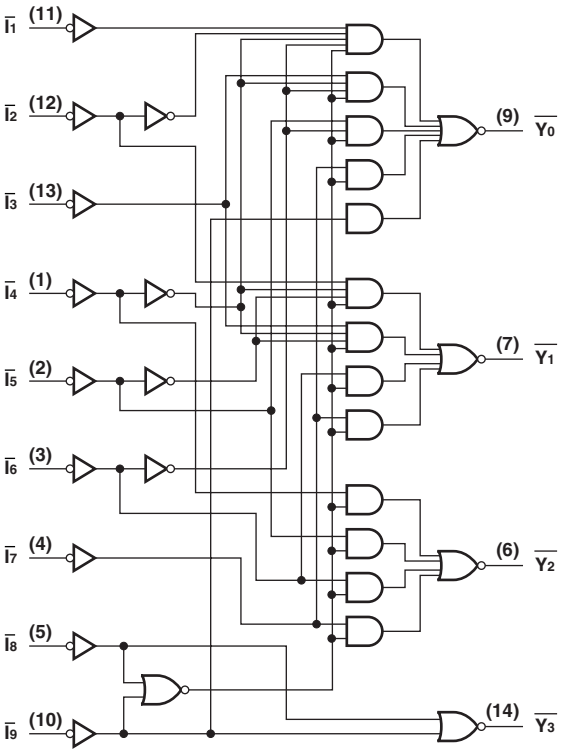
PARAMETER	MAX or MIN	TTL	LS
t_{PLH}	MAX	50	50
t_{PHL}	MAX	50	50

UNIT: ns

147

10-LINE TO 4-LINE BCD PRIORITY ENCODER

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS									OUTPUTS			
$\overline{I}_1$	$\overline{I}_2$	$\overline{I}_3$	$\overline{I}_4$	$\overline{I}_5$	$\overline{I}_6$	$\overline{I}_7$	$\overline{I}_8$	$\overline{I}_9$	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

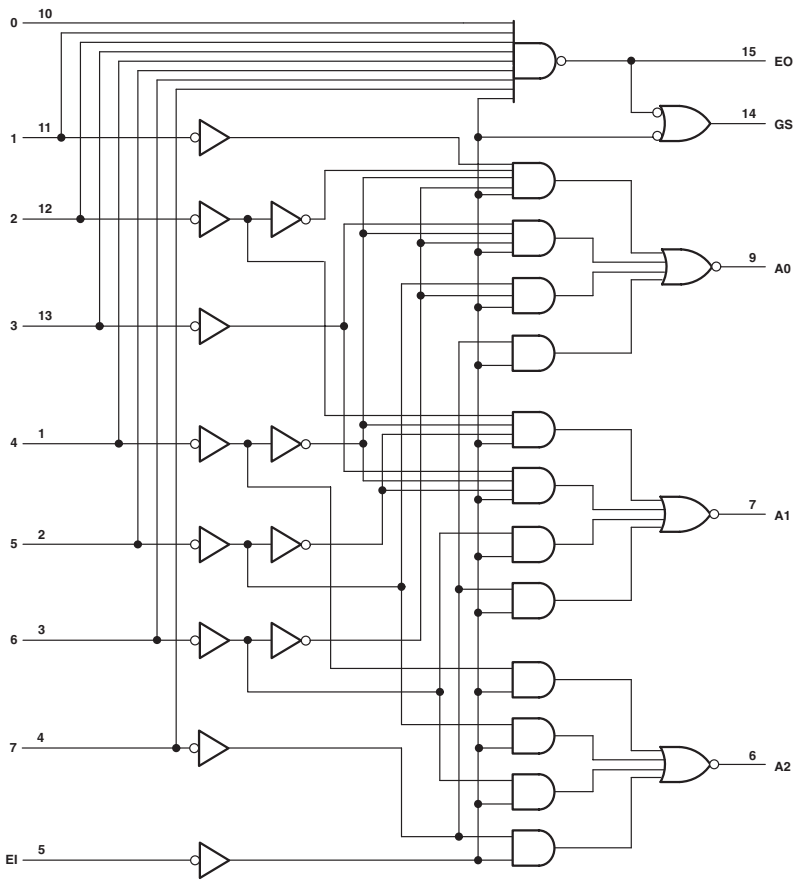
PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	70	20	0.08	0.16	0.16	mA
I_{OH}	MAX	-0.8	-0.4	-4	-4	-4	mA
I_{OL}	MAX	16	8	4	4	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT
t_{PLH}	MAX	19	33	48	48	53
t_{PHL}	MAX	19	23	48	48	53

UNIT:ns

Logic Diagram (SN74)



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE (SN74)

INPUTS									OUTPUTS				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	UNIT
I_{CC}	MAX	60	20	0.08	mA
I_{OL}	MAX	16	8	4	mA
I_{OH}	MAX	-0.8	-0.4	-4	mA

SWITCHING CHARACTERISTICS

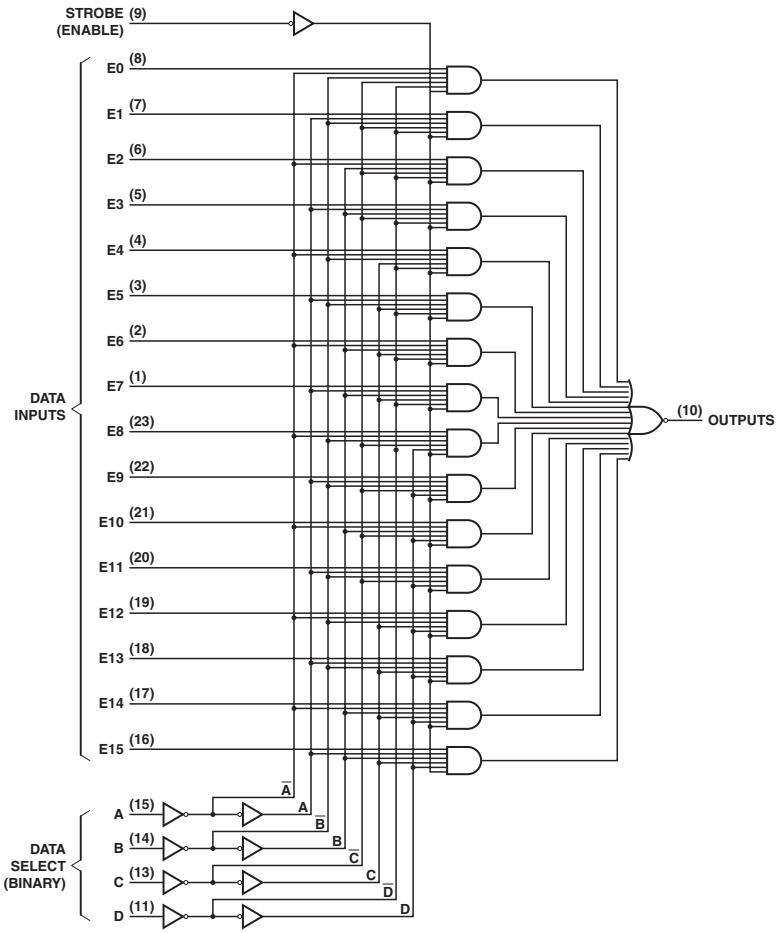
PARAMETER	INPUT	OUTPUT	WAVEFORM	MAX or MIN	TTL	LS	SN74 HC
t_{PLH}	1 to 7	A0, A1 or A2	In-phase output	MAX	15	18	45
t_{PHL}					14	25	45
t_{PLH}	1 to 7	A0, A1 or A2	Out-of-phase output	MAX	19	36	45
t_{PHL}					19	29	45
t_{PLH}	0 to 7	E0	Out-of-phase output	MAX	10	18	38
t_{PHL}					25	40	38
t_{PLH}	0 to 7	GS	In-phase output	MAX	30	55	48
t_{PHL}					25	21	48
t_{PLH}	EI	A0, A1 or A2	In-phase output	MAX	15	25	49
t_{PHL}					15	25	49
t_{PLH}	EI	GS	In-phase output	MAX	12	17	36
t_{PHL}					15	36	36
t_{PLH}	EI	EO	In-phase output	MAX	15	21	41
t_{PHL}					30	35	41

UNIT: ns

150

16-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS					OUTPUT
SELECT				STROBE	W
D	C	B	A	$\overline{G}$	
X	X	X	X	H	H
L	L	L	L	L	$\overline{E0}$
L	L	L	H	L	$\overline{E1}$
L	L	H	L	L	$\overline{E2}$
L	L	H	H	L	$\overline{E3}$
L	H	L	L	L	$\overline{E4}$
L	H	L	H	L	$\overline{E5}$
L	H	H	L	L	$\overline{E6}$
L	H	H	H	L	$\overline{E7}$
H	L	L	L	L	$\overline{E8}$
H	L	L	H	L	$\overline{E9}$
H	L	H	L	L	$\overline{E10}$
H	L	H	H	L	$\overline{E11}$
H	H	L	L	L	$\overline{E12}$
H	H	L	H	L	$\overline{E13}$
H	H	H	L	L	$\overline{E14}$
H	H	H	H	L	$\overline{E15}$

NOTES:
H = High Level, L = Low Level, X = irrelevant
$\overline{E0}$, $\overline{E1}$ ... $\overline{E15}$ = the complement of the level of the respective E input
D0, D1 ... D7 = the level of the D respective input

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

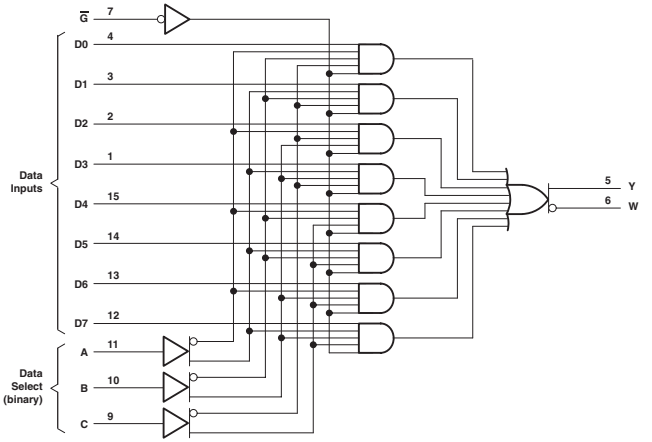
PARAMETER	MAX or MIN	TTL	UNIT
I_{CC}	MAX	48	mA
I_{OH}	MAX	-0.8	mA
I_{OL}	MAX	16	mA

SWITCHING CHARACTERISTICS

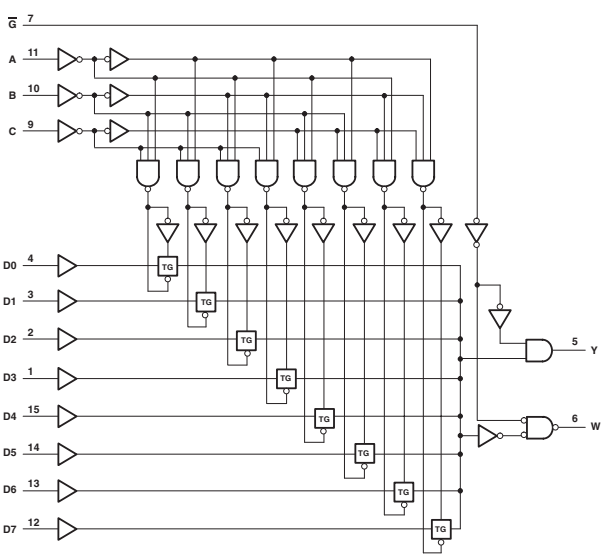
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL
t_{PLH}	A, B, C or D	W	MAX	35
t_{PHL}				33
t_{PLH}	Strobe $\overline{G}$	W	MAX	24
t_{PHL}				30
t_{PLH}	E0 thru E15 or E0 thru D7	W	MAX	14
t_{PHL}				20

UNIT:ns

Logic Diagram (SN74ALS, AS, F, CD74AC/ACT)



Logic Diagram (SN74HC)



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE (SN74)

INPUTS				OUTPUTS	
SELECT					
C	B	A	$\overline{G}$	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	UNIT
I_{CC}	MAX	48	10	70	12	30	21	0.08	0.16	0.16	0.16	0.16	mA
I_{OH}	MAX	-0.8	-0.4	-1	-2.6	-15	-1	-6	-4	-4	-24	-24	mA
I_{OL}	MAX	16	8	20	24	48	24	6	4	4	24	24	mA

SWITCHING CHARACTERISTICS

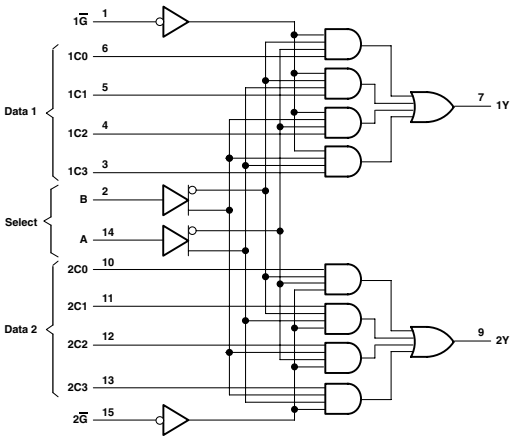
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT
t_{PLH}	A, B or C (CD74HC/HCT: Sn)	Y	MAX	38	43	18	18	14.5	12	63	56	62
t_{PHL}				38	30	18	24	15	9	63	56	62
t_{PLH}	A, B or C (CD74HC/HCT: Sn)	W (CD74HC: $\overline{Y}$)	MAX	26	23	15	24	12	9.5	63	62	65
t_{PHL}				30	32	13.5	23	12	7.5	63	62	65
t_{PLH}	D0 to D7 (CD74HC/HCT: In)	Y	MAX	20	32	16.5	10	10.5	7.5	49	51	57
t_{PHL}				27	26	18	15	11	7.5	49	51	57
t_{PLH}	D0 to D7 (CD74HC/HCT: In)	W (CD74HC: $\overline{Y}$)	MAX	14	21	13	15	6.5	7	49	56	54
t_{PHL}				14	20	12	15	4.5	5	49	56	54
t_{PLH}	$\overline{G}$ (CD74HC/HCT: $\overline{E}$)	Y	MAX	33	42	12	18	14	10.5	32	42	44
t_{PHL}				33	32	12	19	11	7.5	32	42	44
t_{PLH}	$\overline{G}$ (CD74HC/HCT: $\overline{E}$)	W (CD74HC: $\overline{Y}$)	MAX	21	24	7	19	6	7	32	44	54
t_{PHL}				23	30	7	23	10	6	32	44	54

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 AC	CD74 ACT
t_{PLH}	A, B or C (CD74HC/HCT: Sn)	Y	MAX	18.2	20.2
t_{PHL}				18.2	20.2
t_{PLH}	A, B or C (CD74HC/HCT: Sn)	W (CD74HC: $\overline{Y}$)	MAX	19.6	21.6
t_{PHL}				19.6	21.6
t_{PLH}	D0 to D7 (CD74HC/HCT: In)	Y	MAX	13.5	15.5
t_{PHL}				13.5	15.5
t_{PLH}	D0 to D7 (CD74HC/HCT: In)	W (CD74HC: $\overline{Y}$)	MAX	14.9	16.9
t_{PHL}				14.9	16.9
t_{PLH}	$\overline{G}$ (CD74HC/HCT: $\overline{E}$)	Y	MAX	12.2	12.1
t_{PHL}				12.2	12.1
t_{PLH}	$\overline{G}$ (CD74HC/HCT: $\overline{E}$)	W (CD74HC: $\overline{Y}$)	MAX	13.5	13.5
t_{PHL}				13.5	13.5

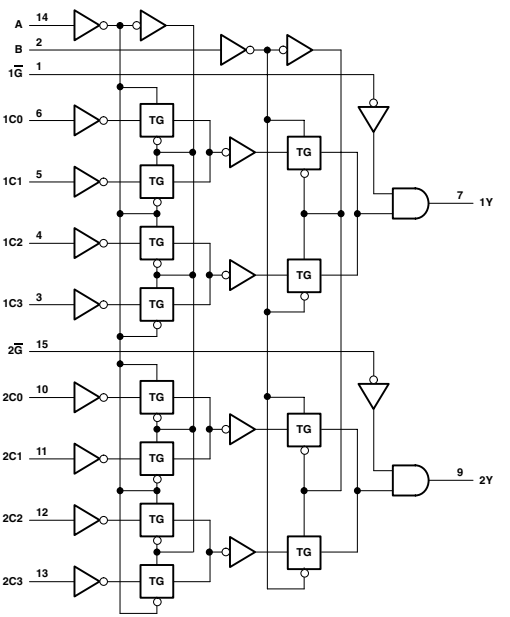
UNIT: ns

DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

Logic Diagram (SN74ALS, AS, F, LS)



Logic Diagram (SN74HC, HCT, CD74AC, ACT)



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE (SN74)

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUTS
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	UNIT
I_{CC}	MAX	60	10	70	14	33	20	0.08	0.16	0.16	0.16	0.16	mA
I_{OH}	MAX	-0.8	-0.4	-1	-2.6	-15	-1	-6	-4	-4	-24	-24	mA
I_{OL}	MAX	16	8	20	24	48	20	6	4	4	24	24	mA

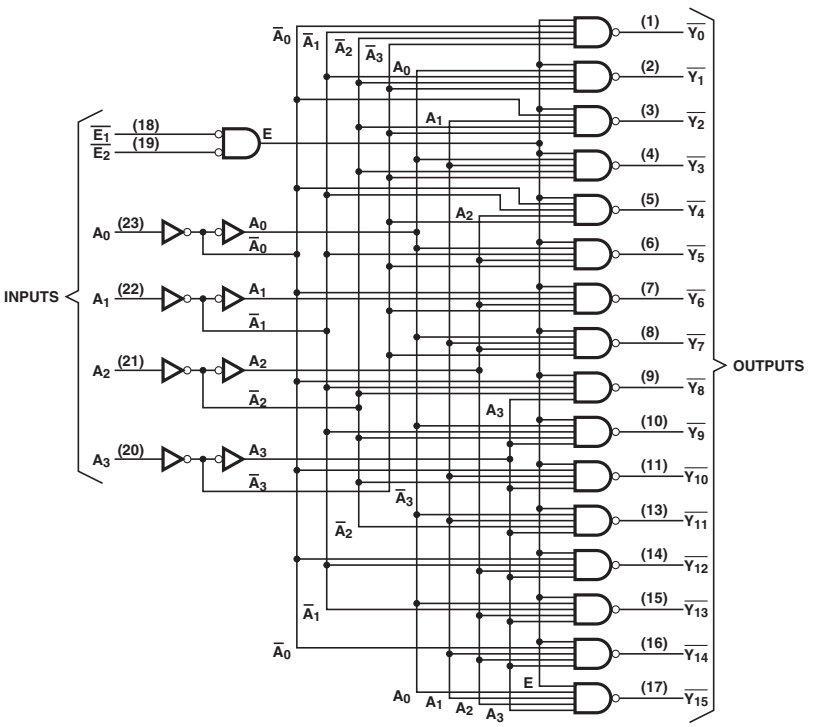
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT
t_{PLH}	DATA	Y	MAX	18	15	9	10	7	8	35	44	51
t_{PHL}			MAX	23	26	9	15	8	7.5	35	44	51
t_{PLH}	SELECT	Y	MAX	34	29	18	21	12.5	12	38	48	51
t_{PHL}			MAX	34	38	18	21	11	10.5	38	48	51
t_{PLH}	STROBE	Y	MAX	30	24	15	18	11.5	10.5	24	36	41
t_{PHL}			MAX	23	32	13.5	18	9	8	24	36	41

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 AC	CD74 ACT
t_{PLH}	DATA	Y	MAX	13.3	18
t_{PHL}			MAX	13.3	18
t_{PLH}	SELECT	Y	MAX	20	22
t_{PHL}			MAX	20	22
t_{PLH}	STROBE	Y	MAX	11.8	12.6
t_{PHL}			MAX	11.8	12.6

UNIT: ns

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS						OUTPUTS														
$\overline{E_1}$	$\overline{E_2}$	A_3	A_2	A_1	A_0	$\overline{Y_0}$	$\overline{Y_1}$	$\overline{Y_2}$	$\overline{Y_3}$	$\overline{Y_4}$	$\overline{Y_5}$	$\overline{Y_6}$	$\overline{Y_7}$	$\overline{Y_8}$	$\overline{Y_9}$	$\overline{Y_{10}}$	$\overline{Y_{11}}$	$\overline{Y_{12}}$	$\overline{Y_{13}}$	$\overline{Y_{14}}$	$\overline{Y_{15}}$
L	L	H	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	ALS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	56	23	0.08	0.16	0.16	mA
I_{OH}	MAX	-0.8	24	-4	-4	-4	mA
I_{OL}	MAX	16	-0.4	4	4	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	ALS	SN74 HC	CD74 HC	CD74 HCT
t_{PLH}	Adress	0 to 15 (CD74: Y0 to $\overline{Y15}$)	MAX	36	12	45	53	53
t_{PHL}				33	12	45	53	53
t_{PLH}	Enable	0 to 15 (CD74: Y0 to $\overline{Y15}$)	MAX	30	12	45	53	51
t_{PHL}				27	12	45	53	51

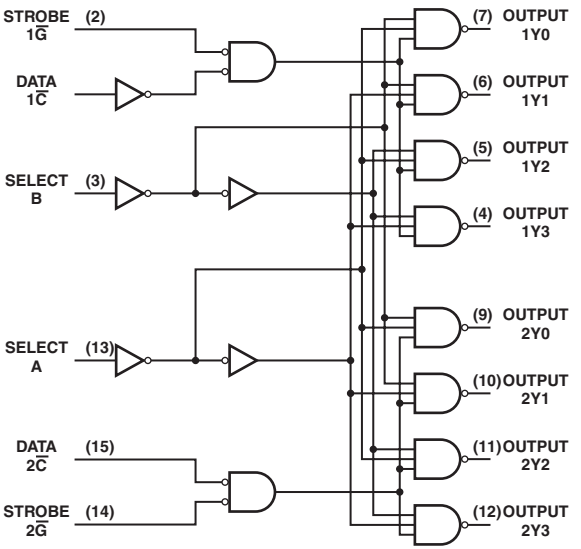
UNIT: ns

155

DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

- Individual Strobes Simplify Cascading for Decoding or Demultiplexing Lager Words
- Outputs: Totem Pole

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLES

2-LINE TO 4-LINE DECODER OR
1-LINE TO 4-LINE DEMULTIPLEXER

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	$1\overline{G}$	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	$2\overline{G}$	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

3-LINE TO 8-LINE DECODER OR
1-LINE TO 8-LINE DEMULTIPLEXER

INPUTS				OUTPUTS							
SELECT			STROBE or DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	$\overline{G}$‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

† C = inputs 1C and $2\overline{C}$ connected together
‡ $\overline{G}$ = inputs $1\overline{G}$ and $2\overline{G}$ connected together

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	UNIT
I_{CC}	MAX	40	10	13	mA
I_{OH}	MAX	-0.8	-0.4	-0.4	mA
I_{OL}	MAX	16	8	8	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS
t_{PLH}	A or B	Y	MAX	32	26	14
t_{PHL}	A or B			32	30	12
t_{PLH}	1C	Y	MAX	24	27	12
t_{PHL}	1C			30	27	14

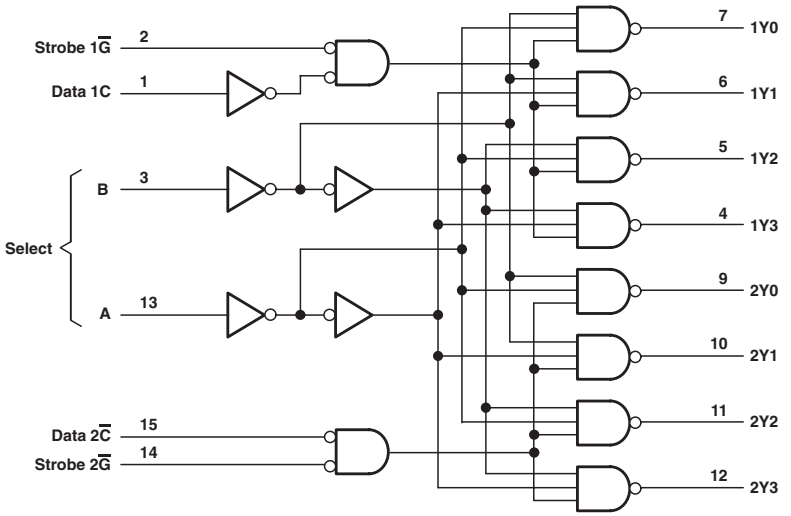
UNIT: ns

156

DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS WITH OPEN-COLLECTOR OUTPUTS

- Individual Strobes Simplify Cascading for Decoding or Demultiplexing Lager Words
- Outputs: Open-Collector

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLES

2-LINE TO 4-LINE DECODER OR
1-LINE TO 4-LINE DEMULTIPLEXER

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	$1\overline{G}$	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	$2\overline{G}$	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

3-LINE TO 8-LINE DECODER OR
1-LINE TO 8-LINE DEMULTIPLEXER

INPUTS				OUTPUTS							
SELECT			STROBE or DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	$\overline{G}$‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

† C = inputs 1C and $2\overline{C}$ connected together
‡ $\overline{G}$ = inputs $1\overline{G}$ and $2\overline{G}$ connected together

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

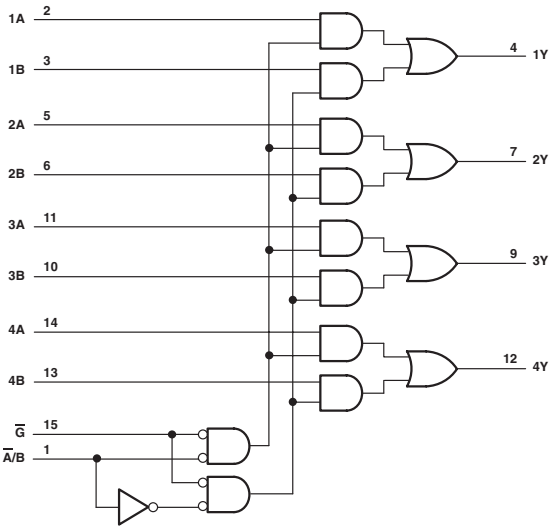
PARAMETER	MAX or MIN	TTL	LS	ALS	UNIT
I_{CC}	MAX	40	10	9	mA
I_{OL}	MAX	16	8	8	mA
V_{OH}	MAX	5.5	5.5	5.5	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS
t_{PLH}	$2\overline{C}$ or $1\overline{G}$ or $2\overline{G}$	Y	MAX	23	40	38
t_{PHL}				30	51	22
t_{PLH}	A or B	Y	MAX	34	46	55
t_{PHL}	A or B			34	51	25
t_{PLH}	1C	Y	MAX	27	48	50
t_{PHL}	1C			33	48	23

UNIT: ns

Logic Diagram (SN74LV/SN74HC)



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE (SN74)

INPUTS				OUTPUT
STROBE	SELECT	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	UNIT
I_{CC}	MAX	48	16	78	11	28	23	0.08	0.16	0.08	mA
I_{OH}	MAX	-0.8	-0.4	-1	-0.4	-2	-1	-6	-4	-6	mA
I_{OL}	MAX	16	8	20	8	20	20	6	4	6	mA

PARAMETER	MAX or MIN	CD74 HCT	CD74 AC	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	UNIT
I_{CC}	MAX	0.16	0.16	0.16	0.04	0.02	-	0.0.2	0.01	mA
I_{OH}	MAX	-4	-24	-24	-8	-8	-6	-12	-24	mA
I_{OL}	MAX	4	24	24	8	8	6	12	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT
t_{PLH}	DATA	Y	MAX	14	14	7.5	14	6	6.5	32	38	35
t_{PHL}				14	14	6.5	12	5.5	7	32	38	35
t_{PLH}	STROBE	Y	MAX	20	20	12.5	20	10.5	11	29	41	33
t_{PHL}				21	21	12	13	7.5	7	29	41	33
t_{PLH}	SELECT	Y	MAX	23	23	15	24	11	11	31	44	40
t_{PHL}				27	27	15	17	10	8	31	44	40

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HCT	CD74 AC	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V
t_{PLH}	DATA	Y	MAX	38	8.5	9.5	9.5	9.8	15	9.5	5.2
t_{PHL}				38	8.5	9.5	9.5	9.8	15	9.5	5.2
t_{PLH}	STROBE	Y	MAX	41	13.5	13.5	12	12	19.5	12	6.5
t_{PHL}				41	13.5	13.5	12	12	19.5	12	6.5
t_{PLH}	SELECT	Y	MAX	44	14.5	14.5	11.5	12	19	11.5	6.8
t_{PHL}				44	14.5	14.5	11.5	12	19	11.5	6.8

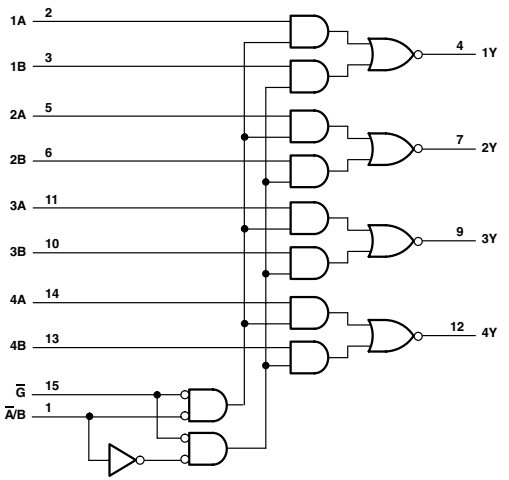
UNIT: ns

158

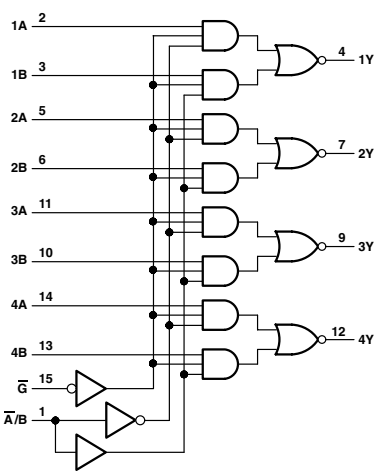
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

- Buffered Inputs and Outputs

Logic Diagram (SN74HC, ALS, LS)



Logic Diagram (SN74AS)



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE (SN74)

INPUTS				OUTPUT
STROBE	SELECT	A	B	
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	11	81	10	22.5	15	0.08	0.16	0.16	mA
I_{OH}	MAX	-0.4	-1	-0.4	-2	-1	-6	-4	-4	mA
I_{OL}	MAX	8	20	8	20	20	6	4	4	mA

PARAMETER	MAX or MIN	CD74 AC	CD74 ACT	AHC	AHCT	UNIT
I_{CC}	MAX	0.16	0.16	0.04	0.02	mA
I_{OH}	MAX	-24	-24	-8	-8	mA
I_{OL}	MAX	24	24	8	8	mA

SWITCHING CHARACTERISTICS

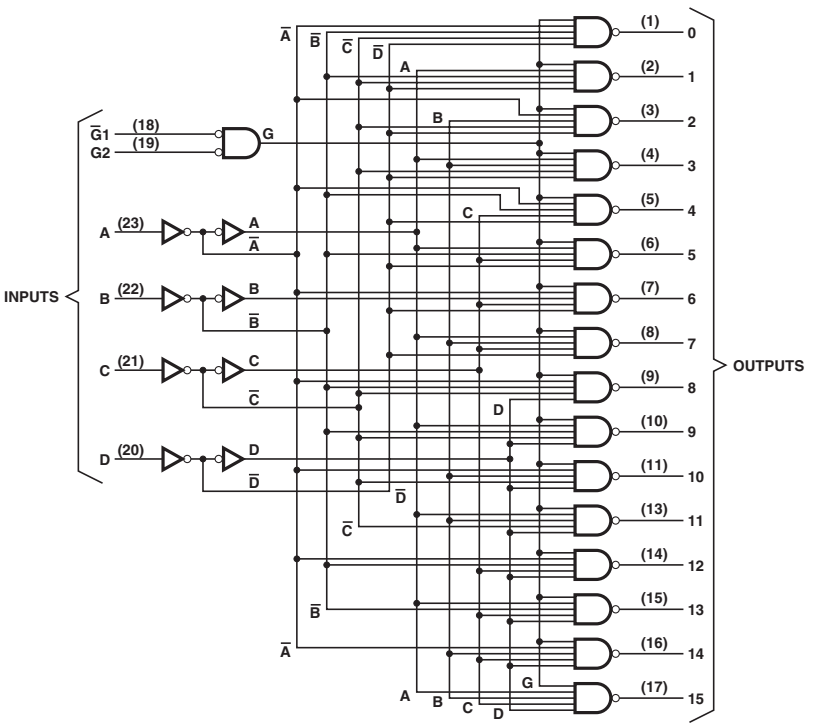
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT
t_{PLH}	DATA	Y	MAX	12	6	15	5	7	32	42	42
t_{PHL}				15	6	8	4.5	4.5	32	42	42
t_{PLH}	STROBE	Y	MAX	17	11.5	18	6.5	7	29	48	48
t_{PHL}				24	12	18	10	6.5	29	48	48
t_{PLH}	SELECT	Y	MAX	20	12	18	9.5	9.5	31	45	45
t_{PHL}				24	12	18	10.5	7	31	45	45

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 AC	CD74 ACT	AHC	AHCT
t_{PLH}	DATA	Y	MAX	8	9.2	9.5	9.8
t_{PHL}				8	9.2	9.5	9.8
t_{PLH}	STROBE	Y	MAX	11.9	12.4	12	12
t_{PHL}				11.9	12.4	12	12
t_{PLH}	SELECT	Y	MAX	12.9	13.5	11.5	12
t_{PHL}				12.9	13.5	11.5	12

UNIT: ns

4-LINE TO 16-LINE DECODERS/DEMULTIPLEXERS WITH OPEN-COLLECTOR OUTPUTS

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS						OUTPUTS													
$\overline{G1}$	$\overline{G2}$	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	UNIT
I_{CC}	MAX	56	mA
I_{OL}	MAX	16	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL
t_{PLH}	INPUT	ANY	MAX	36
t_{PHL}				36
t_{PLH}	STROBE	ANY	MAX	25
t_{PHL}				36

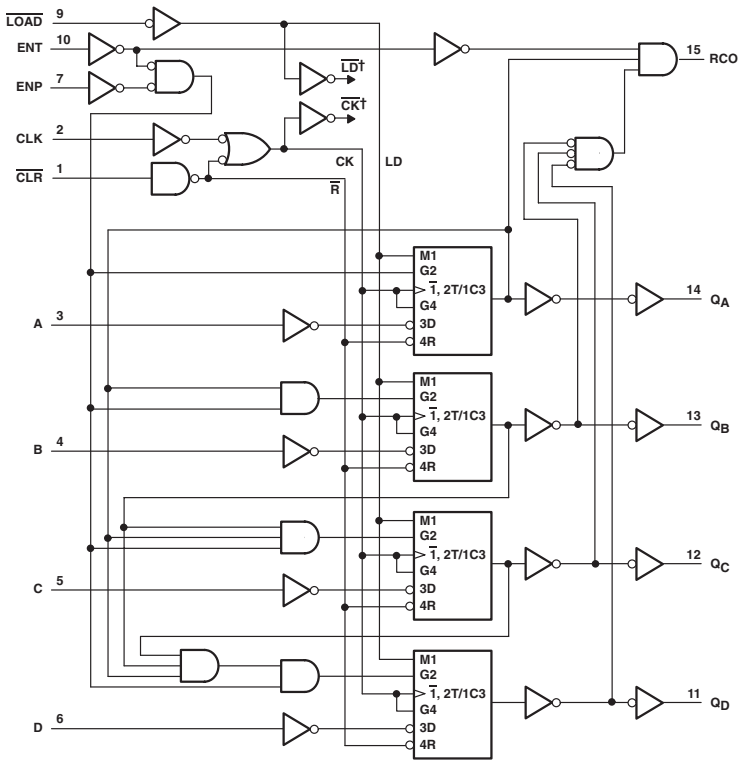
UNIT: ns

161

4-BIT SYNCHRONOUS BINARY COUNTERS

- Asynchronous Clear Function
- Carry Output for n-Bit Cascading

Logic Diagram (SN74)



† For simplicity, routing of complementary signals $\overline{LD}$ and $\overline{CK}$ is not shown on this overall logic diagram. The uses of these signals are shown on the logic diagram of the D/T flip-flops.

FUNCTION TABLE (SN74)

INPUTS					OUTPUTS				FUNCTION
$\overline{CLR}$	$\overline{LOAD}$	ENP	ENT	CLK	QA	QB	QC	QD	
L	X	X	X	X	L	L	L	L	Reset to "0"
H	L	X	X		A	B	C	D	Preset Data
H	H	X	L		No Change				No Count
H	H	L	X		No Change				No Count
H	H	H	H		Count up				Count
H	X	X	X		No Change				No Count

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	LV 3V	LV 5V	UNIT
I_{CC}	MAX	101	32	21	53	55	0.08	0.16	0.16	0.08	0.08	-	0.02	mA
I_{OH}	MAX	-0.8	-0.4	-0.4	-2	-1	4	-4	-4	-24	-24	-6	-12	mA
I_{OL}	MAX	16	8	8	20	20	-4	4	4	24	24	-6	12	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT
fmax				MIN	25	25	40	75	90	25	20	20
tw	CLOCK			MIN	25	25	-	-	7	20	24	24
	CLEAR				20	20	15	8	5	20	30	30
tsu	INPUT			MIN	20	20	15	8	5	38	18	15
	ENABLE				20	20	15	8	11.5	43	15	20
	LOAD				25	20	15	8	11.5	34	18	18
	CLEAR INACTIVE				20	25	10	8	-	31	-	-
th				MIN	0	3	0	0	2	0	3	5
t_{PLH}		CLOCK	RIPPLE CARRY (CD74HC/HCT: TC)	MAX	35	35	20	16.5	15	54	56	63
t_{PHL}					35	35	20	12.5	15	54	56	63
t_{PLH}		CLOCK	ANY Q	MAX	25	24	15	7	9.5	51	56	59
t_{PHL}					29	27	20	13	11	51	56	59
t_{PLH}		ENABLE	RIPPLE CARRY (CD74HC/HCT: TC)	MAX	16	14	13	9	8.5	49	36	48
t_{PHL}					16	14	13	8.5	8.5	49	36	48
t_{PHL}		CLEAR	ANY Q	MAX	38	28	24	13	13	53	63	75
			RIPPLE CARRY (CD74HC/HCT: TC)	MAX	-	-	23	12.5	11.5	55	63	75

PARAMETER		INPUT	OUTPUT	MAX or MIN	CD74 AC	CD74 ACT	LV 3V	LV 5V
fmax				MIN	90	80	50	85
tw	CLOCK			MIN	5.5	6.2	5	5
	CLEAR				5	6	5	5
tsu	INPUT			MIN	5	5	6.5	4.5
	ENABLE				-	-	9	6
	LOAD				6	6	9.5	6
	CLEAR INACTIVE				-	-	2.5	1.5
th				MIN	0	0	1	1
t_{PLH}		CLOCK	RIPPLE CARRY (CD74HC/HCT: TC)	MAX	16.7	16.7	23.5	14
t_{PHL}					16.7	16.7	23.5	14
t_{PLH}		CLOCK	ANY Q	MAX	16.5	16.5	18.5	11.5
t_{PHL}					16.5	16.5	18.5	11.5
t_{PLH}		ENABLE	RIPPLE CARRY (CD74HC/HCT: TC)	MAX	10.3	10.8	18	11.5
t_{PHL}					10.3	10.8	18	11.5
t_{PHL}		CLEAR	ANY Q	MAX	16.5	16.5	19.5	12.5
			RIPPLE CARRY (CD74HC/HCT: TC)	MAX	16.5	16.5	19	12

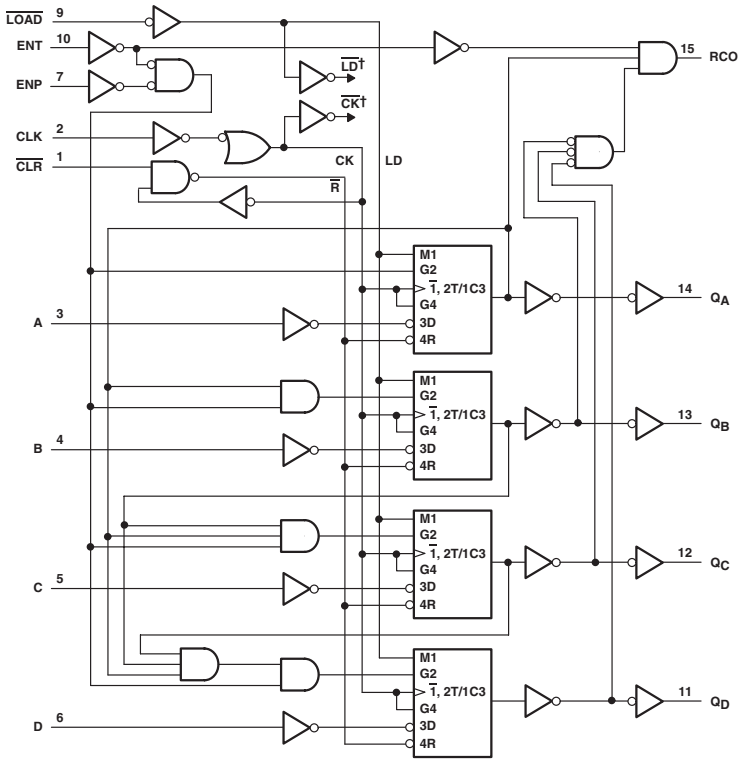
UNIT fmax : MHz, other : ns

163

4-BIT SYNCHRONOUS BINARY COUNTERS

- Synchronous Clear Function
- Carry Output for n-Bit Cascading

Logic Diagram (SN74LV)



† For simplicity, routing of complementary signals $\overline{LD}$ and $\overline{CK}$ is not shown on this overall logic diagram. The uses of these signals are shown on the logic diagram of the D/T flip-flops.

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE (SN74)

INPUTS					OUTPUTS				FUNCTION
$\overline{CLR}$	$\overline{LOAD}$	ENP	ENT	CLK	$\overline{QA}$	QB	QC	QD	
L	X	X	X	X	L	L	L	L	Reset to "0"
H	L	X	X		A	B	C	D	Preset data
H	H	X	L			No change			No count
H	H	L	X			No change			No count
H	H	H	H			Count up			Count
H	X	X	X			No change			No count

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	LV 3V	LV 5V	UNIT
I_{CC}	MAX	101	32	160	21	53	55	0.08	0.16	0.16	0.16	0.16	-	0.02	mA
I_{OH}	MAX	-0.8	-0.4	-1	-0.4	-2	-1	4	-4	-4	-24	-24	-6	-12	mA
I_{OL}	MAX	16	8	20	8	20	20	-4	4	4	24	24	-6	12	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC
fmax				MIN	25	25	40	40	75	90	25
tw	CLOCK			MIN	25	25	10	-	-	7	20
	CLEAR				20	20	10	12.5	6.7	-	-
tsu	INPUT			MIN	20	20	4	15	8	5	38
	ENABLE				20	20	12	15	8	11.5	43
	$\overline{LOAD}$				25	20	14	15	8	11.5	34
	$\overline{CLEAR}$				20	20	14	15	12	-	40
th				MIN	0	3	3	0	0	2	0
t_{PLH}		CLOCK	RIPPLE CARRY	MAX	35	35	25	20	16.5	15	54
t_{PHL}					35	35	25	20	12.5	15	54
t_{PLH}		CLOCK	ANY Q	MAX	25	24	15	15	7	9.5	51
t_{PHL}					29	27	15	20	13	11	51
t_{PLH}		ENABLE	RIPPLE CARRY	MAX	16	14	15	13	9	8.5	49
t_{PHL}					16	14	15	13	8.5	8.5	49

PARAMETER		INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	LV 3V	LV 5V
fmax				MIN	20	20	90	80	50	85
tw	CLOCK			MIN	24	24	5.5	6.2	5	5
	CLEAR				-	-	-	-	-	-
tsu	INPUT			MIN	18	15	5	5	6.5	4.5
	ENABLE				15	20	5	6	9	6
	$\overline{LOAD}$				18	18	6	7.5	9.5	6
	$\overline{CLEAR}$				20	20	6	7.5	4	3.5
th				MIN	3	5	0	0	1	1
t_{PLH}		CLOCK	RIPPLE CARRY	MAX	56	63	16.7	16.7	23.5	14
t_{PHL}					56	63	16.7	16.7	23.5	14
t_{PLH}		CLOCK	ANY Q	MAX	56	59	16.5	16.5	18.5	11.5
t_{PHL}					56	59	16.5	16.5	18.5	11.5
t_{PLH}		ENABLE	RIPPLE CARRY	MAX	36	48	10.3	10.8	18	11.5
t_{PHL}					36	48	10.3	10.8	18	11.5

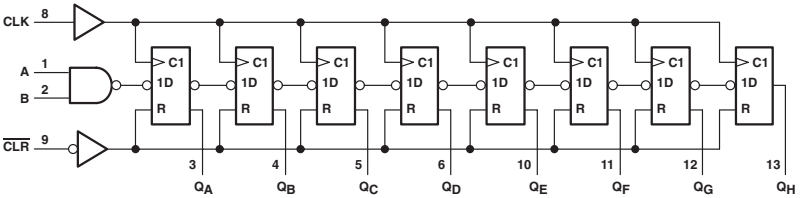
UNIT fmax : MHz, other : ns

164

8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

- AND-Gated (Enable/Disable) Serial Inputs
- Fully Buffered Clock and Serial Inputs

Logic Diagram (SN74)



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE (SN74)

INPUTS				OUTPUTS			
$\overline{CLEAR}$	CLOCK	A	B	Q_A	Q_B	...	Q_H
L	X	X	X	L	L		L
H	L	X	X	Q_{A0}	Q_{B0}		Q_{H0}
H	↑	H	H	H	Q_{An}		Q_{Gn}
H	↑	L	X	L	Q_{An}		Q_{Gn}
H	↑	X	L	L	Q_{An}		Q_{Gn}

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	LV 3V	LV 5V	UNIT
I_{CC}	MAX	54	27	24	0.08	0.16	0.16	0.16	0.16	-	0.02	mA
I_{OH}	MAX	-0.4	-0.4	-0.4	-4	-4	-4	-24	-24	-6	-12	mA
I_{OL}	MAX	8	8	8	4	4	4	24	24	6	12	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT
fmax				MIN	25	25	50	25	20	18	75	70
tw	$\overline{CLR}$ "L"			MIN	20	20	16	25	18	27	4.5	4.5
	CLK "H"			MIN	20	20	10	20	24	27	6.7	7.1
	CLK "L"			MIN	20	20	10	20	24	27	6.7	7.1
tsu	DATA			MIN	15	15	6	25	18	18	2.5	2.5
	$\overline{CLEAR}$ INACTIVE			MIN	20	20	8	25	18	18	2.5	2.5
th				MIN	5	5	2	5	4	4	2.5	3
t_{PHL}		$\overline{CLEAR}$	Q	MAX	42	36	20	51	42	57	13.9	15.8
t_{PLH}		CLOCK	Q	MAX	30	27	16	44	51	54	12.5	14.9
t_{PHL}					37	32	17	44	51	54	12.5	14.9

PARAMETER		INPUT	OUTPUT	MAX or MIN	LV 3V	LV 5V
fmax				MIN	45	75
tw	$\overline{CLR}$ "L"			MIN	5	5
	CLK "H"			MIN	5	5
	CLK "L"			MIN	5	5
tsu	DATA			MIN	6	4.5
	$\overline{CLEAR}$ INACTIVE			MIN	2.5	2.5
th				MIN	0	1
t_{PHL}		$\overline{CLEAR}$	Q	MAX	18.5	12.5
t_{PLH}		CLOCK	Q	MAX	18.5	12.5
t_{PHL}					18.5	12.5

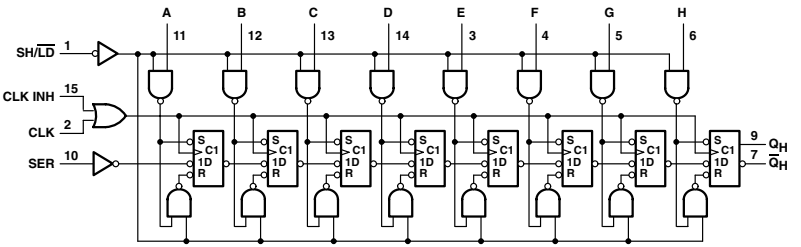
UNIT fmax : MHz, other : ns

165

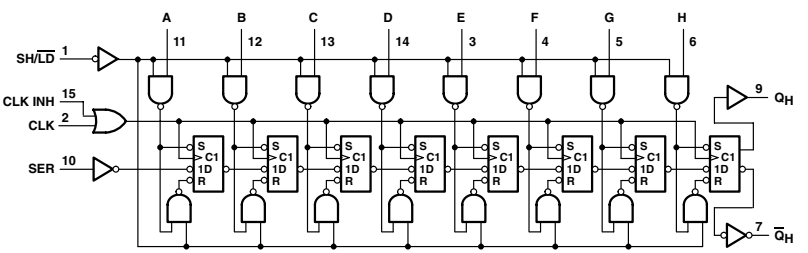
PARALLEL-LOAD 8-BIT SHIFT REGISTERS

- Complementary Outputs: Serial (QH, $\overline{Q}$H)
- Direct Overriding Load (Data) Inputs
- Parallel-to-Serial Data Conversion

Logic Diagram (SN74LV, ALS, LS)



Logic Diagram (SN74HC)



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE (SN74)

INPUTS					INTERNAL OUTPUTS		OUTPUT
SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A...H	Q_A	Q_B	Q_H
L	X	X	X	a...h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	CD74 HCT	LV 3V	LV 5V	UNIT
I_{CC}	MAX	63	30	24	0.08	0.16	0.16	-	0.02	mA
I_{OH}	MAX	-0.8	-0.4	-0.4	-4	-4	-4	-6	-12	mA
I_{OL}	MAX	16	8	8	4	4	4	6	12	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	CD74 HCT	LV 3V	LV 5V
fmax				MIN	20	25	45	25	20	18	50	85
tw	CLOCK (CD74: CP)	High		MIN	25	15	11	20	24	27	7	4
		Low		MIN	25	25	11	20	24	27	7	4
	SH/ $\overline{LD}$ "L" (CD74: $\overline{PL}$)	High		MIN	15	25	-	-	-	-	-	-
		Low		MIN	15	17	12	20	24	30	9	6
tsu	CLK INH (CD74: $\overline{CE}$)			MIN	30	30	11	25	24	30	5	3.5
	DATA				10	10	10	25	24	30	8.5	5
	SER (CD74: DS)				20	20	10	10	24	30	6	4
	SH/ $\overline{LD}$ "H"				45	45	10	20	-	-	6	4
th				MIN	0	0	4	5	11	11	0.5	1
t_{PLH}	CLOCK (CD74: CP)		Q_H or $\overline{Q}_H$ (CD74: Q_7 or $\overline{Q7}$)	MAX	24	25	13	38	50	60	16.9	13.5
t_{PHL}					31	25	14	38	50	60	16.9	13.5
t_{PLH}	SH/ $\overline{LD}$ (CD74: $\overline{PL}$)		Q_H or $\overline{Q}_H$ (CD74: Q_7 or $\overline{Q7}$)	MAX	31	35	20	38	53	60	22	13.5
t_{PHL}					40	35	22	38	53	60	22	13.5
t_{PLH}	H (CD74: D_7)		Q_H (CD74: Q_7)	MAX	17	25	13	38	45	53	20	12.5
t_{PHL}					36	30	16	38	45	53	20	12.5
t_{PLH}	H (CD74: D_7)		$\overline{Q}_H$ (CD74: Q_7)	MAX	27	30	15	38	45	53	20	12.5
t_{PHL}					27	25	16	38	45	53	20	12.5

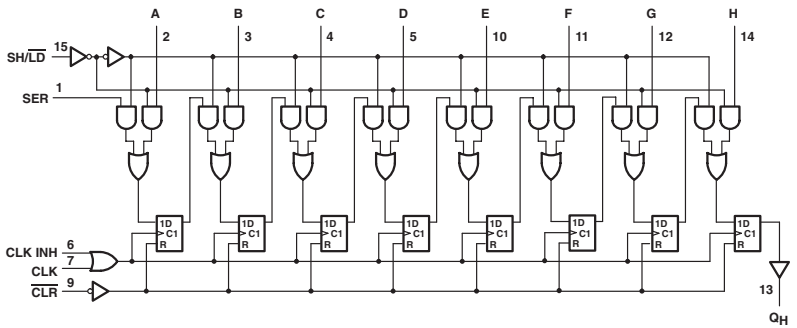
UNIT fmax : MHz, other : ns

166

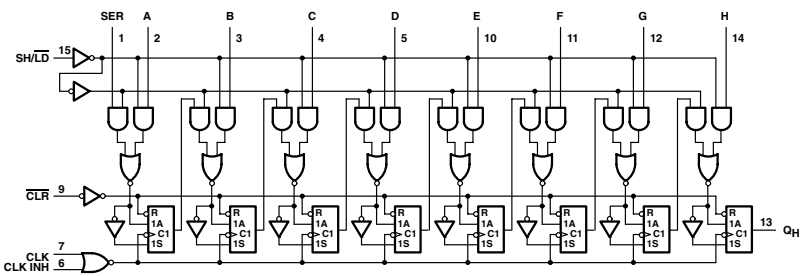
8-BIT PARALLEL-LOAD SHIFT REGISTERS

- Synchronous Load
- Direct Overriding Clear
- Parallel-to-Serial Conversion

Logic Diagram (SN74LV, HC)



Logic Diagram (SN74ALS, LS)



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE (SN74)

INPUTS						INTERNAL OUTPUTS		OUTPUT
$\overline{\text{CLEAR}}$	SHIFT/ $\overline{\text{LOAD}}$	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A...H	Q_A	Q_B	Q_H
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a...h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	F	SN74 HC	CD74 HC	CD74 HCT	LV 3V	LV 5V	UNIT
I_{CC}	MAX	127	32	24	60	0.08	0.16	0.16	-	0.02	mA
I_{OH}	MAX	-0.8	-0.4	-0.4	-1	-4	-4	-4	-6	-12	mA
I_{OL}	MAX	16	8	8	20	4	4	4	6	12	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	F	SN74 HC	CD74 HC	CD74 HCT	LV 3V	LV 5V
fmax				MIN	25	25	45	110	25	20	16	50	85
tw	CLOCK (CD74: CP)			MIN	20	20	10	3.5	20	24	30	7	4
	$\overline{\text{CLEAR}}$ ($\overline{\text{MR}}$)				20	25	9	4	25	30	53	7	5
tsu	Mode Control			MIN	30	30	16	4	36	44	45	6	4
	DATA				20	20	7	3	20	24	24	6	4.5
th				MIN	0	0	3	0	0	1	0	0	1
t_{PHL}		$\overline{\text{CLEAR}}$	QH	MAX	35	30	14	9.5	30	48	60	18.5	12
t_{PHL}		CLOCK	QH	MAX	30	25	13	14	38	48	60	21.5	13.5
t_{PLH}					26	20	12	9	38	48	60	21.5	13.5

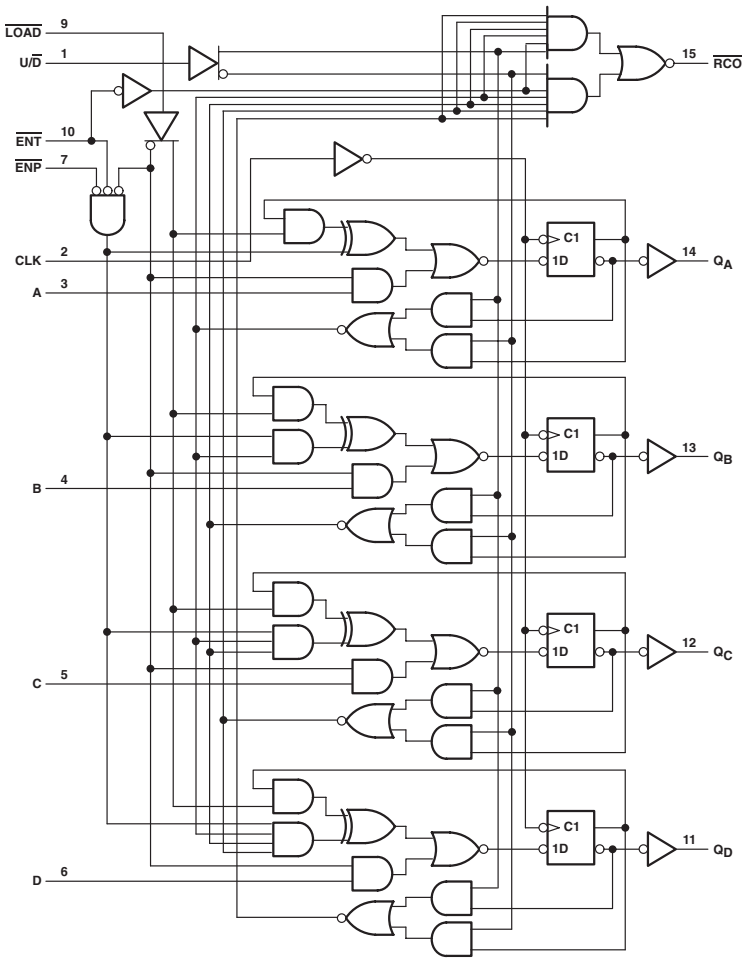
UNIT: fmax : MHz, other : ns

169

SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS

- Fully Synchronous Operation for Counting and Programming
- Internal Carry Look-Ahead Circuitry for Fast Counting
- Carry Output for n-Bit Cascading

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	S	ALS	AS	F	UNIT
I_{CC}		MAX	45	160	25	63	52	mA
I_{OH}	$\overline{RCO}$	MAX	-0.4	-1	-0.4	-2	-1	mA
	Q	MAX	-1.2	-1	-0.4	-2	-1	mA
I_{OL}	$\overline{RCO}$	MAX	8	20	8	20	20	mA
	Q	MAX	24	20	8	20	20	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	AS	F
fmax			MIN	20	40	40	75	90
t_{PLH}	CLK	$\overline{RCO}$	MAX	40	21	20	16.5	17
t_{PHL}				25	28	20	13	12.5
t_{PLH}	CLK	ANY Q	MAX	25	15	15	13	9.5
t_{PHL}				25	15	20	7	13
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$	MAX	25	12	13	9	7
t_{PHL}				20	25	16	9	9
t_{PLH}	$U/\overline{D}$	$\overline{RCO}$	MAX	35	15	19	12	12.5
t_{PHL}				25	22	19	13	12

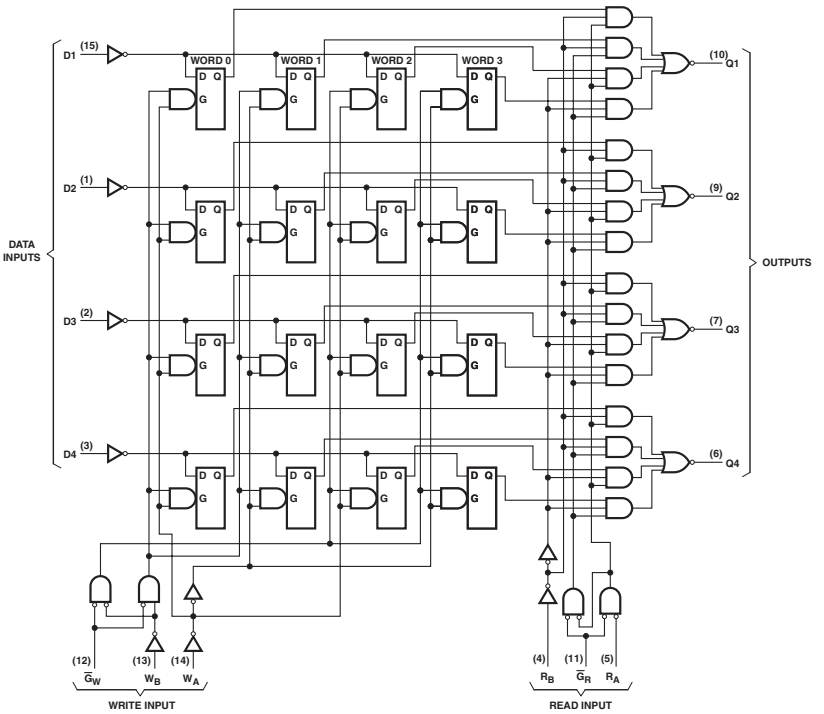
UNIT fmax : MHz, other : ns

170

4-BY-4-REGISTER FILES WITH OPEN-COLLECTOR OUTPUTS

- Separate Read/Write Addressing Permits Simultaneous Reading and Writing
- Fast Access Times: Typically 20ns
- Expandable to 1024 Words of 4 Bits

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

WRITE FUNCTION TABLE

WRITE INPUTS			OUTPUTS			
W_B	W_A	$\overline{G}_W$	0	1	2	3
L	L	L	Q = D	Q_O	Q_O	Q_O
L	H	L	Q_O	Q = D	Q_O	Q_O
H	L	L	Q_O	Q_O	Q = D	Q_O
H	H	L	Q_O	Q_O	Q_O	Q = D
X	X	H	Q_O	Q_O	Q_O	Q_O

READ FUNCTION TABLE

READ INPUTS			OUTPUTS			
R_B	R_A	$\overline{G}_R$	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	H	H	H	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	UNIT
I_{CC}	MAX	150	40	mA
V_{OH}	MAX	5.5	5.5	V
I_{OL}	MAX	16	8	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS
fmax				MIN		
tw				MIN	25	25
tsu	D			MIN	10	10
	W				15	15
th	D			MIN	15	15
	W				5	5
t_{PLH}		READ ENABLE	Q	MAX	15	30
t_{PHL}					30	30
t_{PLH}		READ SELECT	Q	MAX	35	40
t_{PHL}					40	40
t_{PLH}		WRITE ENABLE	Q	MAX	40	45
t_{PHL}					45	40
t_{PLH}		DATA	Q	MAX	30	45
t_{PHL}					45	35

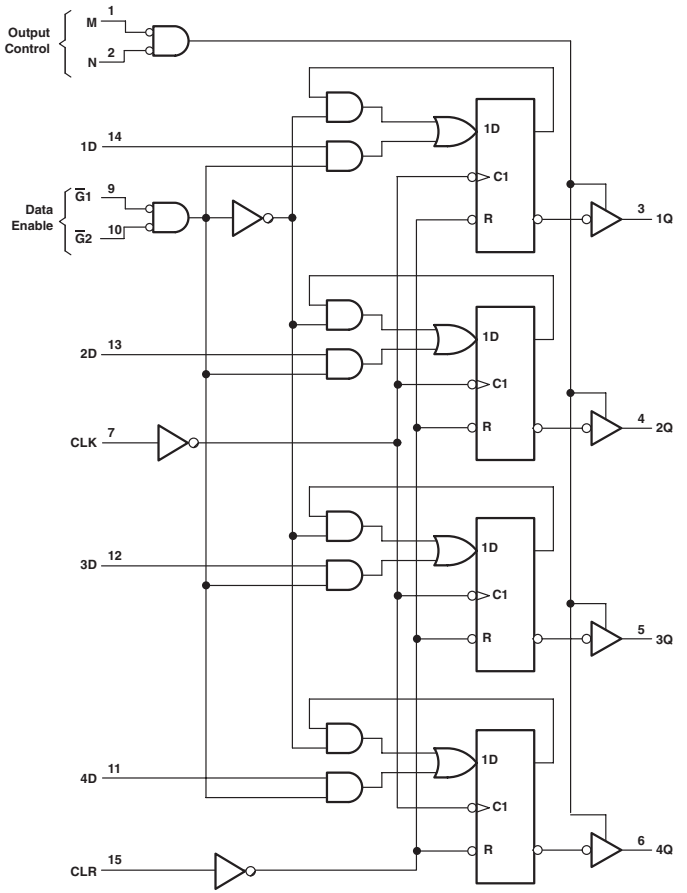
UNIT fmax : MHz, other : ns

173

4-BIT D-TYPE REGISTERS WITH 3-STATE OUTPUTS

- 3-State Outputs Interface Directly
- Fully Independent Clock Virtually

Logic Diagram (SN74LS)



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE (SN74LS)

INPUTS					OUTPUT Q
CLEAR	CLOCK	DATA ENABLE $\overline{G1}$	DATA ENABLE $\overline{G2}$	DATA D	
H	X	X	X	X	L
L	L	X	X	X	Q_0
L	↑	H	X	X	Q_0
L	↑	X	H	X	Q_0
L	↑	L	L	L	L
L	↑	L	L	H	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	72	24	0.08	0.16	0.16	mA
I_{OH}	MAX	-5.2	-2.6	-6	-6	-6	mA
I_{OL}	MAX	16	24	6	6	6	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT
fmax				MIN	25	25	25	20	13
tw				MIN	20	25	20	24	38
tsu	DATA ENABLE			MIN	17	35	25	18	18
	DATA				10	17	25	18	27
	CLR INACTIVE			MIN	10	10	23	-	-
th	DATA ENABLE			MIN	2	0	0	0	0
	DATA				10	3	0	3	0
t_{PHL}		CLEAR	Q	MAX	27	35	38	53	66
t_{PLH}		CLOCK (CD74: CP)	Q	MAX	43	25	38	60	60
t_{PHL}					31	30	38	60	60
t_{PZH}		ENABLE	Q	MAX	30	23	38	45	45
t_{PZL}					30	27	38	45	45
t_{PHZ}		DISABLE	Q	MAX	14	20	38	45	-
t_{PLZ}					20	17	38	45	-

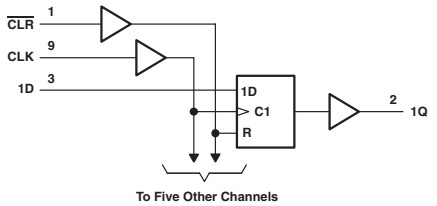
UNIT fmax : MHz, other : ns

174

HEX D-TYPE FLIP-FLOPS WITH CLEAR

- Buffered Clock and Direct Clear Inputs
- Fully Buffered Outputs for Maximum Isolation from External Disturbances

Logic Diagram (SN74)



FUNCTION TABLE (SN74)

INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
L	L	X	Q_0

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	UNIT
I_{CC}	MAX	65	26	144	19	45	55	0.08	0.16	mA
I_{OH}	MAX	-0.8	-0.4	-1	-0.4	-2	-1	-4	-4	mA
I_{OL}	MAX	16	8	20	8	20	20	4	4	mA

PARAMETER	MAX or MIN	CD74 HCT	CD74 AC	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	UNIT
I_{CC}	MAX	0.16	0.16	0.16	0.04	0.04	-	0.02	mA
I_{OH}	MAX	-4	-24	-24	-8	-8	-6	-12	mA
I_{OL}	MAX	4	24	24	8	8	6	12	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC
fmax				MIN	25	30	75	50	100	80	25	20
tw	CLR (MR) LOW			MIN	20	20	10	10	5	5	20	24
	CLK (CP) HIGH			MIN	20	20	7	10	4	4	20	24
	CLK (CP) LOW				20	20	7	10	6	6	20	24
tsu	DATA INPUT			MIN	20	20	5	10	4	4.5	25	18
	CLR (MR) INACTIVE			MIN	25	25	5	6	6	5	25	-
th				MIN	5	5	3	0	1	1	0	5
t_{PLH}		CLR (MR)	ANY Q	MAX	25	-	-	18	-	-	40	45
t_{PHL}					35	35	22	23	14	15	40	45
t_{PLH}		CLK (CP)	ANY Q	MAX	30	30	12	15	8	9	40	50
t_{PHL}					35	30	17	17	10	11	40	50

PARAMETER		INPUT	OUTPUT	MAX or MIN	CD74 HCT	CD74 AC	CD74 ACT	AHC	AHCT	LV 3V	LV 5V
fmax				MIN	17	95	80	80	65	50	80
tw	CLR (MR) LOW			MIN	38	4	4	5	5	5	5
	CLK (CP) HIGH			MIN	30	5.2	6.2	5	5	5	5
	CLK (CP) LOW				30	5.2	6.2	5	5	5	5
tsu	DATA INPUT			MIN	24	2	2	4.5	5	6	4.5
	CLR (MR) INACTIVE			MIN	-	-	-	2.5	3.5	3	2.5
th				MIN	5	3	2.5	0.5	0	0	0.5
t_{PLH}		CLR (MR)	ANY Q	MAX	66	14.5	15.5	-	-	17	11
t_{PHL}					66	14.5	15.5	11	13	17	11
t_{PLH}		CLK (CP)	ANY Q	MAX	60	13.5	14	10.5	10	16.5	10.5
t_{PHL}					60	13.5	14	10.5	10	16.5	10.5

UNIT fmax : MHz, other : ns

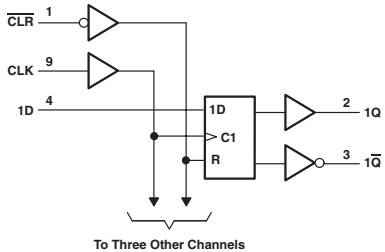
: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

175

QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

- Complementary Outputs (Q, $\overline{Q}$)
- Buffered Clock and Direct Clear Inputs
- Asynchronous Clear Function

Logic Diagram (SN74)



FUNCTION TABLE (SN74)

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	CD74 AC	CD74 ACT	UNIT
I_{CC}	MAX	45	18	96	14	34	34	0.08	0.16	0.16	0.08	0.16	0.16	mA
I_{OH}	MAX	-0.8	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-24	-24	-24	mA
I_{OL}	MAX	16	8	20	8	20	20	4	4	4	24	24	24	mA

PARAMETER	MAX or MIN	LV 3V	LV 5V	UNIT
I_{CC}	MAX	-	0.02	mA
I_{OH}	MAX	-6	-12	mA
I_{OL}	MAX	6	12	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC
fmax				MIN	25	30	75	50	100	100	25	20
tw	$\overline{CLR}$ ($\overline{MR}$) LOW			MIN	20	20	10	10	5	5	20	24
	CLK (CP) HIGH				20	20	7	10	4	4	20	24
	CLK (CP) LOW				20	20	7	10	5	5	20	24
tsu	DATA INPUT			MIN	20	20	5	10	3	3	25	24
	$\overline{CLR}$ ($\overline{MR}$) INACTIVE				25	25	5	6	6	5	25	-
th				MIN	5	5	3	0	1	1	0	5
t_{PLH}		$\overline{CLR}$ ($\overline{MR}$)	ANY Q or $\overline{Q}$	MAX	25	30	15	18	9	9	38	53
t_{PHL}					35	30	22	23	13	13	38	53
t_{PLH}		CLK (CP)	ANY Q or $\overline{Q}$	MAX	30	25	12	15	7.5	7.5	38	53
t_{PHL}					35	25	17	17	10	9.5	38	53

PARAMETER		INPUT	OUTPUT	MAX or MIN	CD74 HCT	AC 11	CD74 AC	CD74 ACT	LV 3V	LV 5V
fmax				MIN	16	125	100	114	45	75
tw	$\overline{CLR}$ ($\overline{MR}$) LOW			MIN	30	4	4	4	5	5
	CLK (CP) HIGH				30	4	5	5	5	5
	CLK (CP) LOW				30	4	5	5	5	5
tsu	DATA INPUT			MIN	30	5.5	2	2	5	4
	$\overline{CLR}$ ($\overline{MR}$) INACTIVE				-	5.5	-	-	5	5
th				MIN	5	0.5	2	2	1	1
t_{PLH}		$\overline{CLR}$ ($\overline{MR}$)	ANY Q or $\overline{Q}$	MAX	53	6.8	12.2	13	15.5	9.5
t_{PHL}					53	9.3	12.2	13	15.5	9.5
t_{PLH}		CLK (CP)	ANY Q or $\overline{Q}$	MAX	50	6.9	12.2	11.5	17	10.5
t_{PHL}					50	9.3	12.2	11.5	17	10.5

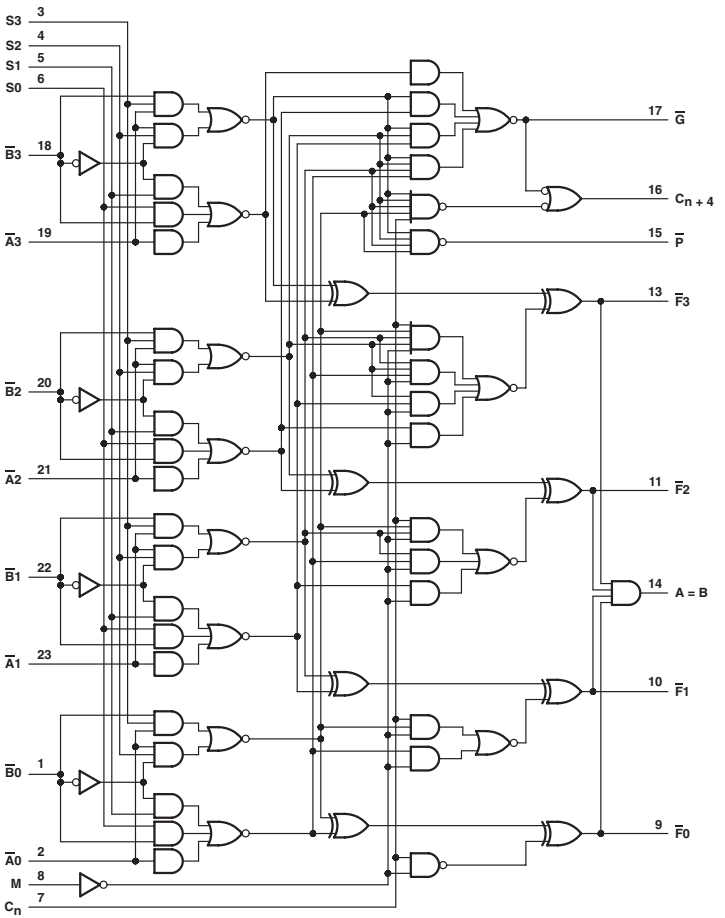
UNIT fmax : MHz, other : ns

181

ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

- Full Look-Ahead for High-Speed Operations on Long Words
- Input Clamping Diodes Minimize Transmission-Line Effects

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE (ACTIVE LOW)

SELECTION				ACTIVE-LOW DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTION	Cn = L (no carry)	Cn = H (with carry)
L	L	L	L	$F = \overline{A}$	F = A MINUS 1	F = A
L	L	L	H	$F = \overline{AB}$	F = AB MINUS 1	F = AB
L	L	H	L	$F = \overline{A} + B$	F = AB MINUS 1	F = $A\overline{B}$
L	L	H	H	F = 1	F = MINUS 1(2's COMP)	F = 0
L	H	L	L	$F = \overline{A + B}$	F = A PLUS (A + $\overline{B}$)	F = A PLUS (A + $\overline{B}$) PLUS 1
L	H	L	H	$F = \overline{B}$	F = AB PLUS (A + $\overline{B}$)	F = AB PLUS (A + $\overline{B}$) PLUS 1
L	H	H	L	$F = \overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	$F = A + \overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
H	L	L	L	$F = \overline{AB}$	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H	L	L	H	F = A ⊕ B	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = A$\overline{B}$ PLUS (A + B)	F = A$\overline{B}$ PLUS (A + B) PLUS 1
H	L	H	H	F = A + B	F = (A + B)	F = (A + B) PLUS 1
H	H	L	L	F = 0	F = A PLUS A*	F = A PLUS A PLUS 1
H	H	L	H	$F = A\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H	H	H	L	F = AB	F = A$\overline{B}$ PLUS A	F = A$\overline{B}$ PLUS A PLUS 1
H	H	H	H	F = A	F = A	F = A PLUS 1

*Each bit is shifted to the next more significant position.

FUNCTION TABLE (ACTIVE HIGH)

SELECTION				ACTIVE-HIGH DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTION	$\overline{Cn}$ = H (no carry)	$\overline{Cn}$ = L (with carry)
L	L	L	L	$F = \overline{A}$	F = A	F = A PLUS 1
L	L	L	H	$F = \overline{A + B}$	F = A + B	F = (A + B) PLUS 1
L	L	H	L	$F = \overline{AB}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
L	L	H	H	F = 0	F = MINUS 1(2's COMPL)	F = 0
L	H	L	L	$F = \overline{AB}$	F = A PLUS A$\overline{B}$	F = A PLUS A$\overline{B}$ PLUS 1
L	H	L	H	$F = \overline{B}$	F = (A + B) PLUS A$\overline{B}$	F = (A + B) PLUS A$\overline{B}$ PLUS 1
L	H	H	L	F = A ⊕ B	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	$F = A\overline{B}$	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
H	L	L	L	$F = \overline{A} + B$	F = A PLUS AB	F = A PLUS AB PLUS 1
H	L	L	H	$F = \overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = (A + $\overline{B}$) PLUS AB	F = (A + $\overline{B}$) PLUS AB PLUS 1
H	L	H	H	F = AB	F = AB MINUS 1	F = AB
H	H	L	L	F = 1	F = A PLUS A*	F = A PLUS A PLUS 1
H	H	L	H	$F = A + \overline{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) PLUS A	F = (A + $\overline{B}$) PLUS A PLUS 1
H	H	H	H	F = A	F = A MINUS 1	F = A

*Each bit is shifted to the next more significant position.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	TTL	LS	S	AS	UNIT
I_{CC}		MAX	150	37	220	200	mA
I_{OH}	All outputs except A = B	MAX	-0.8	-0.4	-1	-2	mA
	$\overline{G}$		-	-	-	-3	mA
I_{OL}	All outputs except $\overline{G}$	MAX	16	8	20	20	mA
	$\overline{G}$		16	8	20	48	mA

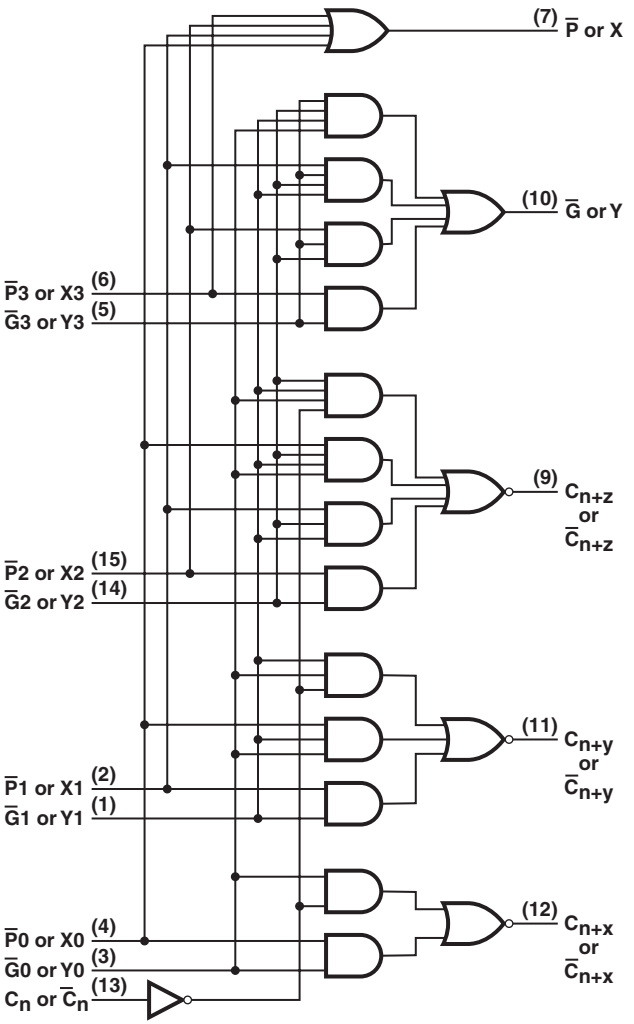
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	AS
t_{PLH}	C_n	$C_n + 4$	MAX	18	27	10.5	9
t_{PHL}				19	20	10.5	9
t_{PLH}	$\overline{A}$, $\overline{B}$	$C_n + 4$	MAX	43	38	18.5	12
t_{PHL}				41	38	18.5	12
t_{PLH}	C_n	$\overline{F}$	MAX	19	26	12	9
t_{PHL}				18	20	12	9
t_{PLH}	$\overline{A_i}$, $\overline{B_i}$	$\overline{F_i}$	MAX	42	32	16.5	9.5
t_{PHL}				32	20	16.5	8

UNIT: ns

LOOK-AHEAD CARRY GENERATOR

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

$\overline{G}$ OUTPUTS

INPUTS							OUTPUT
$\overline{G}3$	$\overline{G}2$	$\overline{G}1$	$\overline{P}3$	$\overline{P}2$	$\overline{P}1$	$\overline{P}0$	$\overline{G}$
L	X	X	X	X	X	X	L
X	L	X	X	L	X	X	L
X	X	L	X	L	L	X	L
X	X	X	L	L	L	L	L
All other combinations							H

$\overline{P}$ OUTPUTS

INPUTS				OUTPUT
$\overline{P}3$	$\overline{P}2$	$\overline{P}1$	$\overline{P}0$	$\overline{P}$
L	L	L	L	L
All other combinations				H

C_{n+x} OUTPUTS

INPUTS			OUTPUT
$\overline{G}0$	$\overline{P}0$	Cn	C_{n+x}
L	X	X	H
X	L	H	H
All other combinations			L

C_{n+y} OUTPUTS

INPUTS					OUTPUT
$\overline{G}1$	$\overline{G}0$	$\overline{P}1$	$\overline{P}0$	C_n	C_{n+y}
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
All other combinations					L

C_{n+z} OUTPUTS

INPUTS							OUTPUT
$\overline{G}2$	$\overline{G}1$	$\overline{G}0$	$\overline{P}2$	$\overline{P}1$	$\overline{P}0$	C_n	C_{n+z}
L	X	X	X	X	X	X	H
X	L	X	L	X	X	X	H
X	X	L	L	L	X	X	H
X	X	X	L	L	L	H	H
All other combinations							L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	S	AS	UNIT
I_{CC}	MAX	72	109	36	mA
I_{OH}	MAX	-0.8	-1	-2	mA
I_{OL}	MAX	16	20	20	mA

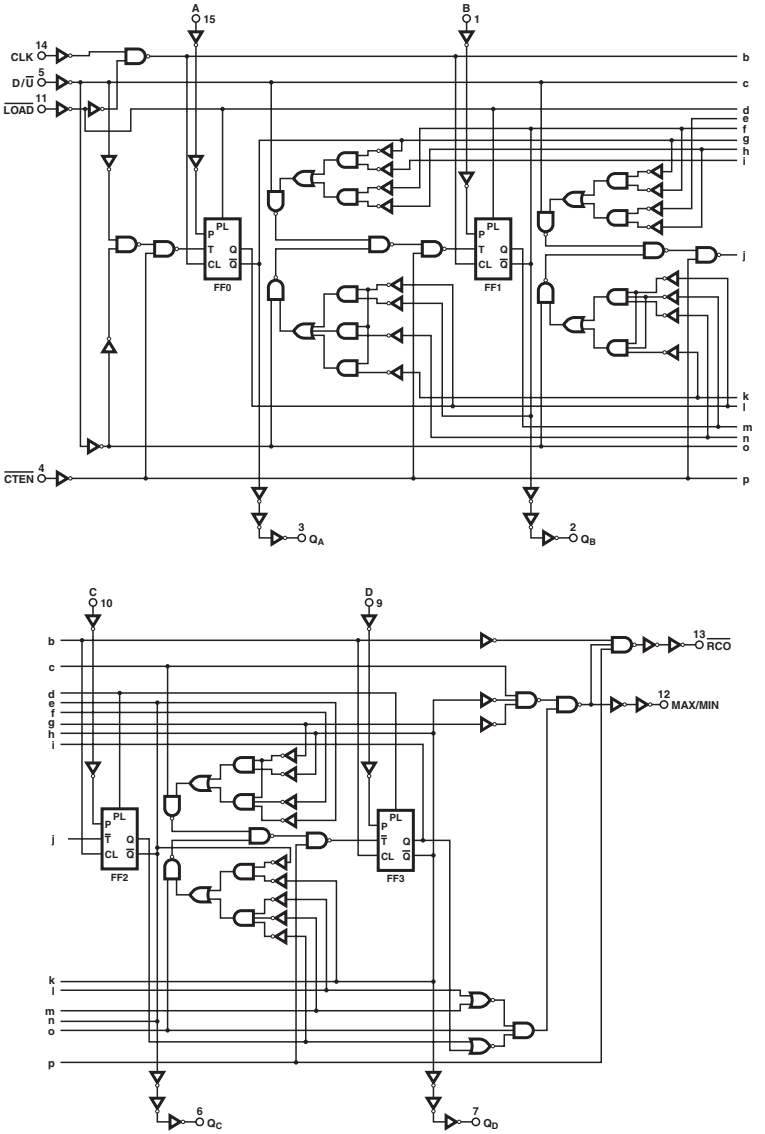
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	S	AS
t_{PLH}	Cn	Cn + X, Cn + Y or Cn + Z	MAX	10	10	10
t_{PHL}				10.5	10.5	9.5
t_{PLH}	P or $\overline{G}$	Cn + X, Cn + Y or Cn + Z	MAX	7	7	10.5
t_{PHL}				7	7	6
t_{PLH}	P or $\overline{G}$	$\overline{G}$	MAX	7.5	7.5	12
t_{PHL}				10.5	10.5	8
t_{PLH}	$\overline{P}$	$\overline{P}$	MAX	6.5	6.5	7.5
t_{PHL}				10	10	6

UNIT: ns

SYNCHRONOUS 4-BIT UP/DOWN DECADE AND BINARY COUNTERS

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS				FUNCTION
$\overline{LOAD}$	$\overline{CTEN}$	D/$\overline{U}$	CLK	
H	L	L	⌐‾	Count up
H	L	H	⌐‾	Count down
L	X	X	X	Asynchronous preset
H	H	X	X	No change

D/$\overline{U}$ or $\overline{CTEN}$ should be changed only when clock is high.
X = Don't care
⌐‾ Low-to-high clock transition

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	UNIT
I_{CC}	MAX	105	35	22	0.08	0.16	mA
I_{OH}	MAX	-0.8	-0.4	-0.4	-4	-4	mA
I_{OL}	MAX	16	8	8	4	4	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC
fmax			MIN	20	20	25	17	20
tw	CLK		MIN	25	25	20	30	30
	$\overline{LOAD}$			35	35	20	30	24
tsu	Data , high or low		MIN	20	20	20	38	18
th	Data hold time		MIN	0	5	5	5	2
t_{PLH}	$\overline{LOAD}$	Q	MAX	33	33	30	66	59
t_{PHL}				50	50	30	66	59
t_{PLH}	DATA	Q	MAX	22	32	21	60	53
t_{PHL}				50	40	21	60	53
t_{PLH}	CLK	$\overline{RCO}$	MAX	20	20	20	30	38
t_{PHL}				24	24	20	30	38
t_{PLH}	CLK	Q	MAX	24	24	18	48	51
t_{PHL}				36	36	18	48	51
t_{PLH}	CLK	MAX/MIN	MAX	42	42	31	63	63
t_{PHL}				52	52	31	63	63
t_{PLH}	D/$\overline{U}$	$\overline{RCO}$	MAX	45	45	37	57	45
t_{PHL}				45	45	28	57	45
t_{PLH}	D/$\overline{U}$	MAX/ MIN	MAX	33	33	25	48	50
t_{PHL}				33	33	25	48	50

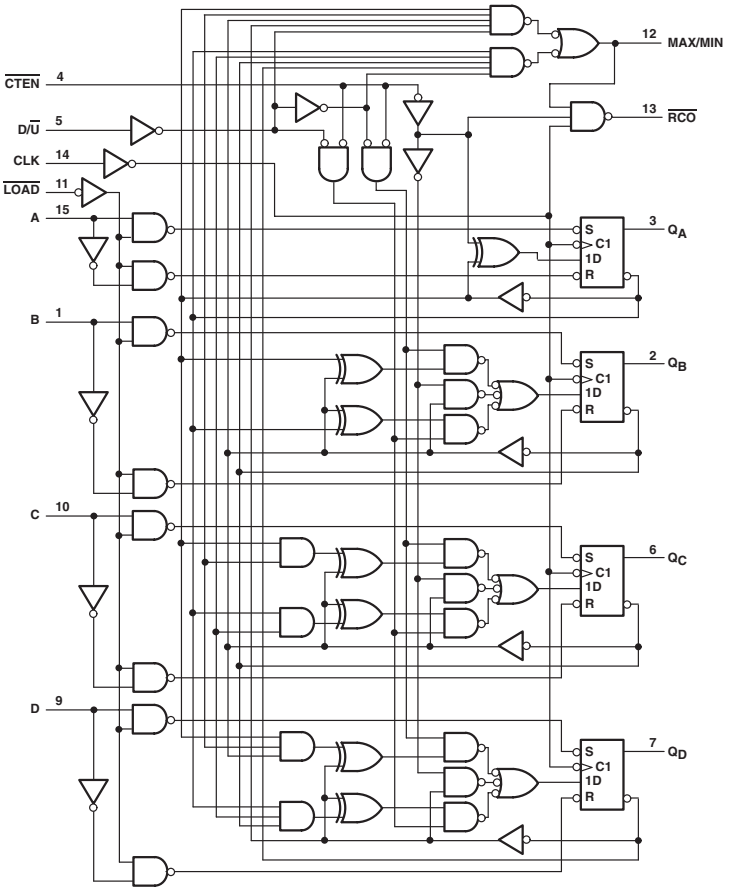
UNIT fmax : MHz other : ns

191

4-BIT SYNCHRONOUS UP/DOWN BINARY COUNTERS

- Count Enable Control Input
- Ripple Clock Output for Cascading
- Asynchronously Presentable with Load Control

Logic Diagram (SN74HC)



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	105	35	22	0.08	0.16	0.16	mA
I_{OH}	MAX	-0.8	-0.4	-0.4	-4	-4	-4	mA
I_{OL}	MAX	16	8	8	4	4	4	mA

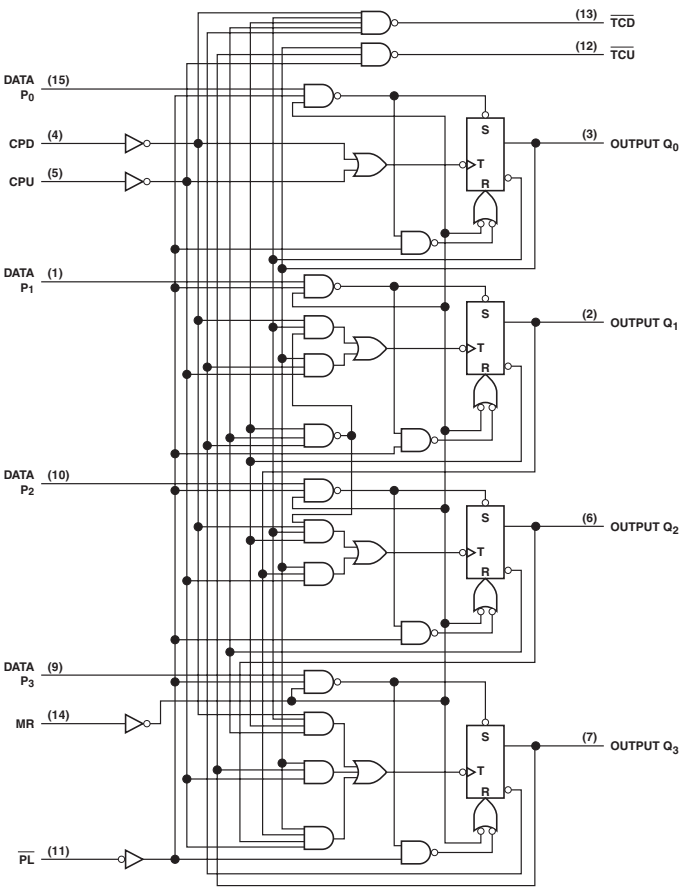
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	CD74 HCT
fmax				MIN	20	20	30	17	20	20
tw	CLK			MIN	25	25	16.5	30	30	30
	$\overline{\text{LOAD}}$ low				35	35	20	30	24	24
tsu	DATA			MIN	20	20	20	38	18	18
th	DATA			MIN	0	5	5	5	2	2
t_{PLH}		$\overline{\text{LOAD}}$	QA, QB QC, QD	MAX	33	33	30	66	59	60
t_{PHL}					50	50	30	66	59	60
t_{PLH}		DATA A, B, C, D	QA, QB QC, QD	MAX	22	32	21	60	53	57
t_{PHL}					50	40	21	60	53	57
t_{PLH}		CLK	RIPPLE CLK	MAX	20	20	20	30	38	53
t_{PHL}					24	24	20	30	38	53
t_{PLH}		CLK	QA, QB QC, QD	MAX	24	24	18	48	51	41
t_{PHL}					36	36	18	48	51	41
t_{PLH}		CLK	MAX or MIN	MAX	42	42	31	63	63	63
t_{PHL}					52	52	31	63	63	63
t_{PLH}		D/$\overline{U}$	RIPPLE CLK	MAX	45	45	37	57	45	45
t_{PHL}					45	45	28	57	45	45
t_{PLH}		D/$\overline{U}$	MAX or MIN	MAX	33	33	25	48	50	57
t_{PHL}					33	33	25	48	50	57

UNIT fmax : MHz, other : ns

PRESETTABLE SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

TRUE TABLE

CLOCK UP	CLOCK DOWN	RESET	PARALLEL LOAD	FANCTION
↑	H	L	H	Count Up
H	↑	L	H	Count Down
X	X	H	X	Reset
X	X	L	L	Load Preset inputs

NOTE: H = High Voltage Level, L = Low Voltage Level, X = Don't Care, ↑ = Transition from Low to High Level

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	UNIT
I_{CC}	MAX	0.16	mA
I_{OH}	MAX	-4	mA
I_{OL}	MAX	4	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC
t_w	CPU, CPD		MIN	35
	$\overline{PL}$			24
	MR			30
t_{su}	Pn to $\overline{PL}$		MIN	24
t_h	Pn to $\overline{PL}$		MIN	0
	CPD to CPU, CPD to CPU			24
t_{PLH}	CPU	$\overline{TCU}$	MAX	38
t_{PHL}				38
t_{PLH}	CPD	$\overline{TCD}$	MAX	38
t_{PHL}				38
t_{PLH}	CPU	Qn	MAX	65
t_{PHL}				65
t_{PLH}	CPD	Qn	MAX	65
t_{PHL}				65
t_{PLH}	$\overline{PL}$	Qn	MAX	66
t_{PHL}				66
t_{PHL}	MR	Qn	MAX	60

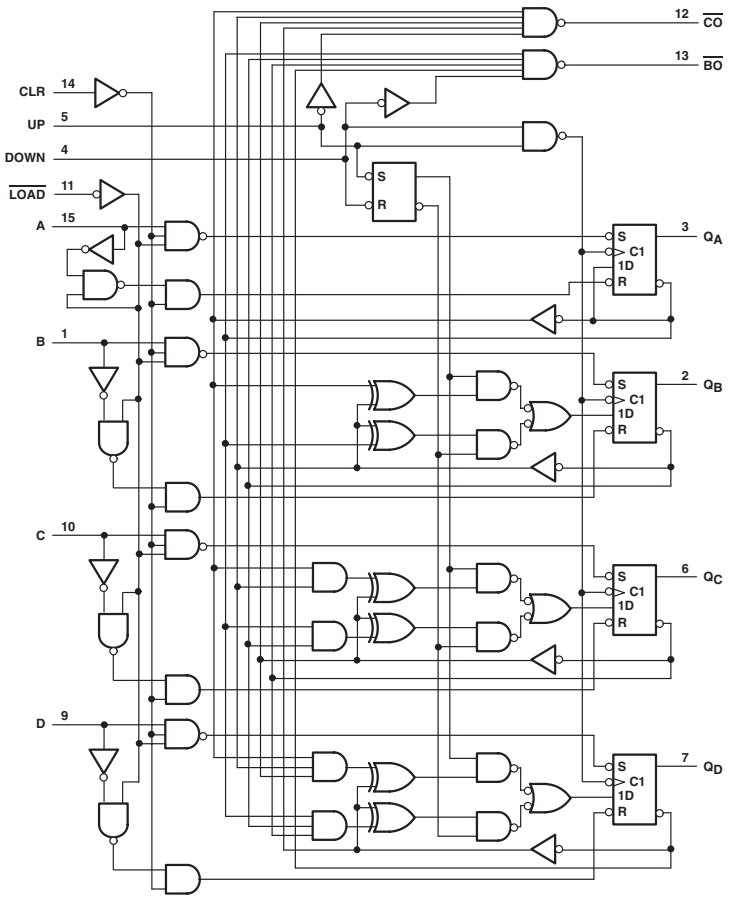
UNIT:ns

193

4-BIT SYNCHRONOUS UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

- Parallel Asynchronous Load for Modulo-N Count Lengths
- Asynchronous Clear

Logic Diagram (SN74)



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	F	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	102	34	22	54	0.08	0.16	0.16	mA
I_{OH}	MAX	-0.4	-0.4	-0.4	-1	-4	-4	-4	mA
I_{OL}	MAX	16	8	8	20	4	4	4	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	F	SN74 HC	CD74 HC	CD74 HCT
fmax				MIN	25	25	30	85	17	17	15
tw				MIN	20	20	20	4	30	30	35
tsu	DATA			MIN	20	20	20	3.5	28	22	22
th	DATA			MIN	0	5	5	2.5	5	0	0
t_{PLH}		UP (CD74: CPU)	$\overline{CO}$	MAX	26	26	16	9	41	38	41
t_{PHL}					24	24	18	9	41	38	41
t_{PLH}		DOWN (CD74: CPD)	$\overline{BO}$	MAX	24	24	16	9	41	38	41
t_{PHL}					24	24	18	9	41	38	41
t_{PLH}		UP or DOWN (CD74: CPU or CPD)	ANY Q	MAX	38	38	19	9	63	65	60
t_{PHL}					47	47	17	13	63	65	60
t_{PLH}		$\overline{LOAD}$ (CD74: $\overline{PL}$)	ANY Q	MAX	40	40	30	11	65	66	69
t_{PHL}					40	40	28	13	65	66	69
t_{PHL}		CLR (CD74: MR)	ANY Q	MAX	35	35	17	12	60	60	65

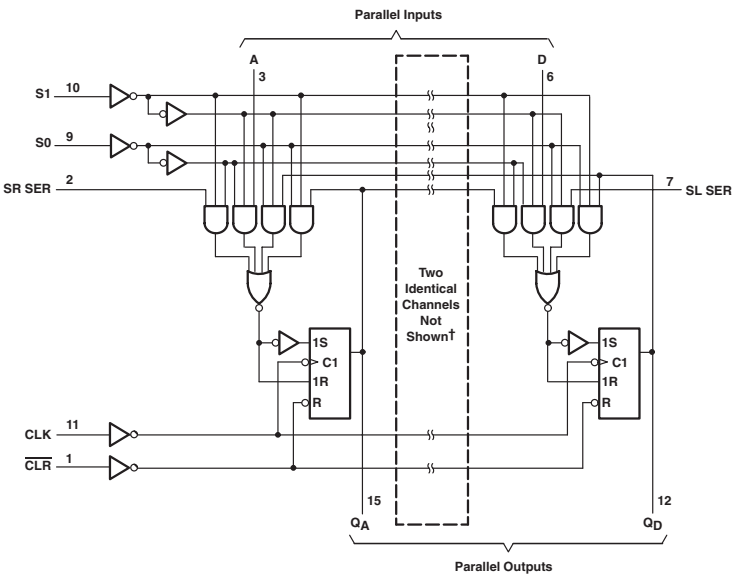
UNIT fmax : MHz, other : ns

194

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

- Direct Overriding Clear
- Parallel-to-Serial, Serial-to-Parallel Conversions
- Left or Right Shifts

Logic Diagram (SN74)



† I/O ports not shown: Q_B (14) and Q_C (13)

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE (SN74)

INPUTS										OUTPUTS			
$\overline{CLEAR}$	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	AS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	63	23	135	53	0.1	0.16	0.16	mA
I_{OH}	MAX	-0.8	-0.4	-1	-2	-4	-4	-4	mA
I_{OL}	MAX	16	8	20	20	4	4	4	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	S	AS	SN74 HC	CD74 HC	CD74 HCT
fmax				MIN	25	25	70	80	25	20	18
tw	$\overline{CLR}$ ($\overline{MR}$)			MIN	20	20	12	4.5	20	24	24
	CLK (CP) "H"				20	20	7	4	20	24	24
	CLK (CP) "L"				20	20	7	7	20	24	24
tsu	Mode Control			MIN	30	30	11	9.5	25	24	30
	DATA				20	20	5	4	25	21	21
	CLR (MR) INACTIVE				25	25	9	6	-	-	-
th				MIN	0	0	3	0.5	0	0	0
t_{PHL}		$\overline{CLEAR}$ ($\overline{MR}$)	ANY	MAX	30	30	18.5	12	38	42	60
t_{PLH}		CLOCK (CP)	ANY	MAX	22	22	12	7	36	53	56
t_{PHL}					26	26	16.5	7	36	53	56

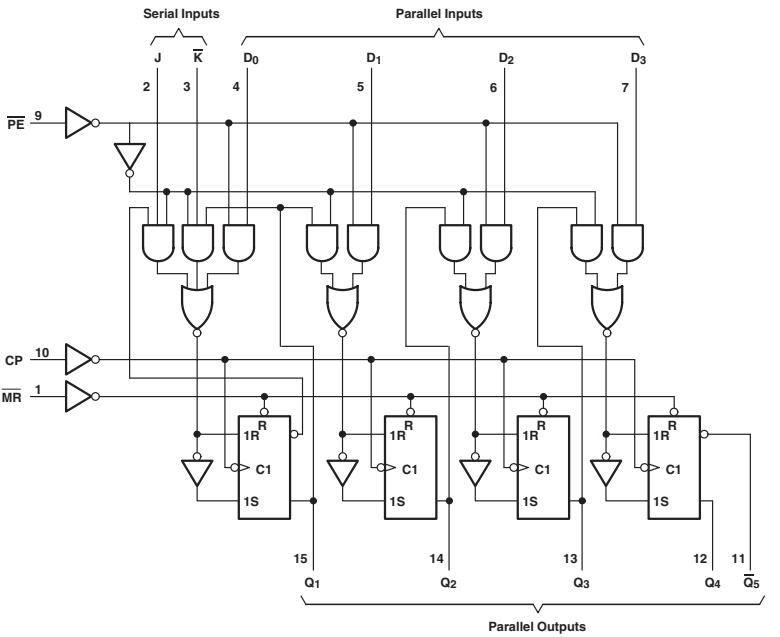
UNIT fmax : MHz, other : ns

195

4-BIT PARALLEL-ACCESS SHIFT REGISTERS

- Direct Overriding Clear
- Parallel-to-Serial, Serial-to-Parallel Conversions

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

TRUTH TABLE

OPERATING MODES	INPUTS						OUTPUT				
	$\overline{MR}$	CP	$\overline{PE}$	J	$\overline{K}$	Dn	Q_0	Q_1	Q_2	Q_3	$\overline{Q}_3$
Asynchronous Reset	L	X	X	X	X	X	L	L	L	L	H
Shift, Set First Stage	H	↑	h	h	h	X	H	q_0	q_1	q_2	$\overline{q}_2$
Shift, Reset First Stage	H	↑	h	l	l	X	L	q_0	q_1	q_2	$\overline{q}_2$
Shift, Toggle First Stage	H	↑	h	h	l	X	$\overline{q}_0$	q_0	q_1	q_2	$\overline{q}_2$
Shift, Retain First Stage	H	↑	h	l	h	X	q_0	q_0	q_1	q_2	$\overline{q}_2$
Parallel Load	H	↑	l	X	X	dn	d_0	d_1	d_2	d3	$\overline{d2}$

H = High Voltage Level
L = Low Voltage Level,
X = Don't Care
↑ = Transition from Low to High Level
l = Low Voltage Level One Set-up Time Prior to the Low to High Clock Transition
h = Low Voltage Level One Set-up Time prior to the High to Low Clock Transition,
dn (q_n) = Lower Case Letters Indicate the State of the Referenced Input (or output) One Set-up Time Prior to the Low to High Clock Transition.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	AS	SN74 HC	CD74 HC	UNIT
I_{CC}	MAX	63	21	109	57	0.1	0.16	mA
I_{OH}	MAX	-0.8	-0.4	-1	-2	-4	-4	mA
I_{OL}	MAX	16	8	20	20	4	4	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	S	AS	SN74 HC	CD74 HC
fmax				MIN	30	30	70	70	25	20
tw	Clock			MIN	16	16	7	4	20	24
	$\overline{MR}$				12	12	12	7.2	20	24
tsu	$\overline{PE}$			MIN	25	25	11	8	25	30
	Serial & Pararel Data				20	15	5	3.5	25	-
	Clear Inactive Data				25	25	9	6	25	-
TRELEASE				MAX	10	20	6	-	-	-
th				MIN	0	0	3	1	0	3
t_{PHL}		$\overline{MR}$	QA, QD	MAX	30	30	18.5	11.5	38	45
t_{PLH}		Clock		MAX	22	22	12	8.5	36	53
t_{PHL}					26	26	16.5	10.5	36	53

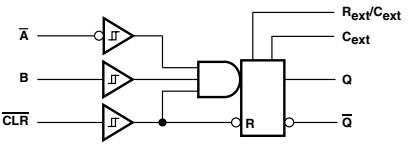
UNIT fmax : MHz, other : ns

221

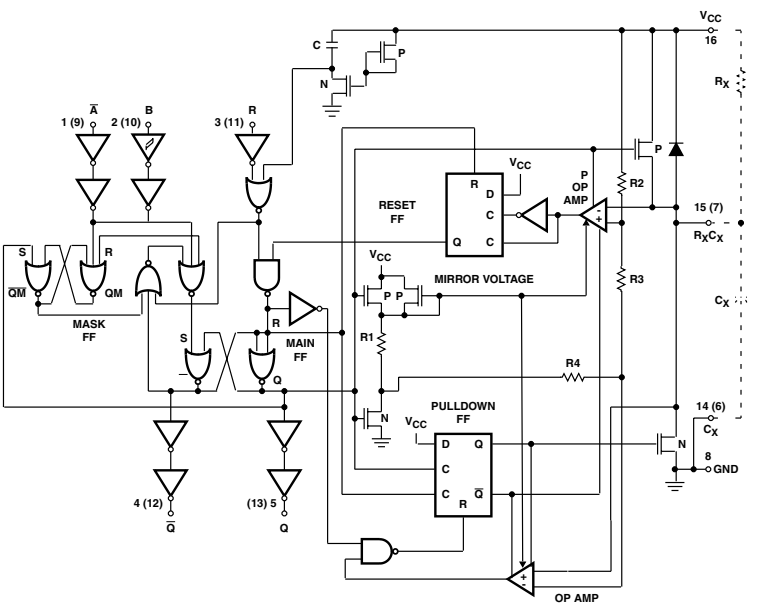
DUAL MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

- Overriding Clear Terminates Outputs Pulse

Logic Diagram (SN74LV)



Logic Diagram (CD74HC/HCT)



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE
(each monostable multivibrator)

INPUTS			OUTPUTS	
$\overline{CLR}$	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍†	⎎†
H	↓	H	⎍†	⎎†
↑‡	L	H	⎍†	⎎†

† Pulsed-output patterns are tested during AC switching at 25°C with R_{ext} = 2 kΩ, and C_{ext} = 80 pF.

‡ This condition is true only if the output of the latch formed by the two NAND gates has been conditioned to the logic 1 state prior to $\overline{CLR}$ going high. This latch is conditioned by taking either A high or B low while $\overline{CLR}$ is inactive (high).

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

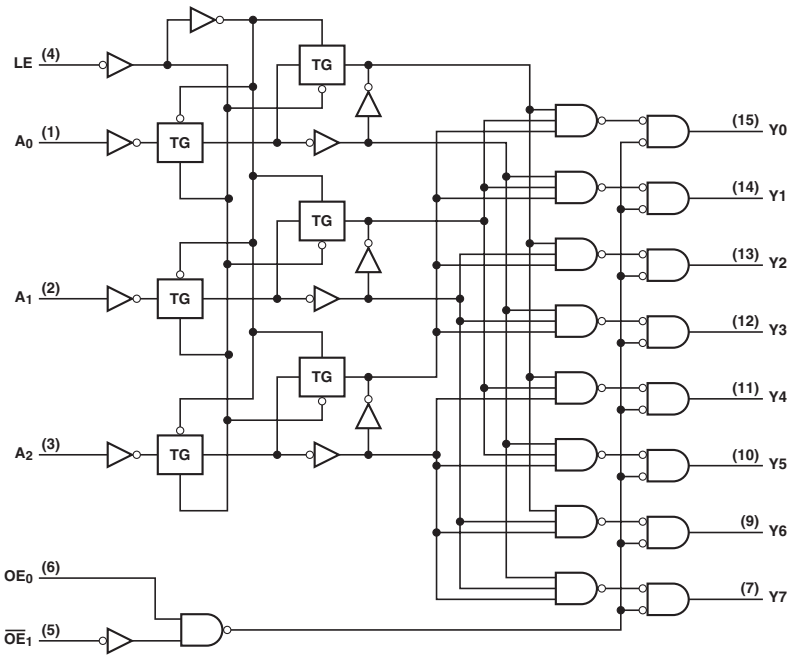
PARAMETER	MAX or MIN	TTL	LS	CD74 HC	CD74 HCT	LV 3V	LV 5V	UNIT
I_{CC}	MAX	80	27	0.16	0.16	0.28	0.65	mA
I_{OH}	MAX	-0.8	-0.4	-4	-4	-6	-12	mA
I_{OL}	MAX	16	8	4	4	6	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	CD74 HC	CD74 HCT	LV 3V	LV 5V
t_{PLH}	A (HC, LV: $\overline{A}$)	Q	MAX	70	70	63	63	27.5	16
	B			55	55	63	63	27.5	16
t_{PHL}	A (HC, LV: $\overline{A}$)	$\overline{Q}$	MAX	80	80	51	51	27.5	16
	B			65	65	51	51	27.5	16
t_{PHL}	Clear	Q	MAX	27	55	48	57	22	13
t_{PLH}		$\overline{Q}$		40	65	54	56	22	13

UNIT: ns

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS						OUTPUTS							
LE	OE0	$\overline{OE1}$	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	L	L	L	L	L	L	L	L
X	L	X	X	X	X	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L
L	H	L	L	L	H	L	H	L	L	L	L	L	L
L	H	L	L	H	L	L	L	H	L	L	L	L	L
L	H	L	L	H	H	L	L	L	H	L	L	L	L
L	H	L	H	L	L	L	L	L	L	H	L	L	L
L	H	L	H	L	H	L	L	L	L	L	H	L	L
L	H	L	H	H	L	L	L	L	L	L	L	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H
H	H	L	X	X	X	Depends upon the address previously applied while LE was at a logic low.							

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

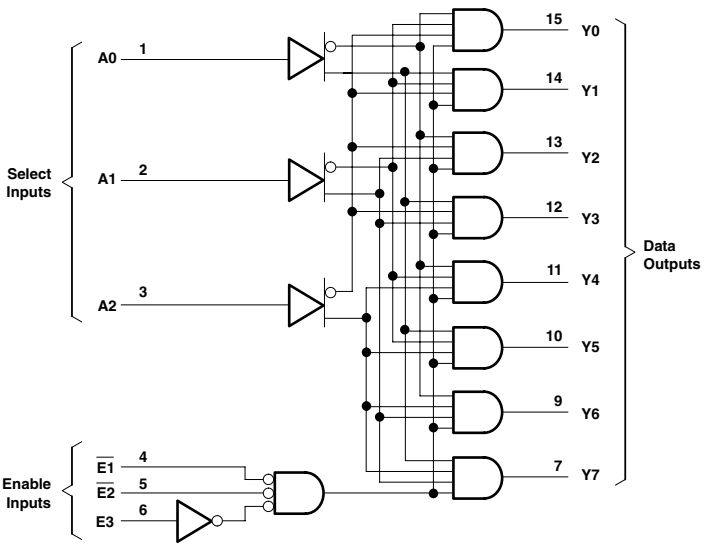
PARAMETER	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	0.08	0.16	0.16	mA
I_{OH}	MAX	-4	-4	-4	mA
I_{OL}	MAX	4	4	4	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT
t_w	LE Pulse Width		MIN	20	15	15
t_{su}	An to LE		MIN	19	15	15
t_h	An to LE		MIN	5	9	5
t_{PLH}	An	Y	MAX	48	48	57
t_{PHL}				48	48	57
t_{PLH}	OE_0	Y	MAX	44	44	60
t_{PHL}				44	44	60
t_{PLH}	$\overline{OE}_1$	Y	MAX	44	44	53
t_{PHL}				44	44	53

UNIT:ns

Logic Diagram (CD74AC/ACT)



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS						OUTPUTS							
ENABLE			ADDRESS										
E3	$\overline{E2}$	$\overline{E1}$	A2	A1	$\overline{A0}$	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	L	L	L	L	L	L	L	L
L	X	X	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	X	L	L	L	L	L	L	L	L
H	L	L	L	L	L	H	L	L	L	L	L	L	L
H	L	L	L	L	H	L	H	L	L	L	L	L	L
H	L	L	L	H	L	L	L	H	L	L	L	L	L
H	L	L	L	H	H	L	L	L	H	L	L	L	L
H	L	L	H	L	L	L	L	L	L	H	L	L	L
H	L	L	H	L	H	L	L	L	L	L	H	L	L
H	L	L	H	H	L	L	L	L	L	L	L	H	L
H	L	L	H	H	H	L	L	L	L	L	L	L	H

Note: H = High Voltage Level, L = Low Volltage Level, X = Don't Care

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	UNIT
I_{CC}	MAX	0.16	0.16	0.16	0.16	mA
I_{OH}	MAX	-4	-4	-24	-24	mA
I_{OL}	MAX	4	4	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT
t_{PLH}	Address	Y	MAX	45	53	15	15.6
t_{PHL}				45	53	15	15.6
t_{PLH}	$\overline{E1}$, $\overline{E2}$ ($\overline{G2A}$, $\overline{G2B}$)	Y	MAX	60	60	11.9	14.2
t_{PHL}				60	60	11.9	14.2
t_{PLH}	E3 (G1)	Y	MAX	60	60	16.6	13.6
t_{PHL}				60	60	16.6	13.6

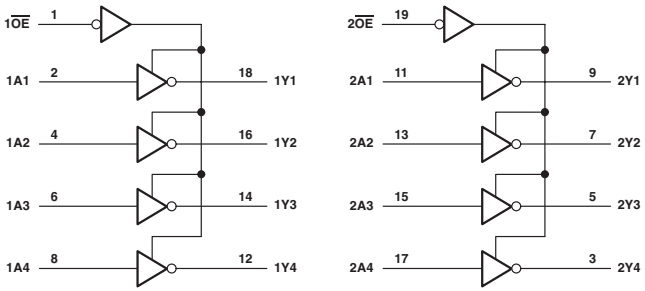
UNIT:ns

240

OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- PNP Inputs Reduce DC Loading
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- CD74AC/ACT240 T_A: –40 to 85°C

Logic Diagram (SN74)



FUNCTION TABLE (each 4-bit buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	ALS A-1	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	UNIT
I_{CCH}	MAX	27	135	11	11	17	29	0.08	0.16	0.08	0.16	31	0.25	mA
I_{CCL}	MAX	44	150	23	23	75	75	0.08	0.16	0.08	0.16	71	30	mA
I_{CCZ}	MAX	50	150	25	25	38	63	0.08	0.16	0.08	0.16	9	0.25	mA
I_{OH}	MAX	-15	-15	-15	-15	-15	-15	-6	-6	-6	-6	-15	-32	mA
I_{OL}	MAX	24	64	24	48	64	64	6	6	6	6	64	64	mA

PARAMETER	MAX or MIN	LVT 3V	LVTH 3V	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	UNIT
I_{CCH}	MAX	0.19	0.19	0.08	0.04	0.08	0.08	0.04	0.08	0.04	0.04	-	0.02	mA
I_{CCL}	MAX	5	5	0.08	0.04	0.08	0.08	0.04	0.08	0.04	0.04	-	0.02	mA
I_{CCZ}	MAX	0.19	0.19	0.08	0.04	0.08	0.08	0.04	0.08	0.04	0.04	-	0.02	mA
I_{OH}	MAX	-32	-32	-24	-24	-24	-24	-24	-24	-8	-8	-8	-16	mA
I_{OL}	MAX	64	64	24	24	24	24	24	24	8	8	8	16	mA

PARAMETER	MAX or MIN	LVC 3V	LVCZ 3V	AUC 1.8V	AUC 2.3V	AUCH 1.8V	AUCH 2.3V	UNIT
I_{CCH}	MAX	0.01	0.1	0.02	0.02	0.02	0.02	mA
I_{CCL}	MAX	0.01	0.1	0.02	0.02	0.02	0.02	mA
I_{CCZ}	MAX	0.01	0.1	0.02	0.02	0.02	0.02	mA
I_{OH}	MAX	-24	-24	-8	-9	-8	-9	mA
I_{OL}	MAX	24	24	8	9	8	9	mA

: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	ALS A-1	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT
t_{PLH}	A	Y (CD74: $\overline{Y}$)	MAX	14	7	9	9	6.5	8	25	30	32	33
t_{PHL}				18	7	9	9	6.5	5.7	25	30	32	33
t_{PZH}	$\overline{OE}$	Y (CD74: $\overline{Y}$)	MAX	23	10	13	13	6.4	6.1	38	-	44	-
t_{PZL}				30	15	18	18	9	10	38	-	44	-
t_{PHZ}	$\overline{OE}$	Y (CD74: $\overline{Y}$)	MAX	25	9	10	10	5	6.3	38	-	44	-
t_{PLZ}				20	15	12	12	9.5	9.5	38	-	44	-

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT	ABT	LVT 3V	LVTH 3V	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT
t_{PLH}	A	Y (CD74: $\overline{Y}$)	MAX	5.6	4.8	3.8	3.8	8.4	7	6.5	10.6	9.5	7.8
t_{PHL}				4	4.8	4	4	7.2	6.5	6.5	8.7	8.5	7.8
t_{PZH}	$\overline{OE}$	Y (CD74: $\overline{Y}$)	MAX	8.8	5.2	4.6	4.6	9.2	8	10.9	12.5	9.5	12.2
t_{PZL}				10.5	6.2	4.4	4.4	8.7	8.5	10.9	12.3	10.5	12.2
t_{PHZ}	$\overline{OE}$	Y (CD74: $\overline{Y}$)	MAX	8.1	6.4	4.4	4.4	6.6	9.5	10.9	10	10.5	12.2
t_{PLZ}				9.5	5.8	4.3	4.3	7.7	9.5	10.9	10.8	10.5	12.2

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LV 3V	LV 5V	LVC 3V	LVCZ 3V	AUC 1.8V	AUC 2.3V	AUCH 1.8V	AUCH 2.3V
t_{PLH}	A	Y	MAX	8.5	9.5	12.5	8.5	6.5	6.5	2.1	1.6	2.1	1.6
t_{PHL}				8.5	9.5	12.5	8.5	6.5	6.5	2.1	1.6	2.1	1.6
t_{PZH}	$\overline{OE}$	Y	MAX	10.5	13	16	10.5	8	8	2.7	2	2.7	2
t_{PZL}				10.5	13	16	10.5	8	8	2.7	2	2.7	2
t_{PHZ}	$\overline{OE}$	Y	MAX	10.5	13	17	15.5	7	7	4	2	4	2
t_{PLZ}				10.5	13	17	15.5	7	7	4	2	4	2

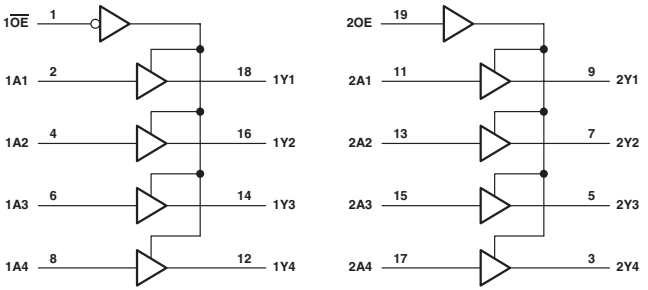
UNIT: ns

241

OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- PNP Inputs Reduce DC Loading
- CD74AC/ACT241 T_A: –40 to 85°C

Logic Diagram (SN74)



FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	SN74 BCT	ABT	LVTH 3V	SN74 AC	UNIT
I_{CCH}	MAX	27	160	18	35	60	0.08	0.16	0.16	43	0.25	0.19	0.04	mA
I_{CCL}	MAX	46	180	26	90	90	0.08	0.16	0.16	85	30	5	0.04	mA
I_{CCZ}	MAX	54	180	30	56	90	0.08	0.16	0.16	10	0.25	0.19	0.04	mA
I_{OH}	MAX	-15	-15	-15	-15	-15	-6	-6	-6	-15	-32	-32	-24	mA
I_{OL}	MAX	24	64	24	64	64	6	6	6	64	64	64	24	mA

PARAMETER	MAX or MIN	CD74 AC	SN74 ACT	CD74 ACT	UNIT
I_{CCH}	MAX	0.16	0.04	0.08	mA
I_{CCL}	MAX	0.16	0.04	0.08	mA
I_{CCZ}	MAX	0.16	0.04	0.08	mA
I_{OH}	MAX	-24	-24	-24	mA
I_{OL}	MAX	24	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	SN74 BCT
t_{PLH}	A	Y (CD74: $\overline{Y}$)	MAX	18	9	11	6.2	6.2	29	33	38	4.9
t_{PHL}				18	9	10	6.2	6.5	29	33	38	5.9
t_{PZH}	$1\overline{OE}$	Y (CD74: $\overline{Y}$)	MAX	23	12	21	9	6.7	38	-	-	8.7
t_{PZL}				30	15	21	7.5	8	38	-	-	9.4
t_{PHZ}	$1\overline{OE}$	Y (CD74: $\overline{Y}$)	MAX	25	9	10	6	7	38	-	-	8.1
t_{PLZ}				20	15	15	9	7	38	-	-	9.9
t_{PZH}	2OE	Y (CD74: $\overline{Y}$)	MAX	23	12	21	10.5	6.7	38	-	-	8.7
t_{PZL}				30	15	21	8.5	8	38	-	-	9.4
t_{PHZ}	2OE	Y (CD74: $\overline{Y}$)	MAX	25	9	10	7	7	38	-	-	8.1
t_{PLZ}				20	15	15	12	7	38	-	-	9.9

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVTH 3V	SN74 AC	CD74 AC	SN74 ACT	CD74 ACT
t_{PLH}	A	Y (CD74: $\overline{Y}$)	MAX	4.6	3.5	7.5	7.5	9.5	8.7
t_{PHL}				4.6	3.4	7.5	7.5	8.5	8.7
t_{PZH}	$1\overline{OE}$	Y (CD74: $\overline{Y}$)	MAX	6.8	4.5	9.5	10.9	9.5	12.2
t_{PZL}				6.8	4.4	9.5	10.9	10.5	12.2
t_{PHZ}	$1\overline{OE}$	Y (CD74: $\overline{Y}$)	MAX	7.1	4.5	10.5	10.9	10.5	12.2
t_{PLZ}				5.9	4.7	10.5	10.9	10.5	12.2
t_{PZH}	2OE	Y (CD74: $\overline{Y}$)	MAX	6.8	4.5	9.5	10.9	9.5	12.2
t_{PZL}				6.8	4.4	9.5	10.9	10.5	12.2
t_{PHZ}	2OE	Y (CD74: $\overline{Y}$)	MAX	7.1	4.5	10.5	10.9	10.5	12.2
t_{PLZ}				5.9	4.7	10.5	10.9	10.5	12.2

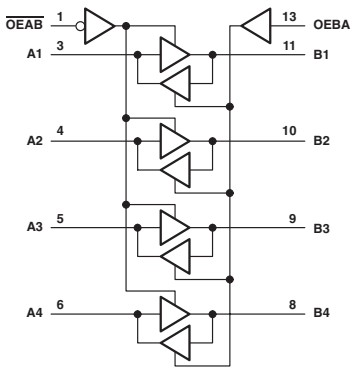
UNIT: ns

243

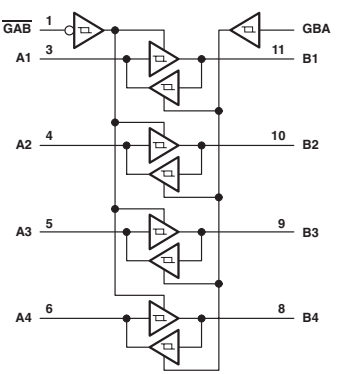
QUADRUPLE BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- Two-Way Asynchronous Communication Between Data Buses
- PNP Inputs Reduce DC Loading

Logic Diagram (SN74ALS)



Logic Diagram (SN74LS)



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE (SN74)

INPUTS		OPERATION
$\overline{G}AB$	GBA	
L	L	A to B
H	H	B to A
H	L	Isolation
L	H	Latch A and B (A = B)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	AS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CCH}	MAX	38	25	44	0.08	0.16	0.16	mA
I_{CCL}	MAX	50	30	74	0.08	0.16	0.16	mA
I_{CCZ}	MAX	54	32	56	0.08	0.16	0.16	mA
I_{OH}	MAX	-15	-15	-	-	-6	-6	mA
I_{OL}	MAX	24	24	64	6	6	6	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS	SN74 HC	CD74 HC	CD74 HCT
t_{PLH}	A or B	A or B	MAX	18	11	7.5	25	27	33
t_{PHL}	A or B	A or B	MAX	18	11	6.5	25	27	33
t_{PZH}	$\overline{G}AB$	B	MAX	23	20	9	38	45	51
t_{PZL}				30	20	7.5	38	45	51
t_{PHZ}	$\overline{G}AB$	B	MAX	25	14	6.5	38	45	53
t_{PLZ}				20	22	9	38	45	53
t_{PZH}	GAB	A	MAX	23	20	10.5	38	45	51
t_{PZL}				30	20	8.5	38	45	51
t_{PHZ}	GAB	A	MAX	25	14	7	38	45	53
t_{PLZ}				20	22	11	38	45	53

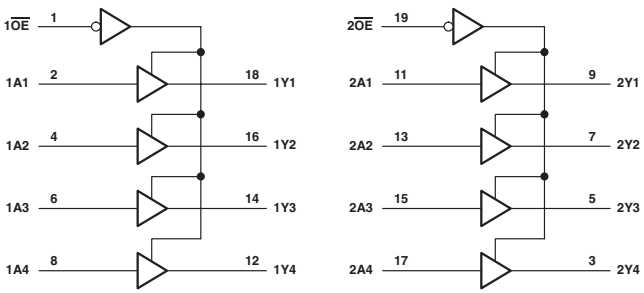
UNIT: ns

244

OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- PNP Inputs Reduce DC Loading
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- CD74AC/ACT244 T_A: –40 to 85°C

Logic Diagram (SN74)



FUNCTION TABLE (each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	ALS C-1	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	SN64 BCT	UNIT
I_{CCH}	MAX	27	160	17	17	34	60	0.08	0.16	0.08	0.16	40	40	mA
I_{CCL}	MAX	46	180	24	24	90	90	0.08	0.16	0.08	0.16	80	80	mA
I_{CCZ}	MAX	54	180	27	27	54	90	0.08	0.16	0.08	0.16	10	10	mA
I_{OH}	MAX	-15	-15	-15	-15	-15	-15	-6	-6	-6	-6	-15	-15	mA
I_{OL}	MAX	24	64	24	48	64	64	6	6	6	6	64	64	mA

PARAMETER	MAX or MIN	ABT	LVT 3V	LVTH 3V	LVTZ 3V	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	UNIT
I_{CCH}	MAX	0.25	0.19	0.19	0.225	0.08	0.04	0.08	0.08	0.04	0.08	0.04	0.04	-	mA
I_{CCL}	MAX	30	5	5	15	0.08	0.04	0.08	0.08	0.04	0.08	0.04	0.04	-	mA
I_{CCZ}	MAX	0.25	0.19	0.19	0.225	0.08	0.04	0.08	0.08	0.04	0.08	0.04	0.04	-	mA
I_{OH}	MAX	-32	-32	-32	-32	-24	-24	-24	-24	-24	-24	-8	-8	-8	mA
I_{OL}	MAX	64	64	64	64	24	24	24	24	24	24	8	8	8	mA

PARAMETER	MAX or MIN	LV 5V	LV-AT 3	LVC 3V	LVCH 3V	LVCZ 3V	ALVC 3V	ALVCH 3V	AUC 1.8V	AUC 2.3V	AUCH 1.8V	AUCH 2.3V	UNIT
I_{CCH}	MAX	0.02	0.02	0.01	0.01	0.1	0.01	0.01	0.02	0.02	0.02	0.02	mA
I_{CCL}	MAX	0.02	0.02	0.01	0.01	0.1	0.01	0.01	0.02	0.02	0.02	0.02	mA
I_{CCZ}	MAX	0.02	0.02	0.01	0.01	0.1	0.01	0.01	0.02	0.02	0.02	0.02	mA
I_{OH}	MAX	-16	-16	-24	-24	-24	-24	-24	-8	-9	-8	-9	mA
I_{OL}	MAX	16	16	24	24	24	24	24	8	9	8	9	mA

: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	ALS C-1	AS	F	SN74 HC	CD74 HC	SN74 HCT
t_{PLH}	A	Y	MAX	18	9	10	10	6.2	6.2	29	33	35
t_{PHL}				18	9	10	10	6.2	6.5	29	33	35
t_{PZH}	$\overline{OE}$	Y	MAX	23	12	20	20	9	6.7	38	-	44
t_{PZL}				30	15	20	20	7.5	8	38	-	44
t_{PHZ}	$\overline{OE}$	Y	MAX	25	9	10	10	6	7	38	-	44
t_{PLZ}				20	15	13	13	9	7	38	-	44

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HCT	SN74 BCT	SN64 BCT	ABT	LVT 3V	LVTH 3V	LVTZ 3V	AC 11	SN74 AC	CD74 AC
t_{PLH}	A	Y	MAX	38	5	5.3	4.6	3.5	3.5	4.1	7.3	7.5	7.5
t_{PHL}				38	5.5	6	4.6	3.3	3.3	4.1	6.9	7.5	7.5
t_{PZH}	$\overline{OE}$	Y	MAX	-	8.7	9	5.1	4.5	4.5	5.2	8.5	8	10.9
t_{PZL}				-	8.9	9.4	6.1	4.4	4.4	5.2	8.5	8.5	10.9
t_{PHZ}	$\overline{OE}$	Y	MAX	-	7.7	8	6.6	4.4	4.4	5.6	7.3	9.5	10.9
t_{PLZ}				-	8.9	9.8	5.7	4.4	4.4	5.1	8.2	9.5	10.9

PARAMETER	INPUT	OUTPUT	MAX or MIN	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LV-AT	LVC 3V	LVCH 3V
t_{PLH}	A	Y	MAX	9.9	10	8.7	8.5	9.5	13.5	8.5	9.5	5.9	5.9
t_{PHL}				9.2	10	8.7	8.5	9.5	13.5	8.5	9.5	5.9	5.9
t_{PZH}	$\overline{OE}$	Y	MAX	12.5	9.5	12.2	10.5	13	16	10.5	13	7.6	7.6
t_{PZL}				11.4	10.5	12.2	10.5	13	16	10.5	13	7.6	7.6
t_{PHZ}	$\overline{OE}$	Y	MAX	10.4	10.5	12.2	10.5	13	18	15.5	13	6.5	5.8
t_{PLZ}				11.2	10.5	12.2	10.5	13	18	15.5	13	6.5	5.8

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVCZ 3V	ALVC 3V	ALVCH 3V	AUC 1.8V	AUC 2.3V	AUCH 1.8V	AUCH 2.3V
t_{PLH}	A	Y	MAX	5.9	2.8	2.8	2.5	1.9	2.5	1.9
t_{PHL}				5.9	2.8	2.8	2.5	1.9	2.5	1.9
t_{PZH}	$\overline{OE}$	Y	MAX	7.6	4.5	4.5	3.1	2.3	3.1	2.3
t_{PZL}				7.6	4.5	4.5	3.1	2.3	3.1	2.3
t_{PHZ}	$\overline{OE}$	Y	MAX	6.5	4.2	4.2	4.2	2.3	4.2	2.3
t_{PLZ}				6.5	4.2	4.2	4.2	2.3	4.2	2.3

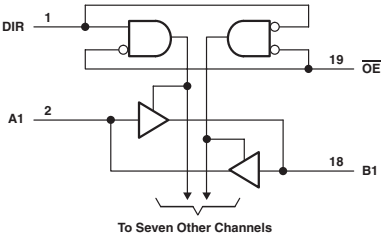
UNIT: ns

245

OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- 3-State Outputs Drive Bus Lines Directly
- PNP Inputs Reduce DC Loading on Bus Lines
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram (SN74)



FUNCTION TABLE

ENABLE $\overline{G}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	ALS A-1	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	SN64 BCT	ABT	ABTH	UNIT
I_{CCH}	MAX	70	45	45	97	90	0.08	0.16	0.08	0.16	57	57	0.25	0.25	mA
I_{CCL}	MAX	90	55	55	143	120	0.08	0.16	0.08	0.16	90	90	30	30	mA
I_{CCZ}	MAX	95	58	58	123	110	0.08	0.16	0.08	0.16	15	15	0.25	0.25	mA
I_{OH} (A port)	MAX	-15	-15	-15	-15	-3	-6	-4	-6	-4	-3	-3	-32	-32	mA
I_{OH} (B port)	MAX	-15	-15	-15	-15	-15	6	-4	-6	-4	-15	-15	-32	-32	mA
I_{OL} (A port)	MAX	24	24	48	64	24	-6	4	6	4	24	24	64	64	mA
I_{OL} (B port)	MAX	24	24	48	64	64	6	4	6	4	64	64	64	64	mA

PARAMETER	MAX or MIN	LVT 3V	LVTH 3V	LVTR 3V	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	UNIT
I_{CCH}	MAX	0.19	0.19	0.19	0.08	0.04	0.16	0.08	0.04	0.16	0.04	0.04	-	0.02	mA
I_{CCL}	MAX	5	5	12	0.08	0.04	0.16	0.08	0.04	0.16	0.04	0.04	-	0.02	mA
I_{CCZ}	MAX	0.19	0.19	0.19	0.08	0.04	0.16	0.08	0.04	0.16	0.04	0.04	-	0.02	mA
I_{OH} (A port)	MAX	-32	-32	-12	-24	-24	-24	-24	-24	-24	-8	-8	-8	-16	mA
I_{OH} (B port)	MAX	-32	-32	-32	-24	-24	-24	-24	-24	-24	-8	-8	-8	-16	mA
I_{OL} (A port)	MAX	64	64	32	24	24	24	24	24	24	8	8	8	16	mA
I_{OL} (B port)	MAX	64	64	32	24	24	24	24	24	24	8	8	8	16	mA

PARAMETER	MAX or MIN	LV-AT	LVC 3V	LVCH 3V	LVCZ 3V	ALVC 3V	ALVCH 3V	AUC 1.8V	AUC 2.3V	AUCH 1.8V	AUCH 2.3V	UNIT
I_{CCH}	MAX	0.02	0.01	0.01	0.1	0.01	0.01	0.02	0.02	0.02	0.02	mA
I_{CCL}	MAX	0.02	0.01	0.01	0.1	0.01	0.01	0.02	0.02	0.02	0.02	mA
I_{CCZ}	MAX	0.02	0.01	0.01	0.1	0.01	0.01	0.02	0.02	0.02	0.02	mA
I_{OH} (A port)	MAX	-16	-24	-24	-24	-24	-24	-8	-9	-8	-9	mA
I_{OH} (B port)	MAX	-16	-24	-24	-24	-24	-24	-8	-9	-8	-9	mA
I_{OL} (A port)	MAX	16	24	24	24	24	24	8	9	8	9	mA
I_{OL} (B port)	MAX	16	24	24	24	24	24	8	9	8	9	mA

: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	ALS A-1	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT
t_{PLH}	A, B	B, A	MAX	12	10	10	7.5	7	26	33	28	39	7
t_{PHL}				12	10	10	7	7	26	33	28	39	7
t_{PZH}	$\overline{OE}$	A, B	MAX	40	20	20	9	8	58	45	58	48	10.9
t_{PZL}				40	20	20	8.5	9	58	45	58	48	11.6
t_{PHZ}	$\overline{OE}$	A, B	MAX	28	10	10	5.5	7.5	50	45	50	45	9.3
t_{PLZ}				25	15	15	9.5	7.5	50	45	50	45	9.1

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN64 BCT	ABT	ABTH	LVT 3V	LVTH 3V	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT
t_{PLH}	A, B	B, A	MAX	7	3.6	3.6	3.5	3.5	9.5	7	8.5	10	8
t_{PHL}				7	3.9	3.9	3.5	3.5	6.9	7	8.5	9.1	9
t_{PZH}	$\overline{OE}$	A, B	MAX	10.9	5.6	5.6	5.5	5.5	11.4	9	14	13.2	11
t_{PZL}				11.6	6.2	6.2	5.5	5.5	9.5	9.5	14	12.9	12
t_{PHZ}	$\overline{OE}$	A, B	MAX	9.3	5.9	5.9	5.9	5.9	9.5	10	14	12.9	11
t_{PLZ}				9.1	4.5	4.5	5	5	10.4	10	14	13.9	11

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LV-AT	LVC 3V	LVCH 3V	LVCZ 3V	ALVC 3V
t_{PLH}	A, B	B, A	MAX	10	8.5	9.5	13.5	8.5	9.5	6.3	6.3	6.3	3.4
t_{PHL}				10	8.5	9.5	13.5	8.5	9.5	6.3	6.3	6.3	3.4
t_{PZH}	$\overline{OE}$	A, B	MAX	14	12	16	19	12	16	8.5	8.5	8.5	5.5
t_{PZL}				14	12	16	19	12	16	8.5	8.5	8.5	5.5
t_{PHZ}	$\overline{OE}$	A, B	MAX	14.4	11	16.5	22	16	16.5	7.5	7.5	7.5	5.5
t_{PLZ}				14.4	11	16.5	22	16	16.5	7.5	7.5	7.5	5.5

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V	AUC 1.8V	AUC 2.3V	AUCH 1.8V	AUCH 2.3V
t_{PLH}	A, B	B, A	MAX	3.4	2.2	1.8	2.2	1.8
t_{PHL}				3.4	2.2	1.8	2.2	1.8
t_{PZH}	$\overline{OE}$	A, B	MAX	5.5	3	2.4	3	2.4
t_{PZL}				5.5	3	2.4	3	2.4
t_{PHZ}	$\overline{OE}$	A, B	MAX	5.5	4	2.6	4	2.6
t_{PLZ}				5.5	4	2.6	4	2.6

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTR 3V
t_{PLH}	A	B	MAX	4.2
	B	A		4.4
t_{PHL}	A	B	MAX	4.6
	B	A		4.1
t_{PZH}	$\overline{OE}$	B	MAX	5.5
		A		6
t_{PZL}	$\overline{OE}$	B	MAX	6.6
		A		6.4
t_{PHZ}	$\overline{OE}$	B	MAX	6.1
		A		5.8
t_{PLZ}	$\overline{OE}$	B	MAX	5.2
		A		5.2

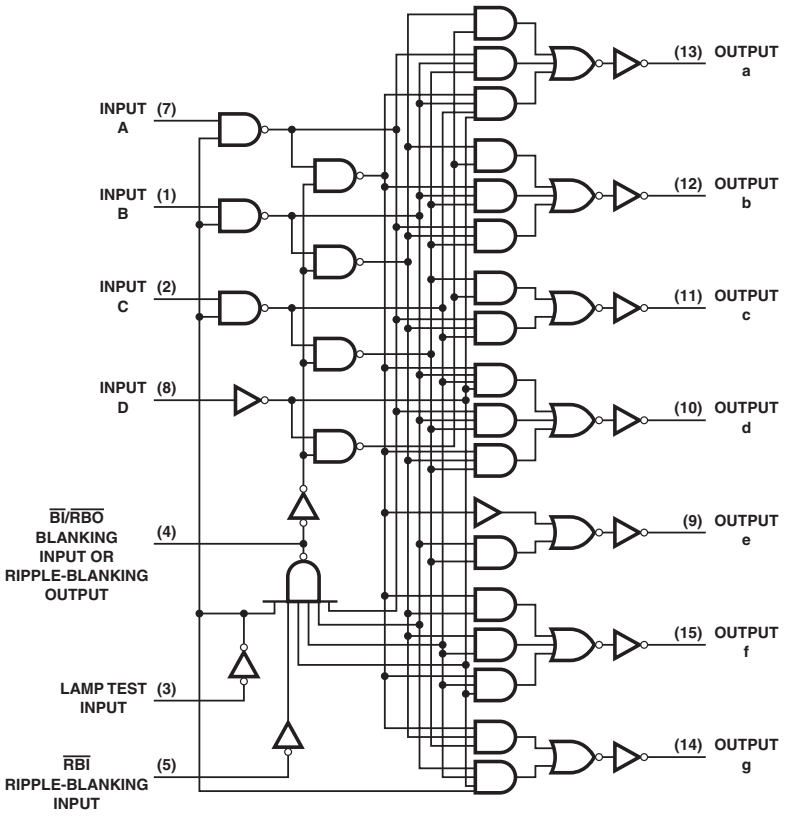
UNIT: ns

247

BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

- Open-Collector Outputs Drive Indicators Directly
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

DECIMAL OR FUNCTION	INPUTS						BI/RBO	OUTPUTS						
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON
6	H	X	L	H	H	L	H	ON	OFF	ON	ON	ON	ON	ON
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON
9	H	X	H	L	L	H	H	ON	ON	ON	ON	OFF	ON	ON
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	TTL	LS	UNIT
I_{CC}		MAX	103	13	mA
V_O (off)	a thru g	MAX	15	15	V
I_O (on)		MAX	40	24	mA
I_{OH}	BI/RBO	MAX	-0.2	-0.05	mA
I_{OL}		MAX	8	3.2	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		MAX or MIN	TTL	LS
toff	INPUT A	MIN	100	100
ton			100	100
toff	INPUT $\overline{RBI}$	MIN	100	100
ton			100	100

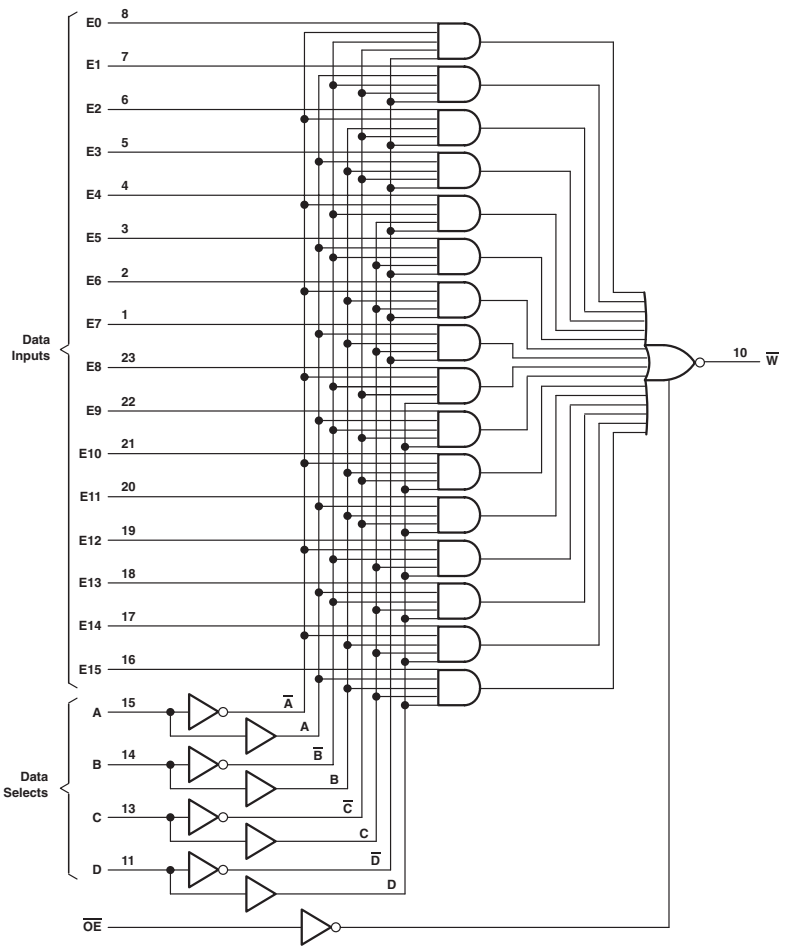
UNIT: ns

250

1-OF-16 DATA GENERATORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

- 4-Line to 1-Line Multiplexers That Can Select 1-of-16 Data Inputs
- Applications:
  - Boolean Function Generator
  - Parallel-to-Serial Converter
  - Data Source Selector
- Buffered 3-State Bus Driver Inputs Permit Multiplexing From n Lines to One Line
- 3-State Outputs

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS						OUTPUT
$\overline{OE}$	A	B	C	D	Ei	$\overline{W}$
L	L	L	L	L	E0	$\overline{E0}$
L	H	L	L	L	E1	$\overline{E1}$
L	L	H	L	L	E2	$\overline{E2}$
L	H	H	L	L	E3	$\overline{E3}$
L	L	L	H	L	E4	$\overline{E4}$
L	H	L	H	L	E5	$\overline{E5}$
L	L	H	H	L	E6	$\overline{E6}$
L	H	H	H	L	E7	$\overline{E7}$
L	L	L	L	H	E8	$\overline{E8}$
L	H	L	L	H	E9	$\overline{E9}$
L	L	H	L	H	E10	$\overline{E10}$
L	H	H	L	H	E11	$\overline{E11}$
L	L	L	H	H	E12	$\overline{E12}$
L	H	L	H	H	E13	$\overline{E13}$
L	L	H	H	H	E14	$\overline{E14}$
L	H	H	H	H	E15	$\overline{E15}$
H	X	X	X	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AS	UNIT
I_{CC}	MAX	50	mA
I_{OH}	MAX	-15	mA
I_{OL}	MAX	48	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AS
t_{PLH}	DATA	$\overline{W}$	MAX	8
t_{PHL}				7
t_{PLH}	SELECT	$\overline{W}$	MAX	13
t_{PHL}				10.5
t_{PZH}	$\overline{OE}$	$\overline{W}$	MAX	7
t_{PZL}				9
t_{PHZ}	$\overline{OE}$	$\overline{W}$	MAX	6
t_{PLZ}				6.5

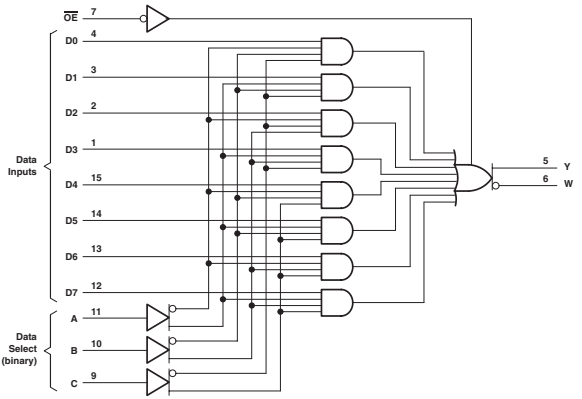
UNIT: ns

251

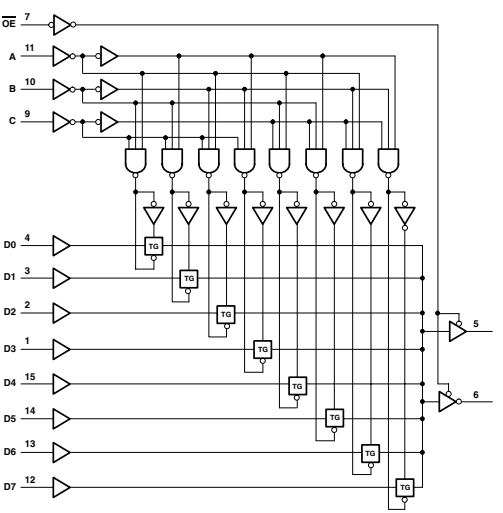
DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

- 3-State Version of '151
- 3-State Outputs Interface Directly with System Bus
- Perform Parallel-to-Serial Conversion
- Complementary Outputs Provide True and Inverted Data

Logic Diagram (SN74ALS,F)



Logic Diagram (SN74HC)



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE (SN74)

INPUTS				OUTPUTS	
SELECT			STROBE	Y	W
C	B	A	$\overline{OE}$		
X	X	X	H	Z	$\overline{Z}$
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	F	SN74 HC	CD74 HC	CD74 HCT	SN74 AC	CD74 AC	UNIT
I_{CC}	MAX	62	12	85	14	24	0.08	0.16	0.16	0.16	0.16	mA
I_{OH}	MAX	-5.2	-2.6	-6.5	-2.6	-3	-6	-4	-4	-24	-24	mA
I_{OL}	MAX	16	8	20	24	24	6	4	4	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	F	SN74 HC	CD74 HC	CD74 HCT	SN74 AC	CD74 AC
t_{PLH}	A, B, C (CD74: S_0, S_1, S_2)	Y	MAX	45	45	18	18	9.5	51	74	63	18.2	18.2
t_{PHL}				45	45	19.5	24	7.5	51	74	63	18.2	18.2
t_{PLH}	A, B, C (CD74: S_0, S_1, S_2)	W (CD74: $\overline{Y}$)	MAX	33	33	15	24	12.5	51	74	63	19.6	19.6
t_{PHL}				33	33	13.5	23	9	51	74	63	19.6	19.6
t_{PLH}	ANY D (CD74: ANYI)	Y	MAX	28	28	12	10	7	49	53	53	13.5	13.5
t_{PHL}				28	28	12	15	5	49	53	53	13.5	13.5
t_{PLH}	ANY D (CD74: ANYI)	W (CD74: $\overline{Y}$)	MAX	15	15	7	15	8	49	53	53	14.9	14.9
t_{PHL}				15	15	7	15	8	49	53	53	14.9	14.9
t_{PZH}	$\overline{G}$	Y	MAX	27	45	19.5	15	7	36	42	45	13.5	13.5
t_{PZL}				40	40	21	15	6.5	36	42	45	13.5	13.5
t_{PZH}	$\overline{G}$	W (CD74: $\overline{Y}$)	MAX	27	27	19.5	15	6	36	42	45	13.5	13.5
t_{PZL}				40	40	21	15	4.5	36	42	45	13.5	13.5
t_{PHZ}	$\overline{G}$	Y	MAX	8	45	8.5	10	8.5	49	42	45	13.5	13.5
t_{PLZ}				23	25	14	10	8	49	42	45	13.5	13.5
t_{PHZ}	$\overline{G}$	W (CD74: $\overline{Y}$)	MAX	8	55	8.5	10	5.5	49	42	45	13.5	13.5
t_{PLZ}				23	25	14	10	4.5	49	42	45	13.5	13.5

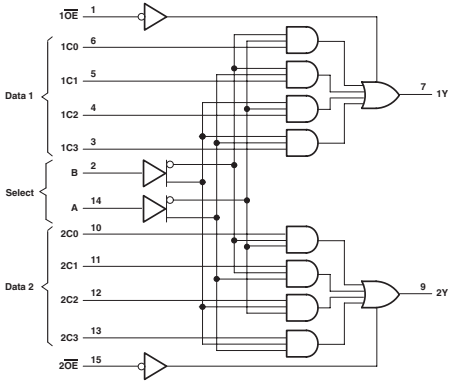
UNIT: ns

253

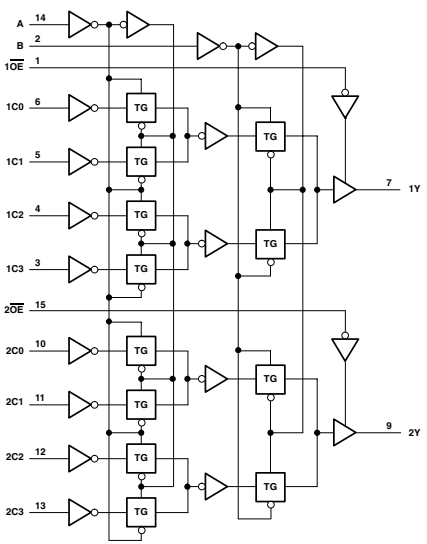
DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

- 3-State Version of '153
- Perform Parallel-to-Serial Conversion

Logic Diagram (SN74ALS, AS, F)



Logic Diagram (SN74HC)



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE (SN74)

SELECT INPUTS		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	**A**	**C0**	**C1**	**C2**	**C3**	$\overline{\text{OE}}$	**Y**
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	UNIT
I_{CC}	MAX	14	14	33	23	0.08	0.16	0.16	0.16	0.16	mA
I_{OH}	MAX	-2.6	-2.6	-15	-3	-6	-6	-4	-24	-24	mA
I_{OL}	MAX	8	24	48	24	6	6	4	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT
t_{PLH}	DATA	Y	MAX	25	10	7.5	8	35	53	57	13.3	18
t_{PHL}				20	14	8	7	35	53	57	13.3	18
t_{PLH}	SELECT	Y	MAX	45	21	13.5	13	38	53	60	20	22
t_{PHL}				32	21	11.5	10	38	53	60	20	22
t_{PZH}	$\overline{\text{OE}}$	Y	MAX	28	14	12.5	9	25	33	45	11.5	12.6
t_{PZL}				23	16	11.5	9	25	33	45	11.5	12.6
t_{PHZ}	$\overline{\text{OE}}$	Y	MAX	41	10	6	6	38	45	45	11.5	12.6
t_{PLZ}				27	14	7	7	38	45	45	11.5	12.6

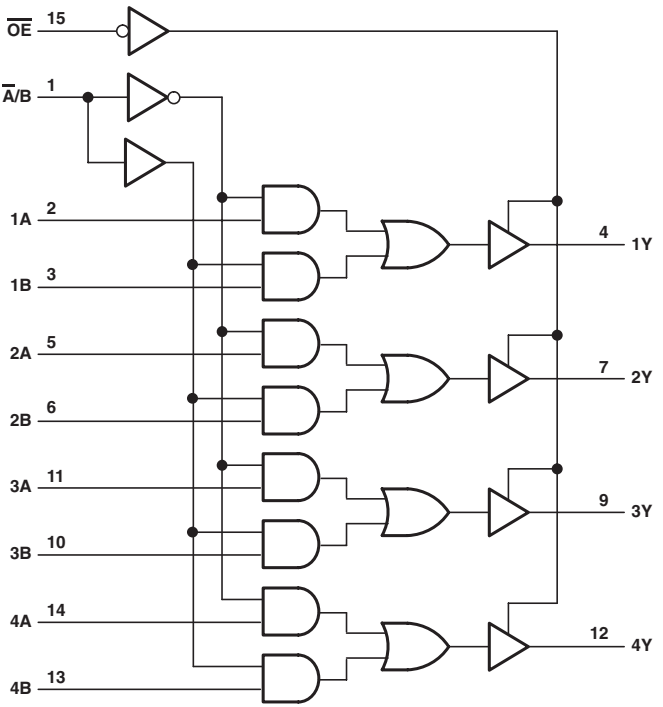
UNIT: ns

257

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

- 3-State Outputs Interface Directly with System Bus
- Provides Bus Interface from Multiple Sources in High-Performance Systems

Logic Diagram (SN74)



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE (SN74)

INPUTS				OUTPUT
OUTPUT CONTROL $\overline{OE}$	SELECT $\overline{A}$/B	A	B	Y
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	CD74 AC	ACT 11	UNIT
I_{CC}	MAX	19	87	14	31.9	23	0.08	0.16	0.08	0.16	0.08	0.16	0.08	mA
I_{OH}	MAX	-2.6	-6.5	-2.6	-15	-3	-6	-6	-6	-6	-24	-24	-24	mA
I_{OL}	MAX	24	20	24	48	24	6	6	6	6	24	24	24	mA

PARAMETER	MAX or MIN	CD74 ACT	LVC 3V	UNIT
I_{CC}	MAX	0.16	0.01	mA
I_{OH}	MAX	-24	-24	mA
I_{OL}	MAX	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT
t_{PLH}	DATA	ANY	MAX	13	7.5	10	5.5	7	25	45	38	50
t_{PHL}				15	6.5	12	6	6.5	25	45	38	50
t_{PLH}	SELECT	ANY	MAX	21	15	18	11	15	25	53	38	57
t_{PHL}				24	15	22	10	9.5	25	53	38	57
t_{PZH}	$\overline{OE}$	Y	MAX	30	19.5	16	7.5	8.5	38	45	38	45
t_{PZL}				30	21	18	9.5	8.5	38	45	38	45
t_{PHZ}	$\overline{OE}$	Y	MAX	30	8.5	10	6.5	7	38	45	38	45
t_{PLZ}				25	14	15	7	7	38	45	38	45

PARAMETER	INPUT	OUTPUT	MAX or MIN	AC 11	CD74 AC	ACT 11	CD74 ACT	LVC 3V
t_{PLH}	DATA	ANY	MAX	6.4	9.3	6.9	10.7	4.6
t_{PHL}				7.2	9.3	8.7	10.7	4.6
t_{PLH}	SELECT	ANY	MAX	7.2	13.4	8.2	15.4	6.4
t_{PHL}				7.9	13.4	9.4	15.4	6.4
t_{PZH}	$\overline{OE}$	Y	MAX	6.5	14.7	7.3	16.1	5.6
t_{PZL}				8.6	14.7	9.6	16.1	5.6
t_{PHZ}	$\overline{OE}$	Y	MAX	7.6	14.7	8.4	16.1	4.3
t_{PLZ}				7.6	14.7	8.5	16.1	4.3

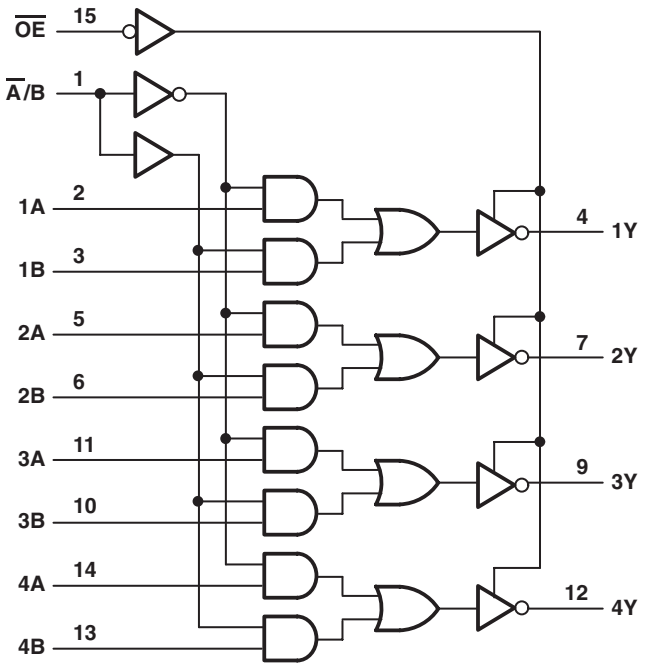
UNIT: ns

258

QUADRUPLE 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

- 3-State Outputs Interface Directly with System Bus
- Provides Bus Interface from Multiple Sources in High-Performance Systems

Logic Diagram (SN74)



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS				OUTPUT
OUTPUT CONTROL $\overline{OE}$	SELECT $\overline{A}$/B	A	B	Y
H	X	X	X	Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 ACT	UNIT
I_{CC}	MAX	16	87	13	25.2	23	0.08	0.16	0.16	0.16	mA
I_{OH}	MAX	-2.6	-6.5	-2.6	-15	-3	-6	-6	-6	-24	mA
I_{OL}	MAX	8	20	24	48	24	6	6	6	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 ACT
t_{PLH}	DATA	Y	MAX	12	6	8	5	6	25	24	34	10.7
t_{PHL}				17	6	7	4	5.5	25	24	34	10.7
t_{PLH}	SELECT	Y	MAX	21	12	25	9.5	9.5	25	35	43	15.4
t_{PHL}				24	12	20	10	11	25	35	43	15.4
t_{PZH}	$\overline{G}$	Y	MAX	30	19.5	18	8	8.5	38	35	35	16.1
t_{PZL}				30	21	18	10	8.5	38	35	35	16.1
t_{PHZ}	$\overline{G}$	Y	MAX	30	8.5	10	6	7	38	38	38	16.1
t_{PLZ}				25	14	18	6.5	7	38	38	38	16.1

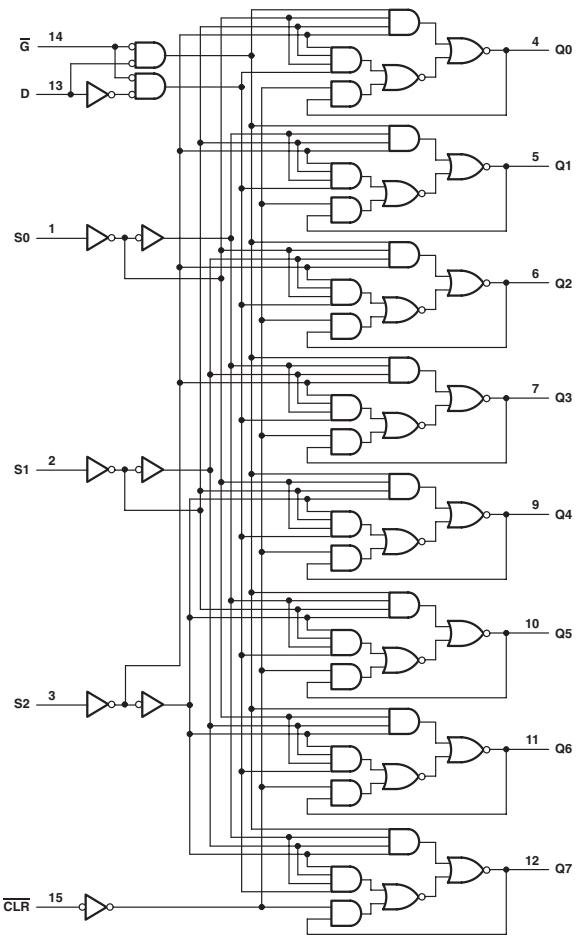
UNIT: ns

259

8-BIT ADDRESSABLE LATCHES

- 8-Bit Parallel-Out Storage Register Performs Serial-to-Parallel Conversion with Storage
- Asynchronous Parallel Clear
- Active-High Decoder
- Enable/Disable Input Simplifies Expansion
- Expandable for n-Bit Applications
- Four Distinct Functional Modes

Logic Diagram (SN74ALS)



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

LATCH SELECTION

SELECT INPUTS			LATCH ADDRESSED
C	B	A	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

FUNCTION TABLE (SN74)

INPUTS		OUTPUT OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
$\overline{CLEAR}$	$\overline{G}$			
H	L	D	Qi0	Addressable latch
H	H	Qi0	Qi0	Memory
L	L	D	L	8-line demultiplexer
L	H	L	L	Clear

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	90	36	22	0.08	0.16	0.16	mA
I_{OH}	MAX	16	8	8	4	4	4	mA
I_{OL}	MAX	-0.8	-0.4	-0.4	-4	-4	-4	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	CD74 HCT
tw	$\overline{G}$ (CDHC/HCT: $\overline{LE}$)			MIN	15	17	15	20	21	27
	$\overline{CLR}$ (CDHC/HCT: $\overline{MR}$)				15	10	10	20	21	27
tsu	DATA			MIN	15	20	15	19	24	26
	ADDRESS				5	17	15	19	24	26
th	DATA			MIN	0	0	0	5	0	0
	ADDRESS				20	0	0	5	0	0
t_{PLH}		$\overline{CLEAR}$ (CDHC/HCT: MR)	Any Q	MAX	25	18	12	38	47	59
t_{PHL}		DATA	Any Q	MAX	24	30	19	33	56	59
t_{PLH}					20	20	12	33	-	59
t_{PHL}		ADDRESS	Any Q	MAX	28	27	22	50	56	61
t_{PLH}					28	20	12	50	-	61
t_{PHL}		ENABLE	Any Q	MAX	20	24	20	43	51	57
t_{PHL}					20	24	13	43	-	57

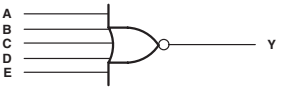
UNIT: ns

260

DUAL 5-INPUT POSITIVE-NOR GATES

● $Y = \overline{A + B + C + D + E}$

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	S	F	UNIT
I_{CC}	MAX	45	9.5	mA
I_{OH}	MAX	-1	-1	mA
I_{OL}	MAX	20	20	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	S	F
t_{PLH}	A, B, C, D, E	Y	MAX	5.5	6.5
t_{PHL}				6	4.5

UNIT: ns

265

QUADRUPLE COMPLEMENTARY-OUTPUT ELEMENTS

● $Y = \overline{A}$, W = A
● Y = AB, W = $\overline{AB}$

Logic Diagram

ELEMENTS 1 and 4

ELEMENTS 2 and 3

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	UNIT
I_{CC}	MAX	34	mA
I_{OH}	MAX	-0.8	mA
I_{OL}	MAX	16	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL
t_{PLH} (W)	A or B	W	MAX	18
t_{PHL} (Y)	A or B	Y	MAX	18
t_{PLH} (W)	A or B	W	MAX	18
t_{PHL} (Y)	A or B	Y	MAX	18
t_{PLH} (W) -t_{PHL} (Y)	A or B	W with respect Y	MAX	±3
t_{PHL} (W) -t_{PLH} (Y)	A or B	W with respect Y	MAX	±3

UNIT: ns

: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

266

QUADRUPLE 2-INPUT EXCLUSIVE-NOR GATES WITH OPEN-DRAIN OUTPUTS

● $Y = \overline{A \oplus B}$

Logic Diagram

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	SN74 HC	UNIT
I_{CC}	MAX	13	0.02	mA
V_{OH}	MAX	5.5	Vcc	V
I_{OL}	MAX	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	SN74 HC
t_{PLH}	A or B Other INPUT Low	Y	MAX	30	31
t_{PHL}	A or B Other INPUT Low	Y	MAX	30	25
t_{PLH}	A or B Other INPUT High	Y	MAX	30	31
t_{PHL}	A or B Other INPUT High	Y	MAX	30	25

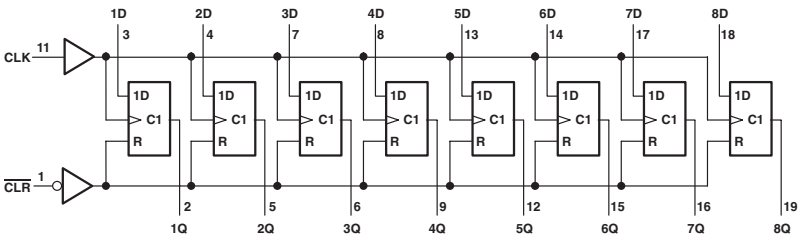
UNIT: ns

273

OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

- Contain Eight Flip-Flops with Single-Rail Outputs
- Buffered Clock and Direct-Clear Inputs

Logic Diagram (SN74)



FUNCTION TABLE (SN74)

INPUTS			OUTPUT Q
$\overline{\text{CLEAR}}$	CLOCK	D	
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	ABT	LVTH 3V	CD74 AC	CD74 ACT	UNIT
I_{CC}	MAX	94	27	29	0.08	0.16	0.08	0.16	30	5	0.16	0.16	mA
I_{OH}	MAX	-0.8	-0.4	-2.6	-4	-4	-4	-4	-32	-32	-24	-24	mA
I_{OL}	MAX	16	8	24	4	4	4	4	64	64	24	24	mA

PARAMETER	MAX or MIN	AHC	AHCT	LV 3V	LV 5V	UNIT
I_{CC}	MAX	0.04	0.04	-	0.02	mA
I_{OH}	MAX	-8	-8	-6	-12	mA
I_{OL}	MAX	8	8	6	12	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	ABT
fmax				MIN	30	30	35	21	20	16	16	150
tw				MIN	16.5	20	14	20	24	25	30	3.3
tsu	DATA INPUT			MIN	20	20	10	25	18	25	18	2.5
	$\overline{CLR}$ INACVIVE			MIN	25	25	15	25	-	25	-	2
th				MIN	5	5	0	0	3	0	3	1.2
t_{PHL}		$\overline{CLEAR}$	ANY Q	MAX	27	27	18	40	45	42	48	7.4
t_{PLH}		CLOCK	ANY Q	MAX	27	27	12	40	45	42	45	6.5
t_{PHL}					27	27	15	40	45	42	45	7.3

PARAMETER		INPUT	OUTPUT	MAX or MIN	LVTH 3V	CD74 AC	CD74 ACT	AHC	AHCT	LV 3V	LV 5V
fmax				MIN	150	100	85	70	45	45	70
tw				MIN	3.3	5	6	5	6.5	6.5	5
tsu	DATA INPUT			MIN	2.3	2	2	4.5	5	6.5	4.5
	$\overline{CLR}$ INACVIVE			MIN	2.3	-	-	2	2.5	2.5	2
th				MIN	0	2	2	1	0	1	1
t_{PHL}		$\overline{CLEAR}$	ANY Q	MAX	4.3	13.5	13.5	12	12.6	19.5	12
t_{PLH}		CLOCK	ANY Q	MAX	4.9	13.5	13.5	12.5	9.8	19.5	12.5
t_{PHL}					4.8	13.5	13.5	12.5	11	19.5	12.5

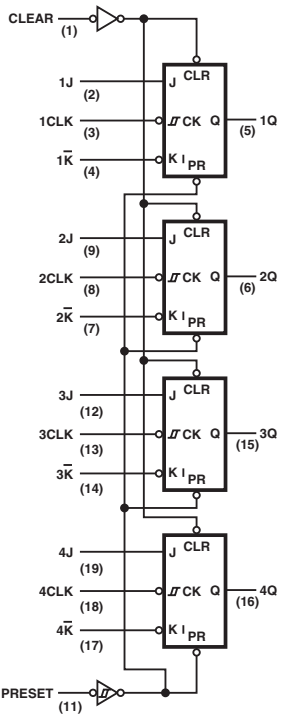
UNIT fmax : MHz, other : ns

276

QUADRUPLE J-$\overline{K}$ FLIP-FLORS

- Separate Negative-Edge-Triggered Clocks
- Fully Buffered Outputs

Logic Diagram



FUNCTION TABLE

COMMON INPUTS		INPUTS			OUTPUT
PRESET	CLEAR	CLOCK	J	K̄	Q
L	H	X	X	X	H
H	L	X	X	X	L
L	L	X	X	X	H†
H	H	↓	L	H	Q_0
H	H	↓	H	H	H
H	H	↓	L	L	L
H	H	↓	H	L	TOGGLE
H	H	H	X	X	Q_0

† The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH}. Furthermore, this configuration is nonstable; that is, it will not persist when either $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	UNIT
I_{CC}	MAX	81	mA
I_{OH}	MAX	-0.8	mA
I_{OL}	MAX	16	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL
fmax				MIN	35
tw	CLOCK high			MIN	13.5
	CLOCK low				15
tsu	J, K			MIN	3
	$\overline{CLR}$, $\overline{PRE}$				10
th				MIN	10
t_{PLH}		$\overline{PRESET}$	Q	MAX	25
t_{PHL}		$\overline{CLEAR}$	Q	MAX	30
t_{PLH}		CLOCK	Q	MAX	30
t_{PHL}					30

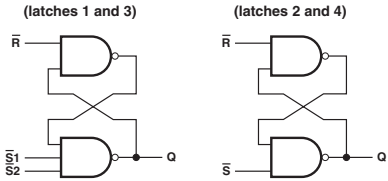
UNIT fmax : MHz, other : ns

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

279

QUADRUPLE $\overline{S}$-$\overline{R}$ LATCHES

Logic Diagram



FUNCTION TABLE
(each latch)

INPUTS		OUTPUT
$\overline{S}$†	$\overline{R}$	Q
H	H	Q_0
L	H	H
H	L	L
L	L	H‡

H = high level L = low level
†For latches with double S inputs:
Q_0 = the level of Q before the indicated input conditions were established.
‡This configuration is nonstable: that is, it may not persist when the $\overline{S}$ and $\overline{R}$ inputs return to their inactive (high) level.
H = both $\overline{S}$ inputs high
L = one or both $\overline{S}$ inputs low

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	UNIT
I_{CC}	MAX	30	7	mA
I_{OH}	MAX	-0.8	-0.4	mA
I_{OL}	MAX	16	8	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS
t_W			MIN	20	20
t_{PLH}	$\overline{S}$	Q	MAX	22	22
t_{PHL}				15	21
t_{PHL}	$\overline{R}$		MAX	27	27

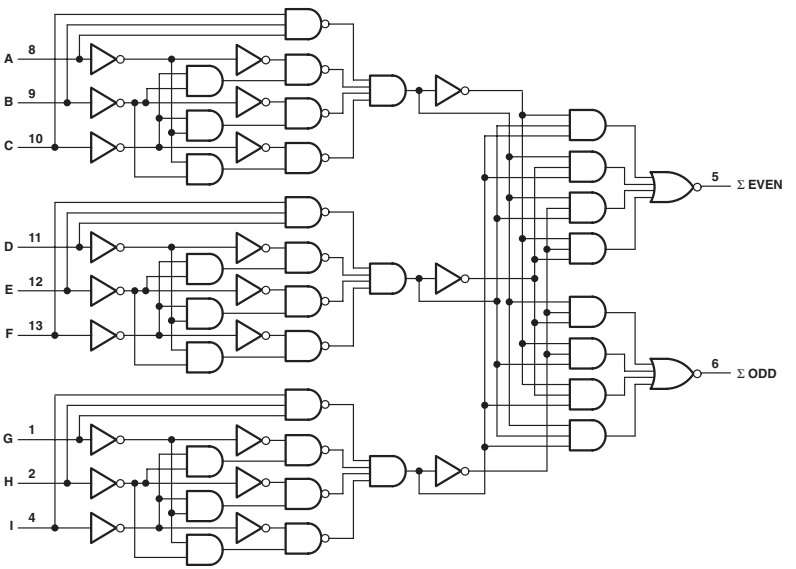
UNIT: ns

280

9-BIT PARITY GENERATORS/CHECKERS

- Generate Either Odd or Even Parity for Nine Data Lines
- Cascadable for n-Bit Parity

Logic Diagram (SN74)



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE (SN74)

NO. OF INPUTS A–I THAT ARE HIGH	OUTPUTS	
	Σ EVEN	Σ ODD
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	UNIT
I_{CC}	MAX	27	105	16	35	35	0.08	0.16	0.16	0.16	0.16	mA
I_{OH}	MAX	-0.4	-1	-2.6	-2	-1	-4	-4	-4	-24	-24	mA
I_{OL}	MAX	8	20	24	20	20	4	4	4	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT
t_{PLH}	DATA	Σ EVEN (CD74: ΣE)	MAX	50	21	20	12	10	52	60	63	20	21.6
t_{PHL}				45	18	20	11	11	52	60	63	20	21.6
t_{PLH}	DATA	Σ ODD (CD74: ΣO)	MAX	35	21	20	12	10	52	60	68	21	21.6
t_{PHL}				50	18	22	11.5	11	52	60	68	21	21.6

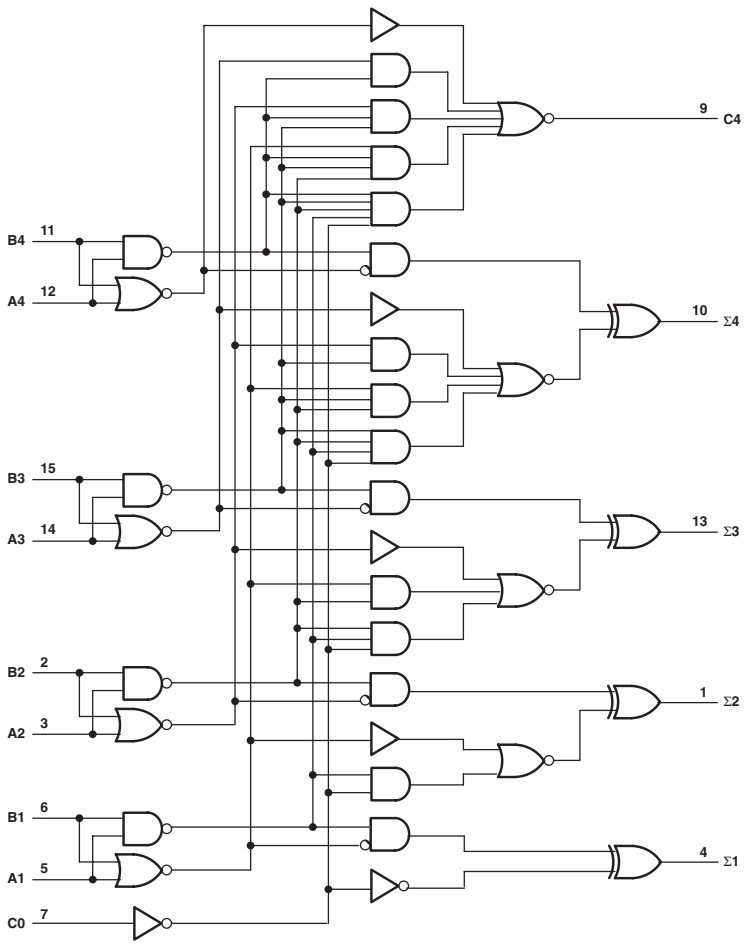
UNIT: ns

283

4-BIT BINARY FULL ADDERS WITH FAST CARRY

- Full-Carry Look-Ahead Across the Four Bits

Logic Diagram (SN74)



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE (SN74)

INPUTS				OUTPUTS					
				WHEN C0 = L			WHEN C0 = H		
				WHEN C2 = L			WHEN C2 = H		
A1	B1	A2	B2	Σ1	Σ2	C2	Σ1	Σ2	C2
A3	B3	A4	B4	Σ3	Σ4	C4	Σ3	Σ4	C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	TTL	LS	S	F	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	UNIT
I_{CC}		MAX	110	39	160	55	0.16	0.16	0.16	0.16	mA
I_{OH}	Any OUTPUT except C4	MAX	-0.8	-0.4	-1	-1	-4	-4	-24	-24	mA
	C4	MAX	-0.4		-0.5						
I_{OL}	Any OUTPUT except C4	MAX	16	8	20	20	4	4	24	24	mA
	C4	MAX	8		10						

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	F	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT
t_{PLH}	C0 (CD74:C_{IN})	Any Σ (CD74:S_i)	MAX	21	24	18	10.5	69	80	17.6	17.6
t_{PHL}			MAX	21	24	18	10.5	69	80	17.6	17.6
t_{PLH}	An or Bn	Σn (CD74:Sn)	MAX	24	24	18	10.5	63	74	18.2	18.2
t_{PHL}			MAX	24	24	18	10.5	63	74	18.2	18.2
t_{PLH}	C0 (CD74:C_{IN})	C4 (CD74:C_{OUT})	MAX	14	17	11	8.5	59	69	17.6	17.6
t_{PHL}			MAX	16	22	11	8	59	69	17.6	17.6
t_{PLH}	An or Bn		MAX	14	17	12	8.5	59	72	17.6	17.6
t_{PHL}			MAX	16	17	12	8	59	72	17.6	17.6

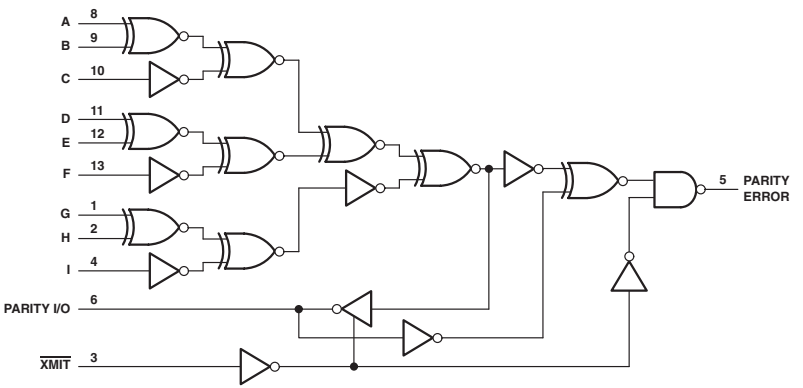
UNIT: ns

286

9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS WITH BUS DRIVER PARITY I/O PORT

- Generate Either Odd or Even Parity for Nine Data Lines
- Cascadable for n-Bit Parity
- Direct Bus Connection for Parity Generation or Checking by Using the Parity I/O Port
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram (SN74AS)



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE (SN74AS)

NUMBER OF INPUTS (A–I) THAT ARE HIGH	$\overline{\text{XMIT}}$	PARITY I/O	PARITY ERROR
0, 2, 4, 6, 8	l	H	H
1, 3, 5, 7, 9	l	L	H
0, 2, 4, 6, 8	h h	h l	H L
1, 3, 5, 7, 9	h h	h l	L H

h = high input level l = low input level
H = high output level L = low output level

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	AS	AC 11	ACT 11	UNIT
I_{CC}		MAX	50	0.08	0.08	mA
I_{OH}	Parity error	MAX	-2	-24	-24	mA
	Parity I/O	MAX	-15	-24	-24	mA
I_{OL}	Parity error	MAX	20	24	24	mA
	Parity I/O	MAX	48	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AS	AC 11	ACT 11
t_{PLH}	A to I	Parity I/O	MAX	15	9	10.4
t_{PHL}				14	107	12
t_{PLH}	A to I	Parity error	MAX	16.5	10	11.3
t_{PHL}				16.5	12	12.9
t_{PLH}	Parity I/O	Parity error	MAX	9	6.2	7.7
t_{PHL}				9	7.9	9.1
t_{PZH}	$\overline{\text{XMIT}}$	Parity I/O	MAX	13	5.3	7.3
t_{PZL}				16	8.9	11.4
t_{PHZ}				11.5	6.5	8.5
t_{PLZ}				10	6.3	7.8

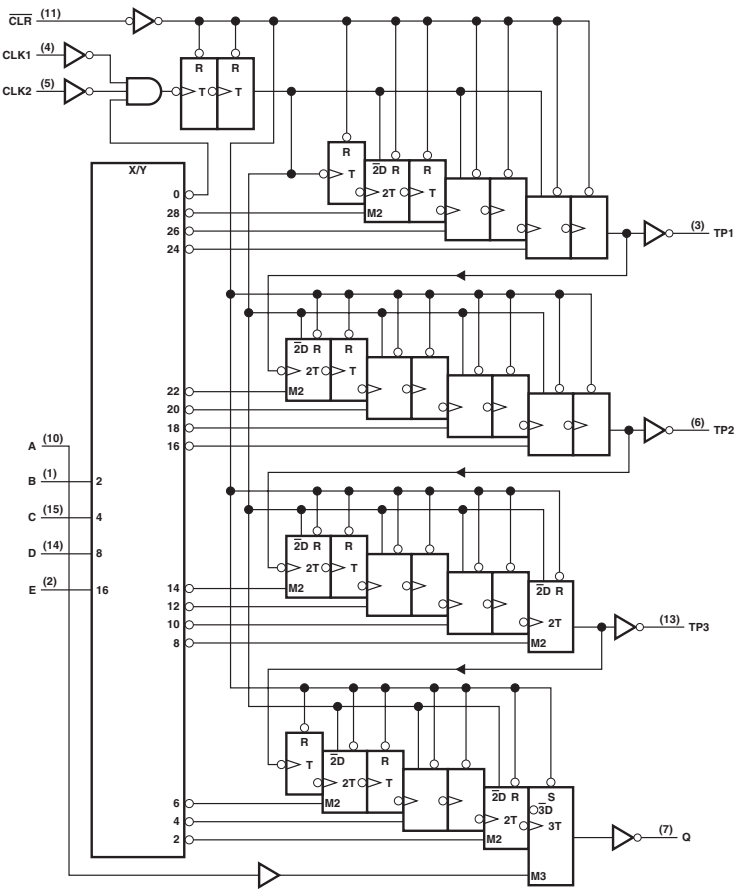
UNIT: ns

292

PROGRAMMABLE FREQUENCY DIVIDERS/DIGITAL TIMERS

- Digitally Programmable from 2^2 to 2^{31}
- Easily Expandable
- Applications:
  Frequency Division
  Digital Timing

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

CLEAR	CLK 1	CLK 2	Q OUTPUT MODE
L	X	X	Cleared to L
H	≠	L	Count
H	L	≠	Count
H	H	X	Inhibit
H	X	H	Inhibit

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

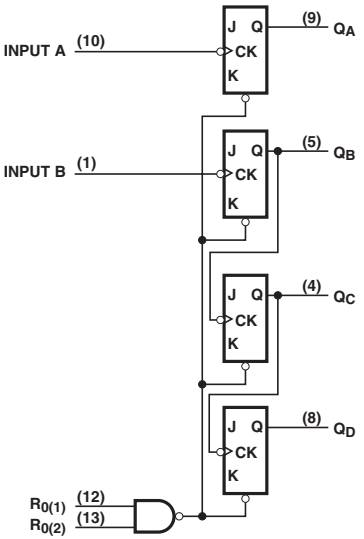
PARAMETER	MAX or MIN	LS	UNIT
I_{CC}	MAX	75	mA
I_{OH} (Q only)	MAX	-1.2	V
I_{OL} (Q only)	MAX	24	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
fmax	CLK		MIN	30
t_{PLH}	CLK	Q	MAX	90
t_{PHL}	CLK	Q	MAX	120
t_{PHL}	$\overline{CLR}$	$\overline{Q}$	MAX	65

UNIT fmax : MHz, other : ns

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

COUNT SEQUENCE

COUNT	OUTPUTS			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTE: Output Q_A is connected to input B.

RESET/COUNT FUNCTION TABLE

RESET INPUTS		OUTPUTS			
$R_{0(1)}$	$R_{0(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	UNIT
I_{CC}	MAX	39	15	mA
I_{OH}	MAX	-0.8	-0.4	mA
I_{OL}	MAX	16	8	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS
fmax		A	QA	MIN	32	32
		B	QB	MIN	16	16
tw	A	A, B		MIN	15	15
	B				30	30
	Reset				15	15
tsu				MIN	25	25
t_{PLH}		A	QA	MAX	16	16
t_{PHL}					18	18
t_{PLH}		A	QB	MAX	70	70
t_{PHL}					70	70
t_{PLH}		B	QB	MAX	16	16
t_{PHL}					21	21
t_{PLH}		B	QC	MAX	32	32
t_{PHL}					35	35
t_{PLH}		B	QD	MAX	51	51
t_{PHL}					51	51

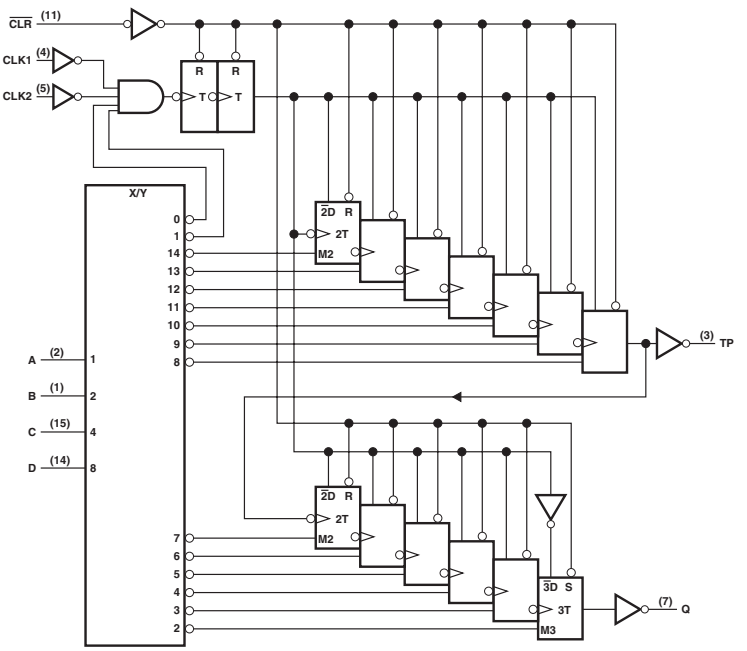
UNIT fmax : MHz, other : ns

294

PROGRAMMABLE FREQUENCY DIVIDERS/DIGITAL TIMERS

- Digitally Programmable from 2^2 to 2^{15}
- Easily Expandable
- Applications
  - Frequency Division
  - Digital Timing

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

PROGRAMMING INPUTS				FREQUENCY DIVISION			
				Q		TP	
D	C	B	A	BINARY	DECIMAL	BINARY	DECIMAL
L	L	L	L	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	H	Inhibit	Inhibit	Inhibit	Inhibit
L	L	H	L	2^2	4	2^9	512
L	L	H	H	2^3	8	2^9	512
L	H	L	L	2^4	16	2^9	512
L	H	L	H	2^5	32	2^9	512
L	H	H	L	2^6	64	2^9	512
L	H	H	H	2^7	128	Disabled Low	
H	L	L	L	2^8	256	2^2	4
H	L	L	H	2^9	512	2^3	8
H	L	H	L	2^{10}	1024	2^4	16
H	L	H	H	2^{11}	2048	2^5	32
H	H	L	L	2^{12}	4096	2^6	64
H	H	L	H	2^{13}	8192	2^7	128
H	H	H	L	2^{14}	16384	2^8	256
H	H	H	H	2^{15}	32768	2^9	512

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

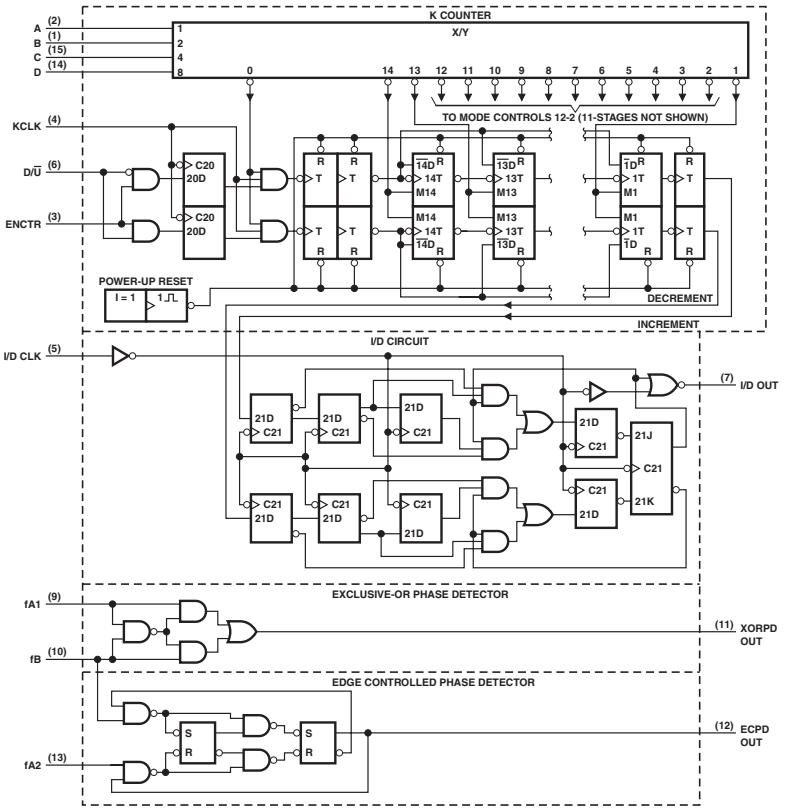
PARAMETER	MAX or MIN	LS	UNIT
I_{CC}	MAX	50	mA
I_{OH}	MAX	-1.2	V
I_{OL}	MAX	24	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
fmax	CLK		MIN	30
tw	CLK 1 or 2		MIN	16
	CLR		MIN	35
t_{PLH}	CLK 1 or 2	Q	MAX	90
t_{PHL}				120
t_{PLH}	$\overline{CLR}$	$\overline{Q}$	MAX	65

UNIT fmax : MHz, other : ns

Logic Diagram (SN74LS)



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLES (SN74LS)

K COUNTER FUNCTION TABLE (DIGITAL CONTROL)

D	C	B	A	MODULO (K)
L	L	L	L	Inhibited
L	L	L	H	2^2
L	L	H	L	2^4
L	L	H	H	2^5
L	H	L	L	2^6
L	H	L	H	2^7
L	H	H	L	2^8
L	H	H	H	2^9
H	L	L	L	2^{10}
H	L	L	H	2^{11}
H	L	H	L	2^{12}
H	L	H	H	2^{13}
H	H	L	L	2^{14}
H	H	L	H	2^{15}
H	H	H	L	2^{16}
H	H	H	H	2^{17}

EXCLUSIVE OR PHASE DETECTOR

ϕA1	ϕB	XORPD OUT
L	L	L
L	H	H
H	L	H
H	H	L

EDGE-CONTROLLED PHASE DETECTOR

ϕA2	ϕB	ECPD OUT
H or L	↓	H
↓	H or L	L
H or L	↑	No change
↑	H or L	No change

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	CD74 HC	CD74 HCT	CD74 ACT	UNIT
I_{CC}		MAX	120	0.16	0.16	0.08	mA
I_{OH}	I/D OUT	MAX	-1	-6	-4	-24	mA
	XOR, ECPD	MAX	-0.4				
I_{OL}	I/D OUT	MAX	24	4	4	24	mA
	XOR, ECPD	MAX	8				

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT		OUTPUT	MAX or MIN	LS	CD74 HC	CD74 HCT	CD74 ACT
fmax		K CLK (K_{CP})		I/D OUT	MIN	32	20	20	45
		I/D CLK (I/D_{CP})		I/D OUT		16	13	13	35
tw	K CLK (K_{CP})				MIN	16	24	24	8
	I/D CLK (I/D_{CP})					33	38	38	9
tsu	$\overline{D}$/U				MIN	30	30	30	17
	ENCLR (EN_{CTR})					31	30	30	16
th	$\overline{D}$/U				MIN	0	0	0	7
	ENCLR (EN_{CTR})					0	0	0	6
t_{PLH}		I/D CLK ↑		I/D OUT	MAX	25	53	53	24
t_{PHL}						35	53	53	24
t_{PLH}		ϕA1 or ϕB	other INPUT low	XORPD OUT	MAX	15	45	45	22
			other INPUT high			25	45	45	22
t_{PHL}		ϕA1 or ϕB	other INPUT low	XORPD OUT		25	45	45	22
			other INPUT high			25	45	45	22
t_{PLH}		ϕB ↓		ECPD OUT	MAX	30	60	60	30
t_{PHL}		ϕA2 ↓		ECPD OUT		30	60	60	30

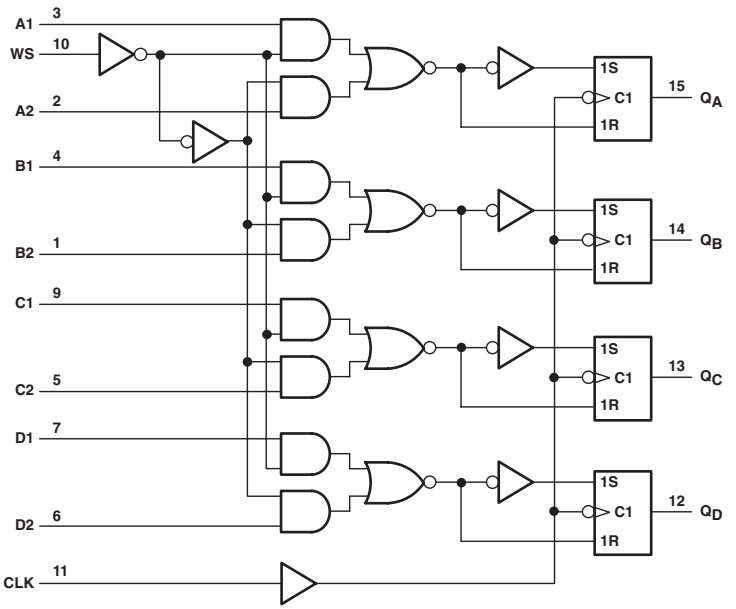
UNIT fmax : MHz, other : ns

298

QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE

- Outputs Storage Register

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS		OUTPUTS			
WORD SELECT	CLOCK	Q_A	Q_B	Q_C	Q_D
L	↓	A1	B1	C1	D1
H	↓	A2	B2	C2	D2
X	H	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

† a1, a2, etc. = the level of steady-state input at A1, A2, etc.
QA0, QB0, etc. = the level of QA, QB, etc. entered
on the most recent O transition of CLK

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	AS	SN74 HC	UNIT
I_{CC}	MAX	65	21	36	0.08	mA
I_{OL}	MAX	16	8	20	4	mA
I_{OH}	MAX	-0.8	-0.4	-2	-4	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	AS	SN74 HC
tw				MIN	20	20	8	27
tsu	Data			MIN	15	15	4.5	21
	Word Select				25	25	13	21
th	Data			MIN	5	5	3.5	0
	Word Select				0	0	1	0
t_{PLH}		CLK	GA to GD	MAX	27	27	9	31
t_{PHL}					32	32	11	31

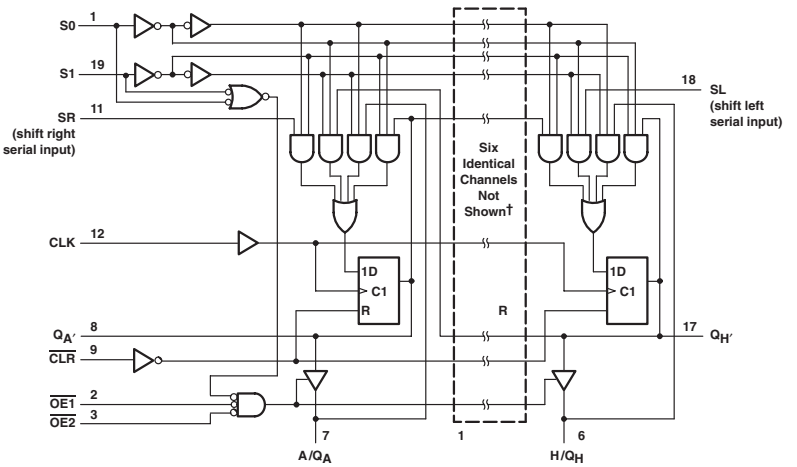
UNIT: ns

299

8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS

- Multiplexed I/O Ports Provide Improved Bit Density
- Four Modes of Operation:
  - Hold (Store)
  - Shift Right
  - Shift Left
  - Load Data
- Operate with Outputs Enabled or at High Impedance
- 3-State Outputs Drive Bus Lines Directly
- Can Be Cascaded for n-Bit Word Lengths

Logic Diagram (SN74)



† I/O ports not shown: B/Q_B (13), C/Q_C (6), D/Q_D (14), E/Q_E (5), F/Q_F (15), and G/Q_G (4).

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE (SN74)

MODE	INPUTS								I/O PORTS								OUTPUTS	
	$\overline{CLR}$	S1	S0	$\overline{OE1}$†	$\overline{OE2}$†	CLK	SL	SR	A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	$Q_{A'}$	$Q_{H'}$
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
	H	L	H	L	L	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

NOTE: a...h=the level of the steady-state input at inputs A through H, respectively. This data is loaded into the flip-flops while the flip-flop outputsare isolated from the I/O terminals.
† When one or both output-enable inputs are high, the eight I/O terminals are disabled to the high-impedance state; however, sequential operationor clearing of the register is not affected.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	S	ALS	F	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	UNIT
I_{CC}		MAX	53	225	40	95	0.16	0.16	0.16	0.16	mA
I_{OH}	Q_A thru Q_H	MAX	-2.6	-6.5	-2.6	-3	-6	-4	-24	-24	mA
	$Q_{A'}$ or $Q_{H'}$		-0.4	-0.5	-0.4	-1	-4	-4	-24	-24	
I_{OL}	Q_A thru Q_H	MAX	24	20	24	24	6	4	24	24	mA
	$Q_{A'}$ or $Q_{H'}$		8	6	8	20	4	4	24	24	

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	LS	S	ALS	F	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT
fmax				MIN	20	50	30	70	20	16	95	90
tw	CLK (CP) high			MIN	30	10	16.5	7	24	30	5.2	5.5
	CLK (CP) low				10	10	16.5	7	24	30	5.2	5.5
	$\overline{CLR}$ (MR)				20	10	10	7	15	22	5	5
tsu	DATA "H"			MIN	20	7	16	5.5	36	30	4.5	4.5
	DATA "L"				20	5	6	5.5	36	30	4.5	4.5
	SELECT				35	15	20	8.5	36	41	9	9
	$\overline{CLR}$ (MR) INACTIVE				20	10	15	7	-	-	-	-
th	DATA			MIN	0	5	0	2	0	0	0	0
	SELECT				10	5	0	0	0	0	0	0
t_{PLH}		CLK (CD74: CP)	$Q_{A'}$ or $Q_{H'}$ (CD74: Q_0 or Q_7)	MAX	33	20	15	10	60	68	12.9	12.9
t_{PHL}					39	20	18	9.5	60	68	12.9	12.9
t_{PLH}		CLK (CD74: CP)	Q_A thru Q_H (CD74: I/O_0 thru I/O_7)	MAX	25	21	13	10	60	68	13.5	14.5
t_{PHL}					39	21	19	12	60	68	13.5	14.5
t_{PHL}		$\overline{CLR}$	$Q_{A'}$ or $Q_{H'}$ (CD74: Q_0 or Q_7)	MAX	40	21	22	10.5	60	69	11.2	12.2
t_{PHL}		$\overline{CLR}$	Q_A thru Q_H (CD74: I/O_0 thru I/O_7)		40	24	22	15	60	69	13.9	18.6
t_{PZH}		$\overline{OE1}$, $\overline{OE2}$	Q_A thru Q_H	MAX	21	18	16	9	47	48	14.9	14.9
t_{PZL}					30	18	22	11	39	45	14.9	14.9
t_{PHZ}		$\overline{OE1}$, $\overline{OE2}$	Q_A thru Q_H	MAX	20	12	8	7	56	56	14.9	14.9
t_{PLZ}					15	12	15	6.5	47	48	14.9	14.9

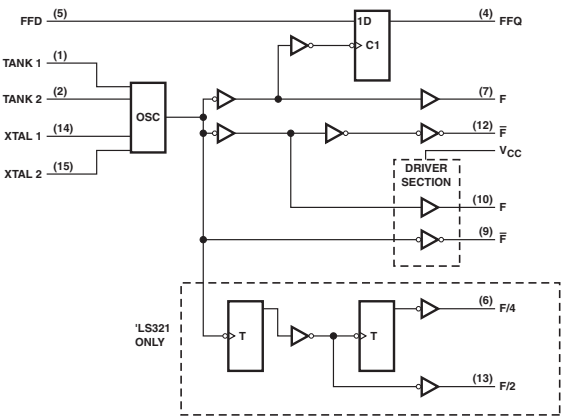
UNIT fmax : MHz, other : ns

321

CRYSTAL-CONTROLLED OSCILLATORS

- Crystal-Controlled Oscillator Operation from 1MHz to 20MHz
- Complementary Outputs

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	UNIT
I_{CC}		MAX	75	mA
I_{OH}	F' or $\overline{F'}$	MAX	-24	mA
	F, $\overline{F}$, F/2, F/4	MAX	-0.4	mA
I_{OL}	F' or $\overline{F'}$	MAX	24	mA
	F, $\overline{F}$, F/2, F/4	MAX	8	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
fmax		F/2	MIN	10
		F/4	MAX	5
		ANY	MIN	20
tr		F',F'	MAX	14
		ANY	MAX	40
tf		F',F'	MAX	10
		ANY	MAX	20

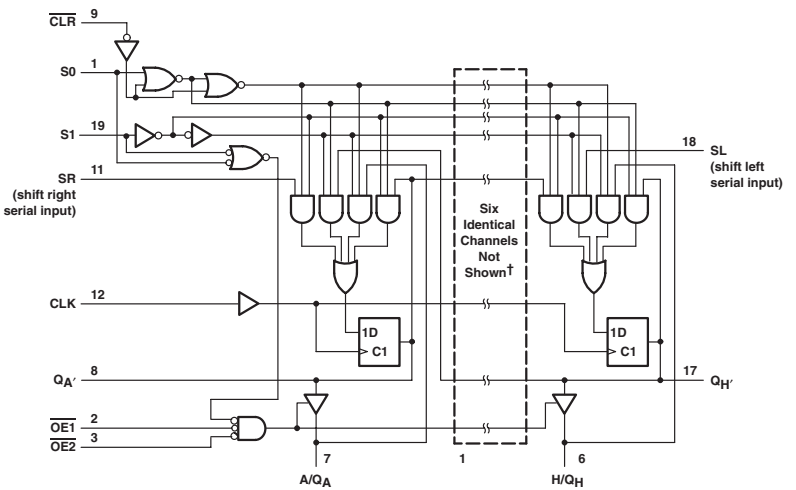
UNIT fmax : MHz, other : ns

323

8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH SYNCHRONOUS CLEAR AND 3-STATE OUTPUTS

- Multiplexed I/O Ports Provide Improved Bit Density
- Four Modes of Operation:
  - Hold (Store)
  - Shift Right
  - Shift Left
  - Load Data
- 3-State Outputs Drive Bus Lines Directly
- Can Be Cascaded for n-Bit Word Lengths

Logic Diagram (SN74ALS)



† I/O ports not shown: B/Q_B (13), C/Q_C (6), D/Q_D (14), E/Q_E (5), F/Q_F (15), and G/Q_G (4).

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE (SN74)

MODE	INPUTS							I/O BORD								OUTPUTS	
	$\overline{CLR}$	SELECT		OUTPUT CONTROL		CLK	SEREAL		A/Q_A	B/Q_B	C/Q_C	C/Q_D	C/Q_E	C/Q_F	C/Q_G	H/Q_H	$Q_{A'}$	$Q_{H'}$
		S1	S0	$\overline{OE1}$†	$\overline{OE2}$†		SL	SR										
Clear	L	X	L	L	L	↑	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	↑	X	X	L	L	L	L	L	L	L	L	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{A0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
	H	L	H	L	L	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

† a ...h=t he level of the steady-state input at inputs A through H, respectively. This data is loaded into the flip-flops while the flip-flop outputsare isolated from the I/O terminals.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	ALS	CD74 AC	CD74 ACT	UNIT
I_{CC}		MAX	225	40	0.16	0.16	mA
I_{OH}	$Q_{A'}$ or $Q_{H'}$	MAX	-0.5	-0.4	-24	-24	mA
	Q_A thru Q_H		-6.5	-2.6	-24	-24	mA
I_{OL}	$Q_{A'}$ or $Q_{H'}$	MAX	6	8	24	24	mA
	Q_A thru Q_H		20	24	24	24	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	LS	ALS	CD74 AC	CD74 ACT
fmax				MIN	25	17	95	90
tw	CLK			MIN	30	16.5	5.2	5.5
	$\overline{CLR}$				20	-	5	5
tsu	DATA H			MIN	20	16	4.5	4.5
	DATA L				20	6	4.5	4.5
	SELECT				-	20	9	9
	$\overline{CLR}$				-	20	5.5	5.5
th	SELECT			MIN	-	0	0	0
	DATA				0	0	0	0
t_{PLH}		CLK	$Q_{A'}$ or $Q_{B'}$	MAX	33	15	12.9	12.9
t_{PHL}					39	18	12.9	12.9
t_{PLH}		CLK	Q_A thru Q_H	MAX	25	13	13.5	14.5
t_{PHL}					39	19	13.5	14.5
t_{PZH}		$\overline{OE1}$	Q_A thru Q_H	MAX	21	16	14.9	14.9
t_{PZL}					30	22	14.9	14.9
t_{PHZ}		$\overline{OE1}$	Q_A thru Q_H	MAX	20	8	14.9	14.9
t_{PLZ}					15	15	14.9	14.9
t_{PZH}		$\overline{OE2}$	Q_A thru Q_H	MAX	21	16	14.9	14.9
t_{PZL}					30	22	14.9	14.9
t_{PHZ}		$\overline{OE2}$	Q_A thru Q_H	MAX	20	8	14.9	14.9
t_{PLZ}					15	15	14.9	14.9

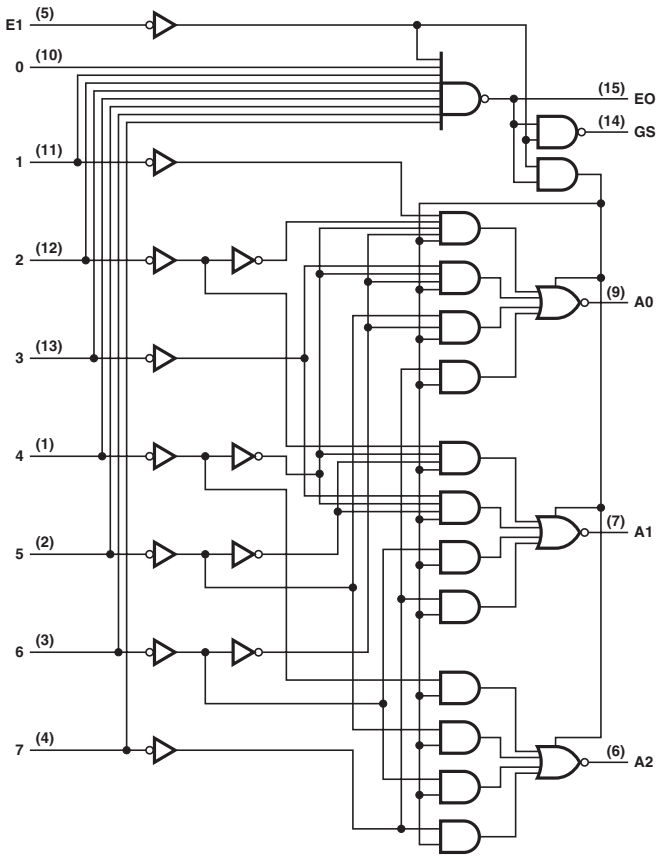
UNIT fmax : MHz, other : ns

348

8-LINE TO 3-LINE PRIORITY ENCODERS WITH 3-STATE OUTPUTS

- 3-State Outputs Drive Bus Lines Directly
- Encodes 8 Data Lines to 3-Line Binary (Octal)

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS								OUTPUTS				
E1	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**A2**	**A1**	**A0**	**GS**	**E0**
H	X	X	X	X	X	X	X	X	Z	Z	Z	H	H
L	H	H	H	H	H	H	H	H	Z	Z	Z	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	UNIT
I_{CC}		MAX	25	mA
I_{OH}	A0, A1, A2	MAX	-2.6	mA
	E0, ES	MAX	-0.4	mA
I_{OL}	A0, A1, A2	MAX	24	mA
	E0, ES	MAX	8	mA

SWITCHING CHARACTERISTICS

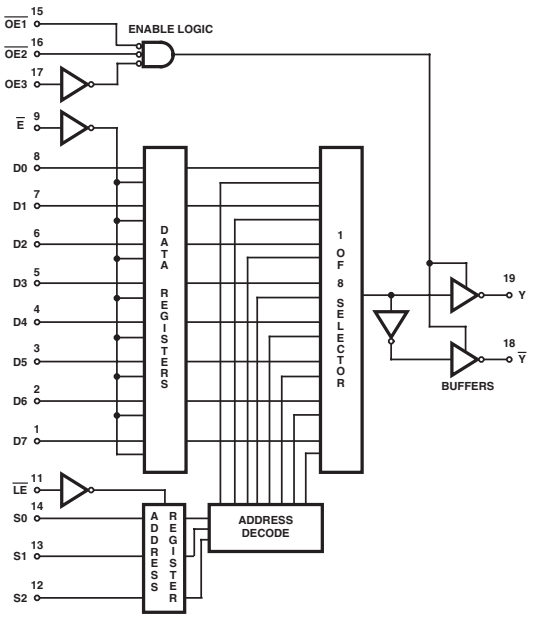
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
t_{PLH}	1 to 7	A0, A1, A2	MAX	35
t_{PHL}			MAX	35
t_{PLH}	0 to 7	E0	MAX	18
t_{PHL}			MAX	40
t_{PLH}	0 to 7	GS	MAX	55
t_{PHL}			MAX	21

UNIT: ns

8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS/TRANSPARENT/REGISTERS WITH 3-STATE OUTPUTS

Logic Diagram

(CD74)



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE (SN74)

INPUTS							OUTPUTS	
SELECT†			$\overline{DC}$	OUTPUT ENABLES				
S2	S1	S0		$\overline{G1}$	$\overline{G2}$	G3	W	Y
X	X	X	X	H	X	X	Z	Z
X	X	X	X	X	H	X	Z	Z
X	X	X	X	X	X	L	Z	Z
L	L	L	L	L	L	H	$\overline{D0}$	D0
L	L	L	H	L	L	H	$\overline{D0}_n$	$D0_n$
L	L	H	L	L	L	H	$\overline{D1}$	D1
L	L	H	H	L	L	H	$\overline{D1}_n$	$D1_n$
L	H	L	L	L	L	H	$\overline{D2}$	D2
L	H	L	H	L	L	H	$\overline{D2}_n$	$D2_n$
L	H	H	L	L	L	H	$\overline{D3}$	D3
L	H	H	H	L	L	H	$\overline{D3}_n$	$D3_n$
H	L	L	L	L	L	H	$\overline{D4}$	D4
H	L	L	H	L	L	H	$\overline{D4}_n$	$D4_n$
H	L	H	L	L	L	H	$\overline{D5}$	D5
H	L	H	H	L	L	H	$\overline{D5}_n$	$D5_n$
H	H	L	L	L	L	H	$\overline{D6}$	D6
H	H	L	H	L	L	H	$\overline{D6}_n$	$D6_n$
H	H	H	L	L	L	H	$\overline{D7}$	D7
H	H	H	H	L	L	H	$\overline{D7}_n$	$D7_n$

NOTES:

H = High Voltage Level (Steady State), L = Low Voltage Level (Steady State), X = Don't Care, Z = High Impedance State (Off State), $D0_n$ ... $D7_n$ = the level of steady-state inputs D0 through D7, respectively, before the most recent low-to-high transition of data control.

† This column shows the input address setup with $\overline{LE}$ low.

TRUTH TABLE (CD74)

INPUTS							OUTPUTS	
SELECT (NOTE 3)			ENABLE DATA	OUTPUT ENABLES				
S2	S1	S0	$\overline{E}$	$\overline{OE1}$	$\overline{OE2}$	OE3	$\overline{Y}$	Y
X	X	X	X	H	X	X	Z	Z
X	X	X	X	X	H	X	Z	Z
X	X	X	X	X	X	L	Z	Z
L	L	L	L	L	L	H	$\overline{D0}$	D0
L	L	L	H	L	L	H	$\overline{D0}_n$	$D0_n$
L	L	H	L	L	L	H	$\overline{D1}$	D1
L	L	H	H	L	L	H	$\overline{D1}_n$	$D1_n$
L	H	L	L	L	L	H	$\overline{D2}$	D2
L	H	L	H	L	L	H	$\overline{D2}_n$	$D2_n$
L	H	H	L	L	L	H	$\overline{D3}$	D3
L	H	H	H	L	L	H	$\overline{D3}_n$	$D3_n$
H	L	L	L	L	L	H	$\overline{D4}$	D4
H	L	L	H	L	L	H	$\overline{D4}_n$	$D4_n$
H	L	H	L	L	L	H	$\overline{D5}$	D5
H	L	H	H	L	L	H	$\overline{D5}_n$	$Dn5$
H	H	L	L	L	L	H	$\overline{D6}$	D6
H	H	L	H	L	L	H	$\overline{D6}_n$	$D6_n$
H	H	H	L	L	L	H	$\overline{D7}$	D7
H	H	H	H	L	L	H	$\overline{D7}_n$	$D7_n$

H = High Voltage Level (Steady State); L = Low Voltage Level (Steady State); X = Don't Care; Z = High Impedance State (Off State); $D0_n$...$D7_n$ = the level of steady-state inputs D0 through D7, respectively, before the most recent low-to-high transition of data control.

NOTE:

1. This column shows the input address setup with $\overline{LE}$ low.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

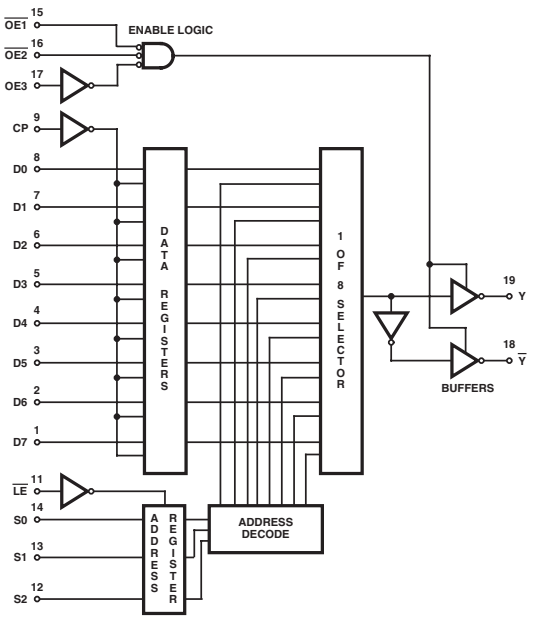
PARAMETER	MAX or MIN	LS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	46	0.08	0.16	0.16	mA
I_{OH}	MAX	-2.6	-6	-6	-4	mA
I_{OL}	MAX	24	6	6	4	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	SN74 HC	CD74 HC	CD74 HCT
t_{su}			MAX	15	19	15	15
t_h			MAX	15	5	14	14
t_{PLH}	D0 thru D7	Y	MAX	36	59	63	71
t_{PHL}			MAX	35	59	63	71
t_{PLH}	D0 thru D7	W (CD74: $\overline{Y}$)	MAX	27	59	63	71
t_{PHL}			MAX	44	59	63	71
t_{PLH}	$\overline{DC}$ (CD74: $\overline{E}$)	Y	MAX	42	68	75	81
t_{PHL}			MAX	39	68	75	81
t_{PLH}	$\overline{DC}$ (CD74: $\overline{E}$)	W (CD74: $\overline{Y}$)	MAX	33	68	75	81
t_{PHL}			MAX	50	68	75	81

UNIT:ns

Logic Diagram
(CD74)



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE (SN74)

INPUTS							OUTPUTS	
SELECT†			CLK	OUTPUT ENABLES				
C2	C1	C0		$\overline{G1}$	$\overline{G2}$	G3	W	Y
X	X	X	X	H	X	X	Z	Z
X	X	X	X	X	H	X	Z	Z
X	X	X	X	X	X	L	Z	Z
L	L	L	↑	L	L	H	$\overline{D0}$	D0
L	L	L	H or L	L	L	H	$\overline{D0_n}$	$D0_n$
L	L	H	↑	L	L	H	$\overline{D1}$	D1
L	L	H	H or L	L	L	H	$\overline{D1_n}$	$D1_n$
L	H	L	↑	L	L	H	$\overline{D2}$	D2
L	H	L	H or L	L	L	H	$\overline{D2_n}$	$D2_n$
L	H	H	↑	L	L	H	$\overline{D3}$	D3
L	H	H	H or L	L	L	H	$\overline{D3_n}$	$D3_n$
H	L	L	↑	L	L	H	$\overline{D4}$	D4
H	L	L	H or L	L	L	H	$\overline{D4_n}$	$D4_n$
H	L	H	↑	L	L	H	$\overline{D5}$	D5
H	L	H	H or L	L	L	H	$\overline{D5_n}$	$D5_n$
H	H	L	↑	L	L	H	$\overline{D6}$	D6
H	H	L	H or L	L	L	H	$\overline{D6_n}$	$D6_n$
H	H	H	↑	L	L	H	$\overline{D7}$	D7
H	H	H	H or L	L	L	H	$\overline{D7_n}$	$D7_n$

NOTES:

H = High Voltage Level (Steady State), L = Low Voltage Level (Steady State), ↑ = Transition form Low to High Level, X = Don't Care, Z = High Impedance State (Off State), $D0_n$ ... $D7_n$ = the level of steady-state inputs D0 through D7, respectively, before the most recent low-to-high transition of data control.

† This column shows the input address setup with $\overline{LE}$ low.

TRUTH TABLE (CD74)

INPUTS							OUTPUTS	
SELECT (NOTE 3)			CLOCK	OUTPUT ENABLES				
S2	S1	S0	CP	$\overline{OE1}$	$\overline{OE2}$	OE3	$\overline{Y}$	Y
X	X	X	X	H	X	X	Z	Z
X	X	X	X	X	H	X	Z	Z
X	X	X	X	X	X	L	Z	Z
L	L	L	↑	L	L	H	$\overline{D0}$	D0
L	L	L	H or L	L	L	H	$\overline{D0_n}$	$D0_n$
L	L	H	↑	L	L	H	$\overline{D1}$	D1
L	L	H	H or L	L	L	H	$\overline{D1_n}$	$D1_n$
L	H	L	↑	L	L	H	$\overline{D2}$	D2
L	H	L	H or L	L	L	H	$\overline{D2_n}$	$D2_n$
L	H	H	↑	L	L	H	$\overline{D3}$	D3
L	H	H	H or L	L	L	H	$\overline{D3_n}$	$D3_n$
H	L	L	↑	L	L	H	$\overline{D4}$	D4
H	L	L	H or L	L	L	H	$\overline{D4_n}$	$D4_n$
H	L	H	↑	L	L	H	$\overline{D5}$	D5
H	L	H	H or L	L	L	H	$\overline{D5_n}$	$D5_n$
H	H	L	↑	L	L	H	$\overline{D6}$	D6
H	H	L	H or L	L	L	H	$\overline{D6_n}$	$D6_n$
H	H	H	↑	L	L	H	$\overline{D7}$	D7
H	H	H	H or L	L	L	H	$\overline{D7_n}$	$D7_n$

H = High Voltage Level (Steady State); L = Low Voltage Level (Steady State); ↑ = Transition from Low to High Level; X = Don't Care; Z = High-Impedance State (Off State); $D0_n$...$D7_n$ = the level of steady-state inputs D0 through D7, respectively, before the most recent low-to-high transition of data control.

NOTE:

1. This column shows the input address setup with $\overline{LE}$ low.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	SN74 HC	CD74 HCT	UNIT
I_{CC}	MAX	46	0.08	0.16	mA
I_{OH}	MAX	-2.6	-6	-4	mA
I_{OL}	MAX	24	6	4	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

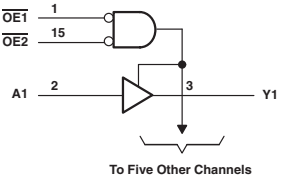
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	SN74 HC	CD74 HCT
t_{su}	D0 thru D7		MIN	15	19	11
t_h	D0 thru D7		MIN	0	5	14
t_{PLH}	CLK	Y	MAX	27	64	77
t_{PHL}				50	64	77
t_{PLH}	CLK	W (CD74 : $\overline{Y}$)	MAX	36	64	77
t_{PHL}				27	64	77
t_{PLH}	S0, S1, S2	Y	MAX	45	71	89
t_{PHL}				48	71	89
t_{PLH}	S0, S1, S2	W (CD74 : $\overline{Y}$)	MAX	54	71	89
t_{PHL}				45	71	89

UNIT: ns

365

HEX BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

Logic Diagram (SN74)



FUNCTION TABLE (SN74)
(each buffer/driver)

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
H	X	X	Z
X	H	X	Z
L	L	H	H
L	L	L	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	85	24	0.08	0.16	0.16	mA
I_{OH}	MAX	-5.2	-2.6	-6	-6	-4	mA
I_{OL}	MAX	32	24	6	6	4	mA

SWITCHING CHARACTERISTICS

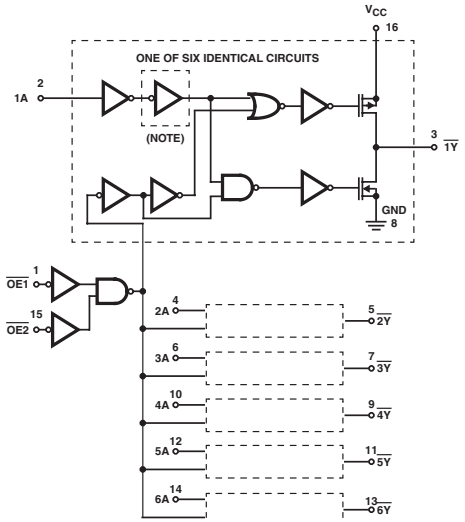
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT
t_{PLH}	A	Y	MAX	16	15	24	32	38
t_{PHL}			MAX	22	18	24	32	38
t_{PZH}	$\overline{G}$ (CD74: $\overline{OE}$)	Y	MAX	35	35	48	45	53
t_{PZL}			MAX	37	45	48	45	53
t_{PHZ}	$\overline{G}$ (CD74: $\overline{OE}$)	Y	MAX	11	32	48	45	53
t_{PLZ}			MAX	27	35	48	45	53

UNIT: ns

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

HEX BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

Logic Diagram
(CD74HC)



NOTE: Inverter not included in HC/HCT365.

FIGURE 1. LOGIC DIAGRAM FOR THE HC/HCT365 AND HC366 (OUTPUTS FOR HC/HCT365 ARE COMPLEMENTS OF THOSE SHOWN, i.e., 1Y, 2Y, ETC.)

FUNCTION TABLE (CD74)

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	H
L	L	H	L
X	H	X	Z
H	X	X	Z

NOTES:
H = High Voltage Level
L = Low Voltage Level
X = Don't Care
Z = High Ompedance (OFF) State

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	UNIT
I_{CC}	MAX	77	21	0.08	160	mA
I_{OH}	MAX	-5.2	-2.6	-6	-6	mA
I_{OL}	MAX	32	24	6	6	mA

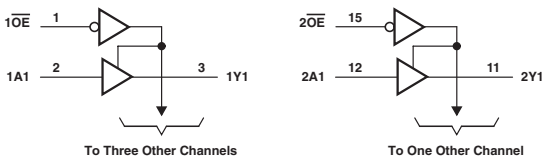
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC
t_{PLH}	A	Y (CD74 : $\overline{Y}$)	MAX	17	15	24	33
t_{PHL}			MAX	16	18	24	33
t_{PZH}	$\overline{G}$ (CD74 : $\overline{OE}$)	Y (CD74 : $\overline{Y}$)	MAX	35	35	48	45
t_{PZL}			MAX	37	45	48	45
t_{PHZ}	$\overline{G}$ (CD74 : $\overline{OE}$)	Y (CD74 : $\overline{Y}$)	MAX	11	32	48	45
t_{PLZ}			MAX	27	35	48	45

UNIT:ns

HEX BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

Logic Diagram (SN74)



FUNCTION TABLE (SN74)
(each buffer/driver)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	AHC	AHCT	LV 3V	LV 5V	UNIT
I_{CC}	MAX	85	24	0.08	0.16	0.16	0.04	0.04	-	0.02	mA
I_{OH}	MAX	-5.2	-2.6	-6	-6	-4	-8	-8	-8	-16	mA
I_{OL}	MAX	32	24	6	6	4	8	8	8	16	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	AHC	AHCT	LV 3V	LV 5V
t_{PLH}	A	Y	MAX	16	16	24	32	38	9	6.5	13.5	9
t_{PHL}			MAX	22	22	24	32	38	9	6.5	13.5	9
t_{PZH}	$\overline{OE}$	Y	MAX	35	35	48	45	53	10.5	9.5	16	10.5
t_{PZL}			MAX	47	40	48	45	53	10.5	8.5	16	10.5
t_{PHZ}	$\overline{OE}$	Y	MAX	11	30	48	45	53	10.5	9.5	15.5	10.5
t_{PLZ}			MAX	27	35	48	45	53	10.5	8.5	15.5	10.5

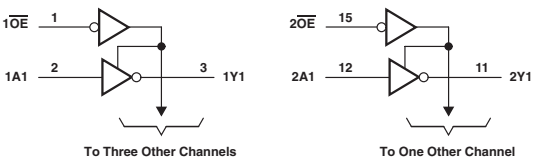
UNIT: ns

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

368

HEX INVERTING BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

Logic Diagram (SN74)



FUNCTION TABLE (SN74)
(each buffer/driver)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
H	X	Z
L	H	L
L	L	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	77	21	0.08	0.16	0.16	mA
I_{OH}	MAX	-5.2	-2.6	-6	-6	-4	mA
I_{OL}	MAX	32	24	6	6	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT
t_{PLH}	A	Y	MAX	17	15	24	32	45
t_{PHL}			MAX	16	18	24	32	45
t_{PZH}	$\overline{OE}$	Y	MAX	35	35	48	45	53
t_{PZL}			MAX	37	45	48	45	53
t_{PHZ}	$\overline{OE}$	Y	MAX	11	32	48	45	53
t_{PLZ}			MAX	27	35	48	45	53

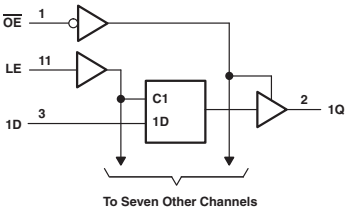
UNIT: ns

373

OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

- 3-State Bus-Driving True Outputs
- Buffered Control Inputs
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram (SN74)



FUNCTION TABLE (SN74)

OUTPUT CONTROL	INPUTS		OUTPUT Q
	LE	D	
L	H	H	H
L	H	L	L
L	L	X	Q0
H	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	LVTH 3V	UNIT
I_{CC}	MAX	40	190	27	100	55	0.08	0.16	0.08	0.16	60	30	5	mA
I_{OH}	MAX	-2.6	-6.5	-2.6	-15	-3	-6	-6	-6	-6	-15	-32	-32	mA
I_{OL}	MAX	24	20	24	48	24	6	6	6	6	64	64	64	mA

PARAMETER	MAX or MIN	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LV-AT	LVC 3V	ALVCH 3V	UNIT
I_{CC}	MAX	0.08	0.04	0.16	0.08	0.04	0.16	0.04	0.04	-	0.02	0.02	0.01	0.02	mA
I_{OH}	MAX	-24	-24	-24	-24	-24	-24	-8	-8	-8	-16	-16	-24	-24	mA
I_{OL}	MAX	24	24	24	24	24	24	8	8	8	16	16	24	24	mA

: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT
tw	High			MIN	15	6	10	4.5	6	20	24	25	24	7.5	3.3
	Low			MIN	15	7.3	-	-	-	-	-	-	-	-	-
tsu				MIN	5	0	10	2	2	13	15	13	20	2	1.9
th				MIN	20	10	7	3	3	12	5	10	15	5.5	1
tPLH		D	Q	MAX	18	12	12	6	8	38	45	44	48	9.3	5.9
tPHL				MAX	18	12	16	6	6	38	45	44	48	9.5	6.2
tPLH		LE	Q	MAX	30	14	22	11.5	13	44	53	44	53	9.3	6.6
tPHL				MAX	30	18	23	7.5	8	44	53	44	53	8.8	7.2
tPZH		$\overline{OE}$	Q	MAX	28	15	18	6.5	12	38	45	44	53	11.8	5.2
tPZL				MAX	36	18	20	9.5	8.5	38	45	44	53	12	6.7
tPHZ		$\overline{OE}$	Q	MAX	25	9	10	6.5	7.5	38	45	44	53	7	6.9
tPLZ				MAX	20	12	12	7	6	38	45	44	53	7.4	6.5

PARAMETER		INPUT	OUTPUT	MAX or MIN	LVTH 3V	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V
tw	High			MIN	3	4	4.5	4	5	8	4	5	6.5	5	5
	Low			MIN	-	-	-	4	-	-	4	-	-	-	-
tsu				MIN	1.1	3.5	4.5	2	3.5	8	2	4	1.5	4	4
th				MIN	1.4	2	1	3	3.5	1	3	1	3.5	1	1
tPLH		D	Q	MAX	3.9	10.3	10.5	8.5	11.8	11.5	10.4	10.5	10.5	17	10.5
tPHL				MAX	3.9	8.4	10.5	8.5	10	11.5	10.4	10.5	10.5	17	10.5
tPLH		LE	Q	MAX	4.2	11.3	10.5	12	13	11.5	12.5	10.5	14.5	16.5	10.5
tPHL				MAX	4.2	10.2	10.5	12	12.2	11.5	12.5	10.5	14.5	16.5	10.5
tPZH		$\overline{OE}$	Q	MAX	4.8	10.8	9.5	10.5	12.5	10.5	13.5	11.5	13.5	17	11.5
tPZL				MAX	4.8	9.7	9.5	10.5	12	10.5	13.5	11.5	13.5	17	11.5
tPHZ		$\overline{OE}$	Q	MAX	4.6	11.1	12.5	11.5	12.2	12.5	12.5	10.5	12	15	10.5
tPLZ				MAX	4.5	8.7	10	11.5	10.1	10	12.5	10.5	12	15	10.5

PARAMETER		INPUT	OUTPUT	MAX or MIN	LV-AT	LVC 3V	ALVCH 3V
tw	High			MIN	8.5	3.3	3.3
	Low			MIN	-	-	-
tsu				MIN	1.5	2	0.5
th				MIN	3.5	1.5	1.2
tPLH		D	Q	MAX	11	6.8	3.6
tPHL				MAX	11	6.8	3.6
tPLH		LE	Q	MAX	15	7.6	3.3
tPHL				MAX	15	7.6	3.3
tPZH		$\overline{OE}$	Q	MAX	14	7.7	4.8
tPZL				MAX	14	7.7	4.8
tPHZ		$\overline{OE}$	Q	MAX	12.5	7	4.4
tPLZ				MAX	12.5	7	4.4

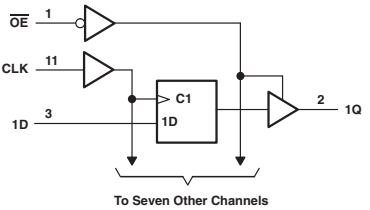
UNIT fmax : MHz, other : ns

374

OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

- Buffered Control Inputs
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram (SN74)



FUNCTION TABLE (SN74)

OUTPUT CONTROL	INPUTS		OUTPUT Q
	CLK	D	
L	↑	H	H
L	↑	L	L
L	L	X	Q0
H	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	LVTH 3V	UNIT
I_{CC}	MAX	40	160	31	128	86	0.08	0.16	0.08	0.16	60	30	5	mA
I_{OH}	MAX	-2.6	-6.5	-2.6	-15	-3	-6	-6	-6	-6	-15	-32	-32	mA
I_{OL}	MAX	24	20	24	48	24	6	6	6	6	64	64	64	mA

PARAMETER	MAX or MIN	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	ALVCH 3V	UNIT
I_{CC}	MAX	0.08	0.04	0.16	0.08	0.04	0.16	0.04	0.04	-	0.02	0.01	0.01	mA
I_{OH}	MAX	-24	-24	-24	-24	-24	-24	-8	-8	-8	-16	-24	-24	mA
I_{OL}	MAX	24	24	24	24	24	24	8	8	8	16	24	24	mA

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT
fmax				MIN	35	75	35	125	70	24	20	25	20	70	150
tw	High			MIN	15	6	14	4	7	20	24	20	24	7	3.3
	Low			MIN	15	7.3	14	3	6	20	24	20	24	-	3.3
tsu				MIN	20	5	10	2	2	25	18	25	18	6.5	1.9
th				MIN	0	2	0	2	2	5	5	10	5	0	2.1
t_{PLH}		CLK (CD74: CP)	Q	MAX	28	15	12	8	10	45	50	45	50	10.6	6.2
t_{PHL}				MAX	28	17	16	9	10	45	50	45	50	10	7.1
t_{PZH}		$\overline{OE}$	Q	MAX	26	15	17	6	12.5	38	45	38	45	12.3	5.2
t_{PZL}				MAX	28	18	18	10	8.5	38	45	38	45	12.7	6.7
t_{PHZ}		$\overline{OE}$	Q	MAX	28	9	10	6	8	38	41	38	42	6.8	6.7
t_{PLZ}				MAX	20	12	18	6	6.5	38	41	38	42	6.8	6.5

PARAMETER		INPUT	OUTPUT	MAX or MIN	LVTH 3V	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V
fmax				MIN	150	95	100	12.5	55	90	110	75	75	50	75
tw	High			MIN	3.3	5	4.5	4	9	5	4.5	5	6.5	5.5	5
	Low			MIN	3.3	5	4.5	4	9	5	4.5	5	6.5	5.5	5
tsu				MIN	1.5	2.5	4.5	2	3	5.5	2	3	2.5	4.5	3
th				MIN	0.8	3.5	1.5	2	5.5	1.5	3	2	2.5	2	2
t_{PLH}		CLK (CD74: CP)	Q	MAX	4.5	10.2	10.5	10.8	12.4	11.5	11.2	11.5	11.5	18.5	11.5
t_{PHL}				MAX	4.2	10.1	10	10.8	13	11	11.2	11.5	11.5	18.5	11.5
t_{PZH}		$\overline{OE}$	Q	MAX	4.7	9.1	9.5	14.5	12.3	10.5	14.5	11	12.5	16.5	11
t_{PZL}				MAX	4.7	9.4	9.5	14.5	12.3	10.5	14.5	11	12.5	16.5	11
t_{PHZ}		$\overline{OE}$	Q	MAX	4.6	11.2	12.5	14.5	13.2	12.5	14.5	10	12	16	10
t_{PLZ}				MAX	4.5	9.2	10	14.5	10.8	10	14.5	10	12	16	10

PARAMETER		INPUT	OUTPUT	MAX or MIN	LVC 3V	ALVCH 3V
fmax				MIN	100	150
tw	High			MIN	3.3	3.3
	Low			MIN	3.3	3.3
tsu				MIN	2	1.8
th				MIN	1.5	0.5
t_{PLH}		CLK	Q	MAX	7	3.6
t_{PHL}				MAX	7	3.6
t_{PZH}		$\overline{OE}$	Q	MAX	7.5	5.2
t_{PZL}				MAX	7.5	5.2
t_{PHZ}		$\overline{OE}$	Q	MAX	6.5	4.5
t_{PLZ}				MAX	6.5	4.5

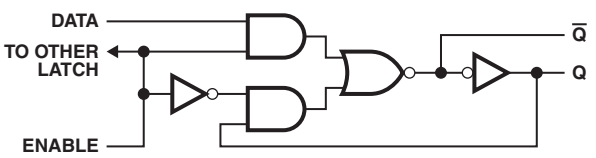
UNIT fmax : MHz, other : ns

375

4-BIT BISTABLE LATCHES

● Complementary Outputs (Q, $\overline{Q}$)

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUTS
D	C	Q
L	H	L H
H	H	H L
X	L	Q_0 $\overline{Q}_0$

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	SN74 HC	UNIT
I_{CC}	MAX	12	0.04	mA
I_{OH}	MAX	-0.4	-4	mA
I_{OL}	MAX	8	4	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	SN74 HC
tw			MIN	20	20
tsu			MIN	20	25
th			MIN	0	5
t_{PLH}	D	Q	MAX	27	30
t_{PHL}			MAX	17	30
t_{PLH}	D	$\overline{Q}$	MAX	20	30
t_{PHL}			MAX	15	30
t_{PLH}	C	Q	MAX	27	33
t_{PHL}			MAX	25	33
t_{PLH}	C	$\overline{Q}$	MAX	30	33
t_{PHL}			MAX	15	33

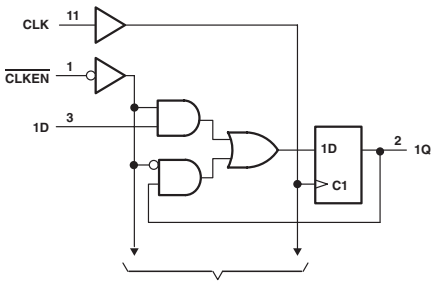
UNIT: ns

: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

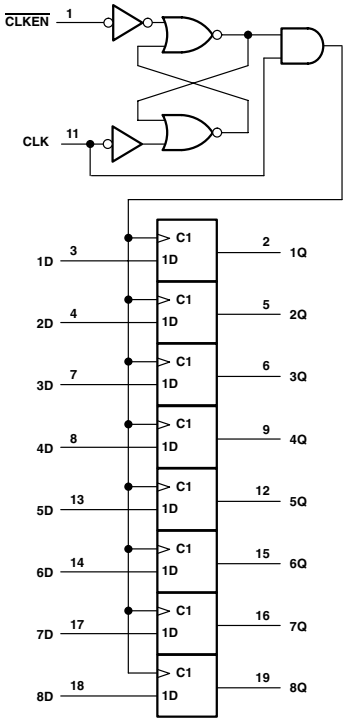
OCTAL D-TYPE FLIP-FLOPS WITH CLOCK ENABLE

- Individual Data Input to Each Flip-Flop
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram (SN74ABT)



Logic Diagram (SN74HC)



FUNCTION TABLE (SN74)

INPUTS			OUTPUTS	
$\overline{CLKEN}$	CLOCK	DATA	Q	$\overline{Q}$
H	X	X	Q_0	$\overline{Q}_0$
L	↑	H	H	L
L	↑	L	L	H
X	L	X	Q_0	$\overline{Q}_0$

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	ABT	AC 11	UNIT
I_{CC}	MAX	28	90	0.08	0.16	0.08	0.16	30	0.08	mA
I_{OH}	MAX	-0.4	-1	-4	-4	-4	-4	-32	-24	mA
I_{OL}	MAX	8	20	4	4	4	4	64	24	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

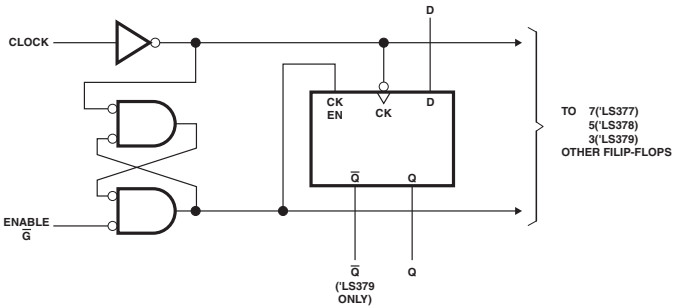
PARAMETER		INPUT	OUTPUT	MAX or MIN	LS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	ABT	AC 11
fmax				MIN	30	110	20	20	17	16	150	100
tw				MIN	20	5	25	24	25	30	3.3	5
tsu	DATA			MIN	20	2	25	18	15	18	2.5	4
	*$\overline{CLKEN}$ ACTIVE			MIN	25	2.5	25	-	15	-	3	6
	*$\overline{CLKEN}$ INACTIVE			MIN	10	4.5	25	18	15	18	3	6
th				MIN	5	1	5	5	5	5	1.8	0
t_{PLH}		CLK (CD74: CP)	Q	MAX	27	10	40	53	45	57	6.5	11.3
t_{PHL}				MAX	27	10.5	40	53	45	57	7.3	12.9

UNIT fmax : MHz, other : ns
*CD74: $\overline{E}$

378

HEX D-TYPE FLIP-FLOPS WITH CLOCK ENABLE

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{G}$	CLOCK	DATA	Q	$\overline{Q}$
H	X	X	Q_0	$\overline{Q}_0$
L	↑	H	H	L
L	↑	L	L	H
X	L	X	Q_0	$\overline{Q}_0$

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	F	SN74 HC	UNIT
I_{CC}	MAX	22	45	0.08	mA
I_{OH}	MAX	-0.4	-1	-4	mA
I_{OL}	MAX	8	20	4	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	LS	F	SN74 HC
fmax				MIN	30	110	20
tw	CLK H			MIN	20	4	25
	CLK L			MIN	20	6	25
tsu	DATA			MIN	20	5	25
	$\overline{G}$ ACTIVE			MIN	25	3.5	25
	$\overline{G}$ INACTIVE			MIN	10	5	25
th				MIN	5 ↑	0	5
t_{PLH}		CLK	Q	MAX	27	6.7	40
t_{PHL}				MAX	27	6.1	40

UNIT fmax : MHz, other : ns

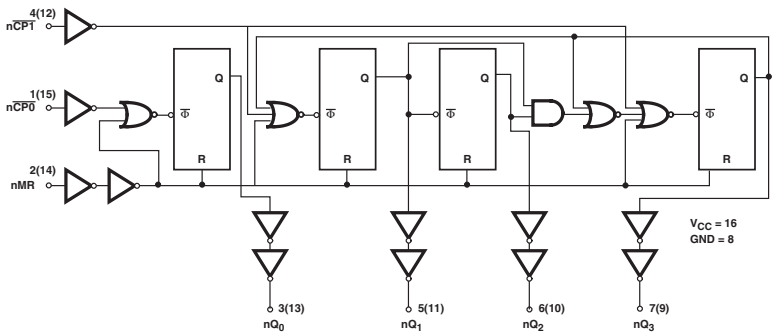
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

390

DUAL 4-BIT DECADE COUNTERS

- Individual Clock for A and B Flip-Flops Provide Dual ÷ 2 and ÷ 5 Counters
- All Have Direct Clear for Each 4-Bit Counter
- Typical maximum Count Frequency: 35MHz
- Buffered Outputs Reduce Possibility of Collector Commutation

Logic Diagram (CD74)



FUNCTION TABLE (CD74)

BCD COUNT SEQUENCE FOR 1/2

COUNT	OUTPUTS			
	Q_3	Q_2	Q_1	Q_0
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BI-QUINARY COUNT SEQUENCE FOR 1/2

COUNT	OUTPUTS			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	69	26	0.08	0.16	0.16	mA
I_{OH}	MAX	-0.8	-0.4	-4	-4	-4	mA
I_{OL}	MAX	16	8	4	4	4	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT
fmax		nCKA (CD74: $n\overline{CP}_0$)	nQA (CD74: nQP_0)	MIN	25	25	25	20	18
		nCKB (CD74: $n\overline{CP}_1$)	nQB (CD74: nQP_1)	MIN	20	12.5	25	20	18
tw	nCKA (CD74: $n\overline{CP}_0$)			MIN	20	20	20	24	29
	nCKB (CD74: $n\overline{CP}_1$)			MIN	25	40	20	24	29
	*CLR H			MIN	20	20	20	15	20
tsu				MIN	25	25	5	-	-
t_{PLH}		nCKA (CD74: $n\overline{CP}_0$)	nQA (CD74: nQ_0)	MAX	20	20	30	53	60
t_{PHL}				MAX	20	20	30	53	60
t_{PLH}		nCKA (CD74: $n\overline{CP}_0$)	nQC (CD74: nQ_2)	MAX	60	60	72	-	126
t_{PHL}				MAX	60	60	72	-	126
t_{PLH}		nCKB (CD74: $n\overline{CP}_1$)	nQB (CD74: nQ_1)	MAX	21	21	33	56	65
t_{PHL}				MAX	21	21	33	56	65
t_{PLH}		nCKB (CD74: $n\overline{CP}_1$)	nQC (CD74: nQ_2)	MAX	39	39	46	74	83
t_{PHL}				MAX	39	39	46	74	83
t_{PLH}		nCKB (CD74: $n\overline{CP}_1$)	nQD (CD74: nQ_3)	MAX	21	21	33	54	63
t_{PHL}				MAX	21	21	33	54	63
t_{PHL}		*CLR	Q	MAX	39	39	41	57	63

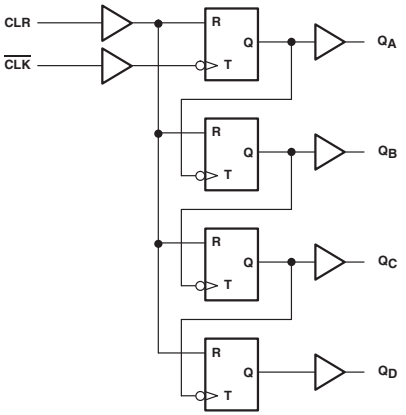
UNIT fmax : MHz, other : ns
*CD74: MR

393

DUAL 4-BIT BINARY COUNTERS

- Dual 4-Bit Binary Counter with Individual Clock
- All Have Direct Clear for Each 4-Bit Counter
- Typical maximum Count Frequency: 35MHz
- Buffered Outputs Reduce Possibility of Collector Commutation

Logic Diagram (SN74)



FUNCTION TABLE (SN74)

COUNT	INPUTS			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	LV 3V	LV 5V	UNIT
I_{CC}	MAX	64	26	0.08	0.16	0.16	-	0.02	mA
I_{OH}	MAX	-0.8	-0.4	-4	-4	-4	-6	-12	mA
I_{OL}	MAX	16	8	4	4	4	6	12	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	LV 3V	LV 5V
fmax				MIN	25	25	25	20	18	35	75
tw	CLK	A		MIN	20	20	20	24	29	5	5
		B		MIN	25	40	20	24	29	5	5
	CLR H			MIN	20	20	20	24	24	5	5
tsu				MIN	25	25	5	-	-	5	4
t_{PLH}		CLKA (CD74:nCP)	QA	MAX	20	20	30	59	48	19	12
t_{PHL}				MAX	20	20	30	59	48	19	12
t_{PLH}		CLKB (CD74:nCP)	QD	MAX	60	60	72	86	93	26.5	16.5
t_{PHL}				MAX	60	60	72	86	93	26.5	16.5
t_{PHL}		CLR	Q	MAX	39	39	41	41	48	18	11.5

UNIT fmax : MHz, other : ns

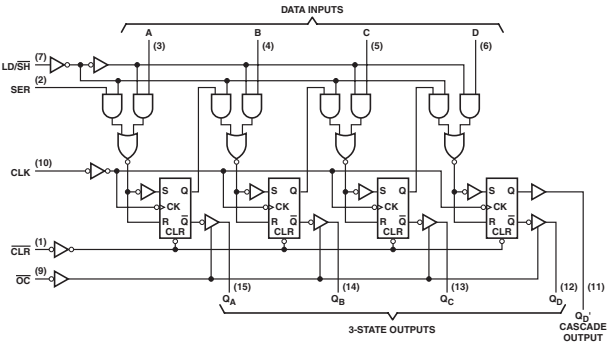
: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

395

CASCADABLE SHIFT REGISTERS

- 3-State Outputs
- Parallel-In, Parallel-Out Registers
- Low Power Dissipation: 75mW Typical (Enable)

Logic Diagram



FUNCTION TABLE

INPUTS								3-STATE OUTPUTS				CASCADE
CLEAR	LOAD/SHIFT CONTROL	CLOCK	SERIAL	PARALLEL				Q_A	Q_B	Q_C	Q_D	OUTPUT QD
				A	B	C	D					
L	X	X	X	X	X	X	X	L	L	L	L	L
H	H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{D0}
H	H	↓	X	a	b	c	d	a	b	c	d	d
H	L	H	X	X	X	X	X	Q_{A0}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{DO}
H	L	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Cn}
H	L	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Cn}

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	UNIT
I_{CC}		MAX	34	mA
I_{OH}	QA, QB, QC, QD	MAX	-2.6	mA
	QD'	MAX	-0.4	mA
I_{OL}	QA, QB, QC, QD	MAX	24	mA
	QD'	MAX	8	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	LS
fmax				MIN	30
tw				MIN	16
tsu	LD/SH			MIN	40
	OTHER			MIN	20
th				MIN	10
t_{PLH}		CLK	Q	MAX	30
t_{PHL}				MAX	30

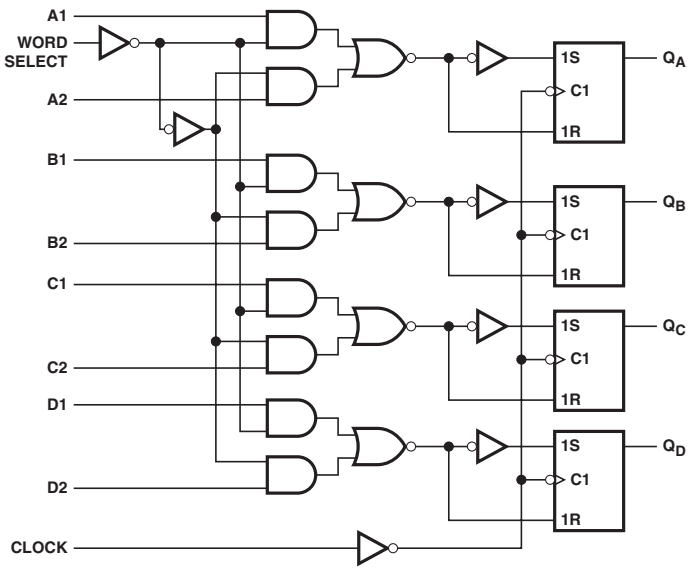
UNIT fmax : MHz, other : ns

399

QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE

- Single-Rail Outputs (Q, $\overline{Q}$)
- Select One of Two 4-Bit Data Sources and Stores Data Synchronously with System Clock

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUTS			
WORD SELECT	CLOCK	Q_A	Q_B	Q_C	Q_D
L	↑	A1	B1	C1	D1
H	↑	A2	B2	C2	D2
X	L	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	UNIT
I_{CC}	MAX	13	mA
I_{OH}	MAX	-0.4	mA
I_{OL}	MAX	8	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	LS
tw				MIN	20
tsu	DATA			MIN	25
	WORD SELECT			MIN	45
th	DATA			MIN	0
	WORD SELECT			MIN	0
t_{PLH}		CLK	Q	MAX	27
t_{PHL}				MAX	32

UNIT: ns

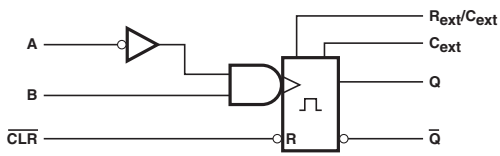
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

423

RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

- Will Not Trigger from Clear

Logic Diagram (SN74LS)



FUNCTION TABLE (SN74LS)

INPUTS			OUTPUTS	
$\overline{CLR}$	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎍
H	↓	H	⎍	⎍

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	20	0.16	0.16	mA
I_{OH}	MAX	-0.4	-4	-4	mA
I_{OL}	MAX	8	4	4	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

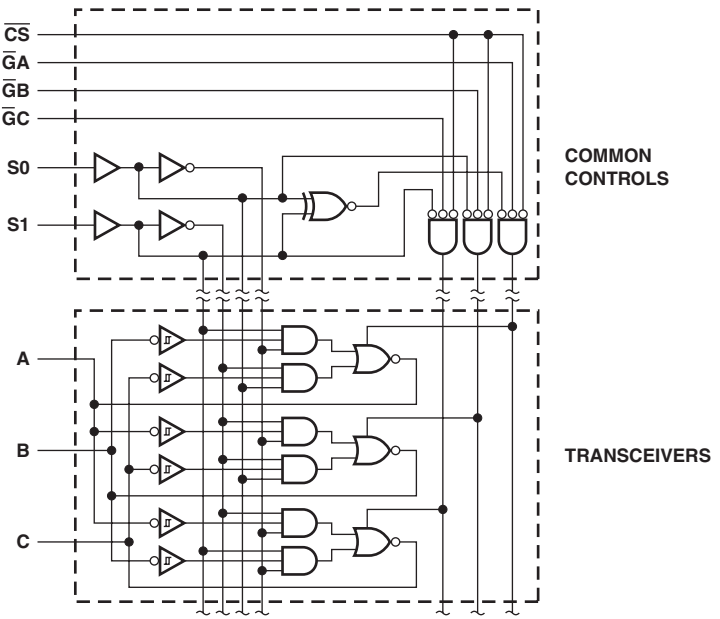
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	CD74 HC	CD74 HCT
t_W			MIN	40	30	30
t_{PLH}	A (CD74: $\overline{A}$)	Q	MAX	33	90	90
	B			44	90	90
t_{PHL}	A (CD74: $\overline{A}$)	$\overline{Q}$	MAX	45	96	102
	B			56	96	102
t_{PLH}	$\overline{CLR}$ (CD74: $\overline{R}$)	Q	MAX	27	65	72
t_{PHL}		$\overline{Q}$	MAX	45	65	72

UNIT: ns

442

QUADRUPLE TRIDIRECTIONAL BUS TRANSCEIVERS

Logic Diagram



FUNCTION TABLE

INPUTS						TRANSFERS BUSES
$\overline{CS}$	S1	S0	$\overline{GA}$	$\overline{GB}$	$\overline{GC}$	
H	X	X	X	X	X	None
X	H	H	X	X	X	None
X	X	X	H	H	H	None
X	L	L	X	H	H	None
X	L	H	H	X	H	None
X	H	L	H	H	X	None
L	L	L	X	L	L	A → B, A → C
L	L	H	L	X	L	B → C, B → A
L	H	L	L	L	X	C → A, C → B
L	L	L	X	L	H	A → B
L	L	H	H	X	L	B → C
L	H	L	L	H	X	C → A
L	L	L	X	H	L	A → C
L	L	H	L	X	H	B → A
L	H	L	H	L	X	C → B

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	UNIT
I_{CC}	MAX	95	mA
I_{OH}	MAX	-15	mA
I_{OL}	MAX	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
t_{PLH}	A	B or C	MAX	14
	B	A or C		
	C	A or B		
t_{PHL}	A	B or C	MAX	20
	B	A or C		
	C	A or B		
t_{PZL}	Any $\overline{G}$	A, B, C	MAX	33
	S0, S1			42
	$\overline{CS}$			36
t_{PZH}	$\overline{G}$, S, $\overline{CS}$	A, B, C	MAX	32
t_{PLZ}	$\overline{G}$, S, $\overline{CS}$	A, B, C	MAX	35
t_{PHZ}	$\overline{G}$, S, $\overline{CS}$	A, B, C	MAX	25

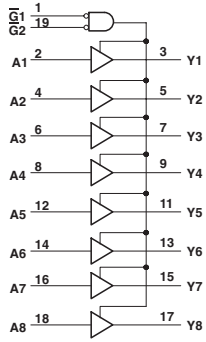
UNIT:ns

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

465

OCTAL BUFFERS WITH 3-STATE OUTPUTS

Logic Diagram



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	UNIT
I_{CC}	MAX	37	33	mA
I_{OH}	MAX	-2.6	-15	mA
I_{OL}	MAX	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS
t_{PLH}	A	Y	MAX	15	13
t_{PHL}				18	12
t_{PZH}	$\overline{G}$	Y	MAX	40	23
t_{PZL}				45	25
t_{PHZ}	$\overline{G}$		MAX	40	10
t_{PLZ}				45	18

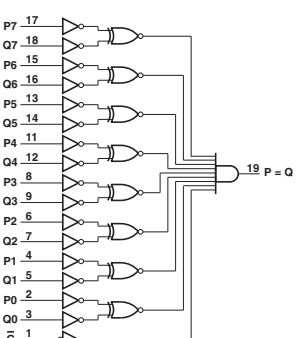
UNIT:ns

518

OCTAL BINARY/BCD IDENTITY COMPARATORS WITH ENABLE

- Open-Collector Outputs
- 20-kΩ Pullup Resistors on Q Inputs

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUT
DATA P, Q	ENABLE G	P = Q
P = Q	L	H
P > Q	L	L
P < Q	L	L
X	H	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	UNIT
I_{CC}	MAX	17	mA
I_{OL}	MAX	24	mA
V_{OH}	MAX	5.5	V

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
t_{PLH}	P or Q	P = Q	MAX	33
t_{PHL}				15
t_{PLH}	$\overline{G}$	P = Q	MAX	33
t_{PHL}				15

UNIT: ns

520

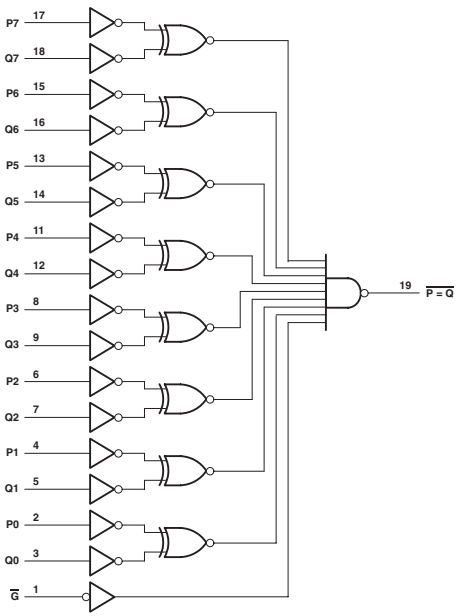
OCTAL BINARY/BCD IDENTITY COMPARATORS WITH ENABLE

- 20-kΩ Pullup Resistors on Q Inputs
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

FUNCTION TABLE

INPUTS		OUTPUT
DATA P, Q	ENABLE $\overline{G}$	$\overline{P = Q}$
P = Q	L	L
P > Q	L	H
P < Q	L	H
X	H	H

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	F	AC 11	UNIT
I_{CC}	MAX	19	32	8	mA
I_{OH}	MAX	-2.6	-1	-24	mA
I_{OL}	MAX	24	20	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	F	AC 11
t_{PLH}	P or Q	$\overline{P = Q}$	MAX	12	8.7	12.6
t_{PHL}				20	10.3	11.3
t_{PLH}	$\overline{OE}$	$\overline{P = Q}$	MAX	12	6.4	7.4
t_{PHL}				22	10.4	7.8

UNIT: ns

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

521

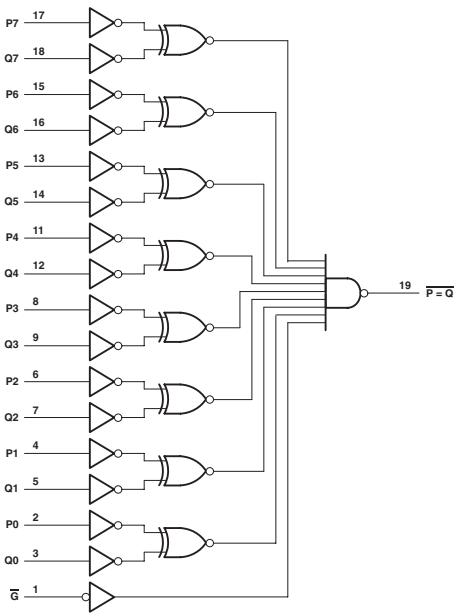
8-BIT IDENTITY COMPARATORS WITH OPEN-COLLECTOR OUTPUTS

● 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

FUNCTION TABLE

INPUTS		OUTPUT
DATA P, Q	ENABLE $\overline{G}$	$\overline{P = Q}$
P = Q	L	L
P > Q	L	H
P < Q	L	H
X	H	H

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	F	AC 11	UNIT
I_{CC}	MAX	19	32	0.08	mA
I_{OH}	MAX	-2.6	-1	-24	mA
I_{OL}	MAX	24	20	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	F	AC 11
t_{PLH}	P or Q	$\overline{P = Q}$	MAX	12	11	13
t_{PHL}				20	11	11.4
t_{PLH}	$\overline{G}$	$\overline{P = Q}$	MAX	12	7.5	7.9
t_{PHL}				22	10	8.1

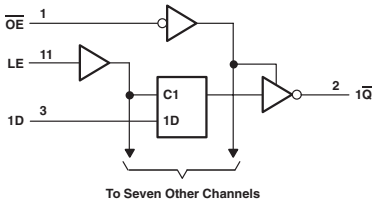
UNIT: ns

533

OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

- 3-State Bus-Driving Inverting Outputs
- Functionally Equivalent to '373, Except for Having Inverted Outputs
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram (SN74)



FUNCTION TABLE (SN74)

INPUTS			OUTPUT
ENABLE $\overline{OE}$	LE	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	ABT	AC 11	SN74 AC	ACT 11	SN74 ACT	UNIT
I_{CC}	MAX	28	110	0.08	0.16	0.08	0.16	30	0.08	0.04	0.08	0.04	mA
I_{OH}	MAX	-2.6	-15	-6	-6	-6	-6	-32	-24	-24	-24	-24	mA
I_{OL}	MAX	24	48	6	6	6	6	64	24	24	24	24	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	ABT	AC 11	SN74 AC	ACT 11	SN74 ACT
t_W			MIN	15	2	20	24	25	24	3.3	4	5	5	6
t_{SU}			MIN	15	2	13	15	13	15	2.1	3.5	4.5	3.5	4
t_H			MIN	7	3	5	11	5	12	2.1	2	1	3.5	2.5
t_{PLH}	D	$\overline{Q}$	MAX	19	7.5	38	50	44	51	6.4	9.8	11	11.3	11.5
t_{PHL}				13	7	38	50	44	51	6.6	8	10.5	9.5	11
t_{PLH}	LE (CD74: $\overline{LE}$)	$\overline{Q}$	MAX	23	9	44	53	44	57	7.3	11.3	11.5	13	11.5
t_{PHL}				18	8	44	53	44	57	7.3	10.3	11	12.2	11.5
t_{PZH}	$\overline{OE}$	$\overline{Q}$	MAX	17	6.5	38	45	44	53	5.7	10.8	10.5	12.5	11
t_{PZL}				18	9.5	38	45	44	53	6.7	9.7	10.5	12	11
t_{PHZ}	$\overline{OE}$	$\overline{Q}$	MAX	10	6.5	38	45	44	45	6.9	11.4	11	12.8	11
t_{PLZ}				16	7	38	45	44	45	6.5	8.9	11	10.3	11

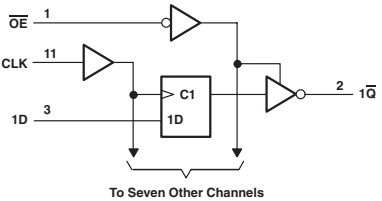
UNIT: ns

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

- 3-State Bus-Driving Inverting Outputs
- '534 Have Inverted Outputs, But Otherwise Are Functionally Equivalent to '374
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram (SN74)



FUNCTION TABLE (SN74)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	H or L	X	$\overline{Q}_0$
H	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	ABT	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	UNIT
I_{CC}	MAX	31	128	0.08	0.16	0.08	0.16	30	0.08	0.04	0.16	0.08	0.04	mA
I_{OH}	MAX	-2.6	-15	-6	-6	-6	-6	-32	-24	-24	-24	-24	-24	mA
I_{OL}	MAX	24	48	6	6	6	6	64	24	24	24	24	24	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	ALS	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	ABT	AC 11	SN74 AC	CD74 AC
fmax				MIN	35	125	25	20	25	16	125	75	140	125
tw	CLK "H"			MIN	14	4	20	24	20	30	3.5	6.5	4	4
	CLK "L"				14	3	20	24	20	30	3.5	6.5	4	4
tsu				MIN	10	2	25	18	25	30	1.6	3.5	4	2
th					0	2	5	5	5	5	2	4.5	1.5	2
tPLH		CLK (CD74: $\overline{CP}$)	$\overline{Q}$	MAX	12	8	45	50	45	53	6.7	11.7	12	11.3
tPHL					16	9	45	50	45	53	7.6	12.1	11	11.3
tPZH		$\overline{OE}$	$\overline{Q}$	MAX	17	6	38	45	37	53	5	10.4	11.5	14.5
tPZL					18	10	38	45	37	53	6.8	10.4	11.5	14.5
tPHZ		$\overline{OE}$	$\overline{Q}$	MAX	10	6	38	45	37	45	7.3	11.6	12.5	14.5
tPLZ					14	6	38	45	37	45	6.5	9.2	11	14.5

PARAMETER		INPUT	OUTPUT	MAX or MIN	ACT 11	SN74 ACT
fmax				MIN	55	120
tw	CLK "H"			MIN	9	3.5
	CLK "L"				9	3.5
tsu				MIN	3	4
th					5.5	1.5
tPLH		CLK (CD74: $\overline{CP}$)	$\overline{Q}$	MAX	14.5	12.5
tPHL					15	12
tPZH		$\overline{OE}$	$\overline{Q}$	MAX	13.3	12.5
tPZL					13.5	11.5
tPHZ		$\overline{OE}$	$\overline{Q}$	MAX	13.5	13.5
tPLZ					12	10.5

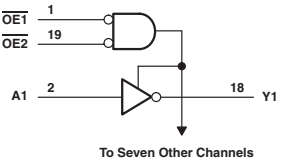
UNIT fmax : MHz, other : ns

540

OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce D-C Loading
- Schmitt-Triggered Inputs (SN74LS540)

Logic Diagram (SN74)



FUNCTION TABLE (SN74)
(each buffer/driver)

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	ALS-1	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	LVTH 3V	CD74 AC	CD74 ACT	AHC	UNIT
I_{CC}	MAX	52	22	22	0.08	0.16	0.08	0.16	71	30	5	0.16	0.16	0.04	mA
I_{OH}	MAX	-15	-15	-15	-6	-6	-6	-6	-15	-32	-32	-24	-24	-8	mA
I_{OL}	MAX	24	24	48	6	6	6	6	64	64	64	24	24	8	mA

PARAMETER	MAX or MIN	AHCT	LV 3V	LV 5V	LVC 3V	UNIT
I_{CC}	MAX	0.04	-	0.02	0.01	mA
I_{OH}	MAX	-8	-8	-16	-24	mA
I_{OL}	MAX	8	8	16	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	ALS-1	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT
t_{PLH}	A	Y (CD74: $\overline{Y}$)	MAX	15	12	12	25	33	25	36	6.9	4.8
t_{PHL}				15	9	9	25	33	25	36	4	4.8
t_{PZH}	$\overline{OE}$	Y (CD74: $\overline{Y}$)	MAX	25	15	15	38	-	38	-	10.1	5.9
t_{PZL}				38	20	20	38	-	38	-	11.3	6.4
t_{PHZ}	$\overline{OE}$	Y (CD74: $\overline{Y}$)	MAX	25	10	10	38	48	38	53	9	7.3
t_{PLZ}				18	12	12	38	48	38	53	8.5	6.2

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTH 3V	CD74 AC	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V
t_{PLH}	A	Y (CD74: $\overline{Y}$)	MAX	3.8	68	7.2	8	10	12	8	5.3
t_{PHL}				3.8	68	7.2	8	10	12	8	5.3
t_{PZH}	$\overline{OE}$	Y (CD74: $\overline{Y}$)	MAX	5.2	12	13.4	10.5	12	16	10.5	6.6
t_{PZL}				5.3	12	13.4	10.5	12	16	10.5	6.6
t_{PHZ}	$\overline{OE}$	Y (CD74: $\overline{Y}$)	MAX	5.6	12	13.4	10	12	17.5	10	7.4
t_{PLZ}				5	12	13.4	10	12	17.5	10	7.4

UNIT: ns

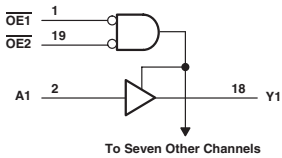
: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

541

OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce D-C Loading
- Schmitt-Triggered Inputs (SN74LS541)

Logic Diagram (SN74)



FUNCTION TABLE (SN74)
(each buffer/driver)

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	ALS-1	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	LVTH 3V	CD74 AC	UNIT
I_{CC}	MAX	55	25	25	75	0.08	0.16	0.08	0.16	72	30	5	0.16	mA
I_{OH}	MAX	-15	-15	-15	-15	-6	-6	-6	-6	-15	-32	-32	-24	mA
I_{OL}	MAX	24	24	48	64	6	6	6	6	64	64	64	24	mA

PARAMETER	MAX or MIN	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LV-AT	LVC 3V	UNIT
I_{CC}	MAX	0.16	0.04	0.04	-	0.02	0.02	0.01	mA
I_{OH}	MAX	-24	-8	-8	-8	-16	-16	-24	mA
I_{OL}	MAX	24	8	8	8	16	16	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	ALS-1	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT
t_{PLH}	A	Y	MAX	15	14	14	6	29	35	29	42	6
t_{PHL}				18	10	10	6	29	35	29	42	8.2
t_{PZH}	$\overline{OE}$	Y	MAX	32	15	15	9.5	38	-	38	-	10.7
t_{PZL}				38	20	20	9.5	38	-	38	-	11.5
t_{PHZ}	$\overline{OE}$	Y	MAX	29	10	10	6.5	38	48	38	53	8.6
t_{PLZ}				18	12	12	6	38	48	38	53	8.6

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVTH 3V	CD74 AC	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LV-AT	LVC 3V
t_{PLH}	A	Y	MAX	3.6	3.5	7.8	8.2	8	9.5	12	8	9	5.1
t_{PHL}				3.9	3.5	7.8	8.2	8	9.5	12	8	9	5.1
t_{PZH}	$\overline{OE}$	Y	MAX	4	5.2	12	13.4	10.5	12	16	10.5	14	7
t_{PZL}				5.9	5.3	12	13.4	10.5	12	16	10.5	14	7
t_{PHZ}	$\overline{OE}$	Y	MAX	5.8	5.6	12	13.4	10	12	17.5	10	13.5	7
t_{PLZ}				4.4	5	12	13.4	10	12	17.5	10	13.5	7

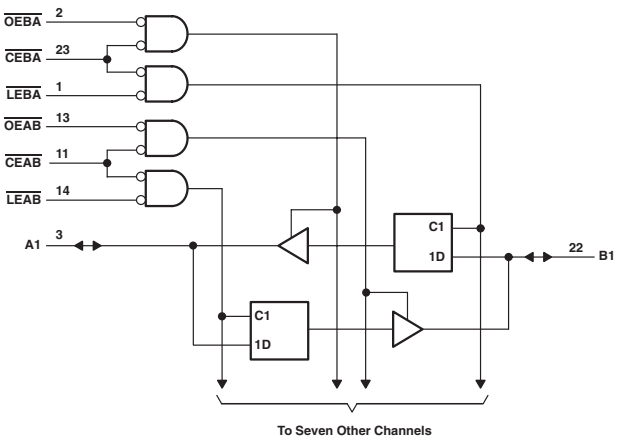
UNIT: ns

543

OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

- Back-to-Back Registers for Storage
- 3-State True Outputs
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE†

INPUTS				OUTPUT
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A	B
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B_0‡
L	L	L	L	L
L	L	L	H	H

† A-to-B data flow is shown; B-to-A flow control is the same except that it uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.
‡ Output level before the indicated steady-state input conditions were established

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	F	SN74 BCT	ABT	LVT 3V	LVTH 3V	ACT 11	LVC 3V	UNIT
I_{CCH}		MAX	100	8	0.25	0.19	0.19	0.08	0.01	mA
I_{CCL}		MAX	125	71	30	12	5	0.08	0.01	mA
I_{CCZ}		MAX	125	15	0.25	0.19	0.19	0.08	0.01	mA
I_{OH}	A	MAX	-3	-15	-32	-32	-32	-24	-24	mA
	B	MAX	-15	-15	-32	-32	-32	-24	-24	mA
I_{OL}	A	MAX	24	64	64	64	64	24	24	mA
	B	MAX	64	64	64	64	64	24	24	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER			INPUT	OUTPUT	MAX or MIN	F	SN74 BCT	ABT	LVT 3V	LVTH 3V	ACT 11	LVC 3V
t_w					MIN	5	7	3.5	3.3	3.3	4	3.3
t_{su}	$\overline{LE}$ ↑ before	"H"			MIN	3.5	4.5	3.5	0	0.4	2.5	1.6
	$\overline{LE}$ ↑ before	"L"				3.5	4.5	3	0.8	1	2.5	1.6
	$\overline{CE}$ ↑ before	"H"				-	-	3.5	0	0.2	3	1.6
	$\overline{CE}$ ↑ before	"L"				-	-	3	0.9	0.7	3	1.6
t_h	$\overline{LE}$ ↑ after	"H"			MIN	3.5	1.5	0.5	1.7	1.5	2	2.1
	$\overline{LE}$ ↑ after	"L"				3.5	1.5	0.5	1.7	1.3	2	2.1
	$\overline{CE}$ ↑ after	"H"				-	-	0.5	1.8	1.6	1.5	2.1
	$\overline{CE}$ ↑ after	"L"				-	-	0.5	1.8	1.4	1.5	2.1
t_{PLH}			A or B	B or A	MAX	8.5	8.8	6.9	4.7	3.7	10.2	7
t_{PHL}						7.5	9.6	6.9	4.6	3.7	12.1	7
t_{PLH}			$\overline{LEBA}$	A	MAX	12.5	12.9	6.6	5.9	4.7	11.2	8.5
t_{PHL}						12.5	12.7	7.1	5.7	4.7	13.2	8.5
t_{PLH}			$\overline{LEAB}$	B	MAX	12.5	12.9	6.6	5.9	4.7	11.2	8.5
t_{PHL}						12.5	12.7	7.1	5.7	4.7	13.2	8.5
t_{PZH}			$\overline{OE}$	A or B	MAX	10	10.7	6.4	5.8	4.9	11.5	7.7
t_{PZL}						12	12.3	7.5	6.4	4.9	15.3	7.7
t_{PHZ}			$\overline{OE}$	A or B	MAX	9	8.1	8.4	6.5	5.3	10.4	7
t_{PLZ}						8.5	7.2	8	5.8	5.3	10.5	7
t_{PZH}			$\overline{CE}$	A or B	MAX	10	12	6.4	6	5.3	12.2	8
t_{PZL}						12	13.5	7.5	6.7	5.3	16	8
t_{PHZ}			$\overline{CE}$	A or B	MAX	9	8.5	8.4	6.4	5.4	11	7
t_{PLZ}						8.5	7.6	8	5.4	5.4	11.1	7

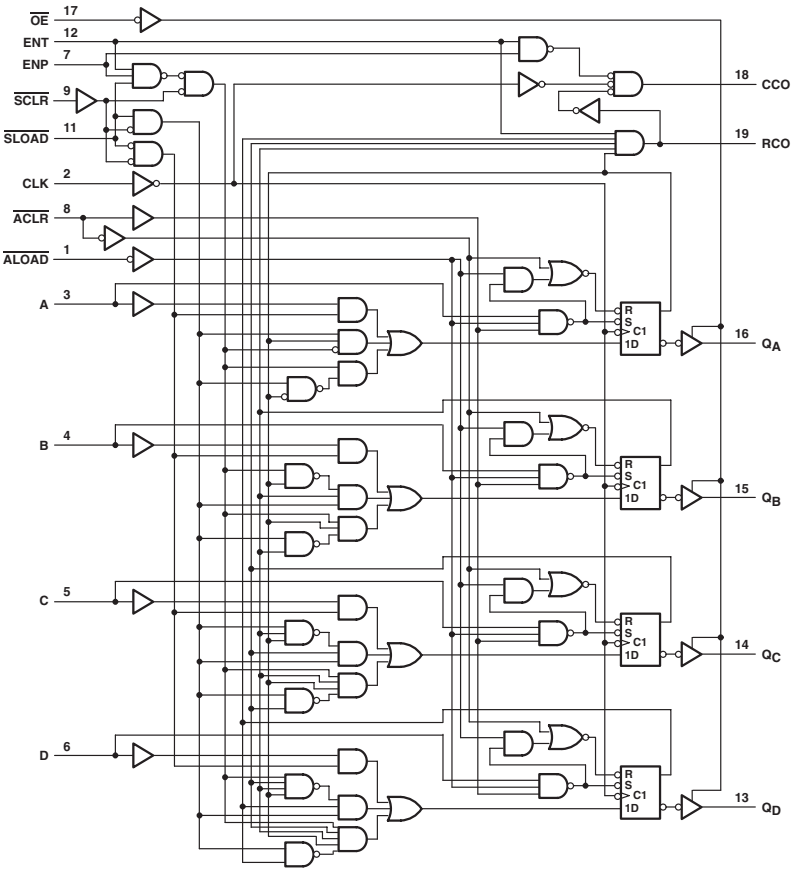
UNIT: ns

561

SYNCHRONOUS 4-BIT COUNTERS WITH 3-STATE OUTPUTS

- 3-State Outputs
- Choice of Asynchronous or Synchronous Clearing and Loading
- Internal Look-Ahead Circuitry for Fast Cascading

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS								OPERATION
OE	ACLR	ALOAD	SCLR	SLOAD	ENT	ENP	CLK	
H	X	X	X	X	X	X	X	Q outputs disabled
L	L	X	X	X	X	X	X	Asynchronous clear
L	H	L	X	X	X	X	X	Asynchronous load
L	H	H	L	X	X	X	↑	Synchronous clear
L	H	H	H	L	X	X	↑	Synchronous load
L	H	H	H	H	H	H	↑	Count
L	H	H	H	H	L	X	X	Inhibit counting
L	H	H	H	H	X	L	X	Inhibit counting

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	ALS	UNIT
I_{CC}		MAX	36	mA
I_{OH}	OUTPUT Q	MAX	-2.6	mA
	CCO & RCO	MAX	-0.4	mA
I_{OL}	OUTPUT Q	MAX	24	mA
	CCO & RCO	MAX	8	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER			INPUT	OUTPUT	MAX or MIN	ALS
fmax					MIN	30
tw	CLK "H"				MIN	16.5
	CLK "L"					16.5
tsu	ENP or ENT	H			MIN	20
		L				20
	A, B, C, D					20
	$\overline{SCLR}$	L				15
		H				30
	$\overline{SLOAD}$	L				15
		H				30
th					MIN	0
t_{PLH}			CLK	Q	MAX	12
t_{PHL}						18
t_{PLH}			CLK	RCO	MAX	29
t_{PHL}						24
t_{PLH}			$\overline{ALOAD}$	Q	MAX	35
t_{PHL}						23
t_{PLH}			$\overline{ALOAD}$	CCO	MAX	55
t_{PHL}						33
t_{PLH}			ENT	RCO	MAX	16
t_{PHL}						14
t_{PHL}			$\overline{ACLR}$	Q	MAX	22

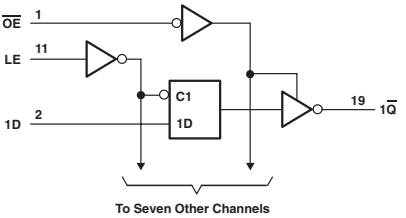
UNIT fmax : MHz, other : ns

563

OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout

Logic Diagram (SN74)



FUNCTION TABLE (SN74)

INPUTS			OUTPUT
ENABLE			
$\overline{OE}$	LE	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	Q_0
H	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 AC	CD74 AC	SN74 ACT	UNIT
I_{CC}	MAX	29	0.08	0.16	0.08	0.16	0.08	0.16	0.04	mA
I_{OH}	MAX	-2.6	-6	-6	-6	-6	-24	-24	-24	mA
I_{OL}	MAX	24	6	6	6	6	24	24	24	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 AC	CD74 AC	SN74 ACT
tw			MIN	15	20	24	25	24	5	4	3
tsu				10	13	15	13	15	2.5	2	4.5
th				10	5	4	10	5	2	3	0
t_{PLH}	D	$\overline{Q}$	MAX	18	44	45	44	45	11.5	10.5	12.5
t_{PHL}				14	44	45	44	45	11	10.5	11
t_{PLH}	LE (CD74: $\overline{LE}$)	$\overline{Q}$	MAX	22	44	50	44	53	11	12	11.5
t_{PHL}				21	44	50	44	53	9.5	12	10.5
t_{PZH}	$\overline{OE}$	$\overline{Q}$	MAX	18	38	45	44	53	10	10.5	10
t_{PZL}				18	38	45	44	53	9.5	10.5	9.5
t_{PHZ}	$\overline{OE}$	$\overline{Q}$	MAX	10	38	45	44	53	12	11.5	11.5
t_{PLZ}				15	38	45	44	53	9	11.5	8.5

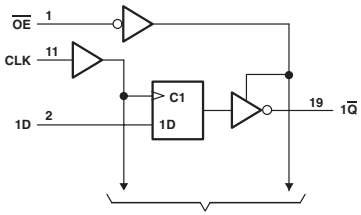
UNIT: ns

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

- 3-State Buffer-Type Inverting Outputs Drive Bus Lines Directly
- Bus-Structured Pinout

Logic Diagram (SN74)



FUNCTION TABLE (SN74)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 AC	SN74 ACT	UNIT
I_{CC}	MAX	30	0.08	0.16	0.08	0.16	0.04	0.04	mA
I_{OH}	MAX	-2.6	-6	-6	-6	-6	-24	-24	mA
I_{OL}	MAX	24	6	6	6	6	24	24	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	ALS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 AC	SN74 ACT
fmax				MIN	30	25	20	25	16	85	75
tw	CLK "H"			MIN	14	20	24	20	30	5	3.5
	CLK "L"				14	20	24	20	30	5	3.5
tsu	CLK ↑				15	25	18	25	30	2.5	3
th	CLK ↑				0	5	5	5	3	2	1
t_{PLH}		CLK	$\overline{Q}$	MAX	14	45	50	45	53	11.5	11.5
t_{PHL}					14	45	50	45	53	10.5	10.5
t_{PZH}		$\overline{OE}$	$\overline{Q}$	MAX	18	38	45	38	53	9.5	9.5
t_{PZL}					18	38	45	38	53	9.5	9.5
t_{PHZ}		$\overline{OE}$	$\overline{Q}$	MAX	10	38	41	38	45	11.5	11.5
t_{PLZ}					15	38	41	38	45	9	8.5

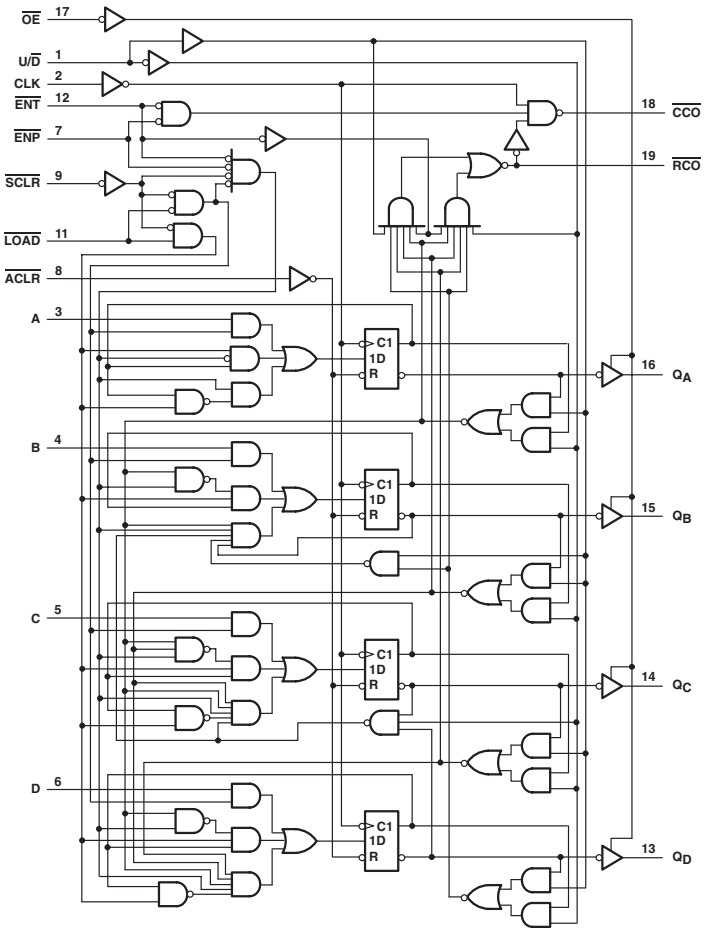
UNIT fmax : MHz, other : ns

569

SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS WITH 3-STATE OUTPUTS

- 3-State Q Outputs Drive Bus Lines Directly
- Fully Synchronous Clear, Count, and Load
- Asynchronous Clear Is Also Provided
- Fully Cascadable

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS								OPERATION
$\overline{OE}$	$\overline{ACLR}$	$\overline{SCLR}$	$\overline{LOAD}$	$\overline{ENT}$	$\overline{ENP}$	U/$\overline{D}$	CLK	
H	X	X	X	X	X	X	X	Q outputs disabled
L	L	X	X	X	X	X	X	Asynchronous clear
L	H	L	X	X	X	X	↑	Synchronous clear
L	H	H	L	X	X	X	↑	Load
L	H	H	H	L	L	H	↑	Count up
L	H	H	H	L	L	L	↑	Count down
L	H	H	H	H	X	X	X	Inhibit count
L	H	H	H	X	H	X	X	Inhibit count

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	ALS	UNIT
I_{CC}		MAX	32	mA
I_{OH}	OUTPUT Q	MAX	-2.6	mA
	$\overline{CCO}$ & $\overline{RCO}$		-0.4	mA
I_{OL}	OUTPUT Q	MAX	24	mA
	$\overline{CCO}$ & $\overline{RCO}$		8	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER			INPUT	OUTPUT	MAX or MIN	ALS
fmax					MIN	30
tw	$\overline{ACLR}$, $\overline{LOAD}$				MIN	15
	CLK "H"					16.5
	CLK "L"					16.5
tsu	Data at A, B, C, D				MIN	20
	$\overline{ENP}$, $\overline{ENT}$	High				30
		Low				20
	$\overline{SCLR}$	High				15
		Low				30
	$\overline{LOAD}$	High				15
		Low				30
	U/$\overline{D}$					30
	$\overline{ACLR}$					10
th					MIN	0
t_{PLH}			CLK	ANY Q	MAX	13
t_{PHL}						16
t_{PLH}			CLK	$\overline{RCO}$	MAX	28
t_{PHL}						19
t_{PLH}			$\overline{ENT}$	$\overline{RCO}$	MAX	15
t_{PHL}						13
t_{PHL}			$\overline{ACLR}$	Q	MAX	20
t_{PZH}			$\overline{OE}$	Q	MAX	18
t_{PZL}						24
t_{PHZ}			$\overline{OE}$	Q	MAX	10
t_{PLZ}						13

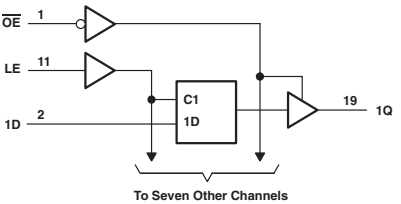
UNIT fmax : MHz, other : ns

573

OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout

Logic Diagram (SN74)



FUNCTION TABLE (SN74)

INPUTS			OUTPUT Q
ENABLE $\overline{OE}$	LE	D	
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	LVT 3V	LVTH 3V	SN74 AC	CD74 AC	UNIT
I_{CC}	MAX	27	106	55	0.08	0.16	0.08	0.16	62	30	12	5	0.04	0.16	mA
I_{OH}	MAX	-2.6	-15	-3	-6	-6	-6	-6	-15	-32	-32	-32	-24	-24	mA
I_{OL}	MAX	24	48	24	6	6	6	6	64	64	64	64	24	24	mA

PARAMETER	MAX or MIN	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LV-AT	LVC 3V	UNIT
I_{CC}	MAX	0.04	0.16	0.04	0.04	-	0.02	0.02	0.01	mA
I_{OH}	MAX	-24	-24	-8	-8	-8	-16	-16	-24	mA
I_{OL}	MAX	24	24	8	8	8	16	16	24	mA

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT
tw	LE			MIN	10	4.5	6	20	24	25	24	4
tsu	LE ↓				10	2	2	13	15	13	20	1
th	LE ↓				7	3	3	5	12	5	15	4
t_{PLH}		D	Q	MAX	14	8	8	44	53	44	53	8.4
t_{PHL}					14	7	6	44	53	44	53	9.6
t_{PLH}		LE	Q	MAX	20	13	13	44	53	44	53	8.1
t_{PHL}					19	7.5	8	44	53	44	53	7.8
t_{PZH}		$\overline{OE}$	Q	MAX	18	6.5	12	38	45	44	53	10.4
t_{PZL}					18	9.5	8.5	38	45	44	53	11
t_{PHZ}		$\overline{OE}$	Q	MAX	10	6.5	7.5	38	45	44	53	6
t_{PLZ}					15	7	6	38	45	44	53	6

PARAMETER		INPUT	OUTPUT	MAX or MIN	ABT	LVT 3V	LVTH 3V	SN74 AC	CD74 AC	SN74 ACT	CD74 ACT	AHC
tw	LE			MIN	3.3	3.3	3	5	4	4	4	5
tsu	LE ↓				1.9	0.7	0.7	3.5	2	3.5	2	3.5
th	LE ↓				1.8	1.6	1.5	2	3	0	3	1.5
t_{PLH}		D	Q	MAX	5.9	4.2	3.9	11.5	8.5	12	10.4	10
t_{PHL}					6.2	4.3	3.9	11	8.5	12	10.4	10
t_{PLH}		LE (CD74AC/ACT: LE)	Q	MAX	6.6	5.6	4.2	11	12	12	12.5	11
t_{PHL}					7.2	6.5	4.2	10	12	10.5	12.5	11
t_{PZH}		$\overline{OE}$	Q	MAX	5.2	5.1	5.1	10	10.5	11	13.5	11
t_{PZL}					6.7	5.5	5.1	9.5	10.5	10.5	13.5	11
t_{PHZ}		$\overline{OE}$	Q	MAX	7.1	5.7	4.9	12	11.5	12.5	12.5	11
t_{PLZ}					6.5	4.6	4.6	9	11.5	9.5	12.5	11

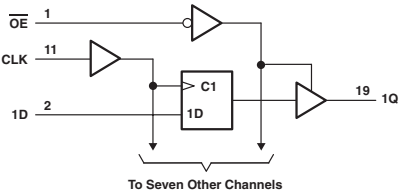
PARAMETER		INPUT	OUTPUT	MAX or MIN	AHCT	LV 3V	LV 5V	LV-AT	LVC 3V
tw	LE			MIN	5	5	5	8.5	3.3
tsu	LE ↓				3.5	3.5	3.5	1.5	2
th	LE ↓				1.5	1.5	1.5	3.5	1.5
t_{PLH}		D	Q	MAX	7.5	16.5	10	10.5	6.9
t_{PHL}					10	16.5	10	10.5	6.9
t_{PLH}		LE (CD74AC/ACT: LE)	Q	MAX	8.5	17.5	11	14.5	7.7
t_{PHL}					10	17.5	11	14.5	7.7
t_{PZH}		$\overline{OE}$	Q	MAX	8	17	11	13.5	7.5
t_{PZL}					11	17	11	13.5	7.5
t_{PHZ}		$\overline{OE}$	Q	MAX	12	16.5	11	12	6.5
t_{PLZ}					10.5	16.5	11	12	6.5

UNIT: ns

OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

- 3-State Buffer-Type Noninverting Outputs Drive Bus Lines Directly
- Bus-Structured Pinout

Logic Diagram (SN74)



FUNCTION TABLE (SN74)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	LVT 3V	LVTH 3V	SN74 AC	UNIT
I_{CC}	MAX	28	134	86	0.08	0.16	0.08	0.16	62	30	12	5	0.04	mA
I_{OH}	MAX	-2.6	-15	-3	-6	-6	-6	-6	-15	-32	-32	-32	-24	mA
I_{OL}	MAX	24	48	24	6	6	6	6	64	64	64	64	24	mA

PARAMETER	MAX or MIN	CD74 AC	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	UNIT
I_{CC}	MAX	0.16	0.04	0.16	0.04	0.04	-	0.02	0.01	mA
I_{OH}	MAX	-24	-24	-24	-8	-8	-8	-16	-24	mA
I_{OL}	MAX	24	24	24	8	8	8	16	24	mA

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT
fmax			MIN	35	125	100	24	20	24	20	77
tw			MIN	14	5.5	7	20	24	20	24	6.5
tsu			MIN	15	5.5	2	25	18	25	18	6
th			MIN	0	0	2	5	5	5	5	0
t_{PLH}	CLK (CD74: CP)	Q	MAX	14	8	10	45	50	45	50	10
t_{PHL}				14	9	10	45	50	45	50	8.9
t_{PZH}	$\overline{OE}$	Q	MAX	18	6	12.5	38	45	38	45	10.4
t_{PZL}				18	10	8.5	38	45	38	45	10.9
t_{PHZ}	$\overline{OE}$	Q	MAX	10	6	8	38	41	38	42	7.5
t_{PLZ}				12	6	6.5	38	41	38	42	6.4

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVT 3V	LVTH 3V	SN74 AC	CD74 AC	SN74 ACT	CD74 ACT	AHC
fmax			MIN	150	150	150	85	125	85	110	75
tw			MIN	3.3	3.3	3.3	5	4	4	4.5	5
tsu			MIN	1.5	2	2	2	2	2.5	2	3
th			MIN	1.8	0.3	0.3	1.5	2	1	3	1.5
t_{PLH}	CLK (CD74: CP)	Q	MAX	6.8	5.4	4.5	11	10.8	12	11.2	12
t_{PHL}				7.1	5.9	4.5	9.5	10.8	11	11.2	12
t_{PZH}	$\overline{OE}$	Q	MAX	5.1	4.8	4.8	9	14.5	10	14.5	12.5
t_{PZL}				6.7	5.1	4.8	9	14.5	10	14.5	12.5
t_{PHZ}	$\overline{OE}$	Q	MAX	7	5.5	4.8	10.5	14.5	11.5	14.5	11.5
t_{PLZ}				6.5	4.5	4.4	8.5	14.5	9	14.5	11.5

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHCT	LV 3V	LV 5V	LVC 3V
fmax			MIN	75	45	75	150
tw			MIN	5.5	5	5	3.3
tsu			MIN	3.5	3.5	3.5	2
th			MIN	1.5	1.5	1.5	1.5
t_{PLH}	CLK (CD74: CP)	Q	MAX	12	19	12	7
t_{PHL}				12	19	12	7
t_{PZH}	$\overline{OE}$	Q	MAX	12.5	18.5	12.5	7.5
t_{PZL}				12.5	18.5	12.5	7.5
t_{PHZ}	$\overline{OE}$	Q	MAX	11.5	17	11.5	6.4
t_{PLZ}				11.5	17	11.5	6.4

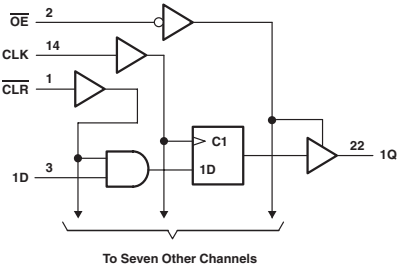
UNIT fmax : MHz, other : ns

575

OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

- 3-State Buffer-Type Noninverting Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Synchronous Clear

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	$\overline{CLR}$	CLK	D	Q
L	L	↑	X	L
L	H	↑	H	H
L	H	↑	L	L
L	H	L	X	Q_0
H	X	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	UNIT
I_{CC}	MAX	30	142	mA
I_{OH}	MAX	-2.6	-15	mA
I_{OL}	MAX	24	48	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER			INPUT	OUTPUT	MAX or MIN	ALS	AS
fmax					MIN	30	90
tw	CLK	H			MIN	16.5	5.5
	CLK	L					5.5
tsu	DATA					15	5.5
	$\overline{CLR}$	L					6.5
th	DATA					0	3
	$\overline{CLR}$						0
t_{PLH}			CLK	Q	MAX	14	8
t_{PHL}						14	9
t_{PZH}			$\overline{OC}$	Q	MAX	18	6
t_{PZL}						18	10
t_{PHZ}			$\overline{OC}$	Q	MAX	10	6
t_{PLZ}						13	6

UNIT fmax : MHz, other : ns

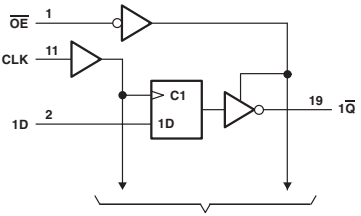
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

576

OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

- 3-State Buffer-Type Inverting Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Functionally Equivalent to '576, Except for Having Inverted Outputs

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	UNIT
I_{CC}	MAX	30	135	mA
I_{OH}	MAX	-2.6	-15	mA
I_{OL}	MAX	24	48	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	ALS	AS
fmax				MIN	30	125
tw	H			MIN	16.5	4
	L					2
tsu	DATA				15	2
th	DATA				0	2
t_{PLH}		CLK	$\overline{Q}$	MAX	14	8
t_{PHL}					14	9
t_{PZH}		$\overline{OE}$	$\overline{Q}$	MAX	18	6
t_{PZL}					18	10
t_{PHZ}		$\overline{OE}$	$\overline{Q}$	MAX	10	6
t_{PLZ}					15	6

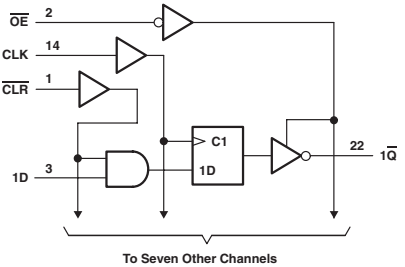
UNIT fmax : MHz, other : ns

577

OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

- 3-State Buffer-Type Inverting Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Synchronous Clear

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	$\overline{CLR}$	CLK	D	$\overline{Q}$
L	L	↑	X	H
L	H	↑	H	L
L	H	↑	L	H
L	H	L	X	$\overline{Q}_0$
H	X	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	UNIT
I_{CC}	MAX	30	142	mA
I_{OH}	MAX	-2.6	-15	mA
I_{OL}	MAX	24	48	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	ALS	AS
fmax				MIN	30	125
tw					16.5	4
tsu	DATA			MIN	15	2
th	$\overline{CLR}$				0	2
t_{PLH}		CLK	$\overline{Q}$	MAX	14	8
t_{PHL}					14	9
t_{PZH}		$\overline{OE}$	$\overline{Q}$	MAX	18	6
t_{PZL}					18	10
t_{PHZ}		$\overline{OE}$	$\overline{Q}$	MAX	10	6
t_{PLZ}					15	6

UNIT fmax : MHz, other : ns

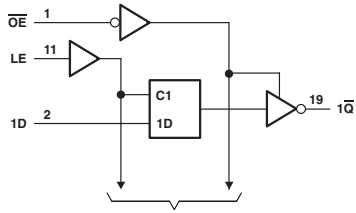
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

580

OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Inverting-Logic Outputs
- Bus-Structured Pinout

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT Q
ENABLE $\overline{OE}$	LE	D	
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	UNIT
I_{CC}	MAX	29	115	mA
I_{OH}	MAX	-2.6	-15	mA
I_{OL}	MAX	24	48	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	ALS	AS
tw	C			MIN	15	2
tsu	C↓				10	2
th	C↓				10	3
t_{PLH}		D	$\overline{Q}$	MAX	18	7.5
t_{PHL}					14	7
t_{PLH}		LE	$\overline{Q}$	MAX	22	9
t_{PHL}					21	8
t_{PZH}		$\overline{OE}$	$\overline{Q}$	MAX	18	6.5
t_{PZL}					18	9.5
t_{PHZ}		$\overline{OE}$	$\overline{Q}$	MAX	10	6.5
t_{PLZ}					15	7

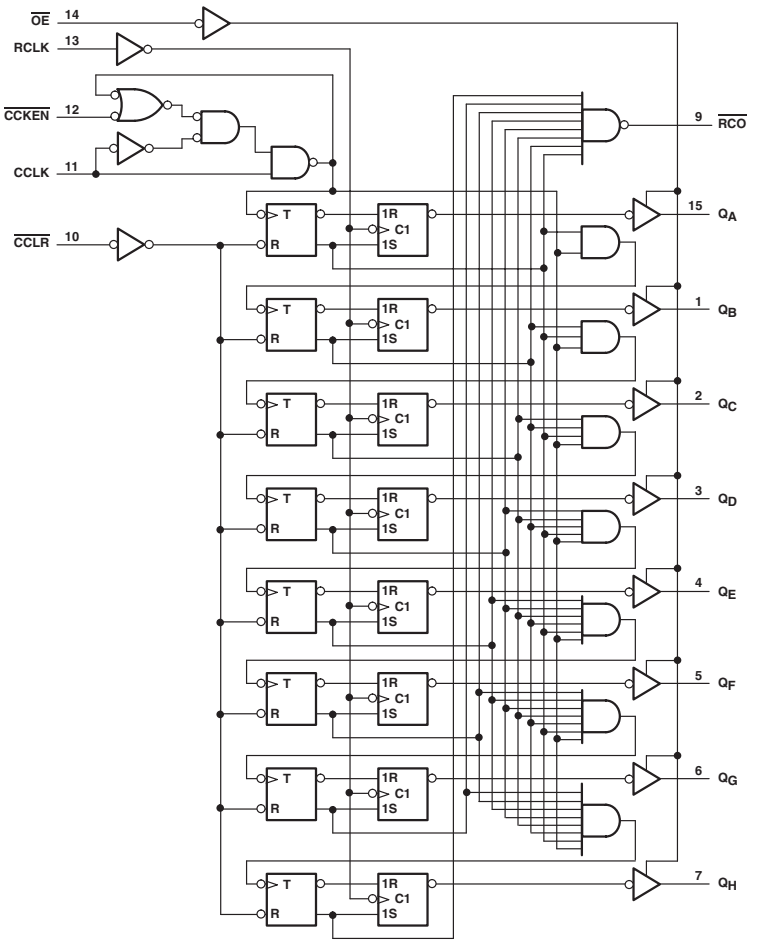
UNIT: ns

590

8-BIT BINARY COUNTERS WITH 3-STATE OUTPUT REGISTERS

- Parallel Register Outputs
- Counter Has Direct Clear
- 3-State Outputs
- Guaranteed Counter Frequency: DC to 20MHz

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	SN74 HC	UNIT
I_{CC}		MAX	65	0.08	mA
I_{OH}	$\overline{RCO}$	MAX	-1	-4	mA
	Q	MAX	-2.6	-6	mA
I_{OL}	$\overline{RCO}$	MAX	16	4	mA
	Q	MAX	24	6	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	LS	SN74 HC
fmax		CCK	$\overline{RCO}$	MIN	20	13
tw	CCK			MIN	25	31
	$\overline{CCLR}$				20	25
	RCK				20	31
tsu	$\overline{CCLR}$ ↑ bofore CCK ↑			MIN	20	25
	CCK ↑ bofore RCK ↑				40	25
t_{PLH}		CCK ↑	$\overline{RCO}$	MAX	22	45
t_{PHL}					30	45
t_{PLH}		$\overline{CCLR}$ ↓	$\overline{RCO}$	MAX	45	39
t_{PLH}		RCK ↑	Q	MAX	18	42
t_{PHL}					33	42
t_{PZH}		$\overline{OE}$ ↓	Q	MAX	38	37
t_{PZL}					45	37
t_{PHZ}		$\overline{OE}$ ↓	Q	MAX	30	37
t_{PLZ}					38	37

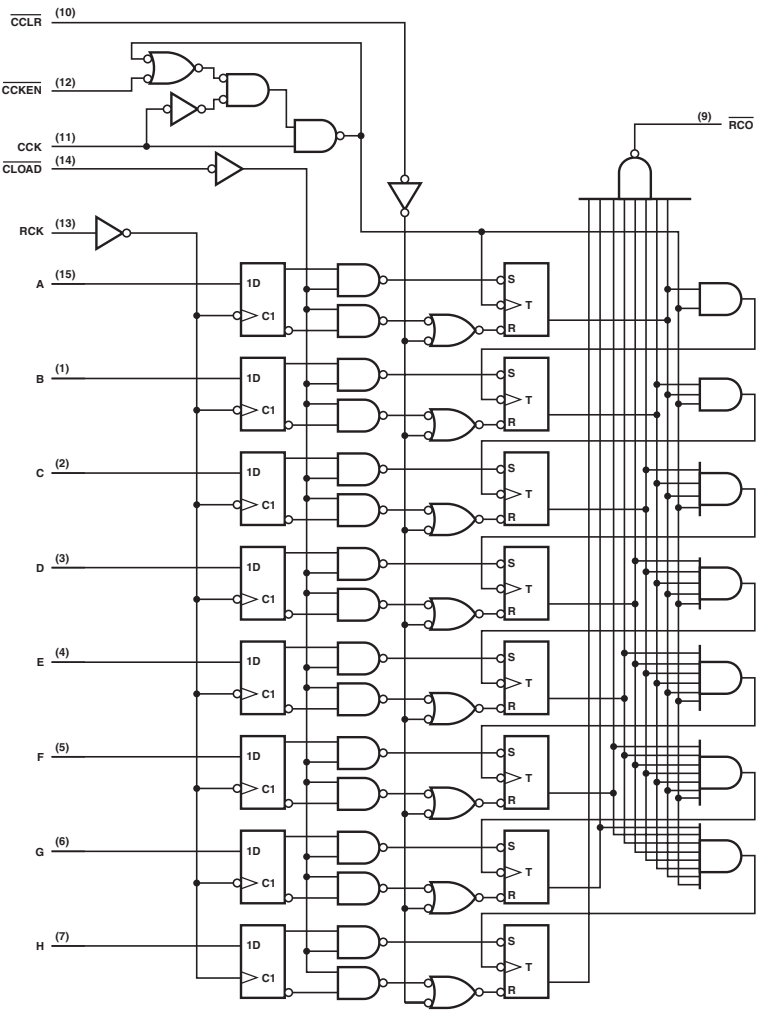
UNIT fmax : MHz, other : ns

592

8-BIT BINARY COUNTERS WITH INPUT REGISTERS

- Parallel Register Inputs
- Counter Has Directly Overriding Load and Clear
- Accurate Counter Frequency: DC to 20MHz

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	UNIT
I_{CC}	MAX	60	mA
I_{OH}	MAX	-1	mA
I_{OL}	MAX	16	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	LS
fmax		CCK	$\overline{RCO}$	MIN	20
tw	CCK			MIN	25
	$\overline{CCLR}$				20
	RCK				20
	$\overline{CLOAD}$				40
tsu	$\overline{CCLR}$ ↑ bofore CCK ↑			MIN	20
	$\overline{CLOAD}$ ↑ bofore CCK ↑				20
	RCK ↑ before $\overline{CLOAD}$ ↑				30
	A to H bofore RCK				20
th				MIN	0
t_{PLH}		CCK ↑	$\overline{RCO}$	MAX	23
t_{PHL}					30
t_{PLH}		$\overline{CLOAD}$ ↓	$\overline{RCO}$	MAX	47
t_{PHL}					17
t_{PLH}		$\overline{CCLR}$ ↓	$\overline{RCO}$	MAX	45
t_{PLH}		RCK ↑	$\overline{RCO}$ Q	MAX	53
t_{PHL}					45

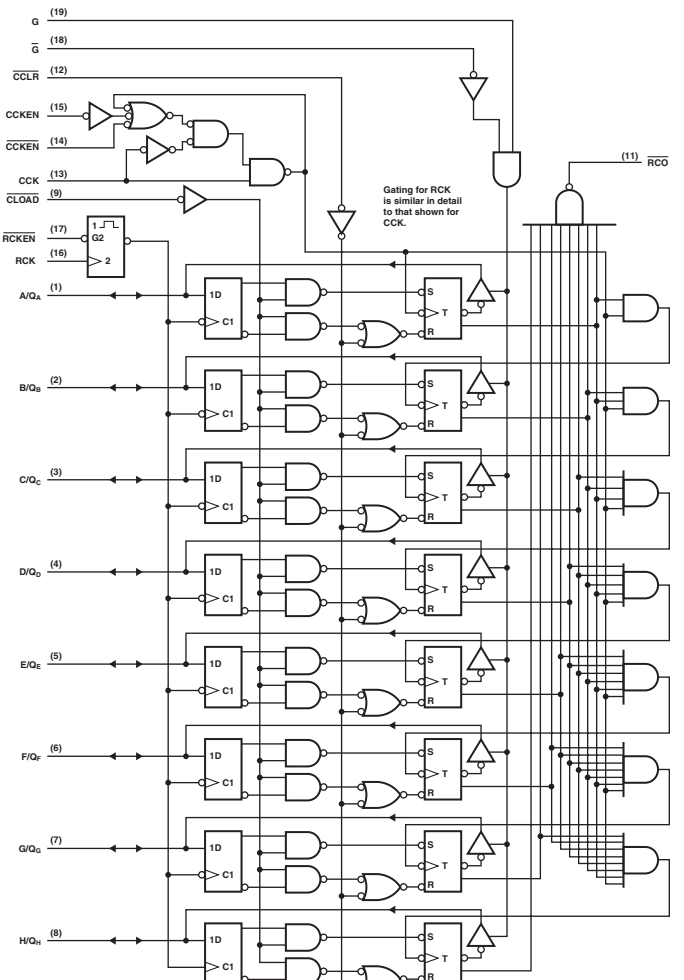
UNIT fmax : MHz, other : ns

593

8-BIT BINARY COUNTERS WITH INPUT REGISTERS

- Parallel 3-State I/O: Register Inputs/Counter Outputs
- Counter Has Directly Overriding Load and Clear
- Accurate Counter Frequency: DC to 20MHz
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	ACT 11	UNIT
I_{CC}		MAX	85	0.08	mA
I_{OH}	$\overline{RCO}$	MAX	-1	-24	mA
	Q	MAX	-2.6	-24	mA
I_{OL}	$\overline{RCO}$	MAX	16	24	mA
	Q	MAX	24	24	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	LS	ACT 11
fmax		CCK	$\overline{RCO}$	MIN	20	52
tw	CCK			MIN	25	9.6
	$\overline{CCLR}$				20	7.6
	RCK				20	5.8
	$\overline{CLOAD}$				40	6.2
tsu	$\overline{CCLR}$ ↑ bofore CCK ↑			MIN	20	1.2
	$\overline{CLOAD}$ ↑ bofore CCK ↑				20	5.1
	RCK ↑ bofore $\overline{CLOAD}$ ↑				30	7.4
	A to H bofore RCK				20	2.4
th				MIN	0	0.8
t_{PLH}		CCK ↑	Q	MAX	21	15.1
t_{PHL}					39	15
t_{PLH}		$\overline{CLOAD}$ ↓	Q	MAX	51	19.1
t_{PHL}					42	21.7
t_{PHL}		$\overline{CCLR}$ ↓	Q	MAX	38	16

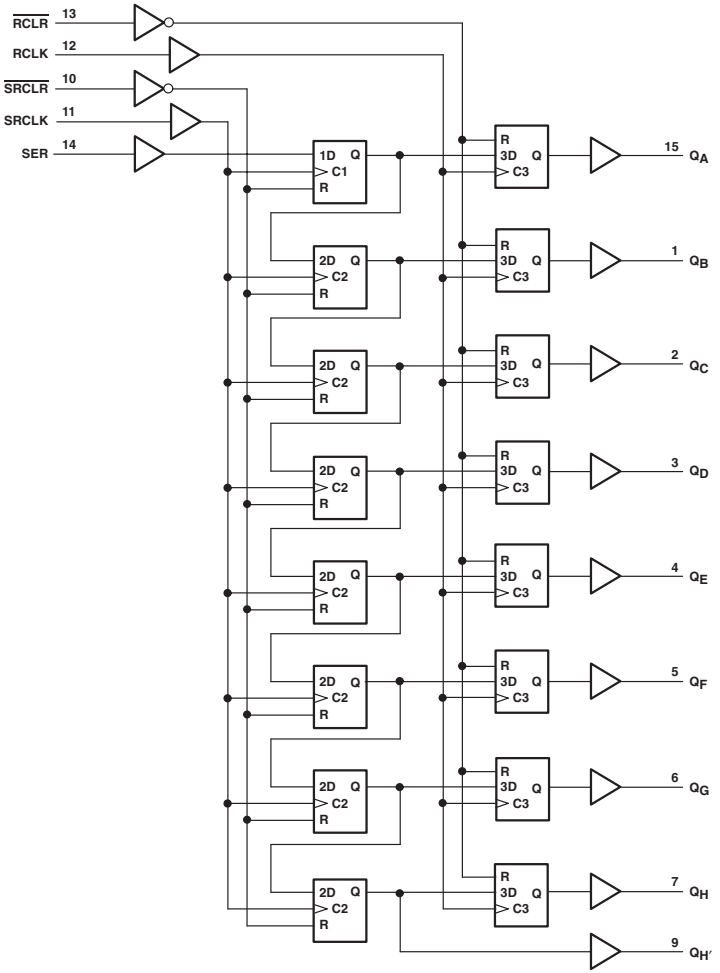
UNIT fmax : MHz, other : ns

594

8-BIT SHIFT REGISTERS WITH OUTPUT REGISTERS

- 8-Bit Serial-In, Parallel-Out Shift Registers with Storage
- Independent Direct Overriding Clears on Shift and Storage Registers
- Independent Clocks for Shift and Storage Registers
- Guaranteed Shift Frequency: DC to 20MHz

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS					FUNCTION
SER	SRCLK	$\overline{\text{SRCLR}}$	RCLK	$\overline{\text{RCLR}}$	
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of shift register goes high. Other stages store the data of previous stage, respectively.
L	↓	H	X	X	Shift register state is not changed.
X	X	X	X	L	Storage register is cleared.
X	X	X	↑	H	Shift register data is stored in the storage register.
X	X	X	↓	H	Storage register state is not changed.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	SN74 HC	AHC	AHCT	LV 3V	LV 5V	UNIT
I_{CC}		MAX	65	0.08	0.04	0.02	-	0.02	mA
I_{OH}	QH'	MAX	-1	-4	-4	-4	-6	-12	mA
	Q	MAX	-2.6	-6	-8	-8	-6	-12	mA
I_{OL}	QH'	MAX	16	4	4	4	6	12	mA
	QA to QH	MAX	24	6	8	8	6	12	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	LS	SN74 HC	AHC	AHCT	LV 3V	LV 5V
t_w	SRCK			MIN	25	20	5	5.5	5.5	5
	RCK				20	20	5	5.5	5.5	5
t_{su}	$\overline{\text{SRCLR}}$ ↑ to SRCK ↑			MIN	20	10	3.3	3.3	4.8	3.3
	SER to SRCK ↑				20	22	3	3	3.5	3
	SRCK ↑ to RCK ↑				40	22	5	5	8.5	5
	$\overline{\text{SRCLR}}$ ↓ to RCK ↑				40	13	5	5	9	5
	$\overline{\text{RCLR}}$ ↑ to RCK ↑				20	5	3.7	3.8	5.3	3.7
th				MIN	0	5	2	2	1.5	2
t_{PLH}		SRCK ↑	QH'	MAX	18	37	9.1	9.1	12.4	9.1
t_{PHL}					23	37	10.1	10.1	13.9	10.1
t_{PLH}		RCK ↑	QA to QH	MAX	18	37	8.3	8.3	11.1	8.3
t_{PHL}					30	37	9.7	9.7	13.1	9.7
t_{PHL}		$\overline{\text{SRCLR}}$ ↓	QH'	MAX	33	37	10.1	10.1	14	10.1
t_{PHL}		$\overline{\text{RCLR}}$ ↓	QA to QH		57	31	10.7	10.7	14.4	10.7

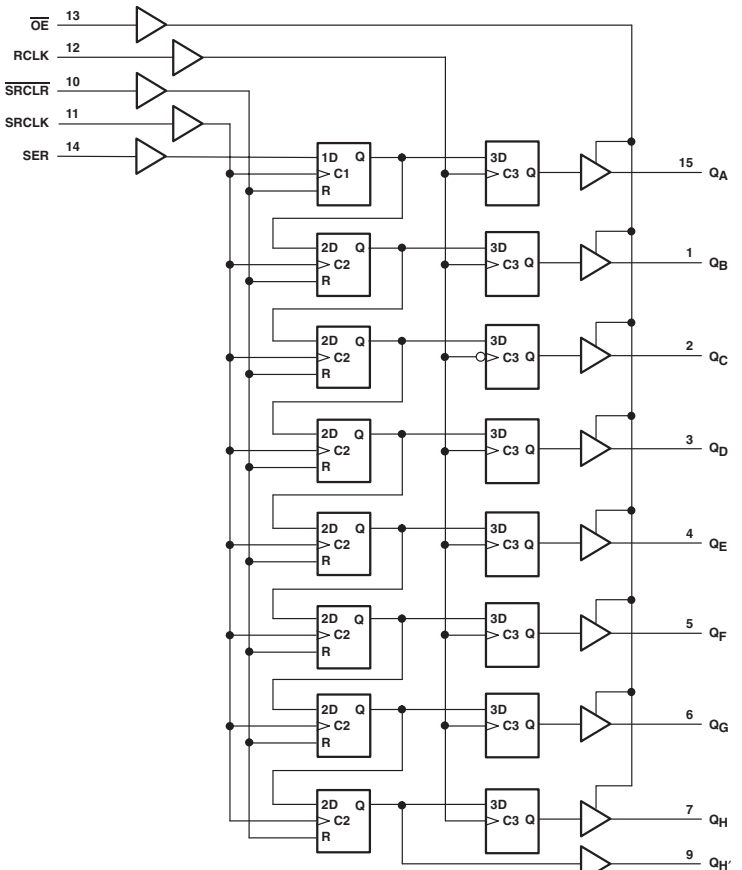
UNIT: ns

595

8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUT REGISTERS

- 8-Bit Serial-In, Parallel-Out Shift Registers with Storage
- 3-State Outputs
- Shift Register Has Direct Clear
- Accurate Shift Frequency: DC to 20MHz

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS					FUNCTION
SER	SRCLK	$\overline{\text{SRCLR}}$	RCLK	$\overline{\text{OE}}$	
X	X	X	X	H	Outputs Q_A-Q_H are disabled.
X	X	X	X	L	Outputs Q_A-Q_H are enabled.
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.
X	↓	H	X	X	Shift-register state is not changed.
X	X	X	↑	X	Shift-register data is stored in the storage register.
X	X	X	↓	X	Storage-register state is not changed.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	SN74 HC	CD74 HC	AHC	AHCT	LV 3V	LV 5V	UNIT
I_{CC}		MAX	65	0.08	0.16	0.04	0.04	-	0.02	mA
I_{OH}	QH'	MAX	-1	-4	-4	-8	-8	-8	-16	mA
	QA to QH	MAX	-26	-6	-6	-8	-8	-8	-16	mA
I_{OL}	QH'	MAX	16	4	4	8	8	8	16	mA
	QA to QH	MAX	24	6	6	8	8	8	16	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	LS	SN74 HC	CD74 HC	AHC	AHCT	LV 3V	LV 5V
tw	SRCK			MIN	25	20	20	5	5.5	5.5	5
	RCK				20	20	20	5	5.5	5.5	5
tsu	$\overline{\text{SRCLR}}$ ↑ to SRCK ↑			MIN	20	12	12	2.5	3.8	3	2.5
	SER to SRCK ↑				20	25	25	3	3	3.5	3
	SRCK ↑ to RCK ↑				40	19	19	5	5	8.5	5
	$\overline{\text{SRCLR}}$ ↓ to RCK ↑				40	13	13	5	5	9	5
th				MIN	0	0	0	2	2	1.5	2
t_{PLH}		SRCK ↑	QH'	MAX	18	40	48	11.4	11.4	18.5	11.4
t_{PHL}					25	40	48	11.4	11.4	18.5	11.4
t_{PLH}		RCK ↑	QA to QH	MAX	18	37	45	10.5	10.5	17	10.5
t_{PHL}					35	37	45	10.5	10.5	17	10.5
t_{PHL}		$\overline{\text{SRCLR}}$ ↓	QH'	MAX	35	44	44	11.1	11.1	17.2	11.1

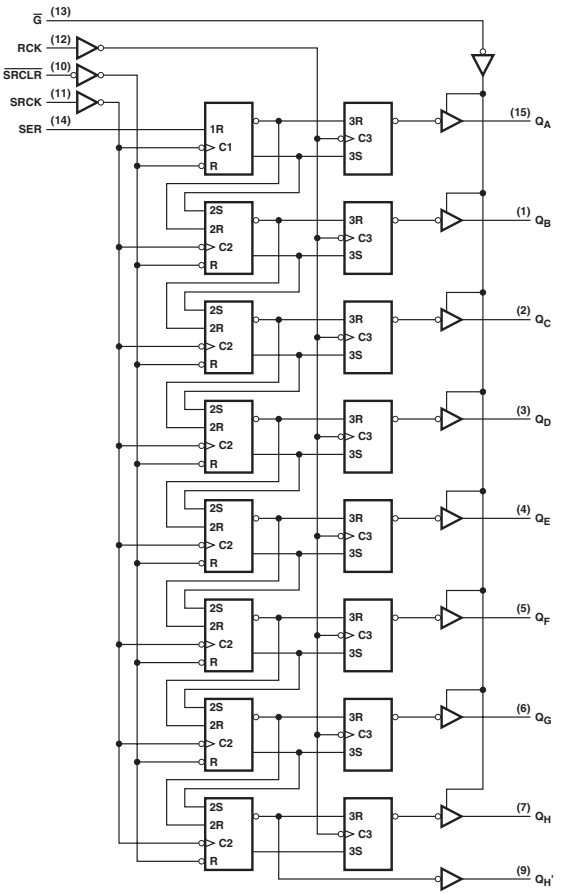
UNIT: ns

596

8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES

- 8-Bit Serial-In, Parallel-Out Shift Registers with Storage
- Open-Collector Parallel Outputs
- Shift Register Has Direct Clear
- Accurate Shift Frequency: DC to 20MHz

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	UNIT
I_{CC}		MAX	55	mA
I_{OH}	$\overline{Q}H'$	MAX	16	mA
	Q	MAX	24	mA
I_{OL}	$\overline{Q}H'$	MAX	-1	mA
V_{OH}	QA to QH	MAX	5.5	V

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	LS
tw	SRCK			MIN	25
	RCK				20
tsu	$\overline{SRCLR}$ ↑ to SRCK ↑			MIN	20
	SER to SRCK ↑				20
	SRCK ↑ to RCK ↑				40
	$\overline{SRCLR}$ ↓ to RCK ↑				40
th				MIN	0
t_{PLH}		SRCK ↑	QH'	MAX	21
t_{PHL}					30
t_{PLH}		RCK ↑	QA to QH	MAX	42
t_{PHL}					35
t_{PHL}		$\overline{SRCLR}$ ↓	QH'	MAX	35

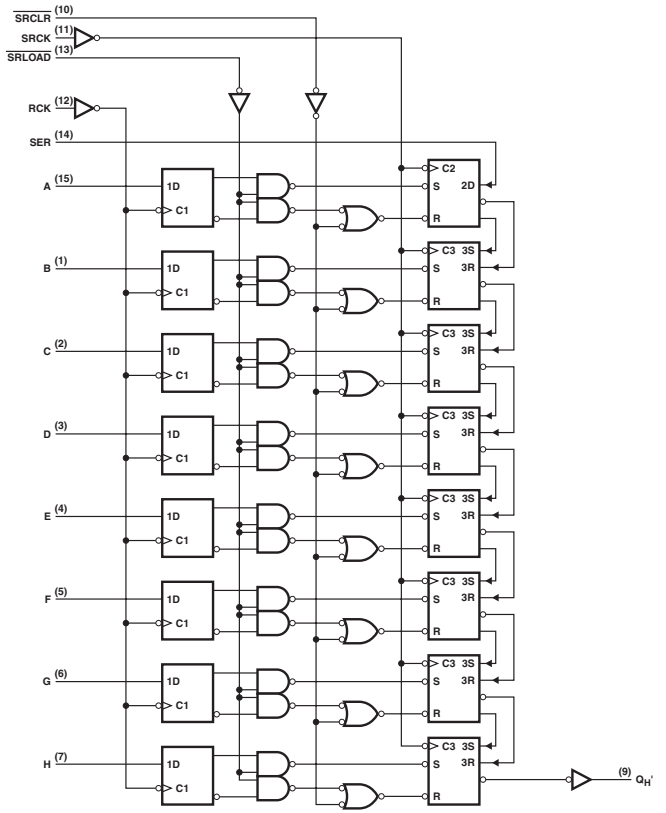
UNIT: ns

597

SERIAL-OUT SHIFT REGISTERS WITH INPUT LATCHES

- 8-Bit Parallel Storage Registers Inputs
- Shift Register Has Direct Overriding Load and Clear
- Accurate Shift Frequency: DC to 20MHz

Logic Diagram (SN74LS)



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

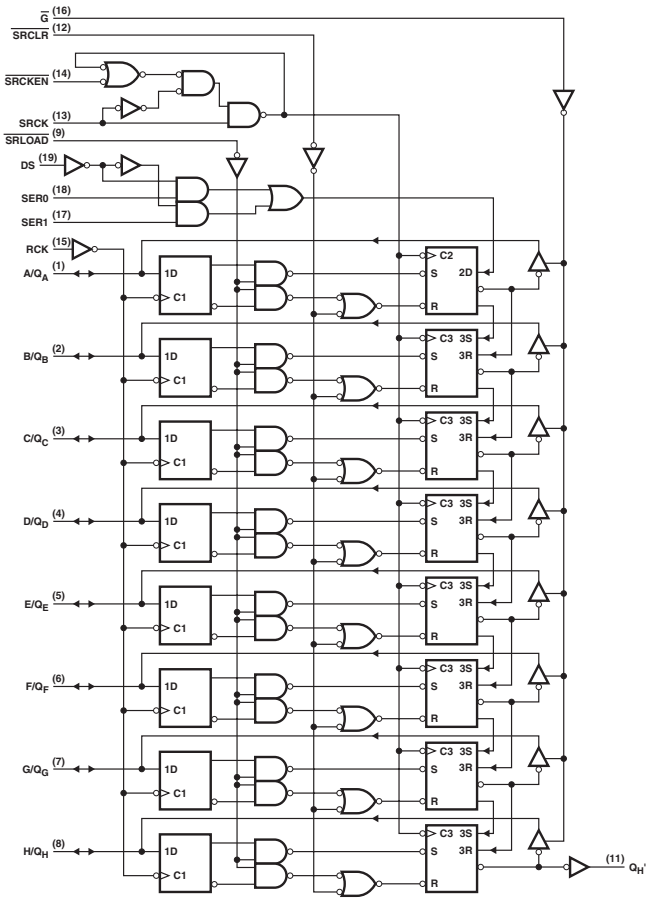
PARAMETER	MAX or MIN	LS	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	53	0.16	0.16	mA
I_{OH}	MAX	-1	-4	-4	mA
I_{OL}	MAX	16	4	4	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	CD74 HC	CD74 HCT
f_{max}	SRCK	Q	MIN	20	-	-
	SRCK	QH'	MIN	20	-	-
	SH_{CP}		MIN	-	20	16
t_w	SRCK high		MIN	15	-	-
	SRCK low		MIN	35	-	-
	RCK		MIN	20	-	-
	$\overline{SRCLR}$		MIN	20	-	-
	$\overline{SRLOAD}$		MIN	40	-	-
	SH_{CP}		MIN	-	20	30
	ST_{CP}		MIN	-	15	20
	$\overline{MR}$		MIN	-	20	27
	$\overline{PL}$		MIN	-	18	24
t_{su}	Data before RCK ↑		MIN	20	-	-
	$\overline{SRCLR}$ inactive beforeSRCK ↑		MIN	25	-	-
	$\overline{SRLOAD}$ inactive before SRCK ↑		MIN	30	-	-
	RCK ↑ brfore SRLOAD ↑		MIN	40	-	-
	SER before SRCK ↑		MIN	20	-	-
	ST_{CP} to SH_{CP}		MIN	-	30	36
	D_s to SH_{CP}		MIN	-	15	15
	D_n to ST_{CP}		MIN	-	15	15
t_h	LS597 only		MIN	0	-	-
	ST_{CP} to SH_{CP}			-	0	0
	D_s to SH_{CP}			-	3	3
	D_n to ST_{CP}			-	3	3
t_{PLH}	SRCK ↑	QH'	MAX	23	-	-
t_{PHL}				23	-	-
t_{PLH}	$\overline{SRLOAD}$ ↓	QH'	MAX	57	-	-
t_{PHL}				44	-	-
t_{PHL}	$\overline{SRCLR}$ ↓	QH'	MAX	36	-	-
t_{PLH}	RCK ↑	QH'	MAX	60	-	-
t_{PHL}				48	-	-
t_{PLH}	SH_{CP}	Q7	MAX	-	53	57
t_{PHL}				-	53	57
t_{PLH}	$\overline{PL}$	Q7	MAX	-	60	72
t_{PHL}				-	60	72
t_{PLH}	ST_{CP}	Q7	MAX	-	72	84
t_{PHL}				-	72	84
t_{PLH}	$\overline{MR}$	Q7	MAX	-	53	66
t_{PHL}				-	53	66

UNIT f_{max} : MHz, other : ns

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	UNIT
I_{CC}	MAX	85	mA
I_{OH}	MAX	-2.6	mA
I_{OL}	MAX	24	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
f_{max}	SRCK	Q	MIN	20
	SRCK	QHB	MIN	20
t_w	SRCK high		MIN	15
	SRCK low		MIN	35
	RCK		MIN	20
	$\overline{SRCLR}$		MIN	20
	$\overline{SRLOAD}$		MIN	40
t_{su}	Data before RCK ↑		MIN	20
	DS before RCK ↑		MIN	30
	SRCKEN iow before SRCK ↑		MIN	20
	$\overline{SRCLR}$ inactive beforeSRCK ↑		MIN	25
	$\overline{SRLOAD}$ inactive before SRCK ↑		MIN	30
	RCK ↑ brfore SRLOAD ↑		MIN	40
	SER before SRCK ↑		MIN	20
t_h			MIN	0
t_{PLH}	SRCK ↑	QHB	MAX	17
t_{PHL}				23
t_{PLH}	$\overline{SRLOAD}$ ↓	QHB	MAX	42
t_{PHL}				39
t_{PHL}	$\overline{SRCLR}$ ↓	QHB	MAX	27
t_{PLH}	RCK ↑	QHB	MAX	48
t_{PHL}				36
t_{PLH}	SHCP	Q7	MAX	18
t_{PHL}				28

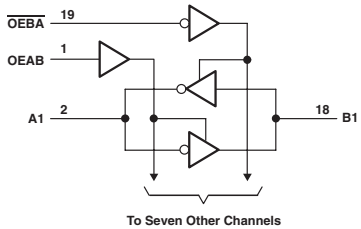
UNIT f_{max} : MHz, other : ns

620

OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- Local Bus-Latch Capability
- 3-State Inverting Outputs
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



FUNCTION TABLE

ENABLE INPUTS		OPERATION
$\overline{OEBA}$	OEAB	
L	L	$\overline{B}$ data to Abus
H	H	$\overline{A}$ data to B bus
H	L	Isoration
L	H	$\overline{B}$ data to Abus $\overline{A}$ data to B bus

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	ALS-1	AS	SN74 HC	SN74 BCT	ABT	AC 11	ACT 11	UNIT
I_{CCZ}	MAX	95	47	47	77	0.08	10	0.25	0.08	0.008	mA
I_{CCL}	MAX	90	44	44	122	0.08	84	30	0.08	0.008	mA
I_{OH} (A port)	MAX	-15	-15	-15	-15	-6	-3	-32	-24	-24	mA
I_{OH} (B port)	MAX	-15	-15	-15	-15	-6	-15	-32	-24	-24	mA
I_{OL} (A port)	MAX	24	24	48	64	6	24	64	24	24	mA
I_{OL} (B port)	MAX	24	24	48	64	6	64	64	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	ALS-1	AS	SN74 HC	SN74 BCT	ABT	AC 11	ACT 11
t_{PLH}	A	B	MAX	10	10	10	7	26	5.8	4.8	7.4	9.4
t_{PHL}				15	10	10	6	26	3.6	4.8	7.1	8.6
t_{PLH}	B	A	MAX	10	10	10	7	26	6.9	4.8	7.4	9.4
t_{PHL}				15	10	10	6	26	3.9	4.8	7.1	8.6
t_{PZH}	$\overline{OEBA}$	A	MAX	40	17	17	8	53	10.6	5.5	8.9	10.3
t_{PZL}				40	25	25	9	53	11.1	7.1	8.5	10.1
t_{PHZ}	$\overline{OEBA}$	A	MAX	25	12	12	6	38	10	7	8.1	10.4
t_{PLZ}				25	18	18	12	38	7.8	5.8	8.7	10.9
t_{PZH}	OEAB	B	MAX	40	18	18	8	53	7.4	6.8	8.8	11.3
t_{PZL}				40	25	25	9	53	9	6.4	8.8	11
t_{PHZ}	OEAB	B	MAX	25	12	12	6	38	8.1	6.5	8.2	9.4
t_{PLZ}				25	18	18	13	38	5.9	5.6	8.6	9.6

UNIT: ns

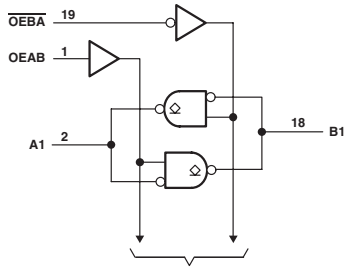
: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

621

OCTAL BUS TRANSCEIVERS

- Local Bus-Latch Capability
- Open-Collector True Outputs
- Schmitt-Triggered Inputs (SN74LS621)

Logic Diagram



FUNCTION TABLE

ENABLE INPUTS		OPERATION
$\overline{OEBA}$	OEAB	
L	L	B data to Abus
H	H	A data to B bus
H	L	Isoration
L	H	B data to Abus A data to B bus

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	ALS A-1	AS	UNIT
I_{CC}	MAX	90	48	48	189	mA
V_{OH}	MAX	5.5	5.5	5.5	5.5	V
I_{OL}	MAX	24	24	48	64	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	ALS A-1	AS
t_{PLH}	A	B	MAX	25	33	33	24
t_{PHL}				25	20	20	21
t_{PLH}	B	A	MAX	25	33	33	7.5
t_{PHL}				25	20	20	7.5
t_{PLH}	$\overline{OEBA}$	A	MAX	40	39	39	21
t_{PHL}				50	35	35	9
t_{PLH}	OEAB	B	MAX	40	39	39	22
t_{PHL}				50	35	35	10

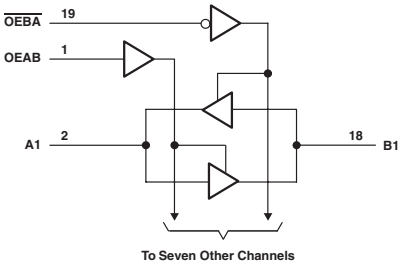
UNIT: ns

623

OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- Local Bus-Latch Capability
- 3-State True Outputs
- Schmitt-Triggered Inputs (SN74LS623)
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram (SN74)



FUNCTION TABLE (SN74)

ENABLE INPUTS		OPERATION
$\overline{OEBA}$	OEAB	
L	L	B data to Abus
H	H	A data to B bus
H	L	Isoration
L	H	B data to Abus A data to B bus

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	AS	F	SN74 HC	SN74 HCT	SN74 BCT	ABT	AC 11	ACT 11	CD74 AC	CD74 ACT	UNIT
I_{CCZ}	MAX	95	55	116	130	0.08	0.08	11	0.25	0.08	0.04	0.16	0.16	mA
I_{CCL}	MAX	90	50	189	140	0.08	0.08	92	30	0.08	0.04	0.16	0.16	mA
I_{OH} (A port)	MAX	-15	-15	-15	-3	-6	-6	-3	-32	-24	-24	-24	-24	mA
I_{OH} (B port)	MAX	-15	-15	-15	-15	-6	-6	-15	-32	-24	-24	-24	-24	mA
I_{OL} (A port)	MAX	24	24	64	24	6	6	24	64	24	24	24	24	mA
I_{OL} (B port)	MAX	24	24	64	64	6	6	64	64	24	24	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS	F	SN74 HC	SN74 HCT	SN74 BCT	ABT	AC 11	ACT 11	CD74 AC	CD74 ACT
t_{PLH}	A	B	MAX	15	13	9	6.5	26	28	5.2	4.6	7.8	8.5	9.6	10.6
t_{PHL}				15	11	8	7.5	26	28	7.4	4.6	7.1	7.9	9.6	10.6
t_{PLH}	B	A	MAX	15	13	9	6.5	26	28	6.7	4.6	7.8	8.5	9.6	10.6
t_{PHL}				15	11	8.5	7.5	26	28	8	4.6	7.1	7.9	9.6	10.6
t_{PZH}	$\overline{OEBA}$	A	MAX	40	22	11	12	53	53	10.6	7.5	9	9.7	13.4	14.4
t_{PZL}				40	22	10	10	53	53	10.7	7.5	9.1	10	13.4	14.4
t_{PHZ}	$\overline{OEBA}$	A	MAX	25	16	7.5	7.5	38	38	9.8	7.5	8.3	10.9	13.4	14.4
t_{PLZ}				25	19	11.5	7	38	38	7.8	7.5	8.8	11.5	13.4	14.4
t_{PZH}	OEAB	B	MAX	40	22	11.5	11.5	53	53	7.6	7.5	9.2	10.7	13.4	14.4
t_{PZL}				40	22	11	9.5	53	53	8.9	7.5	9.4	10.9	13.4	14.4
t_{PHZ}	OEAB	B	MAX	25	16	7	10	38	38	7.7	7.5	8.3	9.5	13.4	14.4
t_{PLZ}				25	19	9	10	38	38	7.1	7.5	8.8	10	13.4	14.4

UNIT: ns

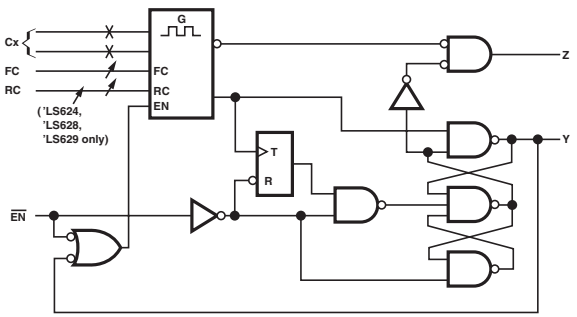
: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

624

VOLTAGE-CONTROLLED OSCILLATORS

- This Voltage Oscillators (VCOs) is Improved Versions of The Original VCO Family: SN74124, 324, 325, 326, 327
- Separate Supply Voltage Pins for Isolation of Frequency Control Inputs and Oscillators from Outputs Circuitry
- Highly Stable Operation over Specified Temperature and / or Supply Voltage Ranges

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OP

PARAMETER	MAX or MIN	LS	UNIT
I_{CC}	MAX	35	mA
I_{OL}	MAX	24	mA
I_{OH}	MAX	-1.2	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERIST

PARAMETER	MAX or MIN	LS
fo	MAX	25

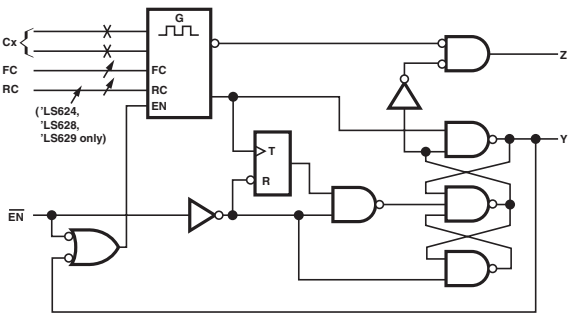
UNIT: MHz

628

VOLTAGE-CONTROLLED OSCILLATORS

- This Voltage Oscillators (VCOs) is Improved Versions of The Original VCO Family: SN74124, 324, 325, 326, 327
- Separate Supply Voltage Pins for Isolation of Frequency Control Inputs and Oscillators from Outputs Circuitry
- Highly Stable Operation over Specified Temperature and / or Supply Voltage Ranges
- Two Rexternal Pins Can Offer More Precise Temprature Compensation

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPER

PARAMETER	MAX or MIN	LS	UNIT
I_{CC}	MAX	35	mA
I_{OH}	MAX	-1.2	mA
I_{OL}	MAX	24	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTIC

PARAMETER	MAX or MIN	LS
fo	MAX	25

UNIT: MHz

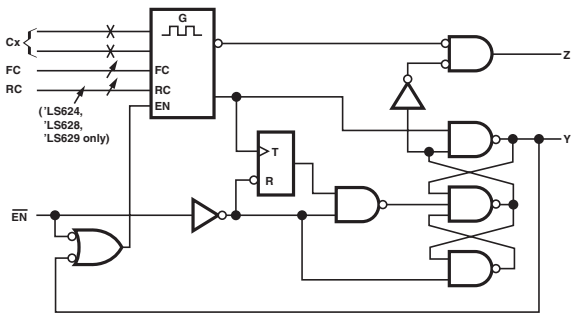
: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

629

DUAL VOLTAGE-CONTROLLED OSCILLATORS

- This Voltage Oscillators (VCOs) is Improved Versions of The Original VCO Family: SN74124, 324, 325, 326, 327
- Separate Supply Voltage Pins for Isolation of Frequency Control Inputs and Oscillators from Outputs Circuitry
- Highly Stable Operation over Specified Temperature and / or Supply Voltage Ranges

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPEI

PARAMETER	MAX or MIN	LS	UNIT
I_{CC}	MAX	55	mA
I_{OH}	MAX	-1.2	mA
I_{OL}	MAX	24	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTI(

PARAMETER	MAX or MIN	LS
fo	MAX	25

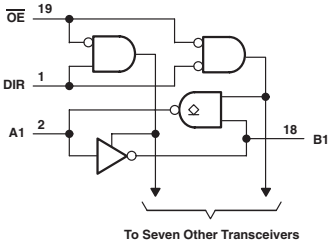
UNIT: MHz

638

OCTAL BUS TRANSCEIVERS

- Bidirectional Bus Tranceivers
- Inverting Logic
- Outputs A-Bus: Open-Collector 3-State
- Schmitt-Triggered Inputs (SN74LS638)

Logic Diagram



FUNCTION TABLE

CONTROL INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	$\overline{B}$ data to A bus
L	H	$\overline{A}$ data to B bus
H	X	Isoration

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	ALS A-1	AS	UNIT
I_{CCZ}	MAX	95	30	30	61	mA
I_{CCL}	MAX	90	41	41	122	mA
I_{OH} (B)	MAX	-15	-15	-15	-15	mA
V_{OH} (A)	MAX	5.5	5.5	5.5	5.5	V
I_{OL}	MAX	24	24	48	64	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	ALS A-1	AS
t_{PLH}	A	B	MAX	10	12	12	7
t_{PHL}				15	12	12	6.5
t_{PLH}	B	A	MAX	25	25	25	20
t_{PHL}				25	30	30	7
t_{PLH}	$\overline{OE}$	A	MAX	40	25	25	19
t_{PHL}				60	45	45	9
t_{PZH}	$\overline{OE}$	B	MAX	40	20	20	8
t_{PZL}				40	22	22	10
t_{PHZ}	$\overline{OE}$	B	MAX	25	10	10	7
t_{PLZ}				25	15	15	10

UNIT: ns

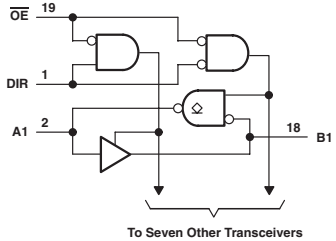
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

639

OCTAL BUS TRANSCEIVERS

- Bidirectional Bus Tranceivers
- True Logic
- Outputs A-Bus: Open-Collector 3-State
- Schmitt-Triggered Inputs (SN74LS638)

Logic Diagram



FUNCTION TABLE

CONTROL INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isoration

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	ALS A-1	AS	UNIT
I_{CCZ}	MAX	95	54	54	100	mA
I_{CCL}	MAX	90	50	50	154	mA
I_{OH} (B)	MAX	-15	-15	-15	-15	mA
V_{OH} (A)	MAX	5.5	5.5	5.5	5.5	V
I_{OL}	MAX	24	24	48	64	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	ALS A-1	AS
t_{PLH}	A	B	MAX	15	12	12	9.5
t_{PHL}				15	12	12	9
t_{PLH}	B	A	MAX	25	30	30	22
t_{PHL}				25	22	22	9
t_{PLH}	$\overline{OE}$	A	MAX	40	30	30	21.5
t_{PHL}				50	35	35	11.5
t_{PZH}	$\overline{OE}$	B	MAX	40	21	21	10.5
t_{PZL}				40	25	25	10.5
t_{PHZ}	$\overline{OE}$	B	MAX	25	10	10	7
t_{PLZ}				25	16	16	10.5

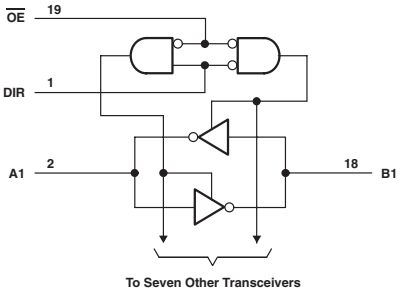
UNIT: ns

640

OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- Bidirectional Bus Tranceivers
- Inverting Logic
- 3-State Outputs
- Schmitt-Triggered Inputs (SN74LS640, 640-1)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram (SN74)



FUNCTION TABLE (SN74)

CONTROL INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	$\overline{B}$ data to A bus
L	H	$\overline{A}$ datato B bus
H	X	Isoration

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	LS-1	ALS	ALS B-1	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	ACT 11	UNIT
I_{CCZ}	MAX	95	95	50	50	80	0.08	0.16	0.08	0.16	11	0.25	0.08	mA
I_{CCL}	MAX	90	90	55	55	123	0.08	0.16	0.08	0.16	94	30	0.08	mA
I_{OH} (A port)	MAX	-15	-15	-15	-15	-15	-6	-6	-6	-6	-3	-32	-24	mA
I_{OH} (B port)	MAX	-15	-15	-15	-15	-15	-6	-6	-6	-6	-15	-32	-24	mA
I_{OL} (A port)	MAX	24	48	24	48	64	6	6	6	6	24	64	24	mA
I_{OL} (B port)	MAX	24	48	24	48	64	6	6	6	6	64	64	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	LS-1	ALS	ALS B-1	AS	SN74 HC	CD74 HC	SN74 HCT
t_{PLH}	A	B	MAX	10	10	11	11	7	26	27	28
t_{PHL}				15	15	10	10	6	26	27	28
t_{PLH}	B	A	MAX	10	10	11	11	7	26	27	28
t_{PHL}				15	15	10	10	6	26	27	28
t_{PZH}	$\overline{OE}$	A	MAX	40	40	21	21	8	58	45	58
t_{PZL}				40	40	24	24	10	58	45	58
t_{PHZ}	$\overline{OE}$	A	MAX	25	25	10	10	8	38	45	50
t_{PLZ}				25	25	15	15	13	38	45	50
t_{PZH}	$\overline{OE}$	B	MAX	40	40	21	21	8	58	45	58
t_{PZL}				40	40	24	24	10	58	45	58
t_{PHZ}	$\overline{OE}$	B	MAX	25	25	10	10	8	38	45	50
t_{PLZ}				25	25	15	15	13	38	45	50

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HCT	SN74 BCT	ABT	ACT 11
t_{PLH}	A	B	MAX	33	6.5	4.9	10.5
t_{PHL}				33	3.7	4.9	9.5
t_{PLH}	B	A	MAX	33	6.5	4.9	10.5
t_{PHL}				33	3.7	4.9	9.5
t_{PZH}	$\overline{OE}$	A	MAX	45	10.2	5.8	13.4
t_{PZL}				45	10.7	7.3	13.6
t_{PHZ}	$\overline{OE}$	A	MAX	45	10.2	6.8	13.9
t_{PLZ}				45	7.8	5.5	14.2
t_{PZH}	$\overline{OE}$	B	MAX	45	10.2	5.8	13.4
t_{PZL}				45	10.7	7.3	13.6
t_{PHZ}	$\overline{OE}$	B	MAX	45	10.2	6.8	13.9
t_{PLZ}				45	7.8	5.5	14.2

UNIT: ns

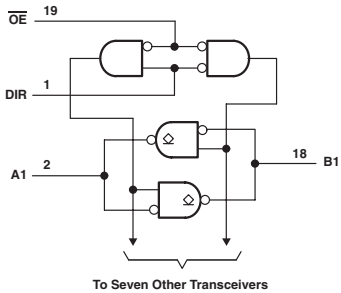
: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

641

OCTAL BUS TRANSCEIVERS

- Bidirectional Bus Tranceivers
- True Logic
- 3-State Outputs
- Schmitt-Triggered Inputs (SN74LS641)

Logic Diagram



FUNCTION TABLE

CONTROL INPUTS		OPERATION
$\overline{G}$	DIR	
L	L	B data to A bus
L	H	A datato B bus
H	X	Isoration

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	LS-1	ALS	ALS A-1	AS	UNIT
I_{CCZ}	MAX	95	95	-	-	-	mA
I_{CCL}	MAX	90	90	47	47	136	mA
V_{OH}	MAX	5.5	5.5	5.5	5.5	5.5	V
I_{OL}	MAX	24	48	24	48	64	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	LS-1	ALS	ALS A-1	AS
t_{PLH}	A	B	MAX	25	25	25	25	21
t_{PHL}				25	25	18	18	7.5
t_{PLH}	B	A	MAX	25	25	25	25	21
t_{PHL}				25	25	18	18	7.5
t_{PLH}	$\overline{OE}$	A,B	MAX	40	40	30	30	21
t_{PHL}				50	50	30	30	9
t_{PLH}	DIR	A,B	MAX	40	40	32	32	22
t_{PHL}				50	50	32	32	10

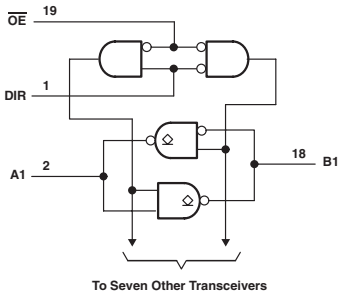
UNIT: ns

642

OCTAL BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

- Bidirectional Bus Tranceivers
- Inverting Logic
- 3-State Outputs
- Schmitt-Triggered Inputs (SN74LS642)

Logic Diagram



FUNCTION TABLE

CONTROL INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	$\overline{B}$ data to A bus
L	H	$\overline{A}$ data to B bus
H	X	Isoration

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	LS-1	ALS	ALS A-1	AS	UNIT
I_{CCZ}	MAX	95	95	-	-	-	mA
I_{CCL}	MAX	90	90	28	28	104	mA
V_{OH}	MAX	5.5	5.5	5.5	5.5	5.5	V
I_{OL}	MAX	24	48	24	48	64	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	LS-1	ALS	ALS A-1	AS
t_{PLH}	A	B	MAX	25	25	30	30	24
t_{PHL}				25	25	22	22	7.5
t_{PLH}	B	A	MAX	25	25	30	30	24
t_{PHL}				25	25	22	22	7.5
t_{PLH}	$\overline{OE}$, DIR	A	MAX	40	40	30	30	23.5
t_{PHL}				60	60	38	38	11.5
t_{PLH}	$\overline{OE}$, DIR	B	MAX	40	40	30	30	23.5
t_{PHL}				60	60	38	38	11.5

UNIT: ns

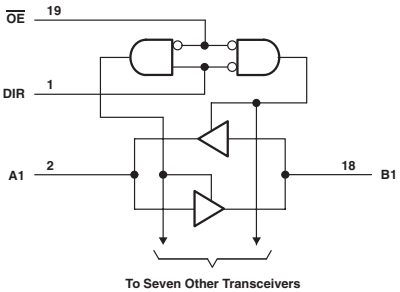
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

645

OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- Bidirectional Bus Tranceivers
- True Logic
- 3-State Outputs
- Schmitt-Triggered Inputs (SN74LS645, 645-1)

Logic Diagram



FUNCTION TABLE

CONTROL INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	$\overline{A}$ data to B bus
H	X	Isoration

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	LS-1	ALS	ALS A-1	AS	SN74 HC	SN74 HCT	UNIT
I_{CCZ}	MAX	95	95	58	58	123	0.08	0.08	mA
I_{CCL}	MAX	90	90	55	55	149	0.08	0.08	mA
I_{OH}	MAX	-15	-15	-15	-15	-15	-6	-6	mA
I_{OL}	MAX	24	48	24	48	64	6	6	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	LS-1	ALS	ALS A-1	AS	SN74 HC	SN74 HCT
t_{PLH}	A	B	MAX	15	15	10	10	9.5	26	28
t_{PHL}				15	15	10	10	9	26	28
t_{PLH}	B	A	MAX	15	15	10	10	9.5	26	28
t_{PHL}				15	15	10	10	9	26	28
t_{PZH}	$\overline{OE}$	A	MAX	40	40	20	20	11	58	58
t_{PZL}				40	40	20	20	10	58	58
t_{PHZ}	$\overline{OE}$	A	MAX	25	25	10	10	7	50	50
t_{PLZ}				25	25	15	15	12	50	50
t_{PZH}	$\overline{OE}$	B	MAX	40	40	20	20	11	58	58
t_{PZL}				40	40	20	20	10	58	58
t_{PHZ}	$\overline{OE}$	B	MAX	25	25	10	10	7	50	50
t_{PLZ}				25	25	15	15	12	50	50

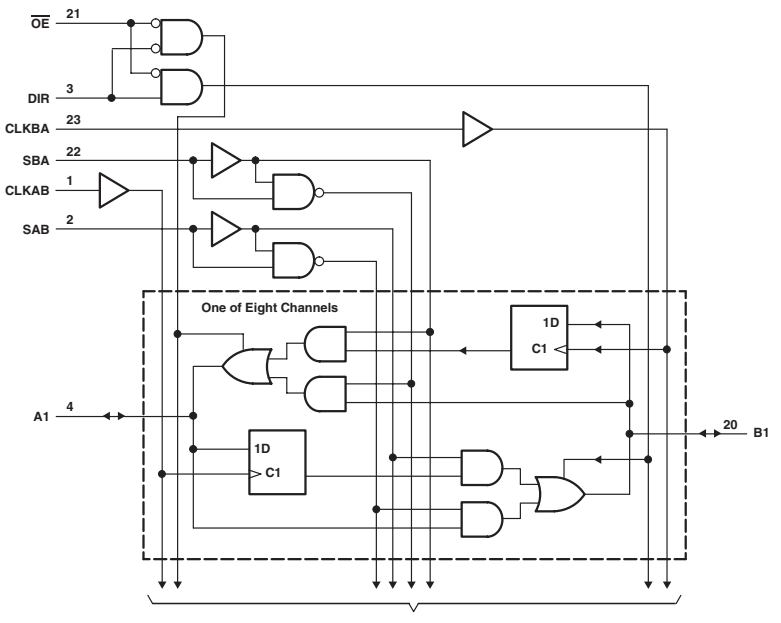
UNIT: ns

646

OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

- Bidirectional Bus Tranceivers
- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- True Data Paths
- 3-State Outputs
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram (SN74)



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	ALS A-1	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	ABT Ver.A	UNIT
I_{CC}	MAX	165	88	88	211	0.08	0.16	0.08	0.16	67	30	30	mA
I_{OH}	MAX	-15	-15	-15	-15	-6	-6	-6	-6	-15	-32	-32	mA
I_{OL}	MAX	24	24	48	48	6	6	6	6	64	64	64	mA

PARAMETER	MAX or MIN	LVTH 3V	AC 11	CD74 AC	ACT 11	CD74 ACT	LVC 3V	UNIT
I_{CC}	MAX	5	0.08	0.08	0.08	0.08	0.01	mA
I_{OH}	MAX	-32	-24	-24	-24	-24	-24	mA
I_{OL}	MAX	64	24	24	24	24	24	mA

: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

FUNCTION TABLE (SN74)

INPUTS						DATA I/O†		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
H	X	H to L	H to L	X	X	Input	Input	Isolation
H	X	↑	↑	X	X	Input	Input	Store A and B data
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H to L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H to L	X	H	X	Input	Output	Stored A data to B bus

† The data output functions can be enabled or disabled by various signals at OE and DIR. Data input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	ALS A-1	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT
f_{max}			MIN	-	40	40	90	27	20	27	17	83
t_w	CLKBA,CLKAB "H"		MIN	15	12.5	12.5	5	19	24	19	38	6
	CLKBA,CLKAB "L"			30	12.5	12.5	6	19	24	19	38	6
	DATA			30	-	-	-	-	-	-	-	-
t_{su}	CLKBA,CLKAB "H"		MIN	15	10	10	6	25	-	25	18	6
	CLKBA,CLKAB "L"			15	10	10	6	25	-	25	18	6
t_h	CLKBA,CLKAB		MIN	0	0	0	0	5	11	5	5	0.5
t_{PLH}	CLOCK	A,B	MAX	25	30	30	8.5	45	66	45	66	11.2
t_{PHL}				35	17	17	9	45	66	45	66	10.6
t_{PLH}	A,B	B,A	MAX	18	20	20	9	34	41	34	56	9.5
t_{PHL}				20	12	12	7	34	41	34	56	10.5
t_{PLH}	SAB,SBA (sored data high)	A,B	MAX	40	25	25	11	48	51	48	69	13.8
t_{PHL}				35	20	20	9	48	51	48	69	9.1
t_{PLH}	SAB,SBA (sored data low)	A,B	MAX	50	35	35	11	48	51	48	69	12
t_{PHL}				25	20	20	9	48	51	48	69	12.9
t_{PZH}	$\overline{OE}$	A,B	MAX	55	17	17	9	61	53	61	68	13.2
t_{PZL}				65	20	20	14	61	53	61	68	14.4
t_{PHZ}	$\overline{OE}$	A,B	MAX	35	10	10	9	61	53	61	53	10.9
t_{PLZ}				35	16	16	9	61	53	61	53	10.5
t_{PZH}	DIR	A,B	MAX	45	30	30	16	61	53	61	-	13.1
t_{PZL}				60	25	25	18	61	53	61	-	14.6
t_{PHZ}	DIR	A,B	MAX	30	10	10	10	61	53	61	-	12.6
t_{PLZ}				30	16	16	10	61	53	61	-	11.8

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ABT Ver.A	LVTH 3V	AC 11	CD74 AC	ACT 11	CD74 ACT	LVC 3V
f_{max}			MIN	125	125	150	100	125	105	110	150
t_w	CLKBA,CLKAB "H"		MIN	4	4	3.3	5	4	4.8	4.5	3.3
	CLKBA,CLKAB "L"			4	4	3.3	5	4	4.8	4.5	3.3
	DATA			-	-	-	-	-	-	-	-
t_{su}	CLKBA,CLKAB "H"		MIN	3.5	3	1.2	4.5	2.5	4.5	2.5	1.5
	CLKBA,CLKAB "L"			3	3	1.6	4.5	2.5	4.5	2.5	1.5
t_h	CLKBA,CLKAB		MIN	0	0	0.8	1	2	2.5	2	1.7
t_{PLH}	CLOCK	A,B	MAX	7.8	5.6	4.7	11	13.5	13.5	15.5	8.4
t_{PHL}				8.4	5.6	4.7	12.2	13.5	14.9	15.5	8.4
t_{PLH}	A,B	B,A	MAX	6.9	4.8	3.5	8.8	11	11.5	12.5	7.4
t_{PHL}				6.9	5.4	3.5	9.8	11	12	12.5	7.4
t_{PLH}	SAB,SBA (sored data high)	A,B	MAX	7.1	6.5	4.9	9.4	12	11.5	14.5	8.6
t_{PHL}				7.9	5.9	4.9	10.7	12	13.5	14.5	8.6
t_{PLH}	SAB,SBA (sored data low)	A,B	MAX	7.1	6.5	4.9	9.9	12	12.4	14.5	8.6
t_{PHL}				7.9	5.9	4.9	11	12	13.1	14.5	8.6
t_{PZH}	$\overline{OE}$	A,B	MAX	6.3	6.3	5.2	12	13.5	14.4	15.5	8.2
t_{PZL}				8.8	8.8	5.2	13.1	13.5	15.3	15.5	8.2
t_{PHZ}	$\overline{OE}$	A,B	MAX	8.3	5	5.5	8.9	13.5	11.6	15.5	7.5
t_{PLZ}				7.5	4.5	5.5	8.3	13.5	10.6	15.5	7.5
t_{PZH}	DIR	A,B	MAX	6.7	6.7	5.2	12.6	13.5	15.3	15.5	8.3
t_{PZL}				9.5	9.5	5.2	13.7	13.5	16.5	15.5	8.3
t_{PHZ}	DIR	A,B	MAX	7.7	5.7	5.6	8.7	13.5	11.3	15.5	7.9
t_{PLZ}				8.2	6	5.6	8.1	13.5	10.3	15.5	7.9

UNIT fmax : MHz other : ns

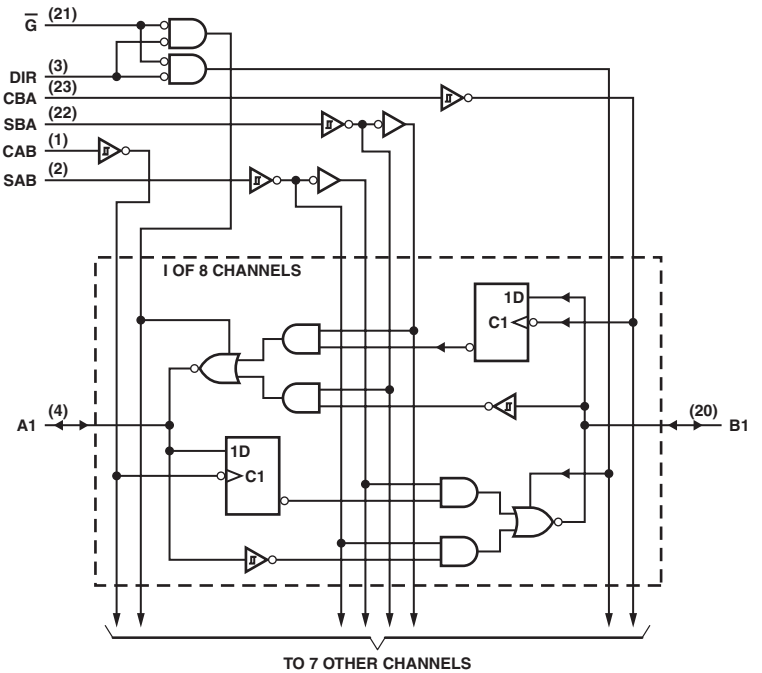
CD74HC: NOT RECOMMENDED FOR NEW DESIGNS

647

OCTAL BUS TRANSCEIVERS AND REGISTERS

- Bidirectional Bus Tranceivers
- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- True Data Paths
- Open-Collector Outputs

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A1–A8	B1–B8	
H	X	H to L	H to L	X	X	Input	Input	Isolation
H	X	↑	↑	X	X	Input	Input	Store A and B data
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H to L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H to L	X	H	X	Input	Output	Stored A data to B bus

† The data output functions can be enabled or disabled by various signals at OE and DIR. Data input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	UNIT
I_{CC}	MAX	150	mA
V_{OH}	MAX	5.5	V
I_{OL}	MAX	24	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
t_w			MIN	30
t_{su}	A,B		MIN	15
t_h	A,B		MIN	0
t_{PLH}	CLOCK	A,B	MAX	35
t_{PHL}				45
t_{PLH}	A,B	B,A	MAX	26
t_{PHL}				27
t_{PLH}	SAB,SBA (With Bus Input High)	A,B	MAX	50
t_{PHL}				45
t_{PLH}	SAB,SBA (With Bus Input Low)	A,B	MAX	60
t_{PHL}				30
t_{PLH}	$\overline{G}$	A,B	MAX	40
t_{PHL}				50
t_{PLH}	DIR	A,B	MAX	35
t_{PHL}				40

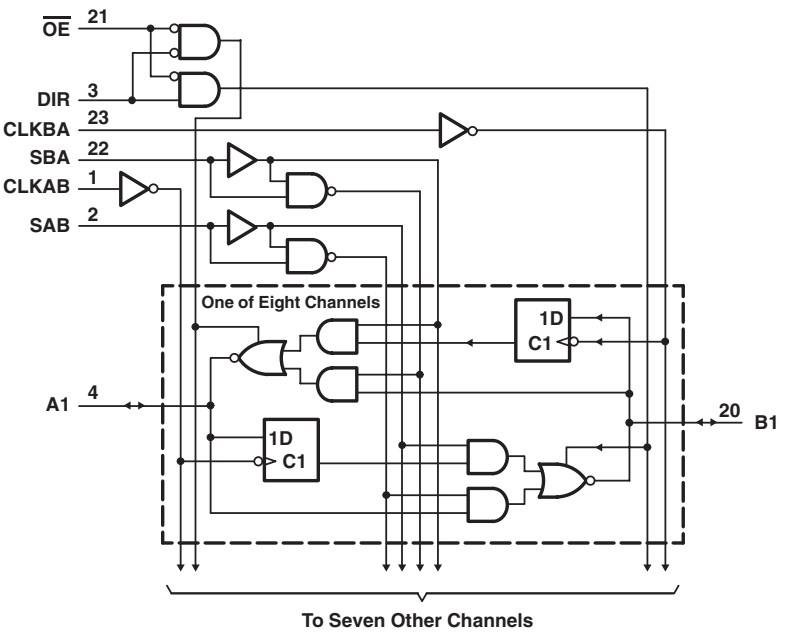
UNIT: ns

648

OCTAL BUS TRANSCEIVERS AND REGISTERS

- Bidirectional Bus Tranceivers
- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- Inverting Data Paths
- 3-State Outputs

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
H	X	H to L	H to L	X	X	Input	Input	Isolation
H	X	↑	↑	X	X	Input	Input	Store A and B data
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H to L	X	H	Output	Input	Stored $\overline{B}$ data to A bus
L	H	X	X	L	X	Input	Output	Real-time $\overline{A}$ data to B bus
L	H	H to L	X	H	X	Input	Output	Stored $\overline{A}$ data to B bus

† The data output functions can be enabled or disabled by various signals at OE and DIR. Data input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	AS	SN74 HC	SN74 HCT	UNIT
I_{CC}	MAX	180	88	195	0.08	0.08	mA
I_{OH}	MAX	-15	-15	-15	-6	-6	mA
I_{OL}	MAX	24	24	48	6	6	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS	SN74 HC	SN74 HCT
f_{max}			MIN	-	40	90	27	27
t_w	CLKAB, CLKBA "H"		MIN	15	12.5	5	19	19
	CLKAB, CLKBA "L"		MIN	30	12.5	6	19	19
	DATA		MIN	30	-	-	-	-
t_{su}	CLKAB, CLKBA		MIN	15	10	6	25	25
t_h	CLKAB, CLKBA		MIN	0	0	0	5	5
t_{PLH}	CLOCK	A,B	MAX	25	33	8.5	45	45
t_{PHL}				40	20	9	45	45
t_{PLH}	A,B	B,A	MAX	18	17	8	34	34
t_{PHL}				25	10	7	34	34
t_{PLH}	SAB,SBA (With Bus Input High)	A,B	MAX	55	25	11	48	48
t_{PHL}				40	21	9	48	48
t_{PLH}	SAB,SBA (With Bus Input Low)	A,B	MAX	40	39	11	48	48
t_{PHL}				40	22	9	48	48
t_{PZH}	$\overline{OE}$	A,B	MAX	50	22	9	61	61
t_{PZL}				55	22	15	61	61
t_{PHZ}	$\overline{OE}$	A,B	MAX	45	10	9	61	61
t_{PLZ}				35	15	9	61	61
t_{PZH}	DIR	A,B	MAX	40	27	16	61	61
t_{PZL}				45	19	18	61	61
t_{PHZ}	DIR	A,B	MAX	35	14	10	61	61
t_{PLZ}				30	15	10	61	61

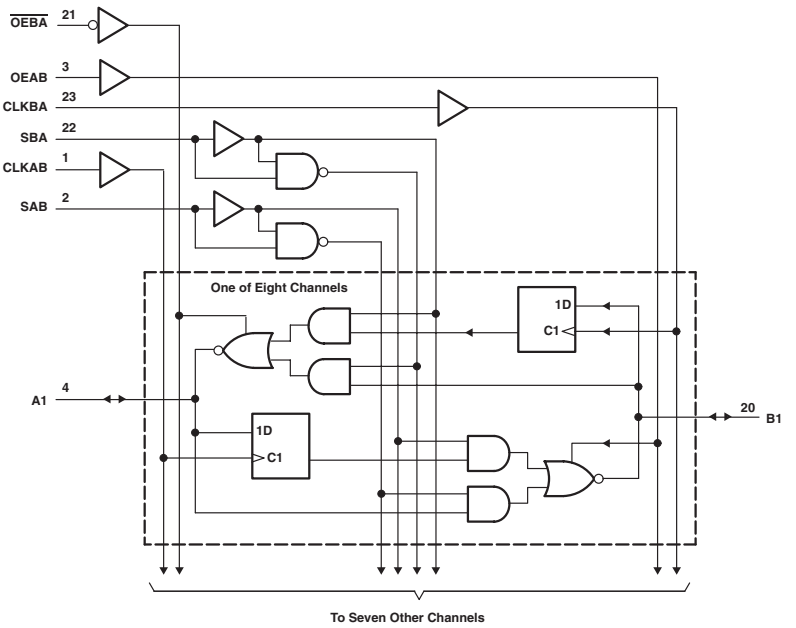
UNIT fmax : MHz other : ns

651

OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

- Bus Tranceivers / Registers
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- Inverting Data Paths
- 3-State Outputs

Logic Diagram (SN74)



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE (SN74)

INPUTS						DATA I/O		OPERATION OR FUNCTION
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
L	H	H to L	H to L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H to L	X	X	Input	Unspecified	Store A, hold B
H	H	↑	↑	X	X	Input	Output	Store A in both registers
L	X	H to L	↑	X	X	Unspecified	Input	Hold A, store B
L	L	↑	↑	X	X	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time $\overline{B}$ data to A bus
L	L	X	H to L	X	H	Output	Input	Stored $\overline{B}$ data to A bus
H	H	X	X	L	X	Input	Output	Real-time $\overline{A}$ data to B bus
H	H	H to L	X	H	X	Input	Output	Stored $\overline{A}$ data to B bus
H	L	H to L	H to L	H	H	Output	Output	Stored $\overline{A}$ data to B bus and stored $\overline{B}$ data to A bus

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	ALS A-1	AS	SN74 HC	SN74 HCT	SN74 BCT	ABT	CD74 ACT	UNIT
I_{CC}	MAX	165	82	82	195	0.08	0.08	62	30	160	mA
I_{OH}	MAX	-15	-15	-15	-15	-6	-6	-15	-32	-24	mA
I_{OL}	MAX	24	24	48	48	6	6	64	64	24	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	ALS A-1	AS	SN74 HC	SN74 HCT	SN74 BCT	ABT	CD74 ACT
f_{max}			MIN	-	40	40	90	27	20	85	125	110
t_w	CLKBA, CLKAB "H"		MIN	15	12.5	12.5	5	19	25	4.8	4	4.5
	CLKBA, CLKAB "L"		MIN	15	12.5	12.5	6	19	25	7	4	4.5
	DATA		MIN	15	-	-	-	-	-	-	-	-
t_{su}	A,B		MIN	15	10	10	6	25	19	6	3	2.5
t_h	A,B		MIN	0	0	0	0	5	5	1	0	2
t_{PLH}	CLOCK	A,B	MAX	24	32	32	8.5	45	45	11.7	5.6	15.5
t_{PHL}				35	17	17	9	45	45	11.8	5.6	15.5
t_{PLH}	A,B	B,A	MAX	18	18	18	9	34	34	12.6	6.2	12.5
t_{PHL}				30	10	10	7	34	34	9.8	5.4	12.5
t_{PLH}	SAB,SBA (With Bus Input High)	A,B	MAX	47	38	38	11	48	48	9.8	6.5	15.5
t_{PHL}				33	21	21	9	48	48	15.5	5.9	15.5
t_{PLH}	SAB,SBA (With Bus Input Low)	A,B	MAX	35	25	25	11	48	48	14.6	6.5	15.5
t_{PHL}				30	21	21	9	48	48	12.8	5.9	15.5
t_{PZH}	$\overline{OEBA}$	A	MAX	44	20	20	10	61	61	12	5.8	15.5
t_{PZL}				60	18	18	16	61	61	13.1	8.5	15.5
t_{PHZ}	$\overline{OEBA}$	A	MAX	38	9	9	9	61	61	10.2	5	15.5
t_{PLZ}				30	12	12	9	61	61	9.6	4.1	15.5
t_{PZH}	OEAB	B	MAX	29	22	22	11	61	61	8.3	6.5	15.5
t_{PZL}				40	21	21	16	61	61	9.7	7.4	15.5
t_{PHZ}	OEAB	B	MAX	38	12	12	10	61	61	15	5.5	15.5
t_{PLZ}				30	14	14	11	61	61	12.3	5.1	15.5

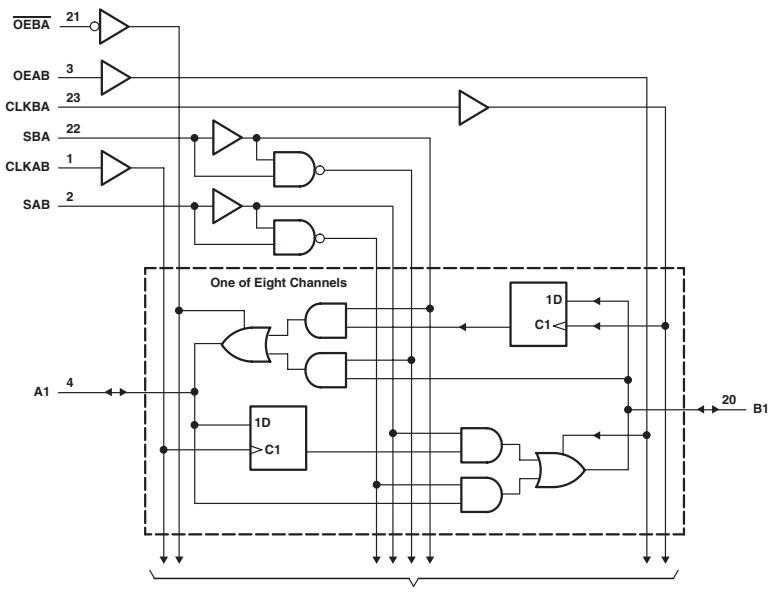
UNIT fmax : MHz other : ns

652

OCTAL BUS TRANSCEIVERS AND REGISTERS

- Bus Tranceivers / Registers
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- True Data Paths
- 3-State Outputs
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram (SN74)



FUNCTION TABLE (SN74)

INPUTS						DATA I/O		OPERATION OR FUNCTION
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
L	H	H to L	H to L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H to L	X	X	Input	Unspecified	Store A, hold B
H	H	↑	↑	X	X	Input	Output	Store A in both registers
L	X	H to L	↑	X	X	Unspecified	Input	Hold A, store B
L	L	↑	↑	X	X	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time $\overline{B}$ data to A bus
L	L	X	H to L	X	H	Output	Input	Stored $\overline{B}$ data to A bus
H	H	X	X	L	X	Input	Output	Real-time $\overline{A}$ data to B bus
H	H	H to L	X	H	X	Input	Output	Stored $\overline{A}$ data to B bus
H	L	H to L	H to L	H	H	Output	Output	Stored $\overline{A}$ data to B bus and stored $\overline{B}$ data to A bus

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	ALS A-1	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	UNIT
I_{CC}	MAX	180	88	88	211	0.08	0.16	0.08	0.16	69	30	mA
I_{OH}	MAX	-15	-15	-15	-15	-6	-6	-6	-6	-15	-32	mA
I_{OL}	MAX	24	24	48	48	6	6	6	6	64	64	mA

PARAMETER	MAX or MIN	ABT Ver.A	LVTH 3V	AC 11	CD74 AC	ACT 11	CD74 ACT	LVC 3V	UNIT
I_{CC}	MAX	30	5	0.08	0.16	0.08	0.16	0.01	mA
I_{OH}	MAX	-32	-32	-24	-24	-24	-24	-24	mA
I_{OL}	MAX	64	64	24	24	24	24	24	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	ALS A-1	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT
f_{max}			MIN	-	40	40	90	27	20	20	17	77
t_w	CLKBA, CLKAB "H"		MIN	15	12.5	12.5	5	19	24	25	38	6.5
	CLKBA, CLKAB "L"		MIN	15	12.5	12.5	6	19	24	25	38	6.5
	DATA		MIN	15	-	-	-	-	-	-	-	-
t_{su}	A,B High		MIN	15	10	10	6	25	18	19	18	5
	A,B Low		MIN	15	10	10	6	25	18	19	18	5
t_h	A,B		MIN	0	0	0	0	5	11	5	5	1
t_{PLH}	CLOCK	A,B	MAX	25	30	30	8.5	45	66	45	66	10.5
t_{PHL}				36	17	17	9	45	66	45	66	9.9
t_{PLH}	A,B	B,A	MAX	18	18	18	9	34	41	34	56	8.9
t_{PHL}				20	12	12	7	34	41	34	56	9.8
t_{PLH}	SAB,SBA (With Bus Input High)	A,B	MAX	35	35	35	11	48	51	48	69	13.1
t_{PHL}				32	20	20	9	48	51	48	69	8.5
t_{PLH}	SAB,SBA (With Bus Input Low)	A,B	MAX	50	25	25	11	48	51	48	69	11.3
t_{PHL}				23	20	20	9	48	51	48	69	12.5
t_{PZH}	$\overline{OEBA}$	A	MAX	45	17	17	10	61	53	61	68	10.6
t_{PZL}				54	18	18	16	61	53	61	68	12
t_{PHZ}	$\overline{OEBA}$	A	MAX	38	10	10	9	61	53	61	53	10
t_{PLZ}				30	16	16	9	61	53	61	53	9.5
t_{PZH}	OEAB	B	MAX	30	22	22	11	61	53	61	68	8.1
t_{PZL}				38	18	18	16	61	53	61	68	9.3
t_{PHZ}	OEAB	B	MAX	38	10	10	10	61	53	61	53	11.6
t_{PLZ}				30	16	16	11	61	53	61	53	11.3

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ABT Ver.A	LVTH 3V	AC 11	CD74 AC	ACT 11	CD74 ACT	LVC 3V
f_{max}			MIN	125	125	150	105	125	105	110	100
t_w	CLKBA, CLKAB "H"		MIN	4	4	3.3	4.8	4	4.8	4.5	3.3
	CLKBA, CLKAB "L"		MIN	4	4	3.3	4.8	4	4.8	4.5	3.3
	DATA		MIN	-	-	-	-	-	-	-	-
t_{su}	A,B High		MIN	3.5	3	1.2	4.5	2.5	4	2.5	1.9
	A,B Low		MIN	3.5	3	1.6	4.5	2.5	4	2.5	1.9
t_h	A,B		MIN	0	0	0.8	1	2	2.5	2	1.7
t_{PLH}	CLOCK	A,B	MAX	7.8	5.6	4.7	10.7	13.5	13.1	15.5	8
t_{PHL}				8.4	5.6	4.7	12	13.5	14.4	15.5	8
t_{PLH}	A,B	B,A	MAX	6.7	4.8	3.5	8.6	11	11.1	12.5	7.4
t_{PHL}				6.7	5.4	3.5	9.6	11	11.6	12.5	7.4
t_{PLH}	SAB,SBA (With Bus Input High)	A,B	MAX	6.9	6.5	4.9	9.1	12	11	14.5	8.7
t_{PHL}				7.7	5.9	4.9	10.7	12	13.3	14.5	8.7
t_{PLH}	SAB,SBA (With Bus Input Low)	A,B	MAX	6.9	6.5	4.9	9.9	12	12.2	14.5	8.7
t_{PHL}				7.7	5.9	4.9	10.9	12	12.6	14.5	8.7
t_{PZH}	$\overline{OEBA}$	A	MAX	5.8	5.8	5.2	10.9	13.5	12.6	15.5	7.4
t_{PZL}				8.5	8.5	5.2	12.2	13.5	13.8	15.5	7.4
t_{PHZ}	$\overline{OEBA}$	A	MAX	8.2	5	5.5	7.6	13.5	9.9	15.5	7.5
t_{PLZ}				6.8	4.1	5.5	7.1	13.5	9.3	15.5	7.5
t_{PZH}	OEAB	B	MAX	6.5	6.5	4.7	11.3	13.5	15.2	15.5	7.1
t_{PZL}				7.4	7.4	4.7	12.3	13.5	16.1	15.5	7.1
t_{PHZ}	OEAB	B	MAX	6.9	5.5	5.6	7.6	13.5	10.3	15.5	7.4
t_{PLZ}				6.2	5.1	5.6	7.2	13.5	9.3	15.5	7.4

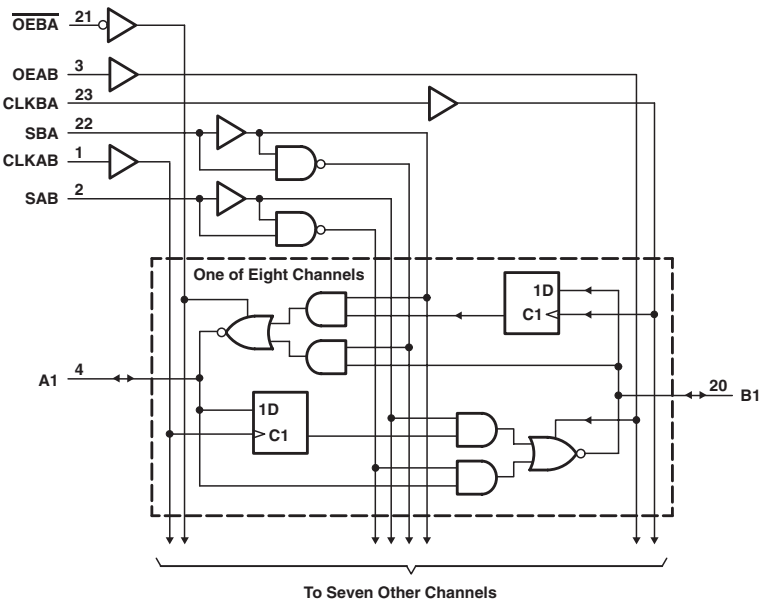
UNIT fmax : MHz other : ns

653

OCTAL BUS TRANSCEIVERS AND REGISTERS

- Bus Tranceivers / Registers
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- Inverting Data Paths
- Outputs
  - A Bus: Open-Collector
  - B Bus: 3-State

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
L	H	H or L	H or L	X	X	Inpu	Input	Isolation Store A and B data
L	H	↑	↑	X	X			
X	H	↑	H or L	X	X	Input	Unspecified‡	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified‡	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time $\overline{B}$ data to A bus Stored $\overline{B}$ data to A bus
L	L	X	H or L	X	H			
H	H	X	X	L	X	Input	Output	Real-time $\overline{A}$ data to B bus Stored $\overline{A}$ data to B bus
H	H	H or L	X	H	X			
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ data to B bus and stored $\overline{B}$ data to A bus

NOTES:
† The data output functions can be enabled or dissabled by a variety of level combinations at GAB or $\overline{G}$BA. Data input functions always are enabled; i.e., data at the bus teminals is storedd on evry low-to-high transition on the clock inputs.
‡ Select control = L: clocks can occur simultaneously.
Select control = H: clock must be staggered to load both registers.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	UNIT
I_{CC}	MAX	165	88	mA
I_{OH}	MAX	-15	-15	mA
I_{OL}	MAX	24	24	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS
t_w	CLK "H"		MIN	15	14.5
	CLK "L"		MIN	30	14.5
	DATA		MIN	30	-
t_{su}	A, B		MIN	15	10
t_h	A, B		MIN	0	0
t_{PLH}	CLKBA	A	MAX	38	64
t_{PHL}				39	22
t_{PLH}	CLKAB	B	MAX	23	30
t_{PHL}				36	17
t_{PLH}	A	B	MAX	18	18
t_{PHL}				30	15
t_{PLH}	B	A	MAX	32	56
t_{PHL}				24	15
t_{PLH}	SBA (B "H")	A	MAX	57	62
t_{PHL}				39	25
t_{PLH}	SBA (B "L")	A	MAX	51	62
t_{PHL}				35	25
t_{PLH}	SAB (A "H")	B	MAX	48	35
t_{PHL}				33	22
t_{PLH}	SAB (A "L")	B	MAX	36	25
t_{PHL}				30	22
t_{PLH}	$\overline{OEBA}$	A	MAX	35	30
t_{PHL}				55	24
t_{PZH}	OEAB	B	MAX	29	22
t_{PZL}				38	22
t_{PHZ}	OEAB	B	MAX	39	14
t_{PLZ}				29	16

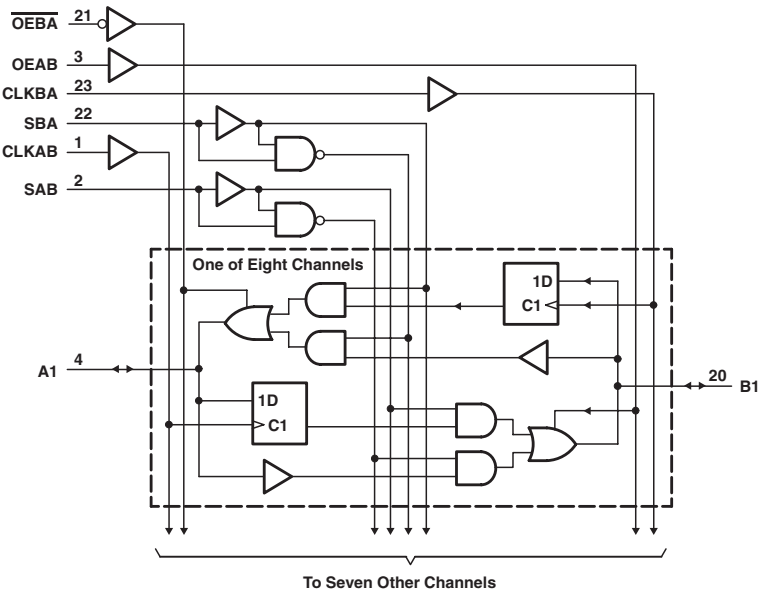
UNIT:ns

654

OCTAL BUS TRANSCEIVERS AND REGISTERS

- Bus Tranceivers / Registers
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- True Data Paths
- Outputs
  - A Bus: Open-Collector
  - B Bus: 3-State

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
L	H	H to L	H to L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H to L	X	X	Input	Unspecified	Store A, hold B
H	H	↑	↑	X	X	Input	Output	Store A in both registers
L	X	H to L	↑	X	X	Unspecified	Input	Hold A, store B
L	L	↑	↑	X	X	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time $\overline{B}$ data to A bus
L	L	X	H to L	X	H	Output	Input	Stored $\overline{B}$ data to A bus
H	H	X	X	L	X	Input	Output	Real-time $\overline{A}$ data to B bus
H	H	H to L	X	H	X	Input	Output	Stored $\overline{A}$ data to B bus
H	L	H to L	H to L	H	H	Output	Output	Stored $\overline{A}$ data to B bus and stored $\overline{B}$ data to A bus

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	UNIT
I_{CC}	MAX	180	88	mA
I_{OH}	MAX	-15	-15	mA
I_{OL}	MAX	24	24	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS
t_w	CLKBA, CLKAB "H"		MIN	15	14.5
	CLKBA, CLKAB "L"		MIN	30	14.5
	DATA		MIN	30	-
t_{su}	A,B		MIN	15	10
t_h	A,B		MIN	0	0
t_{PLH}	CLKBA	A	MAX	33	64
t_{PHL}				36	22
t_{PLH}	CLKAB	B	MAX	21	30
t_{PHL}				33	17
t_{PLH}	A	B	MAX	18	18
t_{PHL}				30	15
t_{PLH}	B	A	MAX	27	56
t_{PHL}				21	21
t_{PLH}	SBA (B "H")	A	MAX	48	62
t_{PHL}				32	25
t_{PLH}	SBA (B "L")	A	MAX	54	62
t_{PHL}				29	25
t_{PLH}	SAB (A "H")	B	MAX	35	25
t_{PHL}				27	22
t_{PLH}	SAB (A "L")	B	MAX	45	35
t_{PHL}				21	22
t_{PLH}	$\overline{OEBA}$	A	MAX	35	30
t_{PHL}				53	24
t_{PZH}	OEAB	B	MAX	29	22
t_{PZL}				33	22
t_{PHZ}	OEAB	B	MAX	39	14
t_{PLZ}				29	16

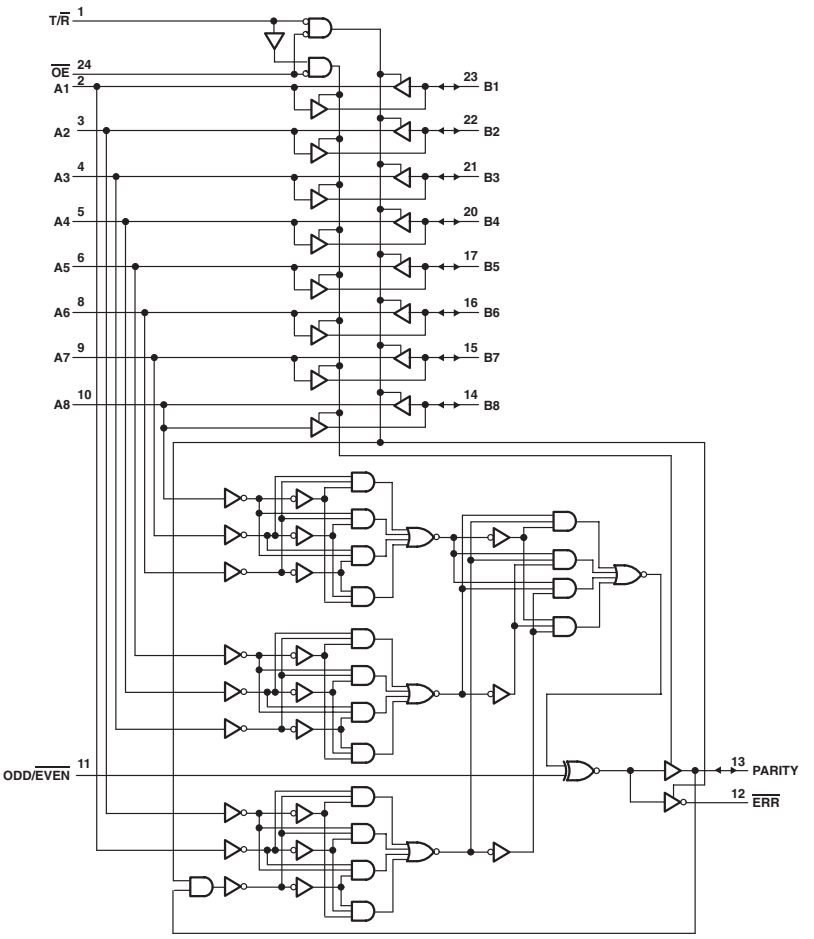
UNIT: ns

657

OCTAL BUS TRANSCEIVERS WITH PARITY GENERATORS/CHECKERS AND 3-STATE OUTPUTS

- Combines SN74F245 and SN74F280B Functions in One Package
- 3-State Outputs
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	F	SN74 BCT	ABT	ACT 11	UNIT
I_{CCH}	MAX	125	2	0.25	0.08	mA
I_{CCL}	MAX	150	90	40	0.08	mA
I_{CCZ}	MAX	145	1	0.25	0.08	mA
I_{OH} A1-A9	MAX	-3	-3	-32	-24	mA
I_{OH} B1-B9, PARITY, $\overline{ERR}$	MAX	-12	-15	-32	-24	mA
I_{OL} A1-A8	MAX	24	24	64	24	mA
I_{OL} B1-B8, PARITY, $\overline{ERR}$	MAX	64	64	64	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	F	SN74 BCT	ABT	ACT 11
t_{PLH}	A,B	B,A	MAX	8	6.6	4.6	9.4
t_{PHL}			MAX	8	9	4.3	9.4
t_{PLH}	A	PARITY	MAX	16	15.4	8.1	14.4
t_{PHL}			MAX	16	15.9	7.7	15
t_{PLH}	ODD/$\overline{EVEN}$	PARITY, $\overline{ERR}$	MAX	12	7.1	4.9	10.7
t_{PHL}			MAX	12.5	9	4.9	11.3
t_{PLH}	B	$\overline{ERR}$	MAX	22.5	15.3	7.9	23.6
t_{PHL}			MAX	22.5	15.5	7.8	24.6
t_{PLH}	PARITY	$\overline{ERR}$	MAX	16.5	13.2	7.7	14.6
t_{PHL}			MAX	17	13.9	7.5	14.7
t_{PZH}	$\overline{OE}$	A, B, PARITY	MAX	9	9.1	6.5	12.1
t_{PZL}			MAX	11	16.3	6.5	13.8
t_{PZH}	$\overline{OE}$	$\overline{ERR}$	MAX	9	9.1	6.6	12.1
t_{PZL}			MAX	11	16.3	9.2	13.8
t_{PHZ}	$\overline{OE}$	A, B, PARITY, ERR	MAX	8	9.1	6.2	12.1
t_{PLZ}			MAX	6.5	8	7.8	11.6

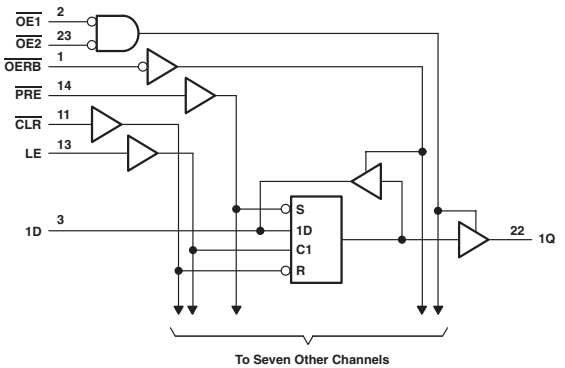
UNIT: ns

666

8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES WITH 3-STATE OUTPUTS

- 3-State I/O-Type Read-Back Inputs
- True Outputs
- Bus-Structured Pinout

Logic Diagram



ELECTRICAL CHARACTERISTICS AND
RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	ALS	UNIT
I_{CC}		MAX	73	mA
I_{OH}	Q	MAX	-2.6	mA
	D	MAX	-0.4	mA
I_{OL}	Q	MAX	24	mA
	D	MAX	8	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	ALS
t_w	LE "H"			MIN	10
	$\overline{CLR}$ "L"			MIN	10
	$\overline{PRE}$ "L"			MIN	10
t_{su}	DATA (LE)			MIN	10
	DATA ($\overline{OERB}$)			MIN	10
t_h	DATA (LE)			MIN	5
t_{PLH}		D	Q	MAX	14
t_{PHL}					18
t_{PLH}		LE	Q	MAX	21
t_{PHL}					27
t_{PHL}		$\overline{CLR}$	Q	MAX	29
			D		32
t_{PLH}		$\overline{PRE}$	Q	MAX	22
t_{PHL}			D		28
t_{en}		$\overline{OERB}$	D	MAX	21
t_{dis}					14
t_{en}		$\overline{OE1}$, $\overline{OE2}$	Q	MAX	21
t_{dis}					14

UNIT: ns

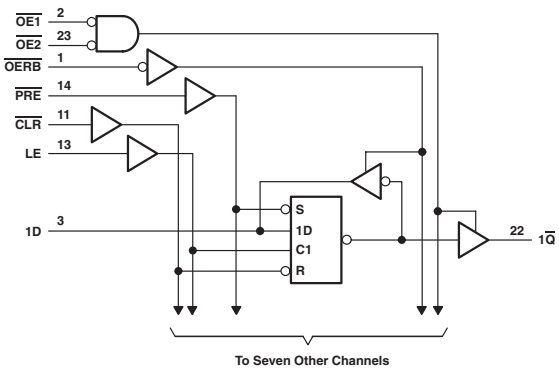
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

667

8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES WITH 3-STATE OUTPUTS

- 3-State I/O-Type Read-Back Inputs
- Inverted Outputs
- Bus-Structured Pinout

Logic Diagram



ELECTRICAL CHARACTERISTICS AND
RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	ALS	UNIT
I_{CC}		MAX	79	mA
I_{OH}	Q	MAX	-2.6	mA
	D	MAX	-0.4	mA
I_{OL}	Q	MAX	24	mA
	D	MAX	8	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	ALS
t_w	LE "H"			MIN	10
	$\overline{CLR}$ "L"			MIN	10
	$\overline{PRE}$ "L"			MIN	10
t_{su}	DATA (LE)			MIN	10
	DATA ($\overline{OERB}$)			MIN	10
t_h	DATA (LE)			MIN	5
t_{PLH}		D	$\overline{Q}$	MAX	20
t_{PHL}					15
t_{PLH}		LE	$\overline{Q}$	MAX	28
t_{PHL}					22
t_{PHL}		$\overline{CLR}$	$\overline{Q}$	MAX	24
			D		26
t_{PLH}		$\overline{PRE}$	$\overline{Q}$	MAX	25
t_{PHL}			D		28
t_{en}		$\overline{OERB}$	D	MAX	21
t_{dis}					14
t_{en}		$\overline{OE1}$, $\overline{OE2}$	$\overline{Q}$	MAX	21
t_{dis}					14

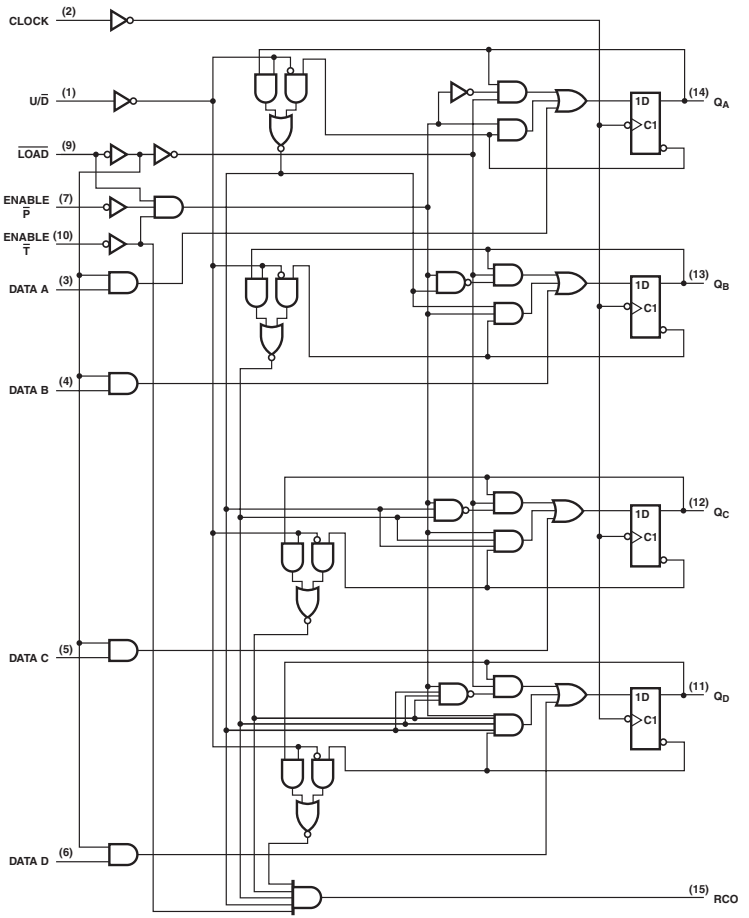
UNIT: ns

669

SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

- Fully Synchronous Operation for Counting and Programming
- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	UNIT
I_{CC}	MAX	34	mA
I_{OH}	MAX	-0.4	mA
I_{OL}	MAX	8	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	LS
f_{max}				MIN	25
t_w				MIN	20
t_{su}	A,B,C,D			MIN	25
	$\overline{ENP}$, $\overline{ENT}$			MIN	40
	$\overline{LOAD}$			MIN	30
	U/$\overline{D}$			MIN	45
t_h				MIN	0
t_{PLH}		CLOCK	$\overline{RCO}$	MAX	40
t_{PHL}					60
t_{PLH}		CLOCK	Q	MAX	27
t_{PHL}					27
t_{PLH}		$\overline{ENT}$	$\overline{RCO}$	MAX	17
t_{PHL}					45
t_{PLH}		U/$\overline{D}$	$\overline{RCO}$	MAX	35
t_{PHL}					40

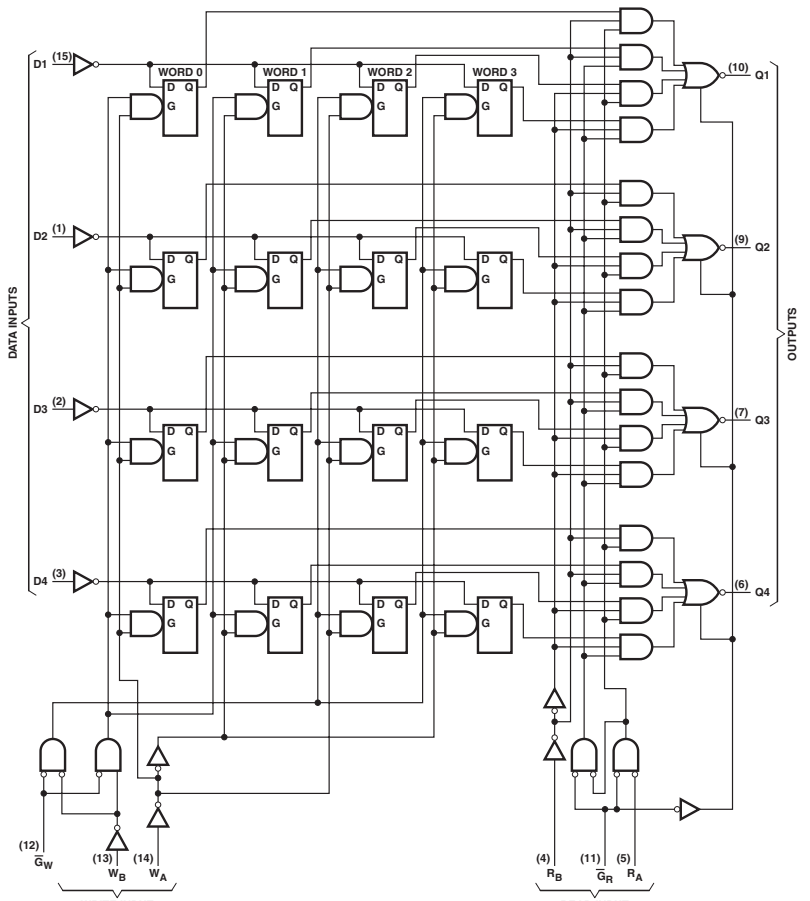
UNIT fmax : MHz other : ns

670

4-BY-4 REGISTER FILES WITH 3-STATE OUTPUTS

- Separate Read / Write Addressing Permits Simultaneous Reading and Writing
- Organized as 4 Words of 4 Bits
- Expandable to 512 Words of n-Bits
- 3-State Outputs

Logic Diagram (SN74LS)



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE (SN74)

WRITE INPUTS			WORD			
W_B	W_A	$\overline{G}_W$	0	1	2	3
L	L	L	Q = D	Q_0	Q_0	Q_0
L	H	L	Q_0	Q = D	Q_0	Q_0
H	L	L	Q_0	Q_0	Q = D	Q_0
H	H	L	Q_0	Q_0	Q_0	Q = D
X	X	H	Q_0	Q_0	Q_0	Q_0

READ INPUTS			OUTPUTS			
R_B	R_A	$\overline{G}_R$	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	Z	Z	Z	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	50	0.16	0.16	mA
I_{OH}	MAX	-2.6	-6	-6	mA
I_{OL}	MAX	8	6	6	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	CD74 HC	CD74 HCT
t_w	Width of write-enable or read-enable pulse		MIN	25	24	30
t_{su}	Data input with respect to write enable		MIN	10	18	18
	Write select with respect to write enable			15	18	27
t_h	Data input with respect to write enable		MIN	15	5	5
	Write select with respect to write enable			5	5	5
t_{latch}			MIN	25	30	38
t_{PLH}	Read Select	Q	MAX	40	59	53
t_{PHL}				45	59	53
t_{PLH}	Write Enable	Q	MAX	45	75	75
t_{PHL}				50	75	75
t_{PLH}	Data	Q	MAX	45	75	75
t_{PHL}				40	75	75
t_{PZH}	Read Enable	Q	MAX	35	45	57
t_{PZL}				40	45	57
t_{PHZ}	Read Disable	Q	MAX	50	45	53
t_{PLZ}				35	45	53

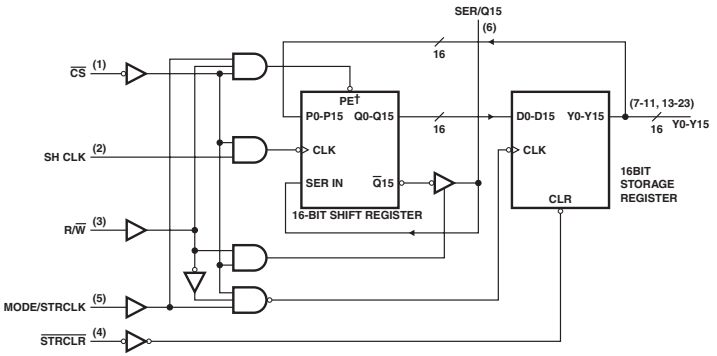
UNIT : ns

673

16-BIT SHIFT REGISTERS

- 16-Bit Serial-In, Serial-Out Shift Register with 16-Bit Parallel-Out Storage Register
- Performs Serial-to-Parallel Conversion

Logic Diagram



† When PE is active, data synchronously parallel loaded into the shift registers form the 16 P inputs and no shifting takes place.

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS					SER/ Q15	SHIFT REGISTER FUNCTIONS				STORAGE REGISTER FUNCTIONS	
$\overline{CS}$	R/$\overline{W}$	SH CLK	$\overline{STRCLR}$	MODE/ STRCLK		SHIFT	READ FROM SERIAL INPUT	WRITE INTO SERIAL INPUT	PARALLEL LOAD	CLEAR	LOAD
H	X	X	X	X	Z	NO	NO	NO	NO		NO
X	X	X	L	X						YES	
L	L	↓	X	X	Z	YES	NO	YES	NO		
L	H	X	X	X	Q15		YES	NO			NO
L	H	↓	X	L	Q14n	YES	YES	NO	NO		NO
L	H	↓	L	X	L	NO	YES		YES	YES;	NO
L	H	↓	H	X	Y15n	NO	YES		YES	NO	NO
L	L	X	H	↑	Z		NO			NO	YES

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	UNIT
I_{CC}		MAX	80	mA
I_{OH}	SER/Q15	MAX	-2.6	mA
	Y0-Y15	MAX	-0.4	mA
I_{OL}	SER/Q15	MAX	24	mA
	Y0-Y15	MAX	8	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	LS
f_{max}				MIN	20
t_w	CLK			MIN	20
	CLR			MIN	20
t_{su}	SER/Q15			MIN	20
	Y0-Y15			MIN	20
	Mode			MIN	35
	R/$\overline{W}$,$\overline{CS}$			MIN	35
t_h	SER/Q15			MIN	0
	Y0-Y15			MIN	0
	Mode			MIN	0
t_{PLH}		$\overline{STRCLR}$	Y0-Y15	MAX	40
t_{PLH}		MODE/ STRCLK	Y0-Y15	MAX	45
t_{PHL}					45
t_{PLH}		SH CLK	SER/Q15	MAX	33
t_{PHL}					40

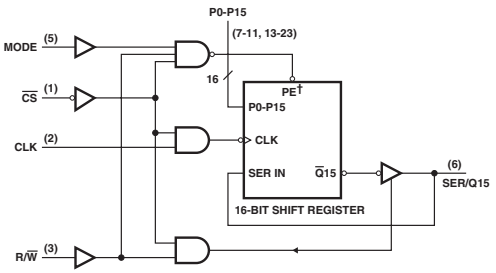
UNIT fmax : MHz other : ns

674

16-BIT SHIFT REGISTERS

- 16-Bit Parallel-In, Serial-Out Shift Register
- Performs Parallel-to-Serial Conversion

Logic Diagram



† When PE is active, data synchronously parallel loaded into the shift registers form the 16 P inputs and no shifting takes place.

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS				SER/ Q15	OPERATION
$\overline{CS}$	R/$\overline{W}$	MODE	CLK		
H	X	X	X	Z	Do nothing
L	L	X	↓	Z	Shift and write (serial load)
L	H	L	↓	Q14n	Shift and read
L	H	H	↓	P15	parallel load

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	UNIT
I_{CC}		MAX	40	mA
I_{OH}	SER/Q15	MAX	-2.6	mA
	P0-P15	MAX	-0.4	mA
I_{OL}	SER/Q15	MAX	24	mA
	P0-P15	MAX	8	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	LS
f_{max}				MIN	20
t_w	CLK			MIN	20
	CLR				20
t_{su}	SER/Q15			MIN	20
	P0-P15				20
	Mode				35
	R/$\overline{W}$,$\overline{CS}$				35
t_h	SER/Q15			MIN	0
	P0-P15				0
	Mode				0
t_{PLH}		CLK	SER/Q15	MAX	33
t_{PHL}					40
t_{PZH}		$\overline{CS}$, R/$\overline{W}$	SER/Q15	MAX	45
t_{PZL}					45
t_{PHZ}		$\overline{CS}$, R/$\overline{W}$	SER/Q15	MAX	40
t_{PLZ}					40

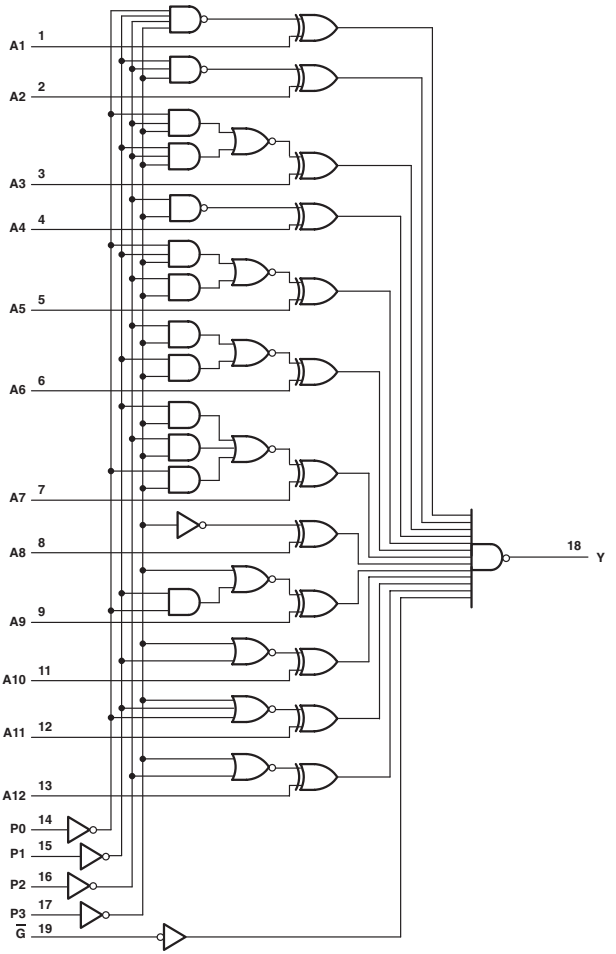
UNIT fmax : MHz other : ns

679

12-BIT ADDRESS COMPARATOR

● 12-Bit Address Comparator with Enable

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

$\overline{G}$	INPUTS																OUTPUT
	P3	P2	P1	P0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	Y
L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L
L	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	L
L	L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	H	L
L	L	H	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L
L	L	H	L	H	L	L	L	L	L	H	H	H	H	H	H	H	L
L	L	H	H	L	L	L	L	L	L	L	H	H	H	H	H	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H	H	H	H	H	L
L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	L
L	H	L	L	H	L	L	L	L	L	L	L	L	L	H	H	H	L
L	H	L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	L
L	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	L
L	H	H	L	L	L	L	L	L	L	L	L	L	H	H	H	L	L
L	H	H	L	H	L	L	L	L	L	L	L	L	L	H	H	L	L
L	H	H	H	L	L	L	L	L	L	L	L	L	L	L	H	L	L
L	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L
L	All other combinations																H
H	Any combination																H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	SN74 HC	UNIT
I_{CC}	MAX	28	0.08	mA
I_{OH}	MAX	-2.6	-4	mA
I_{OL}	MAX	24	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	SN74 HC
t_{PLH}	Any P	Y	MAX	25	375
t_{PHL}				35	375
t_{PLH}	Any A	Y	MAX	22	78
t_{PHL}				30	78
t_{PLH}	$\overline{G}$	Y	MAX	13	31
t_{PHL}				25	31

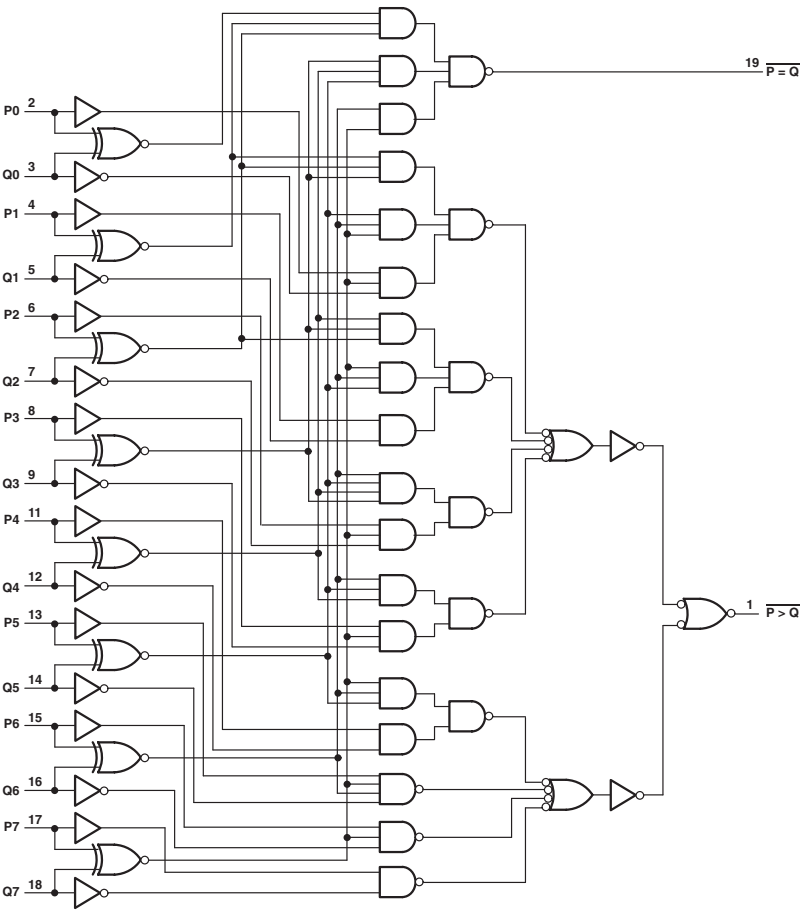
UNIT: ns

682

8-BIT MAGNITUDE COMPARATORS

- Totem-Pole Outputs
- Hysteresis at P and Q Inputs
- 20kΩ Pullup Resistors on the Q Inputs

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

DATA INPUT P, Q	OUTPUTS	
	$\overline{P=Q}$	$\overline{P>Q}$
P=Q	L	H
P>Q	H	L
P<Q	H	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	SN74 HC	UNIT
I_{CC}	MAX	70	0.11	mA
I_{OH}	MAX	-0.4	-4	mA
I_{OL}	MAX	24	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	SN74 HC
t_{PLH}	P	$\overline{P = Q}$	MAX	25	69
t_{PHL}				25	69
t_{PLH}	Q	$\overline{P = Q}$	MAX	25	69
t_{PHL}				25	69
t_{PLH}	P	$\overline{P > Q}$	MAX	30	69
t_{PHL}				30	69
t_{PLH}	Q	$\overline{P > Q}$	MAX	30	69
t_{PHL}				30	69

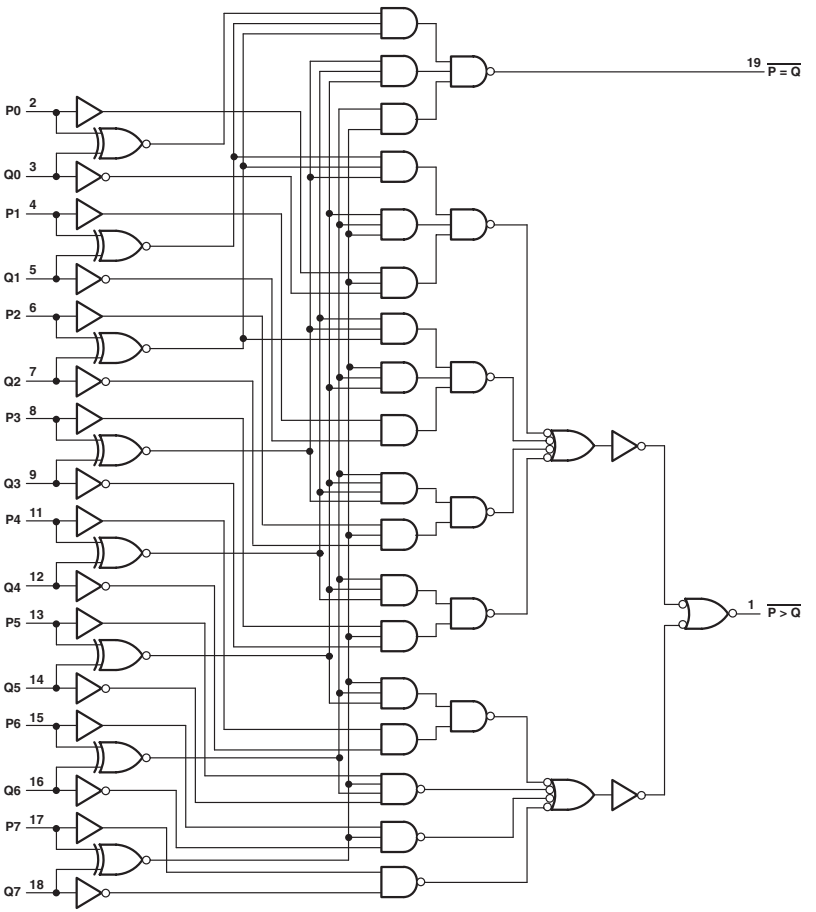
UNIT: ns

684

8-BIT MAGNITUDE COMPARATORS

- Totem-Pole Outputs
- Hysteresis at P and Q Inputs

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

DATA INPUT P, Q	OUTPUTS $\overline{P=Q}$	OUTPUTS $\overline{P>Q}$
$\overline{P=Q}$	L	H
$\overline{P>Q}$	H	L
$\overline{P<Q}$	H	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	SN74 HC	UNIT
I_{CC}	MAX	65	0.08	mA
I_{OH}	MAX	-0.4	-4	mA
I_{OL}	MAX	24	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	SN74 HC
t_{PLH}	P	$\overline{P = Q}$	MAX	25	69
t_{PHL}				25	69
t_{PLH}	Q	$\overline{P = Q}$	MAX	25	69
t_{PHL}				25	69
t_{PLH}	P	$\overline{P > Q}$	MAX	30	69
t_{PHL}				30	69
t_{PLH}	Q	$\overline{P > Q}$	MAX	30	69
t_{PHL}				30	69

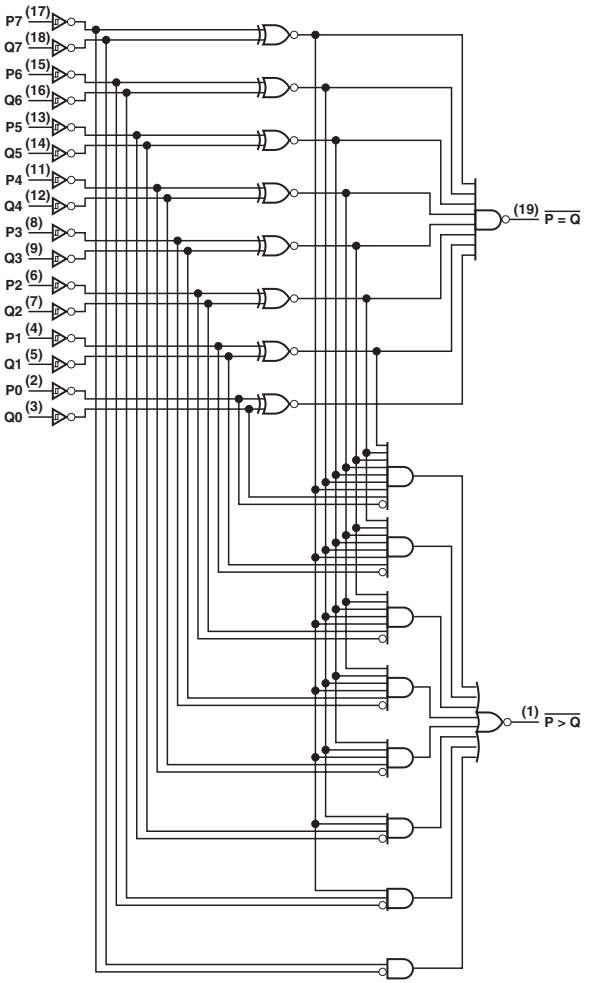
UNIT: ns

686

8-BIT MAGNITUDE/IDENTITY COMPARATORS

- Totem-Pole Outputs
- Hysteresis at P and Q Inputs

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS			OUTPUTS	
DATA	ENABLE		$\overline{P=Q}$	$\overline{P>Q}$
P, Q	$\overline{G}1$	$\overline{G}2$		
P=Q	L	L	L	H
P>Q	L	L	H	L
P<Q	L	L	H	H
X	H	H	H	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	UNIT
I_{CC}	MAX	75	mA
I_{OH}	MAX	-0.4	mA
I_{OL}	MAX	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
t_{PLH}	P	$\overline{P = Q}$	MAX	25
t_{PHL}				30
t_{PLH}	Q	$\overline{P = Q}$	MAX	25
t_{PHL}				30
t_{PLH}	$\overline{G}1$	$\overline{P = Q}$	MAX	20
t_{PHL}				30
t_{PLH}	P	$\overline{P > Q}$	MAX	30
t_{PHL}				30
t_{PLH}	Q	$\overline{P > Q}$	MAX	30
t_{PHL}				30
t_{PLH}	$\overline{G}2$	$\overline{P > Q}$	MAX	30
t_{PHL}				25

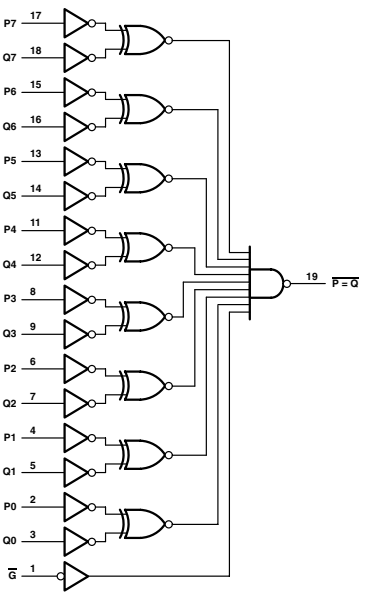
UNIT: ns

688

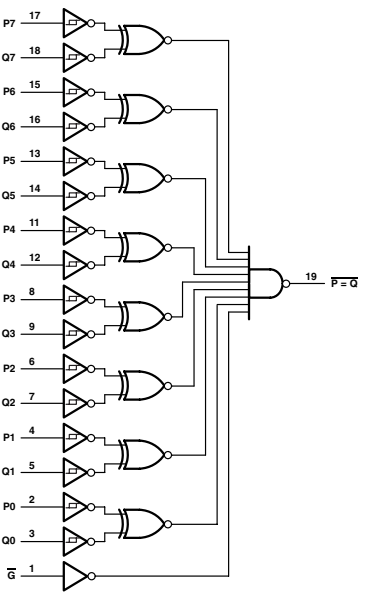
8-BIT IDENTITY COMPARATORS

- Totem-Pole Outputs
- Hysteresis at P and Q Inputs

Logic Diagram
(SN74ALS)



(SN74LS)



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS		OUTPUT
DATA	ENABLE	
P, Q	$\overline{G}$	$\overline{P=Q}$
P=Q	L	L
P>Q	L	H
P<Q	L	H
X	H	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	65	19	0.08	0.16	0.16	mA
I_{OH}	MAX	-0.4	-2.6	-4	-4	-4	mA
I_{OL}	MAX	24	24	4	4	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	SN74 HC	CD74 HC	CD74 HCT
t_{PLH}	P (CD74: A)	$\overline{P = Q}$ (CD74: Y)	MAX	18	12	53	51	51
t_{PHL}				23	20	53	51	51
t_{PLH}	Q (CD74: B)	$\overline{P = Q}$ (CD74: Y)	MAX	18	12	53	51	51
t_{PHL}				23	20	53	51	51
t_{PLH}	$\overline{G}$ (CD74: $\overline{E}$)	$\overline{P = Q}$ (CD74: Y)	MAX	18	12	30	36	36
t_{PHL}				20	22	30	36	36

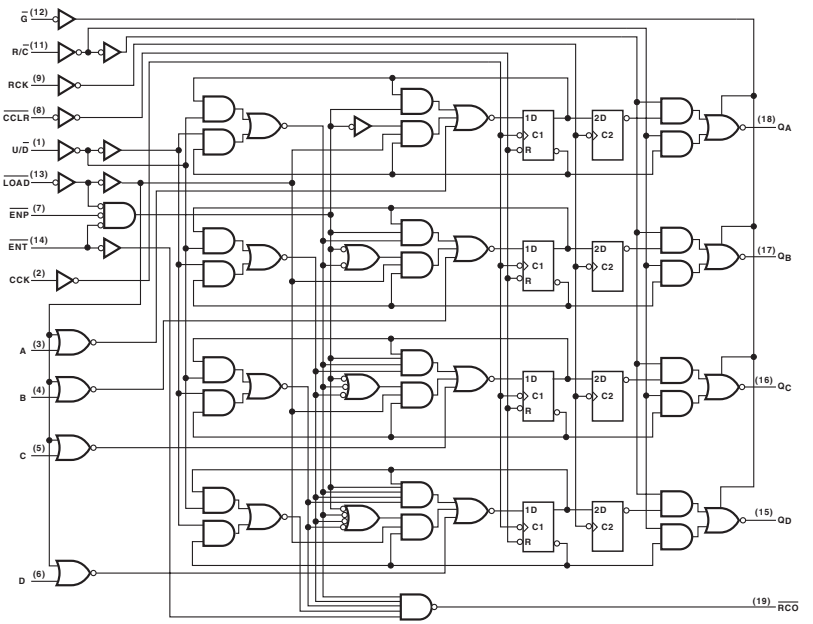
UNIT: ns

697

SYNCHRONOUS UP/DOWN COUNTERS WITH OUTPUT REGISTERS AND MULTIPLEXED 3-STATE OUTPUTS

- Multiplexed Outputs for Counter or Latched Data
- 3-State Outputs Drive Bus Lines Directly
- Binary Counter, Direct Clear

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	UNIT
I_{CC}		MAX	70	mA
I_{OH}	Q	MAX	-2.6	mA
	$\overline{RCO}$		-0.4	mA
I_{OL}	Q	MAX	24	mA
	$\overline{RCO}$		8	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	LS
t_w	CCK			MIN	25
	RCK				25
t_{su}	A thru D			MIN	30
	$\overline{ENT}$, $\overline{ENP}$				30
	U/$\overline{D}$				35
t_h				MIN	0
t_{PLH}		CCK ↑	$\overline{RCO}$	MAX	40
t_{PHL}					40
t_{PLH}		$\overline{ENT}$	$\overline{RCO}$	MAX	20
t_{PHL}					20
t_{PLH}		CCK ↓	Q	MAX	20
t_{PHL}					25
t_{PLH}		RCK ↓	Q	MAX	20
t_{PHL}					25
t_{PHL}		$\overline{CCLR}$ ↓	Q	MAX	40
t_{PLH}		R / $\overline{C}$	Q	MAX	25
t_{PHL}					25

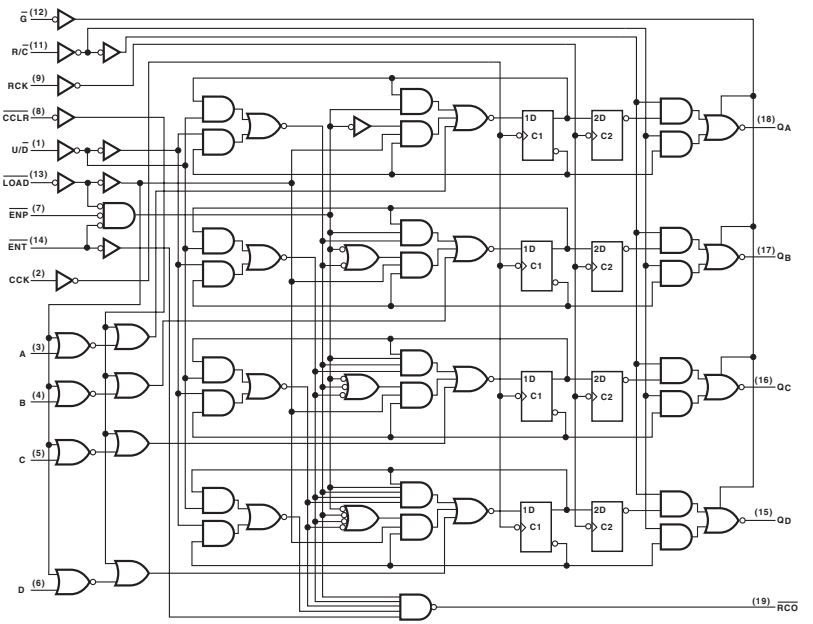
UNIT: ns

699

SYNCHRONOUS UP/DOWN COUNTERS WITH OUTPUT REGISTERS AND MULTIPLEXED 3-STATE OUTPUTS

- Multiplexed Outputs for Counter or Latched Data
- 3-State Outputs Drive Bus Lines Directly
- Binary Counter, Synchronous Clear

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	UNIT
I_{CC}		MAX	70	mA
I_{OH}	Q	MAX	-2.6	mA
	$\overline{RCO}$	MAX	-0.4	mA
I_{OL}	Q	MAX	24	mA
	$\overline{RCO}$	MAX	8	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	LS
t_w	CCK			MIN	25
	RCK				25
t_{su}	A thru D			MIN	30
	$\overline{ENT}$, $\overline{ENP}$				30
	U/$\overline{D}$				35
	$\overline{CCLR}$				30
t_h				MIN	0
t_{PLH}		CCK ↑	$\overline{RCO}$	MAX	40
t_{PHL}					40
t_{PLH}		$\overline{ENT}$	$\overline{RCO}$	MAX	20
t_{PHL}					20
t_{PLH}		CCK ↑	Q	MAX	20
t_{PHL}					25
t_{PLH}		RCK ↑	Q	MAX	20
t_{PHL}					25
t_{PLH}		R/$\overline{C}$	Q	MAX	25
t_{PHL}					25

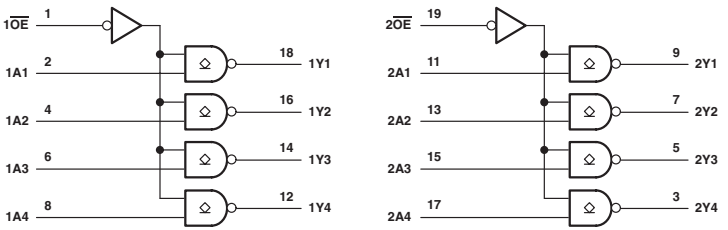
UNIT: ns

756

OCTAL BUFFER/DRIVER WITH OPEN-COLLECTOR OUTPUTS

- Eliminate the Need for 3-State Overlap Protection
- pnp Inputs Reduce dc Loading
- Open-Collector Versions of SN74AS240A

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AS	SN74 BCT	UNIT
I_{CC}	MAX	80	86	mA
V_{OH}	MAX	5.5	5.5	V
I_{OL}	MAX	64	64	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AS	SN74 BCT
t_{PLH}	A	Y	MAX	19	11.3
t_{PHL}				6	4.2
t_{PLH}	$\overline{OE}$	Y	MAX	19.5	16.5
t_{PHL}				7.5	10.3

UNIT:ns

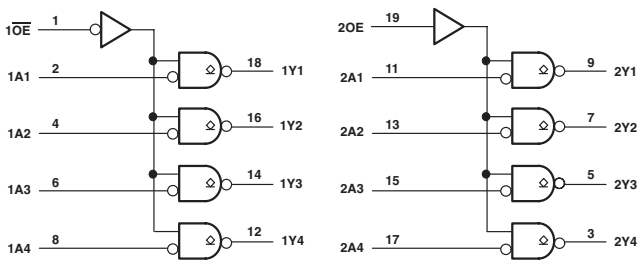
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

757

OCTAL BUFFER/DRIVER WITH OPEN-COLLECTOR OUTPUTS

- Eliminate the Need for 3-State Overlap Protection
- pnp Inputs Reduce dc Loading
- Open-Collector Versions of SN74AS241

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AS	SN74 BCT	SN64 BCT	UNIT
I_{CC}	MAX	95	77	77	mA
V_{OH}	MAX	5.5	5.5	5.5	V
I_{OL}	MAX	64	64	64	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AS	SN74 BCT	SN64 BCT
t_{PLH}	A	Y	MAX	18.5	10.1	10.1
t_{PHL}				6	6.6	6.6
t_{PLH}	$1\overline{OE}$	1Y	MAX	20	19.7	19.7
t_{PHL}				7	6.9	6.9
t_{PLH}	2OE	2Y	MAX	21	18	18
t_{PHL}				7.5	8.5	8.5

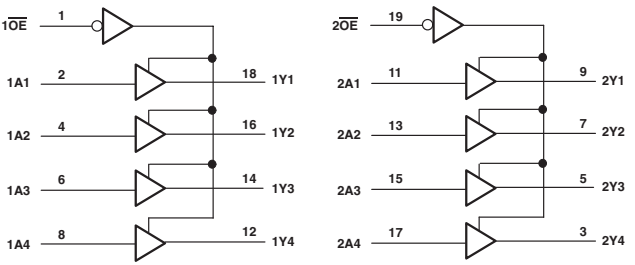
UNIT:ns

760

OCTAL BUFFERS/DRIVERS WITH OPEN-COLLECTOR OUTPUTS

- Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Registers
- pnp Inputs Reduce dc Loading
- Open-Collector Versions of SN74ALS244 and SN74AS244

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	SN74 BCT	UNIT
I_{CC}	MAX	19	94	76	mA
V_{OH}	MAX	5.5	5.5	5.5	V
I_{OL}	MAX	24	64	64	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS	SN74 BCT
t_{PLH}	A	Y	MAX	15	18.5	10
t_{PHL}				12	6	7.2
t_{PLH}	$\overline{OE}$	Y	MAX	16	18.5	17.5
t_{PHL}				13	7	9.9

UNIT:ns

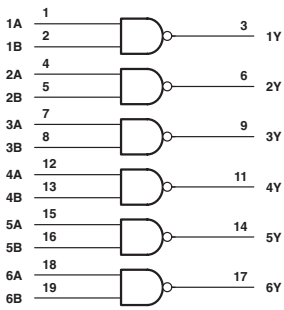
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

804

HEX 2-INPUT NAND DRIVERS

- $Y = \overline{A \bullet B}$
- High Capacitive-Drive Capability

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	SN74 HC	UNIT
I_{CC}	MAX	12	27	0.08	mA
I_{OH}	MAX	-15	-48	-6	mA
I_{OL}	MAX	24	48	6	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS	SN74 HC
t_{PLH}	A, B	Y	MAX	7	4	25
t_{PHL}			MAX	8	4	25

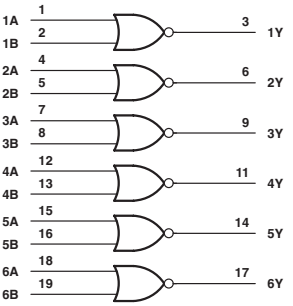
UNIT:ns

805

HEX 2-INPUT NOR DRIVERS

- $Y = \overline{A + B}$
- High Capacitive-Drive Capability

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIOI

PARAMETER	MAX or MIN	ALS	AS	SN74 HC	UNIT
I_{CC}	MAX	14	32	0.08	mA
I_{OH}	MAX	-15	-48	-6	mA
I_{OL}	MAX	24	48	6	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS	SN74 HC
t_{PLH}	A, B	Y	MAX	7	4.3	24
t_{PHL}			MAX	8	4.3	24

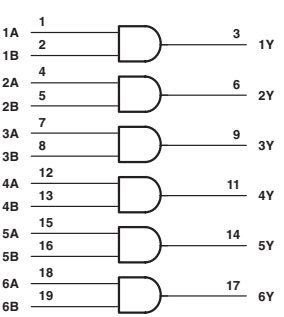
UNIT:ns

808

HEX 2-INPUT AND DRIVERS

- Y = A + B
- High Capacitive-Drive Capability

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIOI

PARAMETER	MAX or MIN	AS	SN74 HC	UNIT
I_{CC}	MAX	33	0.08	mA
I_{OH}	MAX	-48	-6	mA
I_{OL}	MAX	48	6	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AS	SN74 HC
t_{PLH}	A, B	Y	MAX	6	25
t_{PHL}			MAX	6	25

UNIT:ns

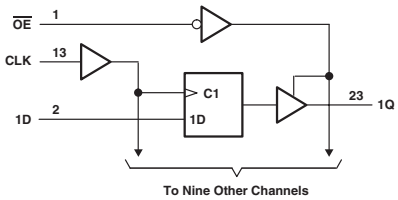
: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

821

10-BIT BUS-INTERFACE FLIP FLOPS WITH 3-STATE OUTPUTS

- Outputs Have Undershoot-Protection Circuitry
- Power-Up High-Impedance State

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AS	ABT	LVC 3V	UNIT
I_{CC}	MAX	113	38	0.01	mA
I_{OH}	MAX	-24	-32	-24	mA
I_{OL}	MAX	48	64	24	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AS	ABT	LVC 3V
t_w	High		MIN	8	2.9	3.3
	Low		MIN	8	3.8	3.3
t_{su}			MIN	6	2.1	1.9
t_h			MIN	0	1.3	1.5
t_{PLH}	CLK	Q	MAX	7.5	6.2	7.3
t_{PHL}				13	6.7	7.3
t_{PZH}	$\overline{OE}$	Q	MAX	11	5.8	7.6
t_{PZL}				12	6.3	7.6
t_{PHZ}	$\overline{OE}$	Q	MAX	8	6.7	6.2
t_{PLZ}				8	6.5	6.2

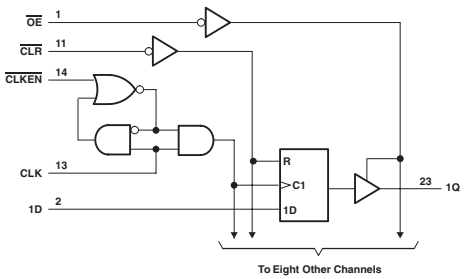
UNIT: ns

823

9-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

- Functionally Equivalent to AMD's AM29823 and AM29824
- Outputs Have Undershoot-Protection Circuitry
- Power-Up High-Impedance State

Logic Diagram



FUNCTION TABLE

INPUTS					OUTPUT
$\overline{OE}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	Q_0
H	X	X	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AS	ABT	LVC 3V	UNIT
I_{CC}	MAX	103	38	0.01	mA
I_{OH}	MAX	-24	-32	-24	mA
I_{OL}	MAX	48	64	24	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	AS	ABT	LVC 3V
t_w	$\overline{CLR}$ "L"			MIN	6.5	5.5	3.3
	CLK "H"				8	2.9	3.3
	CLK "L"				8	3.8	3.3
t_{su}	$\overline{CLR}$ inactive			MIN	8	2.5	1
	DATA				6	2.1	1.3
	$\overline{CLKEN}$ "H"				7.5	2	-
	$\overline{CLKEN}$ "L"				7.5	3.3	1.8
t_h	DATA			MIN	-	1.3	2
	$\overline{CLKEN}$ "H"				-	1	-
	$\overline{CLKEN}$ "L"				0	2	1.3
t_{PLH}		CLK	Q	MAX	7.5	6.8	8
t_{PHL}					13	6.7	8
t_{PHL}		$\overline{CLR}$	Q	MAX	15.5	7.1	7.9
t_{PZH}		$\overline{OE}$	Q	MAX	11	6	7.2
t_{PZL}					12	6.5	7.2
t_{PHZ}		$\overline{OE}$	Q	MAX	8	7.5	6
t_{PLZ}					8	6.9	6

UNIT: ns

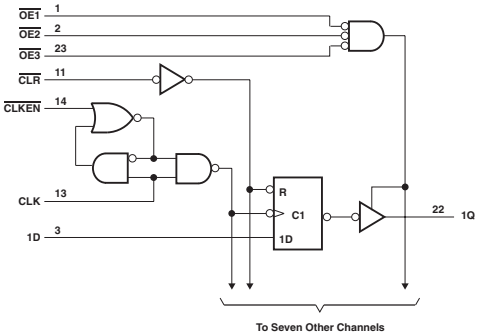
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

825

8-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

- Improved I_{OH} Specifications (Max: -24mA)
- Outputs Have Undershoot-Protection Circuitry
- Power-Up High-Impedance State

Logic Diagram



FUNCTION TABLE

INPUTS					OUTPUT
$\overline{OE}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	Q_0
H	X	X	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AS	UNIT
I_{CC}	MAX	95	mA
I_{OH}	MAX	-24	mA
I_{OL}	MAX	48	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	AS
t_w	$\overline{CLR}$ "L"			MIN	4
	CLK "H"				8
	CLK "L"				8
t_{su}	$\overline{CLR}$			MIN	8
	DATA				6
	$\overline{CLKEN}$				6
t_h				MIN	0
t_{PLH}		CLK	Q	MAX	7.5
t_{PHL}					13
t_{PHL}		$\overline{CLR}$	Q	MAX	15.5
t_{PZH}		$\overline{OE}$	Q	MAX	11
t_{PZL}					12
t_{PHZ}		$\overline{OE}$	Q	MAX	8
t_{PLZ}					8

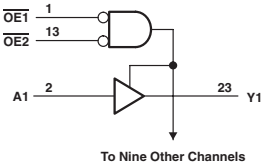
UNIT: ns

827

10-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	H	H
L	L	L	L
X	H	X	Z
H	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	AC 11	ACT 11	LVC 3V	UNIT
I_{CC}	MAX	40	0.08	0.08	0.01	mA
I_{OH}	MAX	-32	-24	-24	-24	mA
I_{OL}	MAX	64	24	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	AC 11	ACT 11	LVC 3V
t_{PLH}	A	Y	MAX	4.8	8.7	9.2	6.7
t_{PHL}				4.7	9.7	11.2	6.7
t_{PZH}	$\overline{OE}$		MAX	5.9	9.7	11.3	7.3
t_{PZL}				6.9	13	14	7.3
t_{PHZ}	$\overline{OE}$		MAX	6.8	9.1	12	6.7
t_{PLZ}				6.9	8.8	11.6	6.7

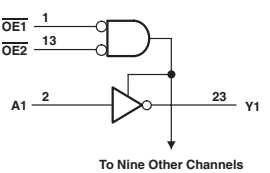
UNIT: ns

828

10-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	H	L
L	L	L	H
H	X	X	Z
X	H	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AC 11	ACT 11	LVC 3V	UNIT
I_{CC}	MAX	0.08	0.08	0.01	mA
I_{OH}	MAX	-24	-24	-24	mA
I_{OL}	MAX	24	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AC 11	ACT 11	LVC 3V
t_{PLH}	A	Y	MAX	9.5	10.2	6.7
t_{PHL}				10.4	11.7	6.7
t_{PZH}	$\overline{OE}$		MAX	10.7	12.1	7.3
t_{PZL}				13.2	14.7	7.3
t_{PHZ}	$\overline{OE}$		MAX	9.6	12.3	6.7
t_{PLZ}				9.2	11.7	6.7

UNIT: ns

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

832

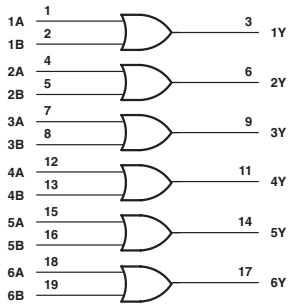
HEX 2-INPUT OR DRIVERS

- Y = A + B
- High Capacitive-Drive Capability

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIO

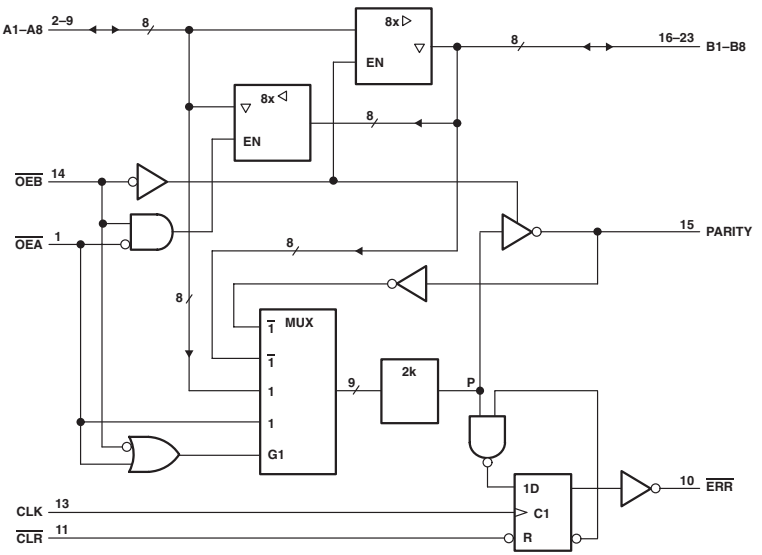
PARAMETER	MAX or MIN	ALS	AS	SN74 HC	UNIT
I_{CC}	MAX	16	36	0.08	mA
I_{OH}	MAX	-15	-48	-6	mA
I_{OL}	MAX	24	48	6	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS	SN74 HC
t_{PLH}	A, B	Y	MAX	9	6.3	25
t_{PHL}			MAX	8	6.3	25

UNIT:ns

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS						OUTPUTS AND I/O				FUNCTION
$\overline{OEB}$	$\overline{OEA}$	$\overline{CLR}$	CLK	Ai Σ OF H's	Bi Σ OF H's	A	B	PARITY	$\overline{ERR}$	
L	H	X	X	Odd Even	NA	NA	A	L H	NA	A data to B bus and generate parity
H	L	H	↑	NA	Odd Even	B	NA	NA	H L	B data to A bus and check parity
X	X	L	X	X	X	X	NA	NA	H	Check error flag register
H	H	H L H H	No↑ No↑ ↑ ↑	X X Odd Even	X	Z	Z	Z	NC H H L	Isolation
L	L	X	X	Odd Even	NA	NA	A	H L	NA	A data to B bus and generate inverted parity

INPUTS		INTERNAL TO DEVICE	OUTPUT PRE-STATE	OUTPUT $\overline{ERR}$	FUNCTION
$\overline{CLR}$	CLK	POINT P	$\overline{ERR}_{n-1}$†		
H	↑	H	H	H	Sample
H	↑	X	L	H	
H	↑	L	X	L	
L	X	X	X	H	Clear

† The state of $\overline{ERR}$ before any changes at $\overline{CLR}$, CLK, or point P

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	UNIT
I_{CC}	MAX	38	mA
I_{OH}	MAX	-32	mA
I_{OL}	MAX	64	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT
t_{PLH}	A or B	B or A	MAX	5.3
t_{PHL}				5.3
t_{PLH}	A	PARITY	MAX	11.2
t_{PHL}				11
t_{PZH}	$\overline{OE}$	PARITY	MAX	10.5
t_{PZL}				10
t_{PLH}	$\overline{CLR}$	$\overline{ERR}$	MAX	5.2
t_{PHL}	CLK			6.2
t_{PZH}	$\overline{OE}$	A,B, or PARITY	MAX	6.5
t_{PZL}				6.5
t_{PHZ}	$\overline{OE}$	A,B, or PARITY	MAX	7.9
t_{PLZ}				8.1

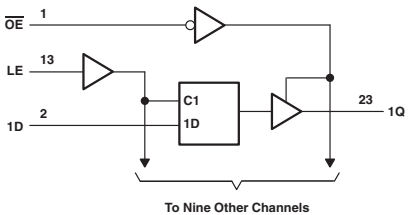
UNIT: ns

841

10-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Provide Extra Bus-Driving Latches Necessary for Wider Address/Data Paths or Buses with Parity
- Power-Up High-Impedance State

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	L
L	H	L	H
L	L	X	Q_0
H	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	ABT	LVC 3V	UNIT
I_{CC}	MAX	62	94	38	0.01	mA
I_{OH}	MAX	-2.6	-24	-32	-24	mA
I_{OL}	MAX	24	48	64	24	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS	ABT	LVC 3V
t_w			MIN	20	4	3.3	3.3
t_{su}	High			10	2.5	2.5	2.1
t_{su}	Low			10	2.5	1.5	2.1
t_h				5	2.5	1.5	1
t_{PLH}	D	Q	MAX	13	6.5	6.2	6.7
t_{PHL}				13	10.5	6.2	6.7
t_{PLH}	LE	Q	MAX	21	12	6.5	7.6
t_{PHL}				26	12	6.7	7.6
t_{PZH}	$\overline{OE}$	Q	MAX	12	14	5.3	7.2
t_{PZL}				12	16	6.3	7.2
t_{PHZ}	$\overline{OE}$	Q	MAX	10	8	7.1	5.9
t_{PLZ}				12	8	6.5	5.9

UNIT: ns

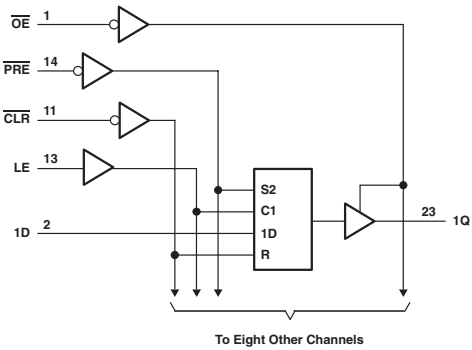
: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

843

9-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Provides Extra Bus-Driving Latches Necessary for Wider Address/Data Paths or Buses with Parity
- Power-Up High-Impedance State

Logic Diagram



FUNCTION TABLE

INPUTS					OUTPUT
PRE	CLR	OE	LE	D	
L	H	L	X	X	H
H	L	L	X	X	L
L	L	L	X	X	H
H	H	L	H	L	L
H	H	L	H	H	H
H	H	L	L	X	Q_0
X	X	H	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

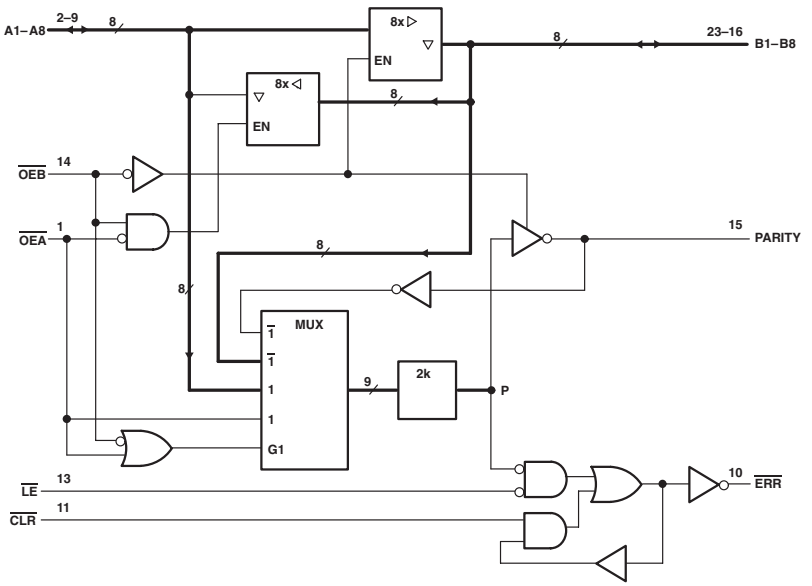
PARAMETER	MAX or MIN	ALS	AS	ABT	UNIT
I_{CC}	MAX	67	92	34	mA
I_{OH}	MAX	-2.6	-24	-32	mA
I_{OL}	MAX	24	48	64	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	ALS	AS	ABT
t_w	$\overline{CLR}$ "L"			MIN	35	4	5.5
	$\overline{PRE}$ "L"				35	4	4.5
	LE "H"				20	4	-
	LE "L"				-	4	3.4
t_{su}	LE "L"			MIN	10	2.5	2.5
	LE "H"				10	2.5	3
	$\overline{PRE}$ inactive				-	15	1.6
	$\overline{CLR}$ inactive				-	14	2
t_h	LE "L"			MIN	5	2.5	1
	LE "H"				5	2.5	1.5
t_{PLH}		D	Q	MAX	13	6.5	6.7
t_{PHL}					18	9	7.2
t_{PLH}		LE	Q	MAX	21	12	7.2
t_{PHL}					26	12	6.9
t_{PLH}		$\overline{CLR}$	Q	MAX	-	-	7.1
t_{PHL}					23	13	8
t_{PLH}		$\overline{PRE}$	Q	MAX	22	10	7.4
t_{PHL}					-	-	7.2
t_{PZH}		$\overline{OE}$	Q	MAX	12	10.5	5.7
t_{PZL}					14	13.5	6.5
t_{PHZ}		$\overline{OE}$	Q	MAX	10	8	6.8
t_{PLZ}					12	8	5.9

UNIT: ns

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS						OUTPUT AND I/Os				FUNCTION
$\overline{OEB}$	$\overline{OEA}$	$\overline{CLR}$	LE	Ai Σ OF H	Bi† Σ OF H	A	B	PARITY	$\overline{ERR}$‡	
L	H	X	X	Odd Even	NA	NA	A	L H	NA	A data to B bus and generate parity
H	L	H	L	NA	Odd Even	B	NA	NA	H L	B data to A bus and check parity
H	L	H	H	X	X	X	NA	NA	NC	Store error flag
X	X	L	H	X	X	X	NA	NA	H	Clear error flag register
H	H	H L H H	H H L L	X X L Odd H Even	X	Z	Z	Z	NC H H L	Isolation§ (parity check)
L	L	X	X	Odd Even	NA	NA	A	H L	NA	A data to B bus and generate inverted parity

NA = not applicable, NC = no change, X = don't care
† Summation of high-level inputs includes PARITY along with Bi inputs.
‡ Output states shown assume $\overline{ERR}$ was previously high.
§ In this mode, $\overline{ERR}$ (when clocked) shows inverted parity of the A bus.

ERROR-FLAG FUNCTION TABLE

INPUTS		INTERNAL TO DEVICE	OUTPUT PRE-STATE	OUTPUT $\overline{ERR}$	FUNCTION
$\overline{CLR}$	LE	POINT P	$\overline{ERR}_{n-1}$†		
L	L	L H	X	L H	Pass
H	L	L X H	X L H	L L H	Sample
L	H	X	X	H	Clear
H	H	X	L H	L H	Store

† The state of $\overline{ERR}$ before changes at $\overline{CLR}$, $\overline{LE}$, or point P

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	UNIT
I_{CC}	MAX	38	mA
I_{OH}	MAX	-32	mA
I_{OL}	MAX	64	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT
t_{PLH}	A or B	B or A	MAX	5.3
t_{PHL}				5.3
t_{PLH}	A	PARITY	MAX	11.2
t_{PHL}				11
t_{PLH}	$\overline{OE}$	PARITY	MAX	10.5
t_{PHL}				10
t_{PLH}	$\overline{CLR}$	$\overline{ERR}$	MAX	6.2
t_{PLH}	$\overline{LE}$	ERR	MAX	6
t_{PHL}				6.6
t_{PLH}	B or RARITY	ERR	MAX	11.7
t_{PHL}				12.8
t_{PZH}	$\overline{OE}$	A or B or PARITY	MAX	6.7
t_{PZL}				6.7
t_{PHZ}	$\overline{OE}$	A or B or PARITY	MAX	7.9
t_{PLZ}				8.1

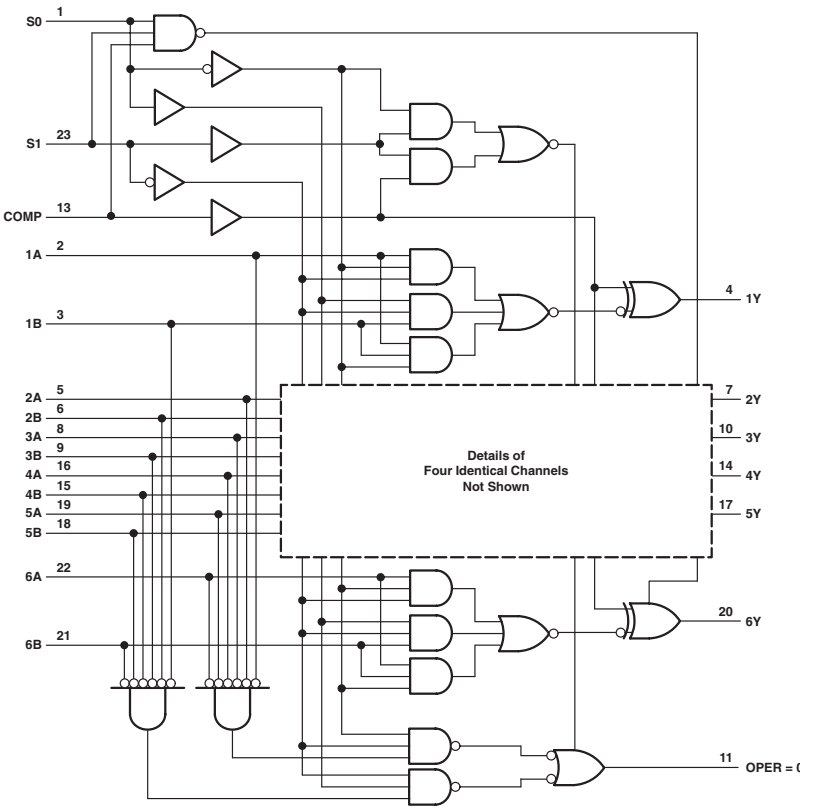
UNIT: ns

857

HEX 2-TO-1 UNIVERSAL MULTIPLEXERS WITH 3-STATE OUTPUTS

- Select True or Complementary Data
- Perform AND/NAND (Masking) of A or B Operand
- Cascadable to Expand Number of Operands
- Detect Zeros on A or B Operands
- 3-State Outputs Interface Directly with System Bus

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS			OUTPUTS	
COMP	S1	S0	Y	OPER = 0
L	L	L	A	H = all A inputs L
L	L	H	B	H = all B inputs L
L	H	L	A•B	Z
L	H	H	L	L
H	L	L	$\overline{A}$	H = all A inputs L
H	L	H	$\overline{B}$	H = all B inputs L
H	H	L	$\overline{A•B}$	Z
H	H	H	Z	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	ALS	AS	UNIT
I_{CCZ}		MAX	36	135	mA
I_{CCL}		MAX	33	175	mA
I_{OH}	Y	MAX	-2.6	-15	mA
	OPER = 0	MAX	-2.6	-2	mA
I_{OL}	Y	MAX	24	48	mA
	OPER = 0	MAX	24	20	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

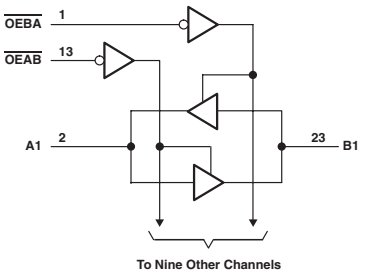
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
t_{pd}	A or B (COMP = "H")	Y inverting	MAX	14	12
t_{pd}	A or B (COMP = "L")	Y non-inverting	MAX	14	10
t_{pd}	S0 or S1	Y	MAX	33	13
t_{pd}	COMP	Y		18	13
t_{pd}	A or B	OPER = 0		37	14
t_{pd}	S0 to S1	OPER = 0		23	18
t_{en}	S0 to S1	Y	MAX	35	12
t_{dis}				23	11
t_{en}	COMP	Y	MAX	24	12
t_{dis}				21	9
t_{en}	S0	OPER = 0	MAX	20	12
t_{dis}				27	9
t_{en}	S1	OPER = 0	MAX	25	12
t_{dis}				19	9
t_{en}	COMP	OPER = 0	MAX	25	13
t_{dis}				20	9

UNIT: ns

861

10-BIT TRANSCEIVERS WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE

INPUTS		OPERATION
$\overline{OEAB}$	$\overline{OEBA}$	
L	H	A data to B bus
H	L	B data to A bus
H	H	Isolation
L	L	Latch A and B (A = B)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	LVC 3V	UNIT
I_{CC}	MAX	38	0.01	mA
I_{OH}	MAX	-32	-24	mA
I_{OL}	MAX	64	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVC 3V
t_{PLH}	A or B	B or A	MAX	5.2	6.4
t_{PHL}				4.9	6.4
t_{PZH}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A	MAX	5.9	7
t_{PZL}				6.9	7
t_{PHZ}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A	MAX	7.5	5.9
t_{PLZ}				7.1	5.9

UNIT: ns

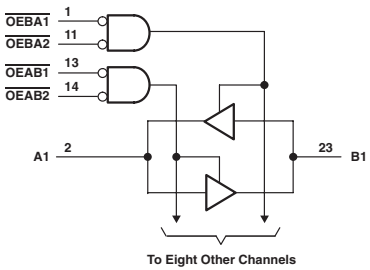
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

863

9-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- 3-State Outputs

Logic Diagram



FUNCTION TABLE

INPUTS				OPERATION
$\overline{OEAB1}$	OEAB2	OEBA1	$\overline{OEBA2}$	
L	L	L	L	Latch A and B
L	L	H	X	A to B
L	L	X	H	
H	X	L	L	B to A
X	H	L	L	
H	X	H	X	Isolation
H	X	X	H	
X	H	X	H	
X	H	H	X	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	LVC 3V	UNIT
I_{CC}	MAX	38	0.01	mA
I_{OH}	MAX	-32	-24	mA
I_{OL}	MAX	64	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVC 3V
t_{PLH}	A or B	B or A	MAX	5.7	6.1
t_{PHL}				3.9	6.1
t_{PZH}	$\overline{OE}$	A or B	MAX	5.5	7.2
t_{PZL}				5.4	7.2
t_{PHZ}	$\overline{OE}$	A or B	MAX	6.7	6.3
t_{PLZ}				6.9	6.3

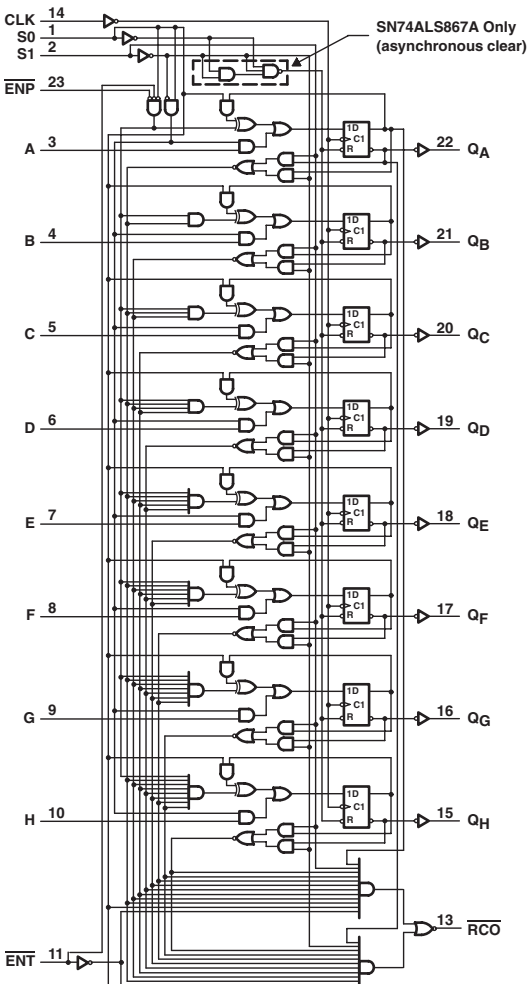
UNIT: ns

867

SYNCHRONOUS 8-BIT UP/DOWN COUNTERS

- Fully Programmable with Synchronous Counting and Loading
- Asynchronous Clear
- Ripple-Carry Output for n-Bit Cascading

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

S1	S0	FUNCTION
L	L	Clear
L	H	Count down
H	L	Load
H	H	Count up

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	UNIT
I_{CC}	MAX	45	195	mA
I_{OH}	MAX	-0.4	-2	mA
I_{OL}	MAX	8	20	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
f_{max}			MIN	35	50
t_w	CLK (clock)		MIN	14	10
	S0 and S1 (clear)			10	10
t_{su}	Data input A-H		MIN	10	4
	$\overline{ENP}$ or $\overline{ENT}$			15	8
	S0 low and S1 high (load)			12	10
	S0 and S1 low (clear)			-	10
	S0 high and S1 low (count down)			12	40
	S0 and S1 high (count up)			12	40
t_h	S0 high after S1 ↑ or S1 high after S0 ↑		MIN	3	-
	Data input A-H			0	0
t_{PLH}	CLK	$\overline{RCO}$	MAX	14	22
t_{PHL}				14	16
t_{PLH}	CLK	Any Q	MAX	16	11
t_{PHL}				16	15
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$	MAX	14	10
t_{PHL}				9	17
t_{PLH}	$\overline{ENP}$	$\overline{RCO}$	MAX	-	14
t_{PHL}				-	17
t_{PHL}	S0, S1 (clear mode)	Any Q	MAX	26	-
t_{PLH}	S0 or S1 (count up/down)	$\overline{RCO}$	MAX	16	-
t_{PHL}				16	-
t_{PHL}	S0 or S1 (clear mode)	$\overline{RCO}$	MAX	16	21

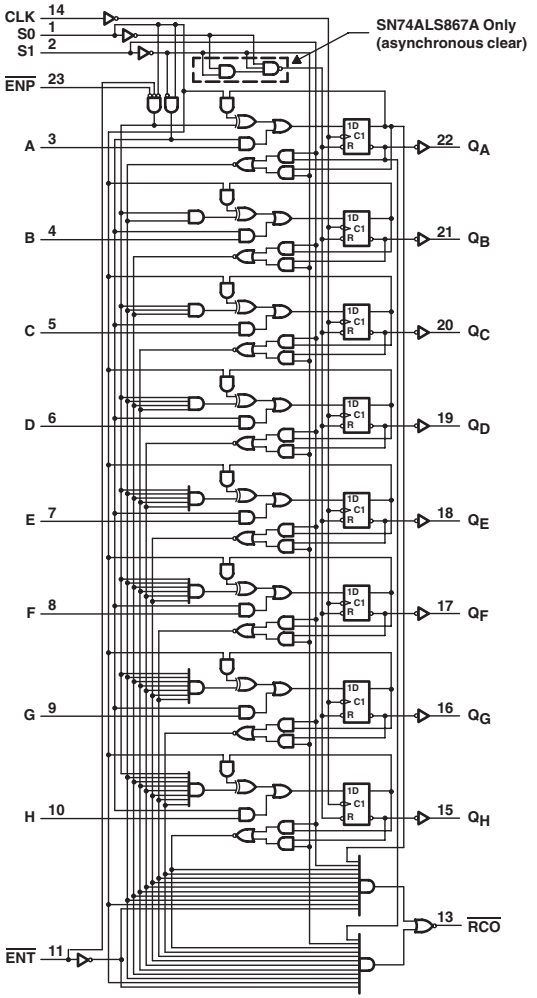
UNIT fmax : MHz other : ns

869

SYNCHRONOUS 8-BIT UP/DOWN COUNTERS

- Fully Programmable with Synchronous Counting and Loading
- Synchronous Clear
- Ripple-Carry Output for n-Bit Cascading

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

S1	S0	FUNCTION
L	L	Clear
L	H	Count down
H	L	Load
H	H	Count up

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	UNIT
I_{CC}	MAX	45	195	mA
I_{OH}	MAX	-0.4	-2	mA
I_{OL}	MAX	8	20	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
f_{max}			MIN	35	45
t_w	CLK		MIN	14	11
t_{su}	Data input A-H		MIN	10	5
	$\overline{ENP}$ or $\overline{ENT}$			15	9
	S0 low and S1 high (load)			13	11
	S0 and S1 low (clear)			13	11
	S0 high and S1 low (count down)			13	50
	S0 and S1 high (count up)			13	50
t_h	S0 high after S1 ↑ or S1 high after S0 ↑		MIN	3	-
	Data input A-H			0	0
t_{PLH}	CLK	$\overline{RCO}$	MAX	14	35
t_{PHL}				14	18
t_{PLH}	CLK	Any Q	MAX	16	11
t_{PHL}				16	15
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$	MAX	14	15
t_{PHL}				9	17
t_{PLH}	$\overline{ENP}$	$\overline{RCO}$	MAX	-	19
t_{PHL}				-	18
t_{PLH}	S1 (count up/down)	$\overline{RCO}$	MAX	15	-
t_{PHL}				15	-
t_{PLH}	S0 (clear/load)	$\overline{RCO}$	MAX	16	-
t_{PHL}				12	-

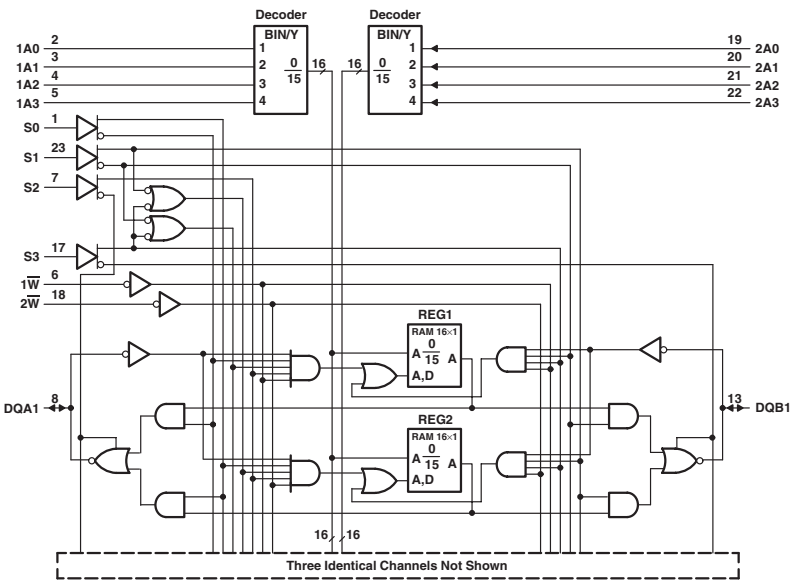
UNIT fmax : MHz other : ns

870

DUAL 16-BY 4-BIT REGISTER FILES

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Each Register File Has Individual Write-Enable Controls and Address Lines

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

FILE SELECT			INPUT/OUTPUT		
S0	**S1**	**FILE SEL**	**S2**	**S3**	**I/O SEL**
L	L	1R to A, 1R to B	L	L	A out B A out, B out
H	L	2R to A, 1R to B			
L	H	1R to A, 2R to B			
H	H	2R to A, 2R to B			
L	L	A to 1R, 1R to B	H	L	A in B A in, B out
H	L	A to 2R, 1R to B			
L	H	A to 1R, 2R to B			
H	H	A to 2R, 2R to B			
L	L	1R to A, B to 1R	L	H	A out B A out, B in
H	L	2R to A, B to 1R			
L	H	1R to A, B to 2R			
H	H	2R to A, B to 2R			
L	L	B to 1R	H	H	A in Bin A in, B
H	L	A to 2R, B to 1R			
L	H	A to 1R, B to 2R			
H	H	B to 2R			

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	UNIT
I_{CC}	MAX	110	190	mA
I_{OL}	MAX	24	48	mA
I_{OH}	MAX	-2.6	-15	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
t_w	write		MIN	12	12
t_{su}	Address before write ↓		MIN	5	5
	Data before write ↑			15	15
	Select before write ↓			12	12
t_h	Address before write ↓		MIN	0	0
	Data before write ↑			0	0
	Select before write ↓			12	12
$t_{a(A)}$	Any A	Any DQ	MAX	19	15
$t_{a(S)}$	S0	Any DQA	MAX	15	13
	S1	Any DQB		15	13
t_{dis}	S2	Any DQA	MAX	14	11
	S3	Any DQB		14	11
t_{en}	S2	Any DQA	MAX	17	12
	S3	Any DQB		17	12
t_{pd}	$\overline{W}$	Any $\overline{DQ}$	MAX	23	19
	DA	DQB		26	22
	DQB	DQA		26	22

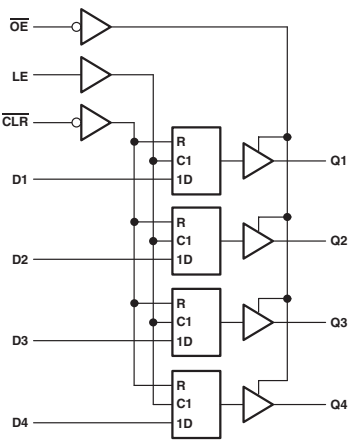
UNIT: ns

873

DUAL 4-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Asynchronous Clear

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUT
OE	CLR	ENABLE LE	D	
L	L	X	X	L
L	H	H	H	H
L	H	H	L	L
L	H	L	X	Q_0
H	X	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIOI

PARAMETER	MAX or MIN	ALS	AS	UNIT
I_{CC}	MAX	31	129	mA
I_{OH}	MAX	-2.6	-15	mA
I_{OL}	MAX	24	48	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	ALS	AS
t_w	CLR low			MIN	15	5
	LE high				10	5
t_{su}					10	2
t_h					7	4.5
t_{PLH}		D	Q	MAX	14	9.5
t_{PHL}					14	7.5
t_{PLH}		LE	Q	MAX	22	13
t_{PHL}					21	7.5
t_{PHL}		CLR	Q	MAX	20	9
t_{PZH}		OE	Q	MAX	18	6.5
t_{PZL}					18	10.5
t_{PHZ}		OE	Q	MAX	10	7.5
t_{PLZ}					15	7.5

UNIT: ns

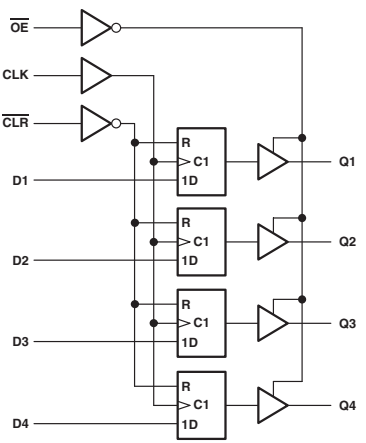
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

874

DUAL 4-BIT D-TYPE EDGE-TRIGGERD FLIP-FLOPS WITH 3-STATE OUTPUTS

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Asynchronous Clear

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUTS
$\overline{OE}$	$\overline{CLR}$	CLK	D	
L	L	X	X	L
L	H	↑	H	H
L	H	↑	L	L
L	H	L	X	Q_0
H	X	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIOI

PARAMETER	MAX or MIN	ALS	AS	UNIT
I_{CC}	MAX	32	160	mA
I_{OH}	MAX	-2.6	-15	mA
I_{OL}	MAX	24	48	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
f_{max}			MIN	30	125
t_w	$\overline{PRE}$ or $\overline{CLR}$ low		MIN	10	2
	CLK "H"			16.5	3
	CLK "L"			16.5	4
t_{su}	Data		MIN	15	2
	$\overline{PRE}$ or $\overline{CLR}$ inactive			10	4
t_h			MIN	0	1
t_{PLH}	CLK	Q	MAX	14	8.5
t_{PHL}				14	10.5
t_{PHL}	$\overline{CLR}$	Q	MAX	17	9.5
t_{PZH}	$\overline{OE}$	Q	MAX	18	7
t_{PZL}				18	10.5
t_{PHZ}	$\overline{OE}$	Q	MAX	10	6
t_{PLZ}				12	7.5

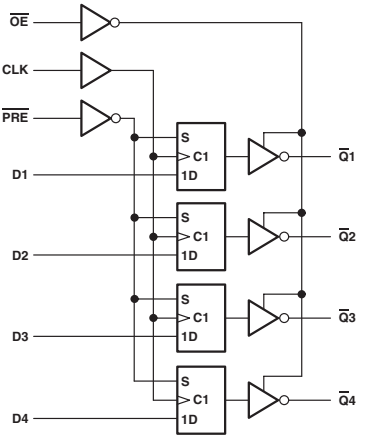
UNIT fmax : MHz other : ns

876

DUAL 4-BIT D-TYPE EDGE-TRIGGERD FLIP-FLOPS WITH 3-STATE OUTPUTS

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Asynchronous Clear

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE
(each filip-flop)

INPUTS				OUTPUT
$\overline{OE}$	$\overline{PRE}$	CLK	D	$\overline{Q}$
L	L	X	X	L
L	H	↑	H	L
L	H	↑	L	H
L	H	L	X	$\overline{Q}_0$
H	X	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	UNIT
I_{CC}	MAX	31	160	mA
I_{OH}	MAX	-2.6	-15	mA
I_{OL}	MAX	24	48	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	ALS	AS
f_{max}				MIN	30	80
t_w	$\overline{PRE}$ "L"			MIN	10	4.5
	CLK "H"				16.5	6.2
	CLK "L"				16.5	6.2
t_{su}	Data			MIN	15	4.5
	$\overline{PRE}$ inactive				10	5
t_h				MIN	0	2
t_{PLH}		CLK	$\overline{Q}$	MAX	14	8.5
t_{PHL}					14	10.5
t_{PHL}		$\overline{PRE}$	$\overline{Q}$	MAX	19	9.5
t_{PZH}		$\overline{OE}$	$\overline{Q}$	MAX	18	7
t_{PZL}					18	11
t_{PHZ}		$\overline{OE}$	$\overline{Q}$	MAX	10	7
t_{PLZ}					13	7

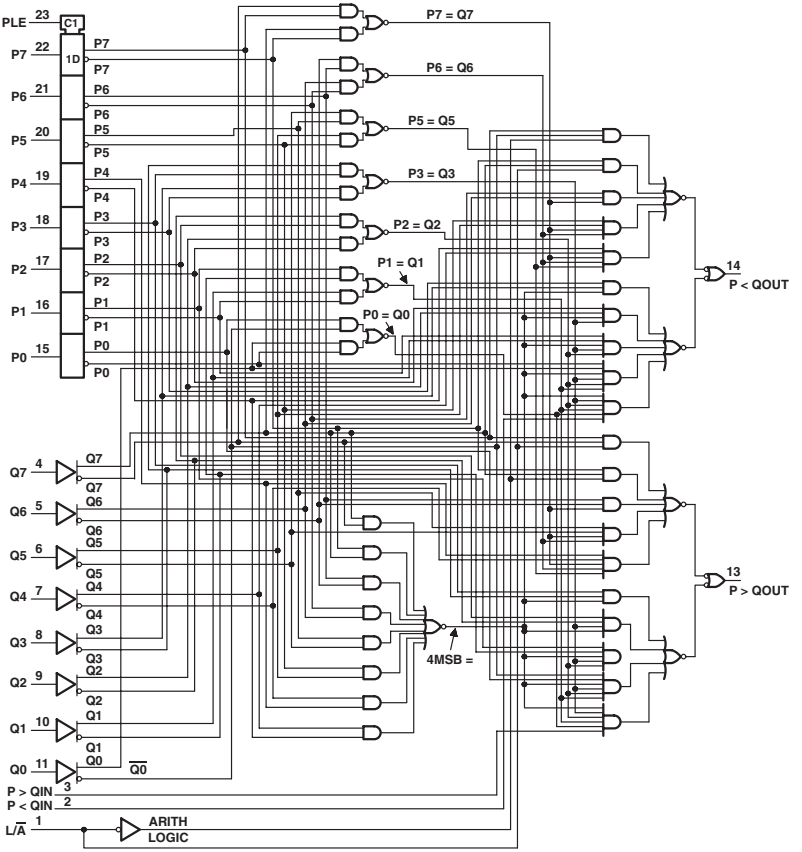
UNIT fmax : MHz, other : ns

885

8-BIT MAGNITUDE COMPARATORS

- SN54AS885 Latchable P-Input Ports with Power-Up Clear
- Choice of Logical or Arithmetic (Two's Complement) Comparison
- Data and PLE Inputs Utilize pnp Input Transistors to Reduce dc Loading Effects
- Cascadable to n Bits While Maintaining High Performance

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

COMPARISON	INPUTS				OUTPUTS	
	L/A	DATA P0–P7, Q0–Q7	P > QIN	P < QIN	P > QOUT	P < QOUT
Logical	H	P > Q	X	X	H	L
Logical	H	P < Q	X	X	L	H
Logical†	H	P = Q	H or L	H or L	H or L	H or L
Arithmetic	L	P AG Q	X	X	H	L
Arithmetic	L	Q AG P	X	X	L	H
Arithmetic†	L	P = Q	H or L	H or L	H or L	H or L

† In these cases, P > QOUT follows P > QIN and P < QOUT follows P < QIN.
AG = arithmetically greater than

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AS	UNIT
I_{CC}	MAX	210	mA
I_{OH}	MAX	-2	mA
I_{OL}	MAX	20	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AS
t_{su}	Data before PLE ↓		MIN	2
t_h	Data after PLE ↓			4
t_{PLH}	L / $\overline{A}$	P < QOUT, P > QOUT	MAX	13
t_{PHL}				13
t_{PLH}	P < QIN, P > QIN	P < QOUT, P > QOUT	MAX	8
t_{PHL}				8
t_{PLH}	Any P or Q data input	P < QOUT, P > QOUT	MAX	17.5
t_{PHL}				15

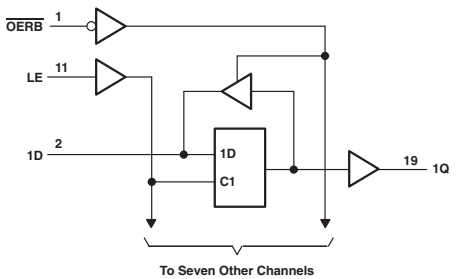
UNIT: ns

990

8-BIT D-TYPE TRANSPARENT READ-BACK LATCH

- 3-State I/O-Type Read-Back Inputs
- True Logic Outputs
- Bus-Structured Pinout

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	ALS	UNIT
I_{CC}		MAX	70	mA
I_{OH}	Q	MAX	-2.6	mA
	D		-0.4	mA
I_{OL}	Q	MAX	24	mA
	D		8	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
t_w	LE high		MIN	10
t_{su}	Data before LE ↓		MIN	10
	Data before $\overline{OERB}$			10
t_h	Data after LE ↓		MIN	5
t_{PLH}	D	Q	MAX	17
t_{PHL}				24
t_{PLH}	LE	Q	MAX	26
t_{PHL}				26
t_{en}	$\overline{OERB}$	D	MAX	21
t_{dis}			MAX	19

UNIT: ns

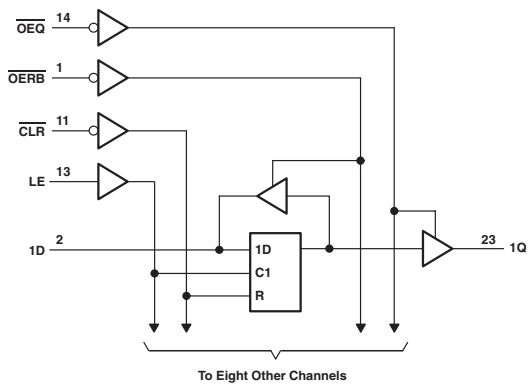
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

992

9-BIT D-TYPE TRANSPARENT READ-BACK LATCH WITH 3-STATE OUTPUTS

- 3-State I/O-Type Read-Back Inputs
- True Logic Outputs
- Bus-Structured Pinout
- Designed with Nine Bits for Parity Applications

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	ALS	UNIT
I_{CC}		MAX	80	mA
I_{OH}	Q	MAX	-2.6	mA
	D		-0.4	mA
I_{OL}	Q	MAX	24	mA
	D		8	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
t_w	C "H"		MIN	10
	CLR "L"			10
t_{su}	Data befor LE ↓		MIN	10
	Data befor $\overline{OERB}$ ↓			10
t_h	Data affter LE ↓		MIN	5
t_{PLH}	D	Q	MAX	14
t_{PHL}				16
t_{PLH}	LE	Q	MAX	20
t_{PHL}				25
t_{PHL}	$\overline{CLR}$	Q	MAX	20
		D		26
t_{en}	$\overline{OERB}$	D	MAX	21
t_{dis}				14
t_{en}	$\overline{OEQ}$	Q	MAX	18
t_{dis}				14

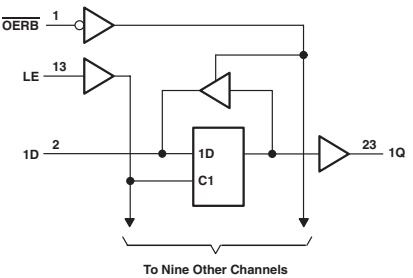
UNIT:ns

994

10-BIT D-TYPE TRANSPARENT READ-BACK LATCH

- 3-State I/O-Type Read-Back Inputs
- True Logic Outputs
- Bus-Structured Pinout

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	ALS	UNIT
I_{CC}		MAX	82	mA
I_{OH}	Q	MAX	-2.6	mA
	D		-0.4	mA
I_{OL}	Q	MAX	24	mA
	D		8	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
t_w	C "H"		MIN	10
t_{su}	Data befor LE ↓		MIN	10
	Data befor $\overline{OERB}$ ↓			10
t_h	Data affter LE ↓		MIN	5
t_{PLH}	D	Q	MAX	14
t_{PHL}				18
t_{PLH}	LE	Q	MAX	21
t_{PHL}				27
t_{en}	$\overline{OERB}$	D	MAX	21
t_{dis}				16

UNIT:ns

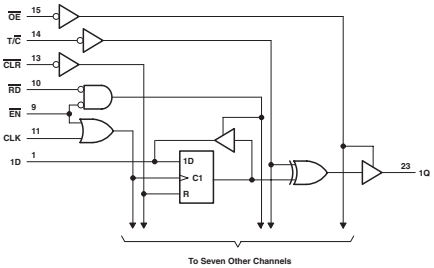
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

996

8-BIT D-TYPE EDGE-TRIGGERED READ-BACK LATCHES

- 3-State I/O-Type Read-Back Inputs
- True Logic Outputs
- T/C Determines True or Complementary Data at Q Outputs

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	ALS	ALS-1	UNIT
I_{CC}		MAX	85	85	mA
I_{OL}	Q	MAX	24	48	mA
	D		8	8	mA
I_{OH}	Q	MAX	-2.6	-2.6	mA
	D		-0.4	-0.4	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	ALS-1
t_w	$\overline{CLR}$ low		MIN	10	10
	CLK low			14.5	14.5
	CLK high			14.5	14.5
t_{su}	Data before CLK ↑		MIN	15	15
	$\overline{EN}$ low before CLK ↑			10	10
	CLK high before $\overline{EN}$ ↑ *1			15	15
	$\overline{CLR}$ high (inactive) before CLK ↑			10	10
t_h	Data after CLK ↑		MIN	0	0
	$\overline{EN}$ low after CLK ↑			5	5
	$\overline{RD}$ high after CLK ↑ *2			5	5
t_{PLH}	CLK (T/$\overline{C}$ = H or L)	Q	MAX	28	28
t_{PHL}				28	28
t_{PLH}	$\overline{CLR}$ (T/$\overline{C}$ = L)	Q	MAX	27	27
t_{PHL}	$\overline{CLR}$ (T/$\overline{C}$ = H)			23	23
t_{PLH}	T / $\overline{C}$	Q	MAX	23	23
t_{PHL}				23	23
t_{PHL}	$\overline{CLR}$	D	MAX	30	30
t_{en} *3	$\overline{RD}$	D	MAX	16	16
t_{dis} *4				19	19
t_{en} *3	$\overline{EN}$	D	MAX	16	16
t_{dis} *4				19	19
t_{en} *3	$\overline{OE}$	Q	MAX	15	15
t_{dis} *4				10	10

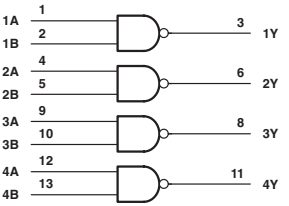
UNIT: ns

1000

QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS/DRIVERS

- Buffer Version of SN74ALS00A
- Driver Version of SN74AS00
- High Capacitive-Drive Capability

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	UNIT
I_{CC}	MAX	7.8	19	mA
I_{OH}	MAX	-2.6	-48	mA
I_{OL}	MAX	24	48	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
t_{PLH}	A or B	Y	MAX	8	4
t_{PHL}				7	4

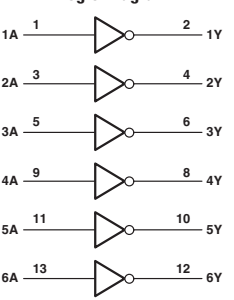
UNIT: ns

1004

HEX INVERTING DRIVERS

- Driver Version of SN74ALS04B and SN74AS04
- High Capacitive-Drive Capability

Logic Diagram



FUNCTION TABLE

INPUT A	OUTPUT Y
H	L
L	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	UNIT
I_{CC}	MAX	12	27	mA
I_{OH}	MAX	-15	-48	mA
I_{OL}	MAX	24	48	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
t_{PLH}	A or B	Y	MAX	7	4
t_{PHL}				6	4

UNIT: ns

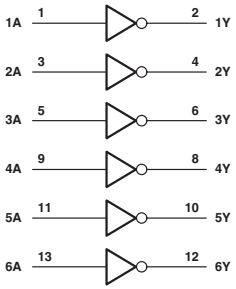
: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

1005

HEX INVERTING BUFFERS WITH OPEN-COLLECTOR OUTPUTS

- Buffer Version of SN74ALS05A

Logic Diagram



FUNCTION TABLE

INPUT A	OUTPUT Y
H	L
L	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	UNIT
I_{CC}	MAX	12	mA
V_{OH}	MAX	5.5	V
I_{OL}	MAX	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
t_{PLH}	A	Y	MAX	30
t_{PHL}				10

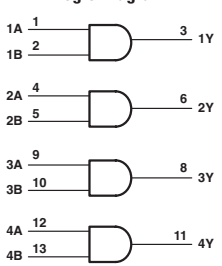
UNIT: ns

1008

QUADRUPLE 2-INPUT POSITIVE-AND BUFFER/DRIVER

- Buffer Version of SN74ALS08
- Driver Version of SN74AS08

Logic Diagram



FUNCTION TABLE

INPUTS A	INPUTS B	OUTPUT Y
H	H	H
L	X	L
X	L	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	UNIT
I_{CC}	MAX	9.3	22	mA
I_{OH}	MAX	-2.6	-48	mA
I_{OL}	MAX	24	48	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
t_{PLH}	A or B	Y	MAX	9	6
t_{PHL}				9	6

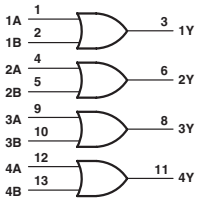
UNIT: ns

1032

QUADRUPLE 2-INPUT POSITIVE-OR BUFFERS/DRIVERS

- Y = A + B
- Driver Version of SN74AS32
- High Capacitive-Drive Capability

Logic Diagram



FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	UNIT
I_{CC}	MAX	10.6	24	mA
I_{OH}	MAX	-2.6	-48	mA
I_{OL}	MAX	24	48	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
t_{PLH}	A or B	Y	MAX	9	6.3
t_{PHL}	A or B	Y	MAX	12	6.3

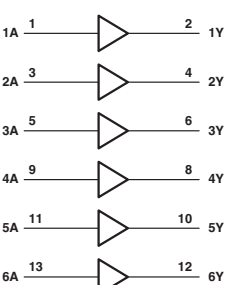
UNIT:ns

1034

HEX DRIVERS

- SN74AS1034A Offer High Capacitive-Drive Capability
- Noninverting Drivers

Logic Diagram



FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIO

PARAMETER	MAX or MIN	ALS	AS	UNIT
I_{CC}	MAX	14	35	mA
I_{OH}	MAX	-15	-48	mA
I_{OL}	MAX	24	48	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
t_{PLH}	A	Y	MAX	8	6
t_{PHL}				8	6

UNIT: ns

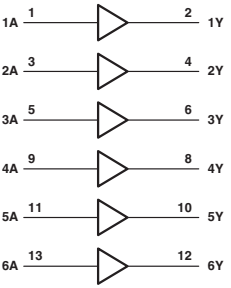
: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

1035

HEX NONINVERTING BUFFERS WITH OPEN-COLLECTOR OUTPUTS

- Noninverting Buffers with Open-Collector Outputs

Logic Diagram



FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	UNIT
I_{CC}	MAX	14	mA
V_{OH}	MAX	5.5	V
I_{OL}	MAX	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
t_{PLH}	A	Y	MAX	30
t_{PHL}				12

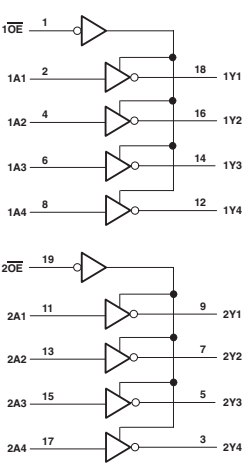
UNIT: ns

1240

OCTAL BUFFER AND LINE DRIVER WITH 3-STATE OUTPUTS

- Low-Power Versions of SN74ALS240A
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	UNIT
I_{CCZ}	MAX	13	mA
I_{CCL}	MAX	14	mA
I_{OH}	MAX	-15	mA
I_{OL}	MAX	16	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
t_{PLH}	A	Y	MAX	13
t_{PHL}				13
t_{PZH}	$\overline{OE}$	Y	MAX	20
t_{PZL}				22
t_{PHZ}	$\overline{OE}$	Y	MAX	10
t_{PLZ}				13

UNIT: ns

1244

OCTAL BUFFERS AND DRIVERS WITH 3-STATE OUTPUTS

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- pnp Inputs Reduce dc Loading
- Low-Power Versions of SN74ALS244 Series

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

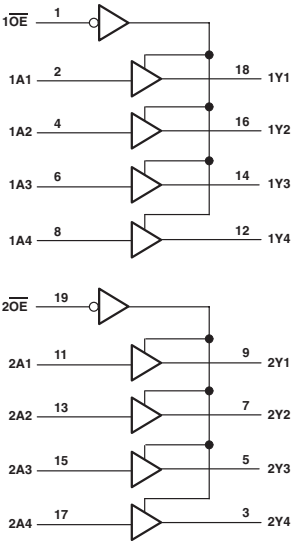
PARAMETER	MAX or MIN	ALS	UNIT
I_{CCZ}	MAX	20	mA
I_{CCL}	MAX	17	mA
I_{OH}	MAX	-15	mA
I_{OL}	MAX	16	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
t_{PLH}	A	Y	MAX	14
t_{PHL}				14
t_{PZH}	$\overline{OE}$	Y	MAX	22
t_{PZL}				22
t_{PHZ}	$\overline{OE}$	Y	MAX	13
t_{PLZ}				16

UNIT: ns

Logic Diagram

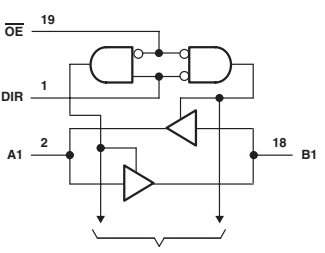


1245

OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- Low-Power Versions of 4ALS245 Series

Logic Diagram



FUNCTION TABLE

CONTROL INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	UNIT
I_{CCZ}	MAX	36	mA
I_{CCL}	MAX	33	mA
I_{OH}	MAX	-15	mA
I_{OL}	MAX	16	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
t_{PLH}	A or B	B or A	MAX	13
t_{PHL}				13
t_{PZH}	$\overline{OE}$	A or B	MAX	25
t_{PZL}				25
t_{PHZ}	$\overline{OE}$	A or B	MAX	12
t_{PLZ}				18

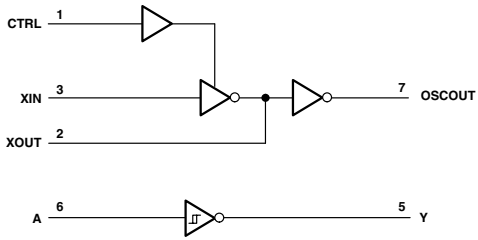
UNIT: ns

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

1404

OSCILLATOR DRIVER FOR CRYSTAL OSCILLATOR OR CERAMIC RESONATOR

Logic Diagram



FUNCTION TABLES

INPUTS		OUTPUTS	
CTRL	XIN	XOUT	OSCOUT
H	L	H	L
H	H	L	H
L	X	L	H

INPUT A	OUTPUT Y
L	H
H	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 1.8V	LVC 2.5V	LVC 3V	LVC 5V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	mA
I_{OH} (OSCOUT, XOUT, Y outputs)	MAX	-4	-8	-24	-32	mA
I_{OH} (OSCOUT, XOUT, Y outputs)	MAX	4	8	24	32	mA
I_{OL} (XOUT)	MAX	2	-	-	-	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 1.8V	LVC 2.5V	LVC 3V	LVC 5V
t_{PLH}	A	Y	MAX	17.3	7.4	6.4	5.3
t_{PHL}				17.3	7.4	6.4	5.3
t_{PLH}	XIN	XOUT	MAX	15.8	5.8	5.4	4.6
t_{PHL}				15.8	5.8	5.4	4.6
t_{PLH}	XIN	OSCOUT	MAX	25.7	7.1	7.8	6.7
t_{PHL}				25.7	7.1	7.8	6.7
t_{PLH}	CTRL	XOUT	MAX	24.5	12	12.7	11.2
t_{PHL}				24.5	12	12.7	11.2

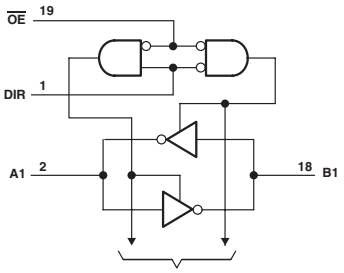
UNIT: ns

1640

OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- Lower-Power Versions of SN74ALS640B
- Inverting Logic
- 3-State Outputs

Logic Diagram



FUNCTION TABLE

CONTROL INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	$\overline{B}$ data to A bus
L	H	$\overline{A}$ data to B bus
H	X	Isolation

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	UNIT
I_{CC}	MAX	32	mA
I_{OH}	MAX	-15	mA
I_{OL}	MAX	16	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
t_{PLH}	A or B	B or A	MAX	15
t_{PHL}				10
t_{PZH}	$\overline{OE}$	A or B	MAX	20
t_{PZL}				22
t_{PHZ}	$\overline{OE}$	A or B	MAX	10
t_{PLZ}				13

UNIT: ns

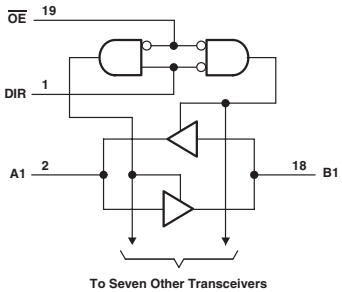
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

1645

OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- Lower-Power Versions of SN74ALS645A
- 3-State Outputs

Logic Diagram



FUNCTION TABLE

CONTROL INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	UNIT
I_{CC}	MAX	38	mA
I_{OH}	MAX	-15	mA
I_{OL}	MAX	16	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
t_{PLH}	A or B	B or A	MAX	13
t_{PHL}				13
t_{PZH}	$\overline{OE}$	A or B	MAX	25
t_{PZL}				25
t_{PHZ}	$\overline{OE}$	A or B	MAX	12
t_{PLZ}				18

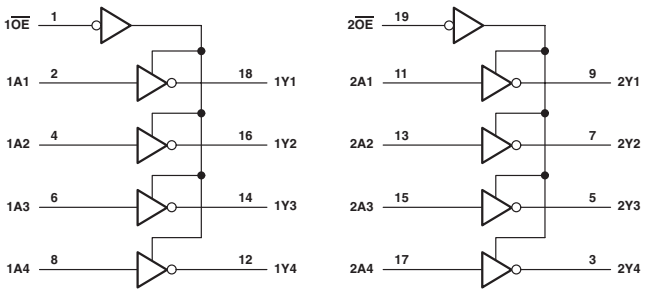
UNIT: ns

2240

OCTAL BUFFERS AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS

- I/O Ports Have 25-Ω Series Resistors, So No External Resistors Are Required (SN74ALS2240, SN74ABT2240A)
- Output Ports Have Equivalent 33-Ω Series Resistors, So No External Resistors Are Required (SN74BCT2240)

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	SN74 BCT	ABT	UNIT
I_{CCZ}	MAX	20	8	0.25	mA
I_{CCL}	MAX	23	76	30	mA
I_{OH}	MAX	-15	-12	-32	mA
I_{OL}	MAX	15	12	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	SN74 BCT	ABT
t_{PLH}	A	Y	MAX	10	5.7	4.8
t_{PHL}				10	4.4	5.4
t_{PZH}	$\overline{OE}$	Y	MAX	17	9.3	5.2
t_{PZL}				20	12.4	6.8
t_{PHZ}	$\overline{OE}$	Y	MAX	10	8.7	6.4
t_{PLZ}				15	10.6	6.2

UNIT: ns

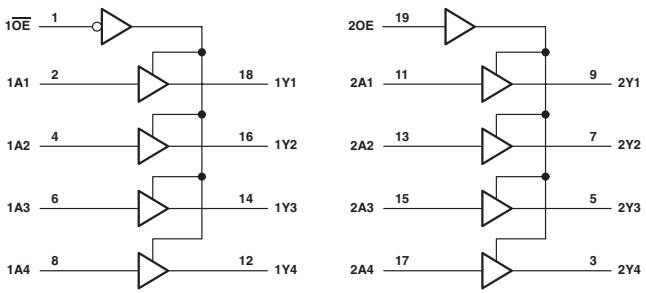
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

2241

OCTAL BUFFERS AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS

- Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required (SN74ABT2241A)
- Output Ports Have Equivalent 33-Ω Series Resistors, So No External Resistors Are Required (SN74BCT2241)

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 BCT	ABT	UNIT
I_{CCZ}	MAX	9	0.25	mA
I_{CCL}	MAX	76	30	mA
I_{OH}	MAX	-12	-32	mA
I_{OL}	MAX	12	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT	ABT
t_{PLH}	A	Y	MAX	4.9	4.7
t_{PHL}				6.9	5.6
t_{PZH}	1$\overline{OE}$	Y	MAX	8.9	5.8
t_{PZL}				10.3	8.4
t_{PHZ}	1$\overline{OE}$	Y	MAX	8.7	6.6
t_{PLZ}				11.3	6.4
t_{PZH}	2OE	Y	MAX	8.9	5.8
t_{PZL}				10.3	8.4
t_{PHZ}	2OE	Y	MAX	8.7	6.6
t_{PLZ}				11.3	6.4

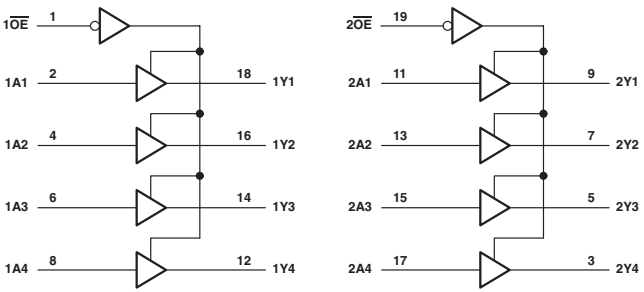
UNIT: ns

2244

OCTAL BUFFERS AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS

- Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required (SN74ABT2244A)
- Output Ports Have Equivalent 33-Ω Series Resistors, So No External Resistors Are Required (SN74BCT2244)
- Output Ports Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required (SN74LVC2244A)

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUT
$\overline{OE}$	A	Y
H	X	Z
L	L	L
L	H	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	SN74 BCT	ABT	LVC 3V	UNIT
I_{CCZ}	MAX	23	10	0.25	0.01	mA
I_{CCL}	MAX	22	77	30	0.01	mA
I_{OH}	MAX	-15	-12	-32	-12	mA
I_{OL}	MAX	15	12	12	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	SN74 BCT	ABT	LVC 3V
t_{PLH}	A	Y	MAX	16	4.9	4.7	5.5
t_{PHL}				17	6.7	5.6	5.5
t_{PZH}	$\overline{OE}$	Y	MAX	17	8.7	5.5	7.1
t_{PZL}				14	10.4	8.3	7.1
t_{PHZ}	$\overline{OE}$	Y	MAX	9	7.8	6.6	6.8
t_{PLZ}				9	9.8	5.8	6.8

UNIT: ns

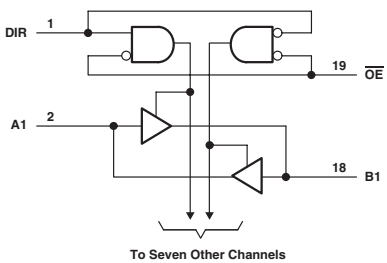
: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

2245

OCTAL TRANSCEIVER AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS

- B Port Has Equivalent 33-Ω Series Resistors, So No External Resistors Are Required (SN74BCT2245)
- B-Port Outputs Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required (SN74ABT2245)
- Outputs Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required (SN74ABTR2245)
- All Outputs Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required (SN74LVCR2245)
- B-Port Outputs Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required (SN74LVTH2245)

Logic Diagram



FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 BCT	ABT	ABTR	LVTH 3V	LVCR 3V	UNIT
I_{CCZ}	MAX	15	0.25	0.25	0.19	0.01	mA
I_{CCL}	MAX	100	32	32	5	0.01	mA
I_{OH} (A port)	MAX	-3	-32	-12	-32	-12	mA
I_{OH} (B port)	MAX	-12	-12	-12	-12	-12	mA
I_{OL} (A port)	MAX	24	64	12	64	12	mA
I_{OL} (B port)	MAX	12	12	12	12	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT	ABT	ABTR	LVTH 3V	LVCR 3V
t_{PLH}	A	B	MAX	5.8	3.8	3.8	4.4	6.3
t_{PHL}				7.8	4.5	4.5	4.4	6.3
t_{PLH}	B	A	MAX	7	3.6	3.8	3.5	6.3
t_{PHL}				7.7	4	4.5	3.5	6.3
t_{PZH}	$\overline{OE}$	B	MAX	9.9	6.1	6.1	6.2	8.2
t_{PZL}				12.2	6.3	6.3	6.2	8.2
t_{PHZ}	$\overline{OE}$	B	MAX	8.2	5.3	5.3	5.9	7.8
t_{PLZ}				9.2	4.8	4.8	5.4	7.8
t_{PZH}	$\overline{OE}$	A	MAX	11.1	5.5	6.1	5.5	8.2
t_{PZL}				11.4	5.7	6.3	5.5	8.2
t_{PHZ}	$\overline{OE}$	A	MAX	9.4	5.6	5.3	5.9	7.8
t_{PLZ}				7.6	4.5	4.8	5	7.8

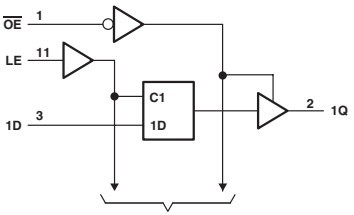
UNIT: ns

2373

25-Ω OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

- 3-State True Outputs with 25-Ω Sink Resistors
- Full Parallel Access for Loading
- Buffered Control Inputs

Logic Diagram



FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	F	UNIT
I_{CC}	MAX	66	mA
I_{OH}	MAX	-3	mA
I_{OL}	MAX	12	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	F
t_w	LE high		MIN	6
t_{su}	Data before LE↓		MIN	2
t_h	Data after LE↓		MIN	6
t_{PLH}	D	Q	MAX	9
t_{PHL}				7
t_{PLH}	LE	Q	MAX	13
t_{PHL}				8
t_{PZH}	$\overline{OE}$	Q	MAX	12
t_{PZL}				9.5
t_{PHZ}	$\overline{OE}$	Q	MAX	7.5
t_{PLZ}				6

UNIT:ns

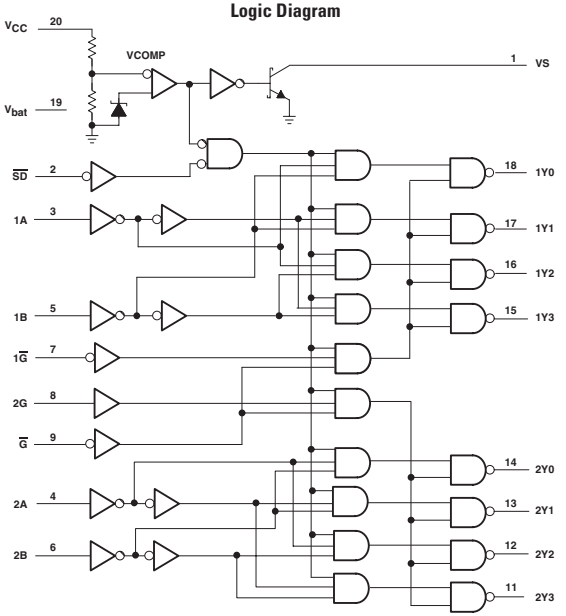
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

2414

MEMORY DECODER WITH ON-CHIP SUPPLY VOLTAGE MONITOR

- Built-In Supply-Voltage Monitor for V_{CC}
- Separate Enable Inputs for Easy Cascading

Logic Diagram



FUNCTION TABLE

INPUTS					OUTPUTS			
CONTROL			SELECT					
$\overline{G}$	1$\overline{G}$	$\overline{SD}$	1B	1A	1Y0	1Y1	1Y2	1Y3
H	X	X	X	X	H	H	H	H
X	H	X	X	X	H	H	H	H
X	X	L	X	X	H	H	H	H
L	L	H	L	L	L	H	H	H
L	L	H	L	H	H	L	H	H
L	L	H	H	L	H	H	L	H
L	L	H	H	H	H	H	H	L

INPUTS					OUTPUTS			
CONTROL			SELECT					
$\overline{G}$	2G	$\overline{SD}$	2B	2A	2Y0	2Y1	2Y2	2Y3
H	X	X	X	X	H	H	H	H
X	H	X	X	X	H	H	H	H
X	X	L	X	X	H	H	H	H
L	H	H	L	L	L	H	H	H
L	H	H	L	H	H	L	H	H
L	H	H	H	L	H	H	L	H
L	H	H	H	H	H	H	H	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 BCT	UNIT
I_{CC}	MAX	3	mA
I_{bat} (Output low)	MAX	3	mA
I_{OH}	MAX	-0.4	mA
I_{OL} (Y Output)	MAX	8	mA
I_{OL} (I/S Output)	MAX	20	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT
t_{PLH}	A or B	Any Y	MAX	12
t_{PHL}				12
t_{PLH}	Any $\overline{G}$	Any Y	MAX	10
t_{PHL}				11
t_{PLH}	$\overline{SD}$	Any Y	MAX	12
t_{PHL}				12
t_{PLH}	V_{cc}	Any Y	MAX	250
t_{PHL}				250
t_{PLH}	V_{cc}	VS	MAX	250
t_{PHL}				250

UNIT: ns

2541

OCTAL LINE DRIVER/MOS DRIVER WITH 3-STATE OUTPUTS

- Outputs Have 25-Ω Series Resistor So No External Resistors Are Required

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

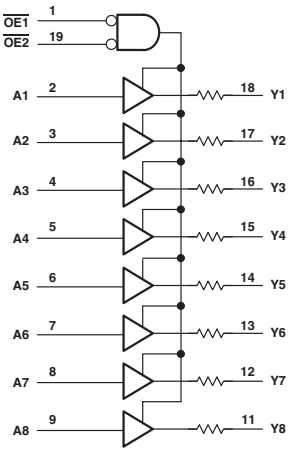
PARAMETER	MAX or MIN	ALS	UNIT
I_{CCZ}	MAX	22	mA
I_{CCL}	MAX	25	mA
I_{OH}	MAX	-0.4	mA
I_{OL}	MAX	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
t_{PLH}	A	Y	MAX	15
t_{PHL}				12
t_{PZH}	$\overline{OE}$	Y	MAX	15
t_{PZL}				20
t_{PHZ}	$\overline{OE}$	Y	MAX	10
t_{PLZ}				12

UNIT: ns

Logic Diagram



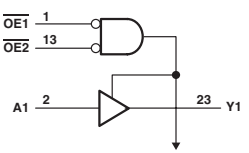
All output resistors are 25 Ω.

2827

10-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required (SN74ABT2827)
- Output Ports Have Equivalent 25-Ω Resistors; No External Resistors Are Required (SN74BCT2827C)

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 BCT	ABT	UNIT
I_{CCZ}	MAX	6	0.25	mA
I_{CCL}	MAX	40	40	mA
I_{OH}	MAX	-1	-12	mA
I_{OL}	MAX	12	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT	ABT
t_{PLH}	A	Y	MAX	6	5.5
t_{PHL}				7.8	5.1
t_{PZH}	$\overline{OE}$	Y	MAX	10.7	6.7
t_{PZL}				12.9	7.8
t_{PHZ}	$\overline{OE}$	Y	MAX	13	7.2
t_{PLZ}				10	7.5

UNIT: ns

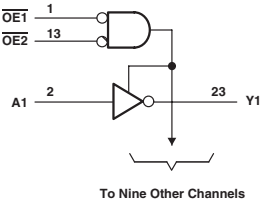
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

2828

10-BIT BUS/MOS MEMORY DRIVERS WITH 3-STATE INVERTING

- Output Ports Have Equivalent 33-Ω Series Resistors, So No External Resistors Are Required (SN74BCT2828)

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 BCT	UNIT
I_{CCZ}	MAX	6	mA
I_{CCL}	MAX	40	mA
I_{OH}	MAX	-1	mA
I_{OL}	MAX	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT
t_{PLH}	A	Y	MAX	6.6
t_{PHL}				5
t_{PZH}	$\overline{OE}$	Y	MAX	9
t_{PZL}				11.5
t_{PHZ}	$\overline{OE}$	Y	MAX	10.8
t_{PLZ}				8.7

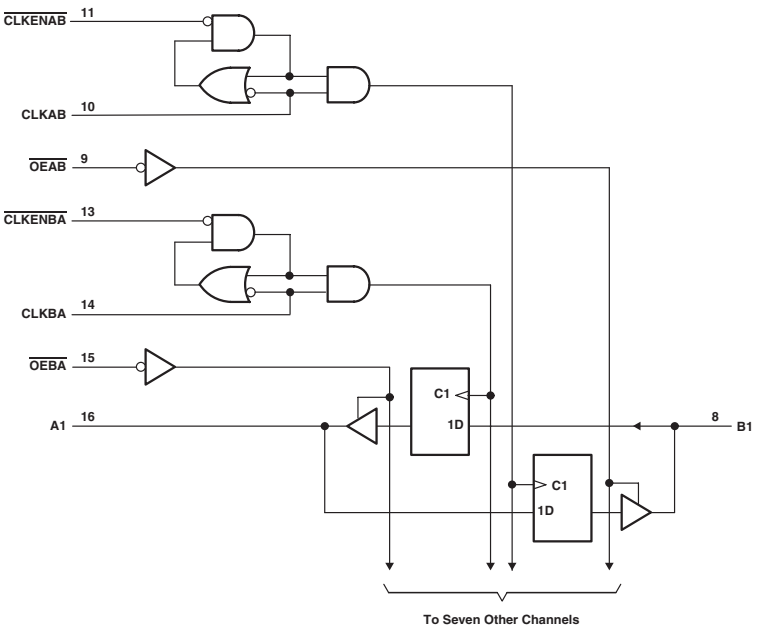
UNIT: ns

2952

OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

- Two 8-Bit Back-to-Back Registers Store Data Flowing in Both Directions
- Noninverting Outputs
- 3-State Outputs

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE†

INPUTS				OUTPUT B
$\overline{CLKENAB}$	CLKAB	$\overline{OEAB}$	A	
H	X	L	X	B_0
X	H or L	L	X	B_0
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

† A-to-B data flow is shown; B-to-A data flow is similar but uses $\overline{CLKENBA}$, CLKBA, and $\overline{OEBA}$.
‡ Level of B before the indicated steady-state input conditions were established

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	SN74 BCT	ABT	LVTH 3V	LVC 3V	UNIT
I_{CC}		MAX	55	35	5	0.01	mA
I_{OH}	A	MAX	-3	-32	-32	-24	mA
	B		-15	-32	-32	-24	mA
I_{OL}	A	MAX	24	64	64	24	mA
	B		64	64	64	24	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT	ABT	LVTH 3V	LVC 3V
f_{max}			MIN	125	150	150	150
t_w	CLK "H"		MIN	4	3.3	3.3	3.3
	CLK "L"			4	3.3	3.3	3.3
t_{su}	A or B before CLK High		MIN	2.5	2.5	1.5	1.3
	A or B before CLK Low			2.5	2.5	1.5	-
	$\overline{CLKENAB}$ or $\overline{CLKENBA}$ High			2	3	1.5	1.1
	$\overline{CLKENAB}$ or $\overline{CLKENBA}$ Low			2	3	1.9	-
t_h	A or B after CLK		MIN	1.5	1.5	1	1.1
	$\overline{CLKENAB}$ or $\overline{CLKENBA}$			2.5	2	1.2	1.1
t_{PLH}	CLKBA	A,B	MAX	9	5.9	4.6	8.2
t_{PHL}	CLKAB			10.5	6.3	4.6	8.2
t_{PZH}	$\overline{OEBA}$	A,B	MAX	8.2	5.6	4.6	7.8
t_{PZL}	$\overline{OEAB}$			12.9	6.6	4.6	7.8
t_{PHZ}	$\overline{OEBA}$	A,B	MAX	8.4	6.4	5.4	7.8
t_{PLZ}	$\overline{OEAB}$			7	6.2	5.1	7.8

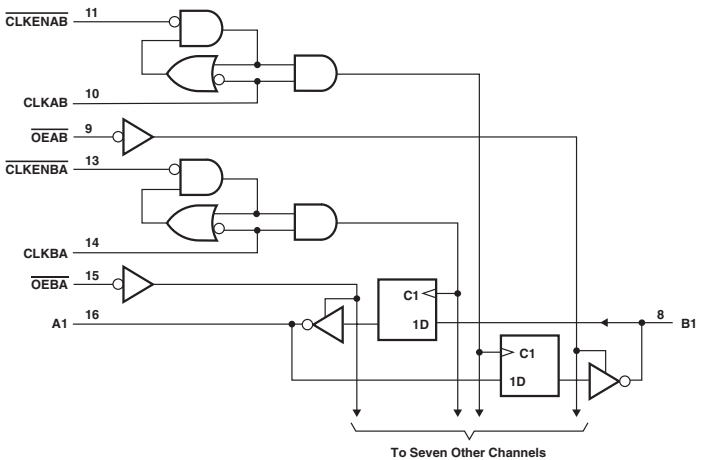
UNIT fmax : MHz other : ns

2953

OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

- Two 8-Bit, Back-to-Back Registers Store Data Flowing in Both Directions
- Inverting Outputs
- 3-State Outputs

Logic Diagram



FUNCTION TABLE†

INPUTS				OUTPUT
$\overline{OEAB}$	CLKAB	$\overline{OEAB}$	A	B
H	↑	L	X	A_0
L	↑	L	L	H
L	↑	L	H	L
X	X	H	X	Z

† A-to-B data flow is shown; B-to-A data flow is similar but uses $\overline{CEBA}$, CLKBA, and $\overline{OEBA}$.
‡ Level of B before the indicated steady-state input conditions were established

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	SN74 BCT	UNIT
I_{CC}		MAX	55	mA
I_{OH}	A	MAX	-3	mA
	B		-15	mA
I_{OL}	A	MAX	24	mA
	B		64	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT
f_{max}			MIN	110
t_w	CLK "H"		MIN	4.5
	CLK "L"			4.5
t_{su}	A or B High		MIN	2.5
	A or B Low			2.5
	$\overline{CLKENAB}$ or $\overline{CLKENBA}$ High			2
	$\overline{CLKENAB}$ or $\overline{CLKENBA}$ Low			2
t_h	A or B		MIN	1.5
	$\overline{CLKENAB}$ or $\overline{CLKENBA}$			2
t_{PLH}	CLKBA	A,B	MAX	9.5
t_{PHL}	CLKAB			10.2
t_{PZH}	$\overline{OEBA}$	A,B	MAX	8.8
t_{PZL}	$\overline{OEAB}$			14
t_{PHZ}	$\overline{OEBA}$	A,B	MAX	9.1
t_{PLZ}	$\overline{OEAB}$			7.6

UNIT fmax : MHz other : ns

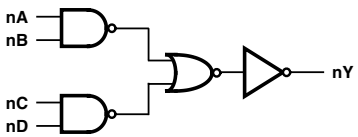
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

4002

DUAL 4-INPUT POSITIVE-NOR GATES

● $Y = \overline{A + B + C + D}$

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
L	L	L	L	H
H	X	X	X	L
X	H	X	X	L
X	X	H	X	L
X	X	X	H	L

NOTES:
H = High Voltage Level
L = Low Voltage Level
X = Irrelevant

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	CD74 HC	UNIT
I_{CC}	MAX	0.02	0.04	mA
I_{OH}	MAX	-4	-4	mA
I_{OL}	MAX	4	4	mA

SWITCHING CHARACTERISTICS

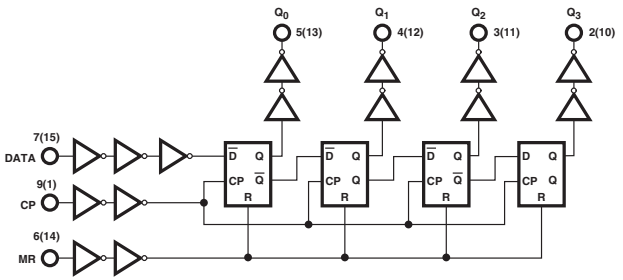
PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC
t_{PLH}	A, B, C, D	Y	MAX	28	30
t_{PHL}			MAX	28	30

UNIT:ns

4015

DUAL 4-STAGE STATIC SHIFT REGISTER

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT			
CP	D	R	Q_0	Q_1	Q_2	Q_3
↑	l	L	L	q'_0	q'_1	q'_2
↑	h	L	H	q'_0	q'_1	q'_2
↓	X	L	q'_0	q'_1	q'_2	q'_3
X	X	H	L	L	L	L

NOTES:
H = High Voltage Level
h = High Voltage Level One Set-up Time Prior to the Low to High Clock Transition
L = Low Voltage Level
l = Low Voltage Level One Set-up Time Prior to the Low to High Clock Transition
X = Don't Care.
↑ = Low to High Clock Transition
↓ = High to Low Clock Transition
q'_n = Lower case letters indicate the state of the referenced output one set-up time prior to the Low to High clock transition.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	UNIT
I_{CC}	MAX	0.16	mA
I_{OH}	MAX	-4	mA
I_{OL}	MAX	4	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

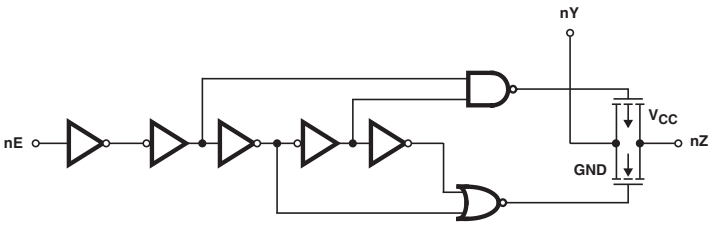
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC
f_{max}			MIN	20
t_W	Clock		MIN	24
	MR			45
t_{SUL}	Data-In to CP		MIN	18
t_{SUH}			MIN	18
t_H	Data-In to CP		MIN	0
t_{PLH}	Clock	Qn	MAX	54
t_{PHL}				54
t_{PLH}	MR	Qn (Clock High)	MAX	83
t_{PHL}				83
t_{PLH}	MR	Qn (Clock Low)	MAX	98
t_{PHL}				98

UNIT fmax : MHz other : ns

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

4016
QUAD BILATERAL SWITCH

Logic Diagram



FUNCTION TABLE

INPUT nE	SWITCH
L	OFF
H	ON

NOTES:
H = High Level Voltage
L = Low Level Voltage

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	UNIT
I_{CC}	MAX	0.04	mA
R_{ON}	MAX	480	Ω

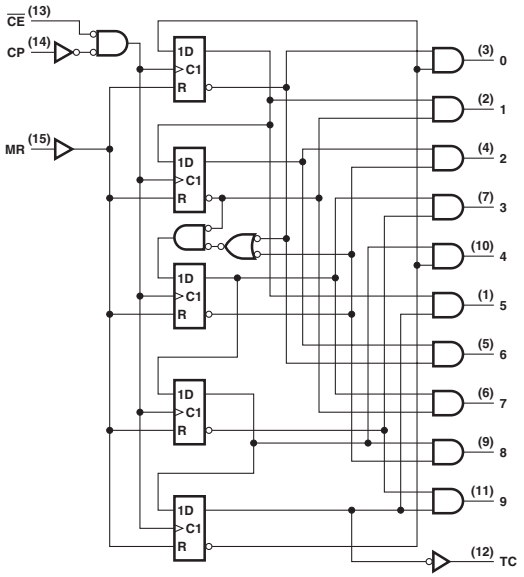
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC
t_{PLH}	Switch In	Switch Out	MAX	18
t_{PHL}				18
t_{PZH}	En	Z	MAX	57
t_{PZL}				57
t_{PHZ}	En	Z	MAX	44
t_{PLZ}				44

UNIT:ns

4017
DECADE COUNTERS/DIVIDER

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT STATE†
CP	$\overline{CE}$	MR	
L	X	L	No Change
X	H	L	No Change
X	X	H	"0" = H, "1"-"9" = L
↑	L	L	Increments Counter
↓	X	L	No Change
X	↑	L	No Change
H	↓	L	Increments Counter

NOTES:
H = High Level
L = Low Level
↑ = High to Low Transition
↓ = Low to High Transition
X = Don't Care
† If n < 5 TC = H, Otherwise = L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	CD74 HC	UNIT
I_{CC}	MAX	0.08	0.16	mA
I_{OH}	MAX	-4	-4	mA
I_{OL}	MAX	4	4	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC
f_{max}			MIN	25	20
t_w	CP		MIN	20	24
	MR			20	24
t_{su}	$\overline{CE}$ to CP		MIN	13	22
	CLK Inactive			13	-
t_h	$\overline{CE}$ to CP		MIN	5	0
t_{PLH}	CP	0 to 9	MAX	58	69
t_{PHL}				58	69
t_{PLH}	$\overline{CE}$	0 to 9	MAX	63	75
t_{PHL}				63	75
t_{PLH}	MR	0 to 9	MAX	58	69
t_{PHL}				58	69
t_{PLH}	MR	TC	MAX	-	69
t_{PHL}				58	69

UNIT fmax : MHz, other : ns

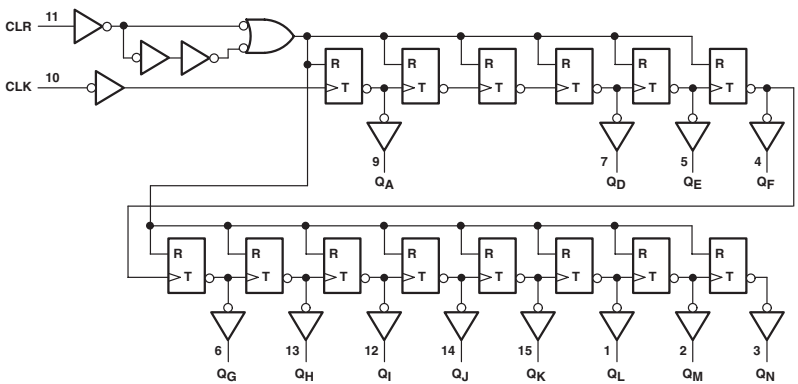
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

4020

14-STAGE BINARY COUNTERS

- Same Pinouts as CMOS4020
- V_{CC}: 2V to 6V

Logic Diagram (SN74HC)



FUNCTION TABLE (SN74)

CLK	CLR	OUTPUT
↑	L	No Change
↓	L	Advance to Next State
X	H	All Outputs Are Low

NOTE: H = High Voltage Level, L = Low Voltage Level, X = Don't Care, = ↑ Transition from Low to High Level, ↓ = Transition from High to Low.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	0.08	0.16	0.16	mA
I_{OH}	MAX	-4	-4	-4	mA
I_{OL}	MAX	4	4	4	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

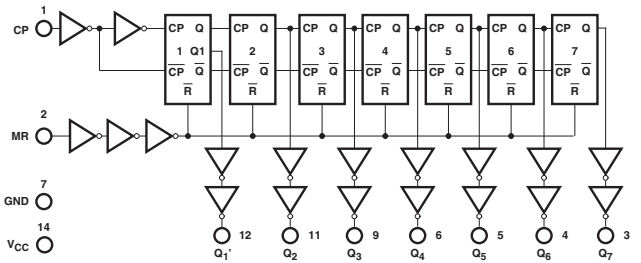
PARAMETER		INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT
f_{max}				MIN	22	20	16
t_w	CLK (CD74: CP)			MIN	23	24	30
	CLR high				18	24	30
t_{su}	CLK (CD74: CP)	CLR inactive before CLK ↓		MIN	15	-	-
t_{PLH}		CLK (CD74: CP)	Q_A ($CD74: Q_1$)	MAX	38	42	60
t_{PHL}					38	42	60
t_{PHL}		CLR (CD74: CP)	Any	MAX	35	51	60

UNIT fmax : MHz other : ns

4024

7-STAGE BINARY COUNTERS

Logic Diagram



FUNCTION TABLE (SN74)

CLK	CLR	OUTPUT
↑	L	No Change
↓	L	Advance to Next State
X	H	All Outputs Are Low

NOTE: H = High Voltage Level, L = Low Voltage Level, X = Don't Care, = ↑ Transition from Low to High Level, ↓ = Transition from High to Low.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	0.08	0.16	0.16	mA
I_{OH}	MAX	-4	-4	-4	mA
I_{OL}	MAX	4	4	4	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT
f_{max}			MIN	22	20	16
t_w	CP (CLK)		MIN	23	24	30
	MR (CLR H)			20	24	30
t_{su}	CLR iow before CLK		MIN	20	-	-
t_{PLH}	CP (CLK)	Q1 (QA)	MAX	30	42	60
t_{PHL}				30	42	60
t_{PLH}	MR (CLR)	any Q	MAX	-	51	60
t_{PHL}				33	51	60

UNIT fmax : MHz, other : ns

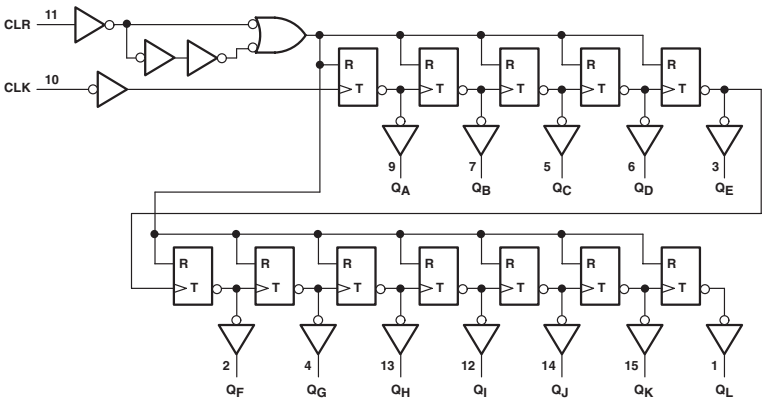
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

4040

12-STAGE BINARY COUNTERS

- Same Pinouts as CMOS4040
- V_{CC}: 2V to 6V

Logic Diagram (SN74HC)



FUNCTION TABLE

CLK	CLR	OUTPUT
↑	L	No Change
↓	L	Advance to Next State
X	H	All Outputs Are Low

NOTE: H = High Voltage Level, L = Low Voltage Level, X = Don't Care, ↑ = Transition from Low to High Level, ↓ = Transition from High to Low.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	LV 3V	LV 5V	UNIT
I_{CC}	MAX	0.08	0.16	0.16	-	0.02	mA
I_{OH}	MAX	-4	-4	-4	-6	-12	mA
I_{OL}	MAX	4	4	4	6	12	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

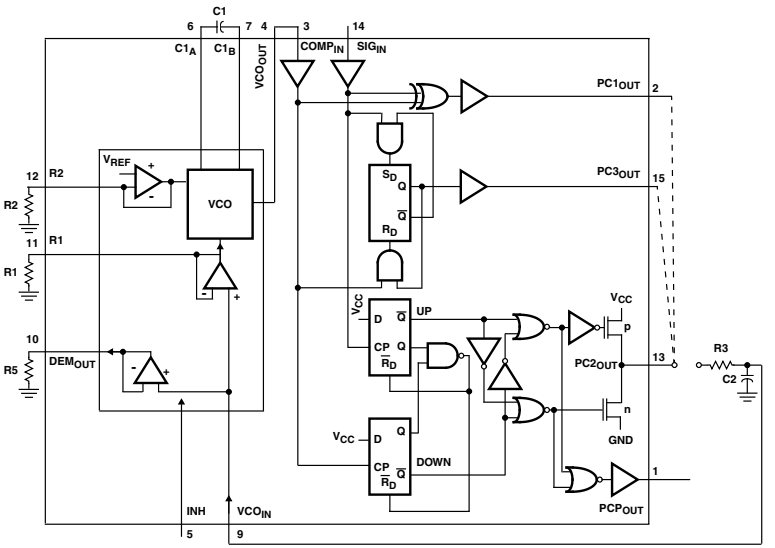
PARAMETER		INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	LV 3V	LV 5V
f_{max}				MIN	22	20	16	50	80
t_w	CLK (CP)			MIN	23	24	30	5	5
	CLR (MR) high				18	24	30	5	5
t_{su}	CLK (CP)	CLR(MR) inactive before CLK(CP) ↓		MIN	15	-	-	5	5
t_{PLH}		CLK (CP)	Q_A (Q_1)	MAX	38	42	60	17.5	10.5
t_{PHL}					38	42	60	17.5	10.5
t_{PHL}		CLR (MR)	Any	MAX	35	51	60	18.5	12

UNIT fmax : MHz other : ns

4046

PHASE-LOCKED-LOOP WITH VCO

Logic Diagram



Pin Descriptions

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	PCP_{OUT}	Phase Comparator Pulse Output
2	$PC1_{OUT}$	Phase Comparator 1 Output
3	$COMP_{IN}$	Comparator Input
4	VCO_{OUT}	VCO Output
5	INH	Inhibit Input
6	$C1_A$	Capacitor C1 Connection A
7	$C1_B$	Capacitor C1 Connection B
8	GND	Ground (0V)
9	VCO_{IN}	VCO Input
10	DEM_{OUT}	Demodulator Output
11	R_1	Resistor R1 Connection
12	R_2	Resistor R2 Connection
13	$PC2_{OUT}$	Phase Comparator 2 Output
14	SIG_{IN}	Signal Input
15	$PC3_{OUT}$	Phase Comparator 3 Output
16	V_{CC}	Positive Supply Voltage

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	0.16	0.16	mA
I_{OH}	MAX	-4	-4	mA
I_{OL}	MAX	4	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
t_{PLH}	SIG_{IN}	PCI_{OUT}	MAX	60	68
t_{PHL}	$COMP_{IN}$			60	68
t_{PLH}	SIG_{IN}	PCP_{OUT}	MAX	90	102
t_{PHL}	$COMP_{IN}$			90	102
t_{PLH}	SIG_{IN}	$PC3_{OUT}$	MAX	74	87
t_{PHL}	$COMP_{IN}$			74	87
t_{TLH}	A	$\overline{Y}$	MAX	22	22
t_{THL}				22	22
t_{PZH}	SIG_{IN}	$PC2_{OUT}$	MAX	80	90
t_{PZL}	$COMP_{IN}$			80	90
t_{PLZ}	SIG_{IN}	$PC2_{OUT}$	MAX	95	102
t_{PHZ}	$COMP_{IN}$			95	102

UNIT:ns

4049

HEX INVERTING BUFFERS

Logic Diagram

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	UNIT
I_{CC}	MAX	0.04	mA
I_{OH}	MAX	-4	mA
I_{OL}	MAX	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC
t_{PLH}	nA	$n\overline{Y}$	MAX	26
t_{PHL}				26

UNIT:ns

4050

HEX NON-INVERTING BUFFERS

Logic Diagram

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	UNIT
I_{CC}	MAX	0.04	mA
I_{OH}	MAX	-4	mA
I_{OL}	MAX	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC
t_{PLH}	nA	nY	MAX	26
t_{PHL}				26

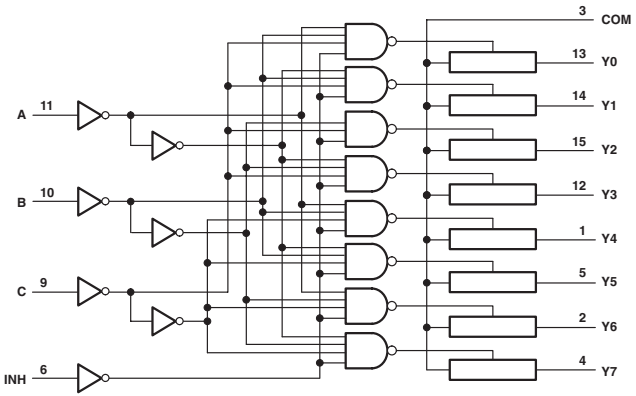
UNIT:ns

: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

4051

8-CHANNEL ANALOG MULTIPLEXERS / DEMULTIPLEXERS

Logic Diagram (SN74LV)



FUNCTION TABLE (SN74)

INPUTS				ON CHANNEL
INH	C	B	A	
L	L	L	L	Y0
L	L	L	H	Y1
L	L	H	L	Y2
L	L	H	H	Y3
L	H	L	L	Y4
L	H	L	H	Y5
L	H	H	L	Y6
L	H	H	H	Y7
H	X	X	X	None

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	LV 3V	LV 5V	UNIT
I_{CC}	MAX	0.16	0.16	-	0.02	mA
R_{ON}	MAX	180	180	190	100	Ω

SWITCHING CHARACTERISTICS

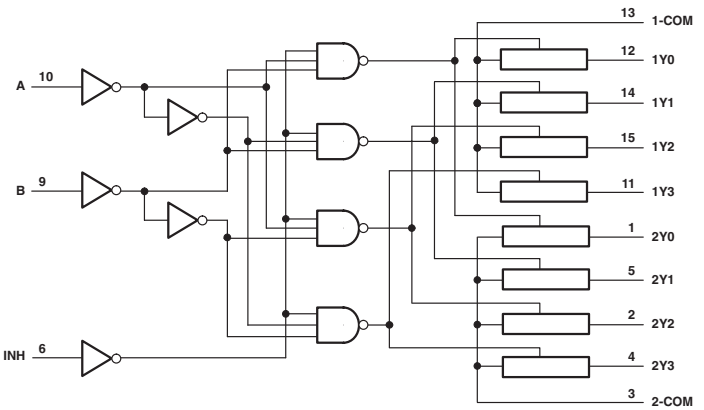
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT	LV 3V	LV 5V
t_{PLH}	COM or Yn (An)	Yn (An) or COM	MAX	18	18	12	8
t_{PHL}				18	18	12	8
t_{PZH}	INH	COM or Yn (An)	MAX	68	83	25	18
t_{PZL}				68	83	25	18
t_{PHZ}	INH	COM or Yn (An)	MAX	68	68	25	18
t_{PLZ}				68	68	25	18

UNIT: ns

4052

DUAL 4-CHANNEL ANALOG MULTIPLEXERS / DEMULTIPLEXERS

Logic Diagram (SN74LV)



FUNCTION TABLE (SN74)

INPUTS			ON CHANNEL
INH	B	A	
L	L	L	1Y0, 2Y0
L	L	H	1Y1, 2Y1
L	H	L	1Y2, 2Y2
L	H	H	1Y3, 2Y3
H	X	X	None

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	LV 3V	LV 5V	UNIT
I_{CC}	MAX	0.16	0.16	-	0.02	mA
R_{ON}	MAX	180	180	190	100	Ω

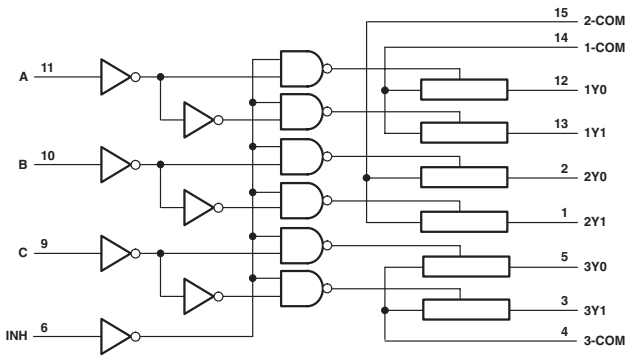
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT	LV 3V	LV 5V
t_{PLH}	COM or Yn (An)	Yn (An) or COM	MAX	18	18	12	8
t_{PHL}				18	18	12	8
t_{PZH}	INH	COM or Yn (An)	MAX	98	105	25	18
t_{PZL}				98	105	25	18
t_{PHZ}	INH	COM or Yn (An)	MAX	75	75	25	18
t_{PLZ}				75	75	25	18

UNIT: ns

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

Logic Diagram (SN74LV)



FUNCTION TABLE (SN74)

INPUTS				ON CHANNEL
INH	C	B	A	
L	L	L	L	1Y0, 2Y0, 3Y0
L	L	L	H	1Y1, 2Y0, 3Y0
L	L	H	L	1Y0, 2Y1, 3Y0
L	L	H	H	1Y1, 2Y1, 3Y0
L	H	L	L	1Y0, 2Y0, 3Y1
L	H	L	H	1Y1, 2Y0, 3Y1
L	H	H	L	1Y0, 2Y1, 3Y1
L	H	H	H	1Y1, 2Y1, 3Y1
H	X	X	X	None

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	LV 3V	LV 5V	UNIT
I_{CC}	MAX	0.16	0.16	-	0.02	mA
R_{ON}	MAX	180	180	190	100	Ω

SWITCHING CHARACTERISTICS

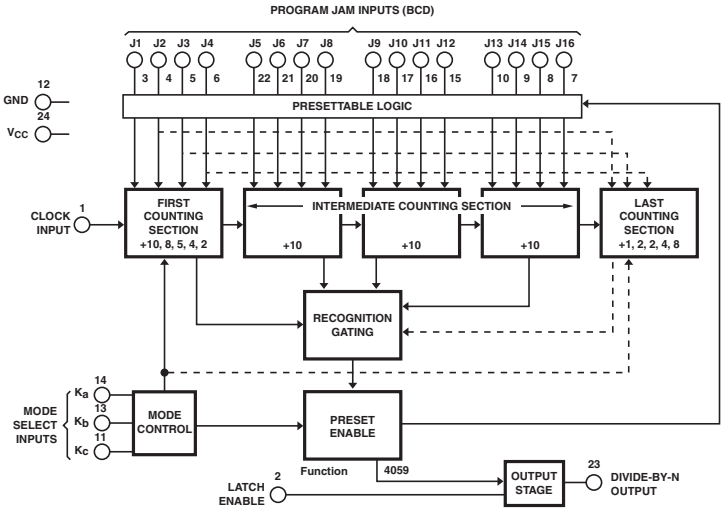
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT	LV 3V	LV 5V
t_{PLH}	COM or Yn (An, Bn, Cn)	Yn (An, Bn, Cn) or COM	MAX	18	18	12	8
t_{PHL}				18	18	12	8
t_{PZH}	INH	COM or Yn (An, Bn, Cn)	MAX	66	72	25	18
t_{PZL}				66	72	25	18
t_{PHZ}	INH	COM or Yn (An, Bn, Cn)	MAX	63	66	25	18
t_{PLZ}				63	66	25	18

UNIT: ns

4059

CMOS PROGRAMMABLE DIVIDE-BY-N COUNTER

Function Diagram



FUNCTION TABLE

MODE SELECT INPUT		
Ka	Kb	Kc
H	H	H
L	H	H
H	L	H
L	L	H
H	H	L
X	L	L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	UNIT
I_{CC}	MAX	0.16	mA
I_{OH}	MAX	-4	mA
I_{OL}	MAX	4	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC
f_{max}	CP		MIN	18
t_w	CP		MIN	27
t_{su}	Kb, Kc to CP		MIN	22
t_{PLH}	CP	Q	MAX	60
t_{PHL}				60
t_{PLH}	LE	Q	MAX	53
t_{PHL}				53

UNIT fmax : MHz other : ns

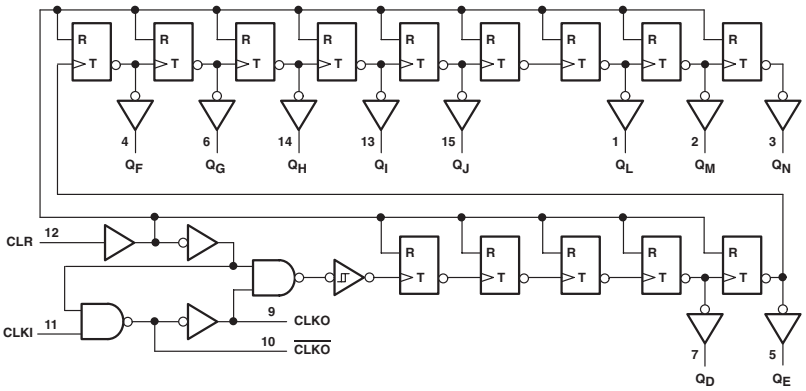
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

4060

ASYNCHRONOUS 14-STAGE BINARY COUNTERS AND OSCILLATORS

- Same Pinouts as CMOS4060
- Allow Design of Either RC or Crystal Oscillator Circuits
- V_{CC}: 2V to 6V

Logic Diagram (SN74HC)



FUNCTION TABLE (SN74)

INPUTS		OUTPUTS		
CLKI	CLR	Q_D to Q_N	CLKO	$\overline{CLKO}$
↑	L	No Change	↑	↓
↓	L	Advance to Next State	↓	↑
X	H	All Outputs are Low	L	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	0.08	0.16	0.16	mA
I_{OH}	MAX	-4	-4	-4	mA
I_{OL}	MAX	4	4	4	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT
f_{max}			MIN	22	20	20
t_w	CLKI (ϕI)		MIN	23	24	24
	CLR high (MR)			23	24	38
t_{su}	CLR inactive before CLK ↓		MIN	40	-	-
t_{PLH}	CLKI (ϕI)	Q_D (Q4)	MAX	123	90	100
t_{PHL}				123	90	100
t_{PHL}	CLR (MR)	Any	MAX	35	53	66

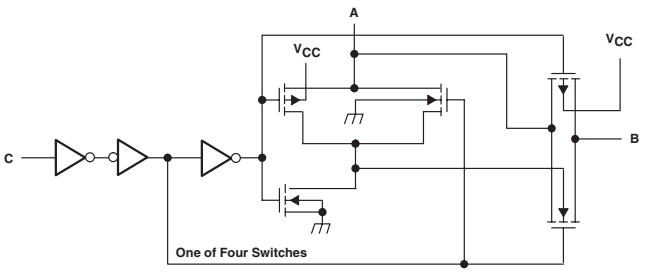
UNIT fmax : MHz other : ns

4066

QUADRUPLE BILATERAL SWITCHES

- Same Pinouts as CMOS4016, 4066
- Low On-State Impedance: 50-Ω TYP at V_{CC} = 6V
- Individual Switch Controls
- Extremely Low Input Current
- High On-Off Output Voltage Ratio
- Low Crosstalk Between Switches

Logic Diagram (SN74)



FUNCTION TABLE (SN74)

INPUT (C)	SWITCH
L	OFF
H	ON

NOTE:
H = High Level
L = Low Level

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	AHC	LV 3V	LV 5V	UNIT
I_{CC}	MAX	0.02	0.04	0.04	0.02	-	0.02	mA
R_{ON}	MAX	106	128	128	100	190	100	Ω

SWITCHING CHARACTERISTICS

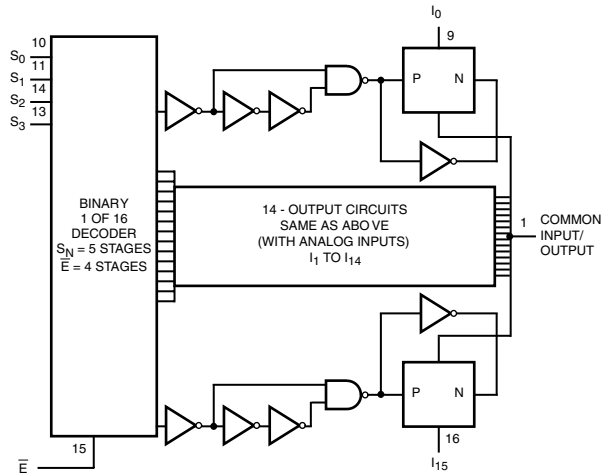
PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	AHC	LV 3V	LV 5V
t_{PLH}	A or B (Y or Z)	B or A (Z or Y)	MAX	15	18	18	8	12	8
t_{PHL}				15	18	18	8	12	8
t_{PZH}	C (E)	A or B (Y or Z)	MAX	45	30	36	16	22	16
t_{PZL}				45	30	36	16	22	16
t_{PHZ}	C (E)	A or B (Y or Z)	MAX	50	45	53	16	22	16
t_{PLZ}				50	45	53	16	22	16

UNIT: ns

: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

16-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

Function Diagram



FUNCTION TABLE

S0	S1	S2	S3	$\overline{E}$	SELECTED CHANNEL
X	X	X	X	X	None
0	0	0	0	0	0
1	0	0	0	0	1
0	1	0	0	0	2
1	1	0	0	0	3
0	0	1	0	0	4
1	0	1	0	0	5
0	1	1	0	0	6
1	1	1	0	0	7
0	0	0	1	0	8
1	0	0	1	0	9
0	1	0	1	0	10
1	1	0	1	0	11
0	0	1	1	0	12
1	0	1	1	0	13
0	1	1	1	0	14
1	1	1	1	0	15

NOTES:
H = High Level
L = Low Level
X = Don't Care

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	0.16	0.16	mA
R_{ON}	MAX	240	240	Ω

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
t_{PLH}	Switch In	COMON I/O	MAX	22	22
t_{PHL}				22	22
t_{PZH}	$\overline{E}$	COMON I/O	MAX	83	90
t_{PZL}				83	90
t_{PHZ}	$\overline{E}$	COMON I/O	MAX	83	83
t_{PLZ}				83	83
t_{PZH}	Sn	COMON I/O	MAX	90	90
t_{PZL}				90	90
t_{PHZ}	Sn	COMON I/O	MAX	87	87
t_{PLZ}				87	87

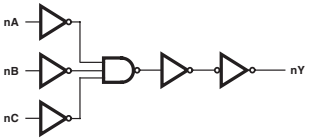
UNIT:ns

4075

TRIPLE 3-INPUT OR GATES

● Y = A + B + C

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
L	L	L	L
H	X	X	H
X	H	X	H
X	X	H	H

NOTES:
H = High Voltage Level
L = Low Voltage Level
X = Don't Care

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	0.02	0.04	0.04	mA
I_{OH}	MAX	-4	-4	-4	mA
I_{OL}	MAX	4	4	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT
t_{PLH}	A, B or C	Y	MAX	25	30	36
t_{PHL}	A, B or C	Y	MAX	25	30	36

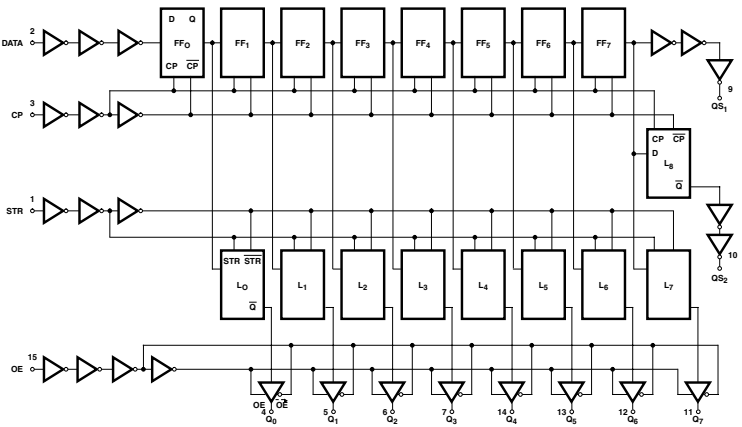
UNIT:ns

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

4094

8-STAGE SHIFT AND STORE BUS REGISTER, THREE-STATE

Logic Diagram



FUNCTION TABLE

INPUTS				PALALLEL OUTPUT		SERIAL OUTPUT	
CP	OE	STR	D	Q_0	Q_n	QS_1‡	QS_2
↑	L	X	X	Z	Z	Q'_6	NC
↓	L	X	X	Z	Z	NC	Q'_7
↑	H	L	X	NC	NC	Q'_6	NC
↑	H	H	L	L	Q_n-1	Q'_6	NC
↑	H	H	H	H	Q_n-1	Q'_6	NC
↓	H	H	H	NC	NC	NC	Q'_7

NOTES:

†. H = High Voltage Level, L = Low Voltage Level, X = Don't Care,
NC = No charge, Z = High Impedance Off-state,
↑ = Transition from Low to High Level, ↓ = Transition from High Low.

‡. At the positive clock edge the information in the seventh resister stage is transferred to the 8th register stage and QS_1 output.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	0.16	0.16	mA
I_{OL}	MAX	4	4	mA
I_{OH}	MAX	-4	-4	mA

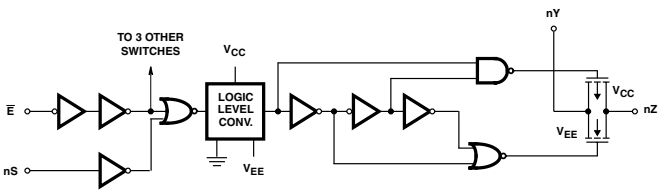
TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
t_W	CP		MIN	24	24
t_{WH}	STR		MIN	24	24
t_{SU}	Data		MIN	15	15
	STR			30	30
t_H	Data		MIN	3	4
	STR			0	0
t_{PLH}	CP	QS1	MAX	45	-
t_{PHL}				45	-
t_{PLH}	CP	QS2	MAX	41	-
t_{PHL}				41	-
t_{PLH}	CP	Qn	MAX	59	-
t_{PHL}				59	-
t_{PLH}	STR	Qn	MAX	54	-
t_{PHL}				54	-
t_{PZH}	OE	Qn	MAX	53	-
t_{PZL}				53	-
t_{PLZ}	OE	Qn	MAX	38	-
t_{PHZ}				38	-

UNIT:ns

4316
QUAD ANALOG SWITCH WITH LEVEL TRANSLATION

Logic Diagram



FUNCTION TABLE

INPUTS		
$\overline{E}$	S	SWITCH
L	L	OFF
L	H	ON
H	X	OFF

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	0.32	0.32	mA
R_{ON}	MAX	270	270	Ω

SWITCHING CHARACTERISTICS

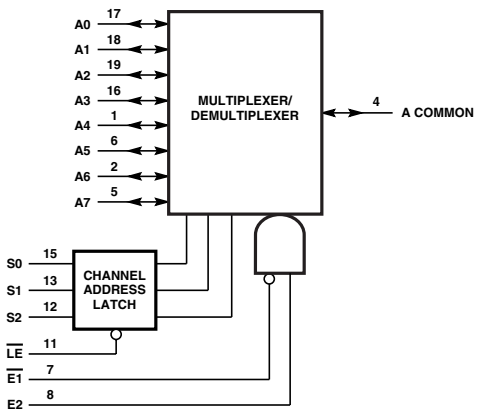
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
t_{PLH}	Switch in	Switch out	MAX	18	18
t_{PHL}				18	18
t_{PZH}	$\overline{E}$	Z	MAX	62	66
t_{PZL}				62	85
t_{PLZ}	$\overline{E}$	Z	MAX	62	75
t_{PHZ}				62	-
t_{PZH}	nS	Z	MAX	53	60
t_{PZL}				53	75
t_{PLZ}	nS	Z	MAX	53	-
t_{PHZ}				53	66

UNIT:ns

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

ANALOG MULTIPLEXERS/DEMULTIPLEXERS WITH LATCH

Logic Diagram



FUNCTION TABLE

INPUTS					"ON"† SWITCCHES
$\overline{E1}$	E2	S2	S1	S0	$\overline{LE}$ = H
L	H	L	L	L	A_0
L	H	L	L	H	A_1
L	H	L	H	L	A_2
L	H	L	H	H	A_3
L	H	H	L	L	A_4
L	H	H	L	H	A_5
L	H	H	H	L	A_6
L	H	H	H	H	A_7
H	L	X	X	X	None

NOTES:
† When LE is low S0-S2 data are latched and switches cannot change state.
H = High Voltage Level, L = Low Voltage Level, X = Don't Care

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	0.32	0.32	mA
R_{ON}	MAX	240	240	Ω

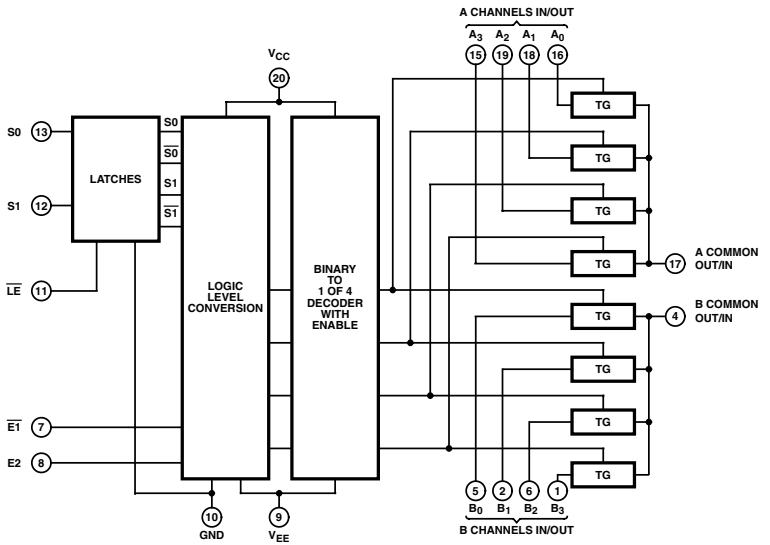
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
t_W	$\overline{LE}$		MIN	30	28
t_{su}	Sn to $\overline{LE}$		MAX	18	18
t_H	Sn to $\overline{LE}$		MIN	5	5
t_{PLH}	Switch In	Switch Out	MAX	11	11
t_{PHL}				11	11
t_{PZH}	$\overline{E1}$, E2, $\overline{LE}$	Vos	MAX	90	113
t_{PZL}				90	113
t_{PZH}	Sn	Vos	MAX	90	113
t_{PZL}				90	113
t_{PLZ}	$\overline{E1}$	Vos	MAX	75	83
t_{PHZ}				75	83
t_{PLZ}	E2	Vos	MAX	75	90
t_{PHZ}				75	90
t_{PLZ}	$\overline{LE}$	Vos	MAX	83	90
t_{PHZ}				83	90
t_{PHZ}	Sn	Vos	MAX	83	98
t_{PLZ}				83	98

UNIT:ns

ANALOG MULTIPLEXERS/DEMULTIPLEXERS WITH LATCH

Function Diagram



FUNCTION TABLE

INPUTS				"ON"† SWITCCHES
$\overline{E1}$	E2	S1	S0	$\overline{LE}$ = H
L	H	L	L	A_0, B_0
L	H	L	H	A_1, B_1
L	H	H	L	A_2, B_2
L	H	H	H	A_3, B_3
H	L	X	X	None

NOTES:
† When LE is low S0-S2 data are latched and switches cannot change state.
H = High Voltage Level, L = Low Voltage Level, X = Don't Care

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	UNIT
I_{CC}	MAX	0.32	mA
R_{ON}	MAX	240	Ω

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC
t_W	$\overline{LE}$		MIN	30
t_{su}	Sn to $\overline{LE}$		MIN	-
t_H	Sn to $\overline{LE}$		MIN	5
t_{PLH}	Switch In	Switch Out	MAX	11
t_{PHL}				11
t_{PZH}	$\overline{E1}$, E2, $\overline{LE}$	Vos	MAX	105
t_{PZL}				105
t_{PZH}	Sn	Vos	MAX	113
t_{PZL}				113
t_{PLZ}	$\overline{E1}$, E2, $\overline{LE}$	Vos	MAX	83
t_{PHZ}				83

UNIT:ns

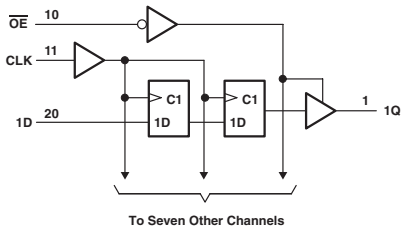
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

4374

OCTAL EDGE-TRIGGERED D-TYPE DUAL-RANK FLIP-FLOP WITH 3-STAE OUTPUTS

- 3-State Outputs Drive Bus Lines Directly

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_O
H	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AS	UNIT
I_{CC}	MAX	150	mA
I_{OH}	MAX	-15	mA
I_{OL}	MAX	48	mA

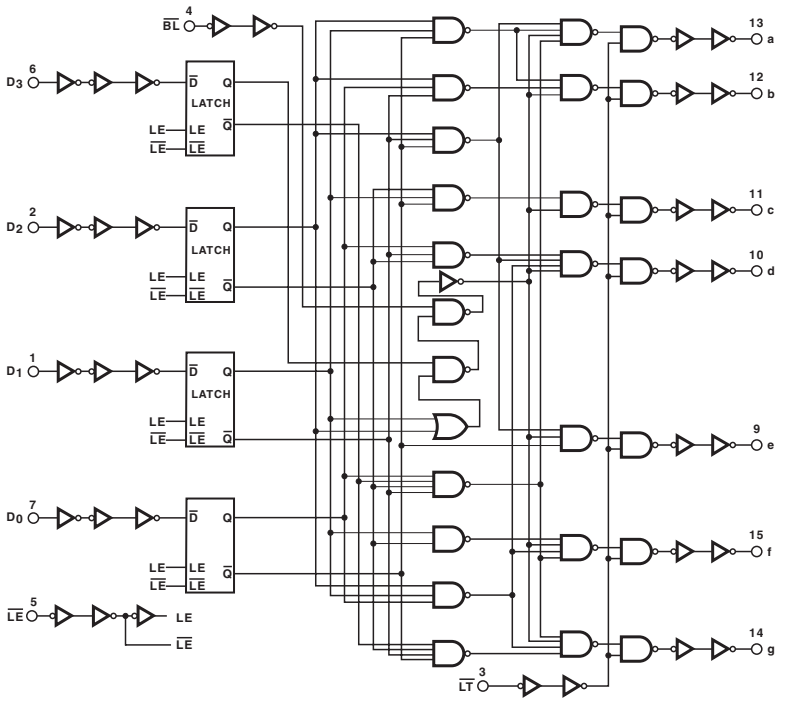
TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AS
f_{max}			MIN	125
t_w			MIN	4
t_{su}			MIN	4
t_h			MIN	1
t_{PLH}	CLK	Q	MAX	8
t_{PHL}				8
t_{PZH}	$\overline{OE}$	Q	MAX	6
t_{PZL}				8
t_{PHZ}	$\overline{OE}$	Q	MAX	6.5
t_{PLZ}				7

UNIT fmax : MHz other : ns

BCD-TO-7 SEGMENT LATCH/DECODER/DRIVERS

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

$\overline{LE}$	$\overline{BL}$	$\overline{LT}$	D_3	D_2	D_1	D_0	a	b	c	d	e	f	g	Display
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8
X	L	H	X	X	X	X	L	L	L	L	L	L	L	Blank
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	H	L	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	H	L	L	H	H	9
L	H	H	H	L	H	L	L	L	L	L	L	L	L	Blank
L	H	H	H	L	H	H	L	L	L	L	L	L	L	Blank
L	H	H	H	H	L	L	L	L	L	L	L	L	L	Blank
L	H	H	H	H	L	H	L	L	L	L	L	L	L	Blank
L	H	H	H	H	H	L	L	L	L	L	L	L	L	Blank
L	H	H	H	H	H	H	L	L	L	L	L	L	L	Blank
H	H	H	X	X	X	X	†	†	†	†	†	†	†	†

X = Don't care
† Depends on BCD code previously appied when $\overline{LE}$ = L
NOTES: Display is blank for all illegal input codes (BCD > HLLH).

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	0.16	0.16	mA
I_{OH}	MAX	-7.4	-4	mA
I_{OL}	MAX	4	4	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

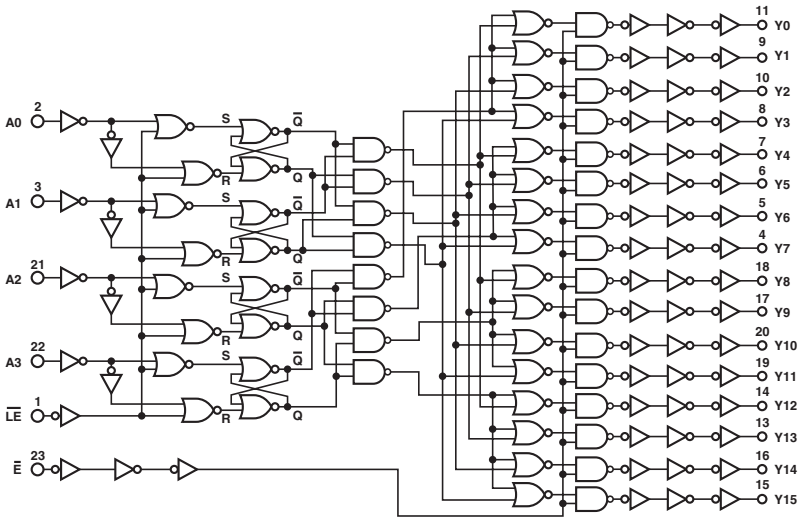
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
t_W	Latch Enable		MIN	24	24
t_{su}	Dn to $\overline{LE}$		MIN	18	24
t_H	Dn to $\overline{LE}$		MIN	3	5
t_{PLH}	Dn	a to g	MAX	90	90
t_{PHL}				90	90
t_{PLH}	$\overline{LE}$	a to g	MAX	81	81
t_{PHL}				81	81
t_{PLH}	$\overline{BL}$	a to g	MAX	66	66
t_{PHL}				66	66
t_{PLH}	$\overline{LT}$	a to g	MAX	48	50
t_{PHL}				48	50

UNIT:ns

4514

4-LINE TO 16-LINE DECODERS/DEMULTIPLEXERS WITH INPUT LATCHES

Logic Diagram



FUNCTION TABLE
($\overline{LE}$ = H)

$\overline{E}$	DECODER INPUTS				ADDRESSED OUTPUT H
	A3	A2	A1	A0	
L	L	L	L	L	Y0
L	L	L	L	H	Y1
L	L	L	H	L	Y2
L	L	L	H	H	Y3
L	L	H	L	L	Y4
L	L	H	L	H	Y5
L	L	H	H	L	Y6
L	L	H	H	H	Y7
L	H	L	L	L	Y8
L	H	L	L	H	Y9
L	H	L	H	L	Y10
L	H	L	H	H	Y11
L	H	H	L	L	Y12
L	H	H	L	H	Y13
L	H	H	H	L	Y14
L	H	H	H	H	Y15
H	X	X	X	X	All outputs = L

H = high, L = low, X = don't care

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	0.08	0.16	0.16	mA
I_{OH}	MAX	-4	-4	-4	mA
I_{OL}	MAX	4	4	4	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT
t_w	$\overline{LE}$ (LE)		MIN	20	22	45
t_{su}	$\overline{LE}$ (LE)		MIN	25	30	30
t_h	$\overline{LE}$ (LE)		MIN	5	0	5
t_{PLH}	A0, 1, 2, 3 (A, B, C, D)	Y	MAX	58	83	83
t_{PHL}				58	83	83
t_{PLH}	$\overline{LE}$ (LE)	Y	MAX	58	68	75
t_{PHL}				58	68	75
t_{PLH}	$\overline{E}$ (G)	Y	MAX	44	53	60
t_{PHL}				44	53	60

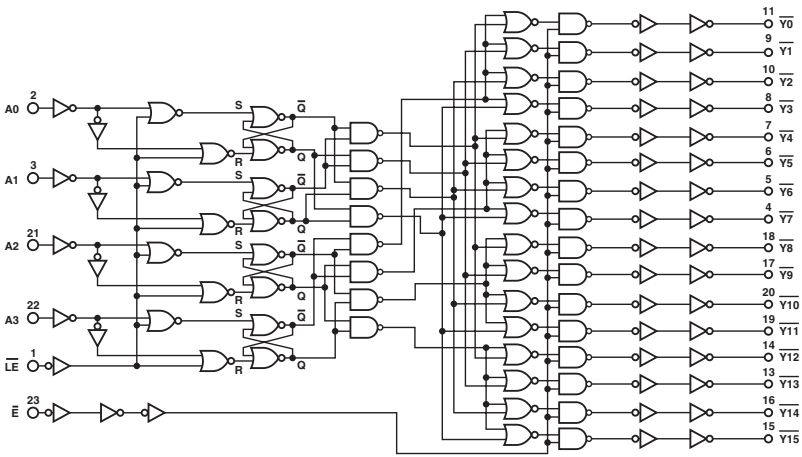
UNIT:ns

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

4515

4-LINE TO 16-LINE DECODERS/DEMULTIPLEXERS WITH INPUT LATCHES

Logic Diagram



FUNCTION TABLE
($\overline{LE}$ = H)

$\overline{E}$	DECODER INPUTS				ADDRESSED OUTPUT
	A3	A2	A1	A0	L
L	L	L	L	L	Y0
L	L	L	L	H	Y1
L	L	L	H	L	Y2
L	L	L	H	H	Y3
L	L	H	L	L	Y4
L	L	H	L	H	Y5
L	L	H	H	L	Y6
L	L	H	H	H	Y7
L	H	L	L	L	Y8
L	H	L	L	H	Y9
L	H	L	H	L	Y10
L	H	L	H	H	Y11
L	H	H	L	L	Y12
L	H	H	L	H	Y13
L	H	H	H	L	Y14
L	H	H	H	H	Y15
H	X	X	X	X	All outputs = H

H = high, L = low, X = don't care

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	0.08	0.16	0.16	mA
I_{OH}	MAX	-4	-4	-4	mA
I_{OL}	MAX	4	4	4	mA

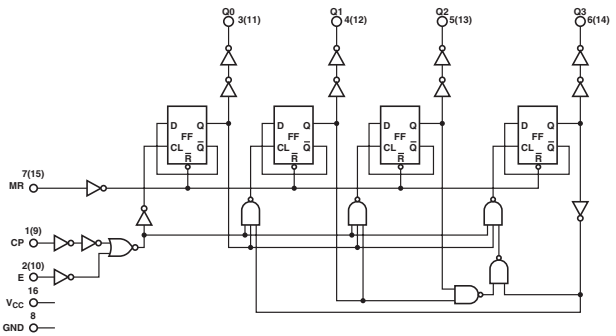
TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT
t_w	$\overline{LE}$ (LE)		MIN	20	22	45
t_{su}	$\overline{LE}$ (LE)		MIN	25	30	30
t_h	$\overline{LE}$ (LE)		MIN	5	0	5
t_{PLH}	A0, 1, 2, 3 (A, B, C, D)	CD74HCT:Y ($\overline{Y}$)	MAX	58	83	83
t_{PHL}				58	83	83
t_{PLH}	$\overline{LE}$ (LE)	CD74HCT:Y ($\overline{Y}$)	MAX	58	68	75
t_{PHL}				58	68	75
t_{PLH}	$\overline{E}$ ($\overline{G}$)	CD74HCT:Y ($\overline{Y}$)	MAX	44	53	60
t_{PHL}				44	53	60

UNIT:ns

4518
DUAL SYNCHRONOUS COUNTERS

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT STATE
CP	E	MR	
↑	H	L	Increment Counter
L	↓	L	Increment Counter
↓	X	L	No Change
H	↑	L	No Change
↑	L	L	No Change
H	↓	L	No Change
L	X	H	Q_0 thru Q_3 = L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	UNIT
I_{CC}	MAX	0.16	mA
I_{OH}	MAX	-4	mA
I_{OL}	MAX	4	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC
fmax			MIN	20
tw	CP		MIN	24
	MR			30
tsu	Enable to CP		MIN	24
	CP to Enable			24
t_{PLH}	CP	Qn	MAX	72
t_{PHL}				72
t_{PLH}	Enable	Qn	MAX	72
t_{PHL}				72
t_{PLH}	MR	Qn	MAX	45
t_{PHL}				45

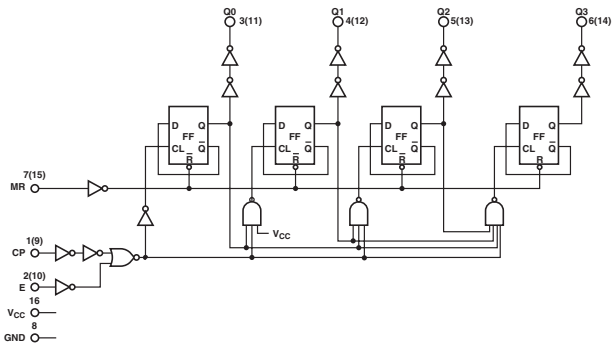
UNIT fmax : MHz other : ns

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

4520

DUAL SYNCHRONOUS COUNTERS

Logic Diagram



FUNCTION TABLE

INPUTS			
CP	E	MR	OUTPUT STATE
↑	H	L	Increment Counter
L	↓	L	Increment Counter
↓	X	L	No Change
X	↑	L	No Change
↑	L	L	No Change
H	↓	L	No Change
X	X	H	Q_0 thru Q_3 = L

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	0.16	0.16	mA
I_{OH}	MAX	-4	-4	mA
I_{OL}	MAX	4	4	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

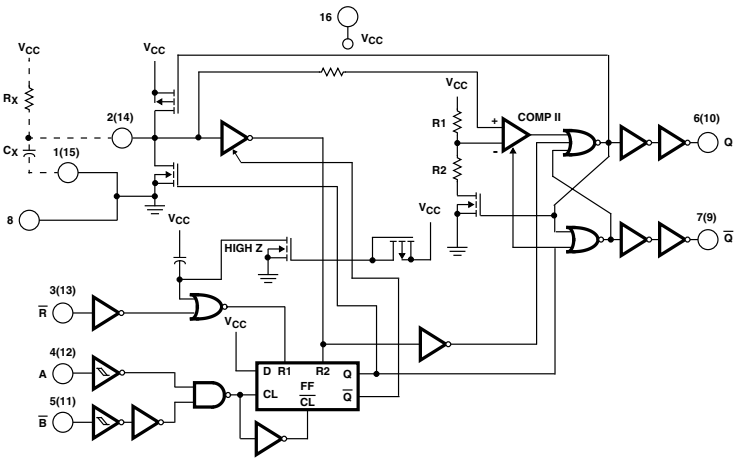
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
fmax			MIN	20	17
tw	CP		MIN	24	30
	MR			30	30
tsu	Enable to CP		MIN	24	24
	CP to Enable			24	-
t_{PLH}	CP	Qn	MAX	72	80
t_{PHL}				72	80
t_{PLH}	Enable	Qn	MAX	72	83
t_{PHL}				72	83
t_{PLH}	MR	Qn	MAX	45	53
t_{PHL}				45	53

UNIT fmax : MHz other : ns

4538

DUAL RETRIGGERABLE PRECISION MONO STABLE MULTIVIBRATOR

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{R}$	A	$\overline{B}$	E	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↓	⎍	⎏
H	↑	H	⎍	⎏

H = High Level, L = Low Level, ↑ = Transition from Low to High, ↓ = Transition from High to Low, ⎍ One High Level Pulse, ⎏ One Low Level Pulse, X = Irrelevant.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

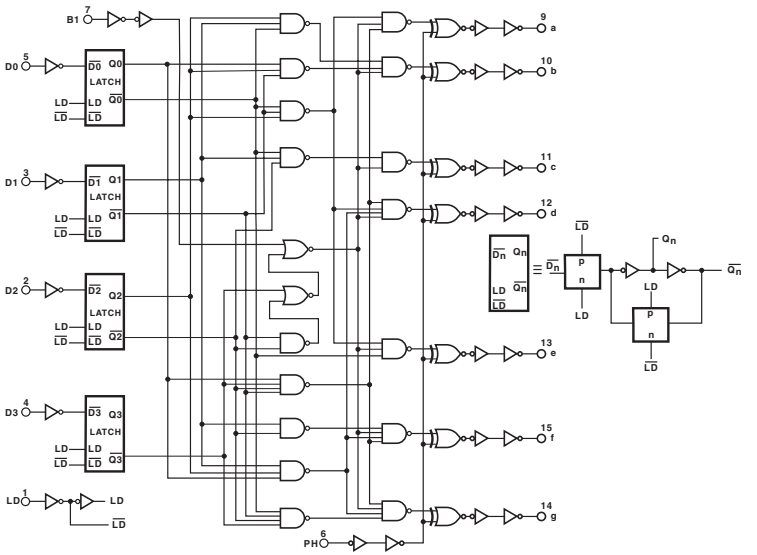
PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	0.16	0.16	mA
I_{OH}	MAX	-4	-4	mA
I_{OL}	MAX	4	4	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
t_{WH}	A, $\overline{B}$		MIN	24	24
t_{WL}	A, $\overline{B}$			24	24
t_{WL}	$\overline{R}$			24	30
t_{PLH}	$\overline{A}$, B	Q	MAX	75	83
t_{PHL}		$\overline{Q}$		75	83
t_{PLH}	$\overline{R}$	$\overline{Q}$	MAX	75	75
t_{PHL}		Q		75	60

UNIT:ns

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

LD	B1	PH	D3	D2	D1	D0	a	b	c	d	e	f	g	Display
X	H	L	X	X	X	X	L	L	L	L	L	L	L	Blank
H	L	L	L	L	L	L	H	H	H	H	H	H	L	0
H	L	L	L	L	L	H	L	H	H	L	L	L	L	1
H	L	L	L	L	H	L	H	H	L	H	H	L	H	2
H	L	L	L	L	H	H	H	H	H	H	L	L	H	3
H	L	L	L	H	L	L	L	H	H	L	L	H	H	4
H	L	L	L	H	L	H	H	L	H	H	L	H	H	5
H	L	L	L	H	H	L	H	L	H	H	H	H	H	6
H	L	L	L	H	H	H	H	H	H	L	L	L	L	7
H	L	L	H	L	L	L	H	H	H	H	H	H	H	8
H	L	L	H	L	L	H	H	H	H	H	L	H	H	9
H	L	L	H	L	H	L	L	L	L	L	L	L	L	Blank
H	L	L	H	L	H	H	L	L	L	L	L	L	L	Blank
H	L	L	H	H	L	L	L	L	L	L	L	L	L	Blank
H	L	L	H	H	L	H	L	L	L	L	L	L	L	Blank
H	L	L	H	H	H	L	L	L	L	L	L	L	L	Blank
H	L	L	H	H	H	H	L	L	L	L	L	L	L	Blank
L	L	L	X	X	X	X	NOTE							NOTE
as above		N	as above				inverse above							as above

NOTE:
Depends open the BCD code previously appied when LE = High

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	0.16	0.16	mA
I_{OH}	MAX	-1	-4	mA
I_{OL}	MAX	1	4	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

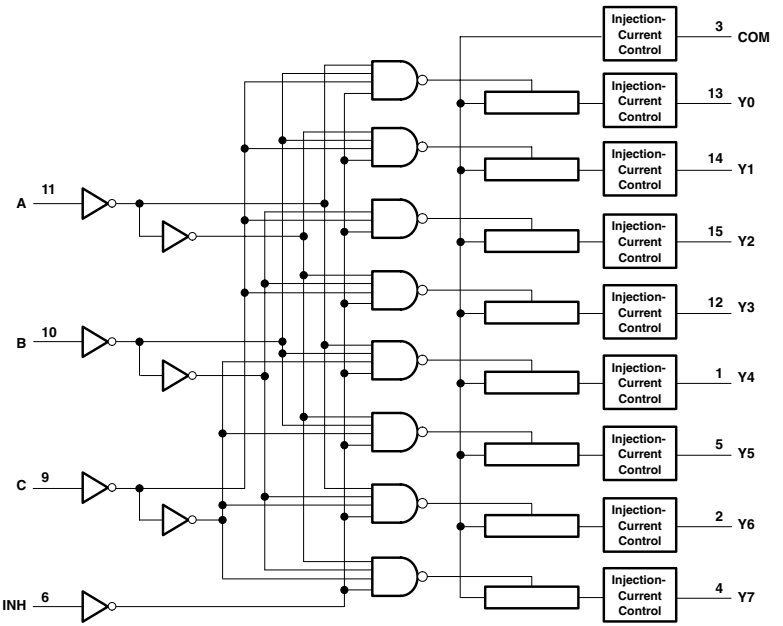
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
t_W	Latch Disable		MIN	15	15
t_{su}	Dn to LD		MIN	18	18
t_H	Dn to LD		MIN	9	12
t_{PLH}	Dn	a - g	MAX	102	120
t_{PHL}				102	120
t_{PLH}	LD	a - g	MAX	111	116
t_{PHL}				111	116
t_{PLH}	BI	a - g	MAX	80	99
t_{PHL}				80	99
t_{PLH}	PH	a - g	MAX	60	99
t_{PHL}				60	99

UNIT:ns

4851

8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER WITH INJECTION-CURRENT EFFECT CONTROL

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	UNIT
I_{CC}	MAX	0.01	mA
R_{ON}	MAX	250	Ω

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC
t_{PLH}	COM or Yn	Yn or COM	MAX	12.5
t_{PHL}				12.5
t_{PLH}	INH	COM or Yn	MAX	15
t_{PHL}				15
t_{PLH}	INH	COM or Yn	MAX	90
t_{PHL}				90
t_{PLH}	INH	COM or Yn	MAX	90
t_{PHL}				90

UNIT: ns

FUNCTION TABLE

INPUTS				ON CHANNEL
INH	C	B	A	
L	L	L	L	Y0
L	L	L	H	Y1
L	L	H	L	Y2
L	L	H	H	Y3
L	H	L	L	Y4
L	H	L	H	Y5
L	H	H	L	Y6
L	H	H	H	Y7
H	X	X	X	None

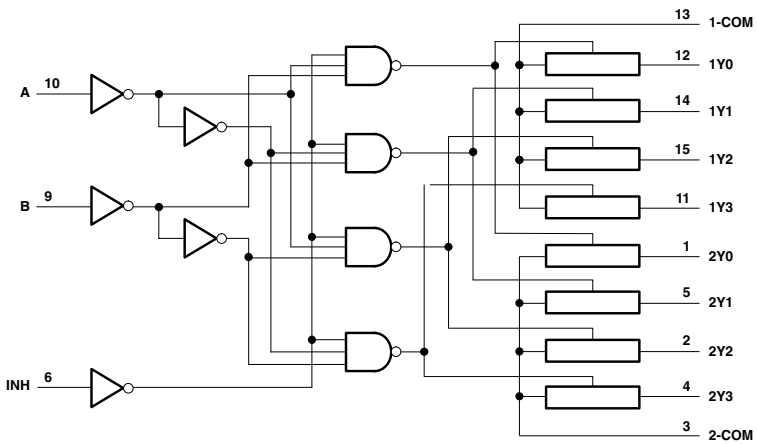
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

4852

DUAL 4-TO-1 CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER WITH INJECTION-CURRENT EFFECT CONTROL

- Low Crosstalk Between Switches
- Pin Compatible with SN74HC4052

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	UNIT
I_{CC}	MAX	0.01	mA
R_{ON}	MAX	270	Ω

FUNCTION TABLE

INPUTS			ON CHANNEL
INH	B	A	
L	L	L	1Y0, 2Y0
L	L	H	1Y1, 2Y1
L	H	L	1Y2, 2Y2
L	H	H	1Y3, 2Y3
H	X	X	None

SWITCHING CHARACTERISTICS

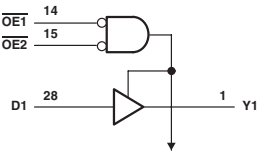
PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC
t_{PLH}	COM or Yn	Yn or COM	MAX	12.5
t_{PHL}				12.5
t_{PLH}	Channel Select	COM or Yn	MAX	15
t_{PHL}				15
t_{PLH}	INH	COM or Yn	MAX	45
t_{PHL}				45
t_{PLH}	INH	COM or Yn	MAX	90
t_{PHL}				90

UNIT: ns

5400
11-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS

- Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required (SN74ABT5400A)

Logic Diagram



FUNCTION TABLE

INPUTS			INPUT
$\overline{OE1}$	$\overline{OE2}$	D	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	UNIT
I_{CC}	MAX	45	mA
I_{OH}	MAX	-12	mA
I_{OL}	MAX	12	mA

SWITCHING CHARACTERISTICS

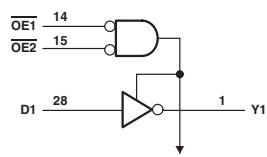
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT
t_{PLH}	D	Y	MAX	6.2
t_{PHL}				5.6
t_{PZH}	$\overline{OE}$	Y	MAX	8.7
t_{PZL}				7.5
t_{PHZ}	$\overline{OE}$	Y	MAX	5.2
t_{PLZ}				6.9

UNIT: ns

5401
11-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS

- Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required (SN74ABT5401)

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	D	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	UNIT
I_{CC}	MAX	45	mA
I_{OH}	MAX	-12	mA
I_{OL}	MAX	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT
t_{PLH}	D	Y	MAX	6.9
t_{PHL}				5.7
t_{PZH}	$\overline{OE}$	Y	MAX	8.5
t_{PZL}				6.8
t_{PHZ}	$\overline{OE}$	Y	MAX	5.2
t_{PLZ}				6.9

UNIT: ns

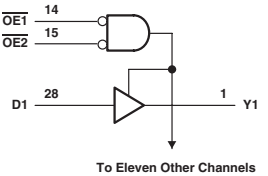
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

5402

12-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS

- Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required (SN74ABT5402A)

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	D	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	UNIT
I_{CC}	MAX	48	mA
I_{OH}	MAX	-12	mA
I_{OL}	MAX	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT
t_{PLH}	D	Y	MAX	6.2
t_{PHL}				5.6
t_{PZH}	$\overline{OE}$	Y	MAX	8.7
t_{PZL}				7.5
t_{PHZ}	$\overline{OE}$	Y	MAX	5.2
t_{PLZ}				6.9

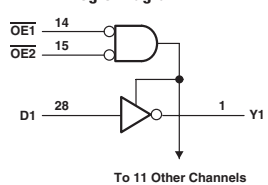
UNIT: ns

5403

12-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS

- Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required (SN74ABT5403)

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	D	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	UNIT
I_{CC}	MAX	45	mA
I_{OH}	MAX	-12	mA
I_{OL}	MAX	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT
t_{PLH}	D	Y	MAX	6.9
t_{PHL}				5.7
t_{PZH}	$\overline{OE}$	Y	MAX	8.5
t_{PZL}				6.8
t_{PHZ}	$\overline{OE}$	Y	MAX	5.2
t_{PLZ}				6.9

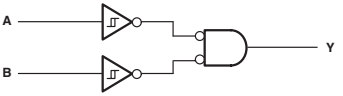
UNIT: ns

7001

QUADRUPLE POSITIVE-AND GATES WITH SCHMITT-TRIGGER INPUTS

- Same Pinouts as SN74HC08
- V_{CC}: 2V to 6V
- Schmitt-Triggered Inputs
- Y = A•B

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	UNIT
I_{CC}	MAX	0.02	mA
I_{OH}	MAX	-4	mA
I_{OL}	MAX	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC
t_{PLH}	A or B	Y	MAX	33
t_{PHL}				33

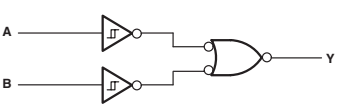
UNIT: ns

7002

QUADRUPLE POSITIVE-NOR GATES WITH SCHMITT-TRIGGER INPUTS

- Same Pinouts as SN74HC36
- V_{CC}: 2V to 6V
- Schmitt-Triggered Inputs
- $Y = \overline{A} + \overline{B}$

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	UNIT
I_{CC}	MAX	0.02	mA
I_{OH}	MAX	-4	mA
I_{OL}	MAX	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC
t_{PLH}	A or B	Y	MAX	33
t_{PHL}				33

UNIT: ns

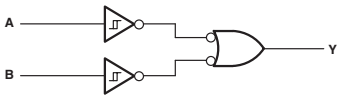
: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

7032

QUADRUPLE POSITIVE-OR GATES WITH SCHMITT-TRIGGER INPUTS

- Same Pinouts as SN74HC32
- V_{CC}: 2V to 6V
- Schmitt-Triggered Inputs
- Y = A + B

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	UNIT
I_{CC}	MAX	0.02	mA
I_{OH}	MAX	-4	mA
I_{OL}	MAX	4	mA

SWITCHING CHARACTERISTICS

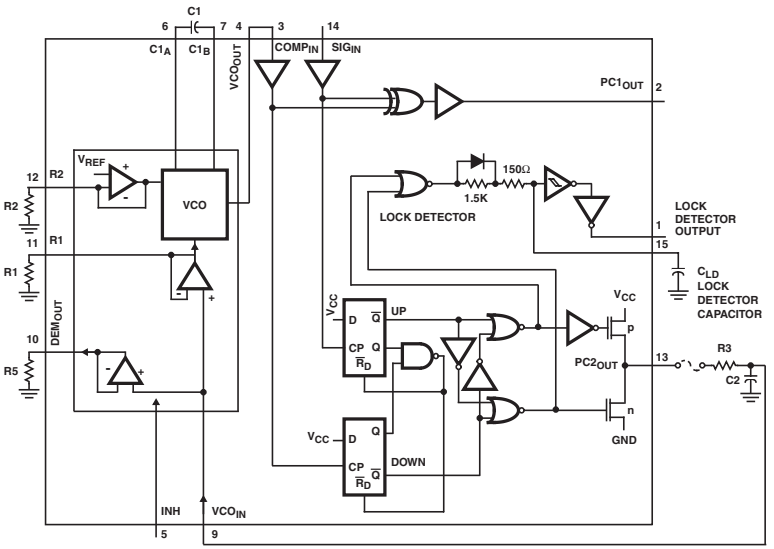
PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC
t_{PLH}	A or B	Y	MAX	33
t_{PHL}				33

UNIT: ns

7046

PHASE-LOCKED LOOP WITH VCO AND LOCK DETECTOR

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	0.16	0.16	mA
I_{OH}	MAX	-4	-4	mA
I_{OL}	MAX	4	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
t_{PLH}	SIGIN, COMPIN	PC1OUT	MAX	60	68
t_{PHL}				60	68
t_{PZH}	SIGIN, COMPIN	PC2OUT	MAX	84	90
t_{PZL}				84	90
t_{PHZ}	SIGIN, COMPIN	PC2OUT	MAX	98	105
t_{PLZ}	SIGIN, COMPIN	PC2OUT	MAX	98	105

UNIT:ns

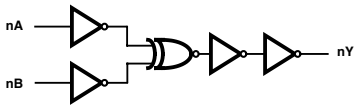
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

7266

QUAD 2-INPUT EXCLUSIVE-NOR GATES

● $Y = \overline{A \oplus B}$

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

NOTES:
H = High Voltage Level
L = Low Voltage Level

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	CD74 HC	UNIT
I_{CC}	MAX	0.02	0.04	mA
I_{OH}	MAX	-4	-4	V
I_{OL}	MAX	4	4	V

SWITCHING CHARACTERISTICS

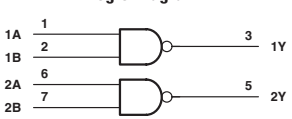
PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC
t_{PLH}	A or B	Y	MAX	25	35
t_{PHL}		Y	MAX	25	35

UNIT:ns

8003

DUAL 2-INPUT POSITIVE-NAND GATES

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

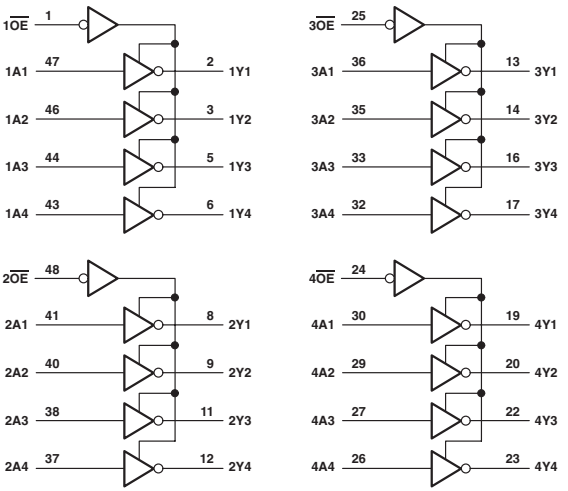
PARAMETER	MAX or MIN	ALS	AS	UNIT
I_{CC}	MAX	1.5	8.7	mA
I_{OH}	MAX	-0.4	-2	mA
I_{OL}	MAX	8	20	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
t_{PLH}	A or B	Y	MAX	11	4.5
t_{PHL}				8	4

UNIT: ns

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE
(each 4-bit buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	LVT 3V	LVTH 3V	ALVTH 3V	AC	ACT	AHC	AHCT	LVCH 3V	LVCZ 3V	ALVCH 3V	UNIT
I_{CC}	MAX	34	5	5	5	0.08	0.08	0.04	0.04	0.02	0.1	0.04	mA
I_{OH}	MAX	-32	-32	-32	-32	-24	-24	-8	-8	-24	-24	-24	mA
I_{OL}	MAX	64	64	64	64	24	24	8	8	24	24	24	mA

PARAMETER	MAX or MIN	AUC 1.8V	AUC 2.3V	UNIT
I_{CC}	MAX	0.02	0.02	mA
I_{OH}	MAX	-8	-9	mA
I_{OL}	MAX	8	9	mA

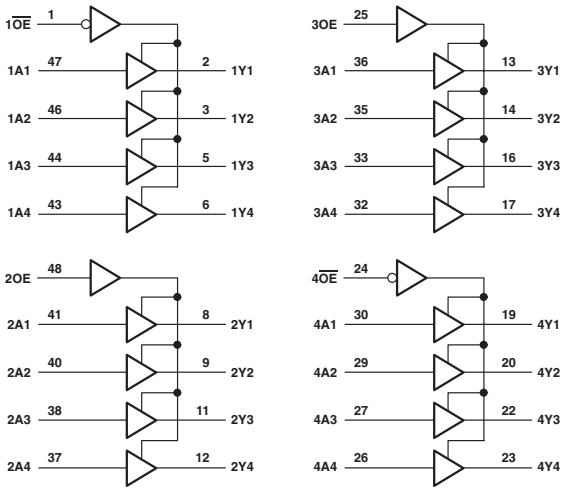
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVT 3V	LVTH 3V	ALVTH 3V	AC	ACT	AHC	AHCT
t_{PLH}	A	Y	MAX	4.7	3.5	3.5	3.3	5.8	8.5	8.5	10.5
t_{PHL}				4.8	3.5	3.5	3.2	7.1	10.2	8.5	10.5
t_{PZH}	$\overline{OE}$	Y	MAX	5.3	4	4	3.7	6.6	9.4	10.5	13
t_{PZL}				7.1	4.4	4.4	3.1	8.1	11.4	10.5	13
t_{PHZ}	$\overline{OE}$	Y	MAX	6.1	4.5	4.5	5	8.1	12	10.5	13
t_{PLZ}				5.6	4.2	4.2	4.1	7.3	10.7	10.5	13

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVCH 3V	LVCZ 3V	ALVCH 3V	AUC 1.8V	AUC 2.3V
t_{PLH}	A	Y	MAX	4.2	4.2	3.9	2.0	1.6
t_{PHL}				4.2	4.2	3.9	2.0	1.6
t_{PZH}	$\overline{OE}$	Y	MAX	4.7	4.7	5	2.5	2
t_{PZL}				4.7	4.7	5	2.5	2
t_{PHZ}	$\overline{OE}$	Y	MAX	5.9	5.9	4.4	4.5	2.3
t_{PLZ}				5.9	5.9	4.4	4.5	2.3

UNIT: ns

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS		OUTPUTS
$1\overline{OE}$, $4\overline{OE}$	1A, 4A	1Y, 4Y
L	H	L
L	L	H
H	X	Z

INPUTS		OUTPUTS
2OE, 3OE	2A, 3A	2Y, 3Y
H	H	H
H	L	L
L	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

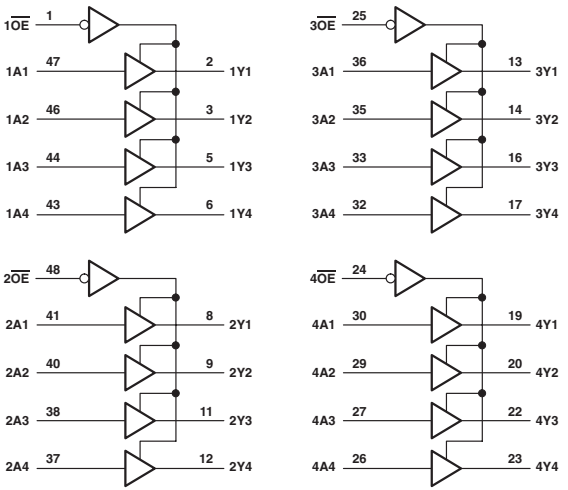
PARAMETER	MAX or MIN	ABT	LVTH 3V	ACT	UNIT
I_{CC}	MAX	34	5	0.08	mA
I_{OH}	MAX	-32	-32	-24	mA
I_{OL}	MAX	64	64	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVTH 3V	ACT
t_{PLH}	A	Y	MAX	3.7	3.5	9.5
t_{PHL}				4.5	3.5	9.1
t_{PZH}	$\overline{OE}$ or OE	Y	MAX	5	4.5	9.4
t_{PZL}				6.9	4.5	10.5
t_{PHZ}	$\overline{OE}$ or OE	Y	MAX	6.2	5.3	11.6
t_{PLZ}				5.6	4.9	10.7

UNIT: ns

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ABTH	LVT 3V	LVTH 3V	ALB 3V	ALVTH 3V	AC	ACT	AHC	AHCT	LVC 3V	UNIT
I_{CC}	MAX	32	32	5	5	5.6	5	0.08	0.08	0.04	0.04	0.02	mA
I_{OH}	MAX	-32	-32	-32	-32	-25	-32	-24	-24	-8	-8	-24	mA
I_{OL}	MAX	64	64	64	64	25	64	24	24	8	8	24	mA

PARAMETER	MAX or MIN	LVCH 3V	LVCZ 3V	ALVC 3V	ALVCH 3V	AVC 3V	AUC 1.8V	AUC 2.3V	AUCH 1.8V	AUCH 2.3V	UNIT
I_{CC}	MAX	0.02	0.1	0.04	0.04	0.04	0.02	0.02	0.02	0.02	mA
I_{OH}	MAX	-24	-24	-24	-24	-12	-8	-9	-8	-9	mA
I_{OL}	MAX	24	24	24	24	12	8	9	8	9	mA

SWITCHING CHARACTERISTICS

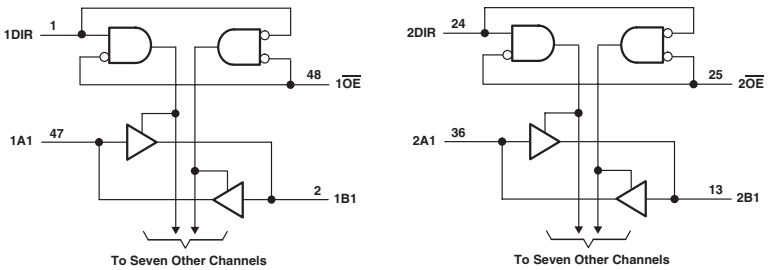
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ABTH	LVT 3V	LVTH 3V	ALB 3V	ALVTH 3V	AC	ACT
t_{PLH}	A	Y	MAX	3.5	3.5	3.2	3.2	2	2.4	7.1	9.4
t_{PHL}				4.1	4.1	3.2	3.2	2	2.5	7.9	9.5
t_{PZH}	$\overline{OE}$	Y	MAX	4.8	4.8	4	4	4.7	3.8	7.5	8.9
t_{PZL}				4.8	4.8	4	4	4.7	2.9	9	10.3
t_{PHZ}	$\overline{OE}$	Y	MAX	4.8	4.8	4.5	4.5	4.2	4.2	8.4	11.3
t_{PLZ}				4.1	4.1	4.2	4.2	4.2	3.6	7.6	10.3

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LVC 3V	LVCH 3V	LVCZ 3V	ALVC 3V	ALVCH 3V	AVC 3V
t_{PLH}	A	Y	MAX	8.5	10.5	4.1	4.1	4.1	3	3	1.7
t_{PHL}				8.5	10.5	4.1	4.1	4.1	3	3	1.7
t_{PZH}	$\overline{OE}$	Y	MAX	10.5	13	4.6	4.6	4.6	4.4	4.4	3.5
t_{PZL}				10.5	13	4.6	4.6	4.6	4.4	4.4	3.5
t_{PHZ}	$\overline{OE}$	Y	MAX	10.5	13	5.8	5.8	5.8	4.1	4.1	3.5
t_{PLZ}				10.5	13	5.8	5.8	5.8	4.1	4.1	3.5

PARAMETER	INPUT	OUTPUT	MAX or MIN	AUC 1.8V	AUC 2.3V	AUCH 1.8V	AUCH 2.3V
t_{PLH}	A	Y	MAX	1.8	1.8	1.8	1.8
t_{PHL}				1.8	1.8	1.8	1.8
t_{PZH}	$\overline{OE}$	Y	MAX	2.5	1.9	2.5	1.9
t_{PZL}				2.5	1.9	2.5	1.9
t_{PHZ}	$\overline{OE}$	Y	MAX	4.0	2	4.0	2
t_{PLZ}				4.0	2	4.0	2

UNIT: ns

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ABTH	LVT 3V	LVTH 3V	ALB 3V	ALVTH 3V	ALVT HR 3V	AC	ACT	AHCT	UNIT
I_{CC}	MAX	32	32	5	5	5.6	5	5	0.08	0.08	0.04	mA
I_{OH}	MAX	-32	-32	-32	-32	-25	-32	-12	-24	-24	-8	mA
I_{OL}	MAX	64	64	64	64	25	64	12	24	24	8	mA

PARAMETER	MAX or MIN	LVC 3V	LVCH 3V	LVCHR 3V	LVCR 3V	LVCZ 3V	ALVCH 3V	ALVC HR 3V	AVC 3V	AUC 1.8V	AUC 2.3V	UNIT
I_{CC}	MAX	0.02	0.02	0.02	0.02	0.06	0.04	0.04	0.04	0.02	0.02	mA
I_{OH}	MAX	-24	-24	-12	-12	-24	-24	-12	-12	-8	-9	mA
I_{OL}	MAX	24	24	12	12	24	24	12	12	8	9	mA

SWITCHING CHARACTERISTICS

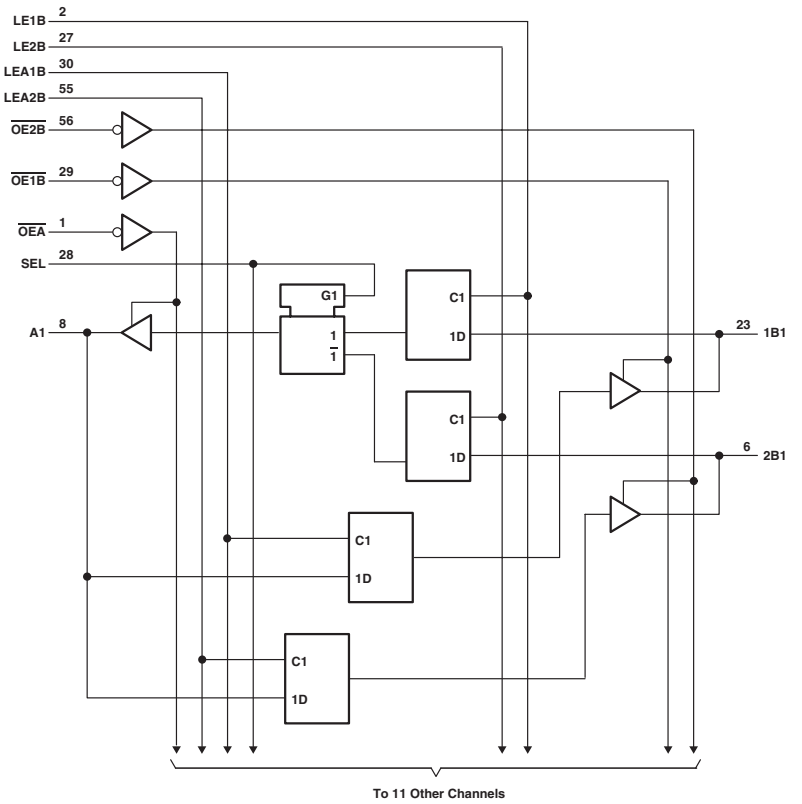
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ABTH	LVT 3V	LVTH 3V	ALB 3V	ALVTH 3V	ALVT HR 3V	AC
t_{PLH}	A or B	B or A	MAX	3.9	3.9	3.3	3.3	2	3.1	3.7	7.9
t_{PHL}				4.2	4.2	3.3	3.3	2	2.9	3.9	8.9
t_{PZH}	$\overline{OE}$	B or A	MAX	6.3	6.3	4.5	4.5	6	4.2	5.2	8.6
t_{PZL}				6.4	6.4	4.6	4.6	6	3.5	4	10.7
t_{PHZ}	$\overline{OE}$	B or A	MAX	6.3	6.3	5.1	5.1	4.2	5.3	5.1	9.8
t_{PLZ}				5.2	5.2	5.1	5.1	4.2	5	4.8	8.7

PARAMETER	INPUT	OUTPUT	MAX or MIN	ACT	AHCT	LVC 3V	LVCH 3V	LVCHR 3V	LVCR 3V	LVCZ 3V	ALVCH 3V
t_{PLH}	A or B	B or A	MAX	10.5	10.5	4	4	4.8	4.8	4	3
t_{PHL}				10.2	10.5	4	4	4.8	4.8	4	3
t_{PZH}	$\overline{OE}$	B or A	MAX	10	15	5.5	5.5	6.3	6.3	5.6	4.4
t_{PZL}				11.6	15	5.5	5.5	6.3	6.3	5.6	4.4
t_{PHZ}	$\overline{OE}$	B or A	MAX	12.6	15	6.6	6.6	7.4	7.4	6.6	4.1
t_{PLZ}				11.8	15	6.6	6.6	7.4	7.4	6.6	4.1

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVC HR 3V	AVC 3V	AUC 1.8V	AUC 2.3V
t_{PLH}	A or B	B or A	MAX	4.2	1.7	2	1.9
t_{PHL}				4.2	1.7	2	1.9
t_{PZH}	$\overline{OE}$	B or A	MAX	5.6	3.7	3.1	2.6
t_{PZL}				5.6	3.7	3.1	2.6
t_{PHZ}	$\overline{OE}$	B or A	MAX	5.5	3.9	4.8	2.9
t_{PLZ}				5.5	3.9	4.8	2.9

UNIT: ns

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

B TO A ($\overline{OEB}$ = H)

INPUTS						OUTPUT
1B	2B	SEL	LE1B	LE2B	$\overline{OEA}$	A
H	X	H	H	X	L	H
L	X	H	H	X	L	L
X	X	H	L	X	L	A_0
X	H	L	X	H	L	H
X	L	L	X	H	L	L
X	X	L	X	L	L	A_0
X	X	X	X	X	H	Z

A TO B ($\overline{OEA}$ = H)

INPUTS					OUTPUTS	
1B	LEA1B	LEA2B	$\overline{OE1B}$	$\overline{OE2B}$	1B	2B
H	H	H	L	L	H	H
L	H	H	L	L	L	L
H	H	L	L	L	H	$2B_0$
L	H	L	L	L	L	$2B_0$
H	L	H	L	L	$1B_0$	H
L	L	H	L	L	$1B_0$	L
X	L	L	L	L	$1B_0$	$2B_0$
X	X	X	H	H	Z	Z
X	X	X	L	H	Active	Z
X	X	X	H	L	Z	Active
X	X	X	L	L	Active	Active

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

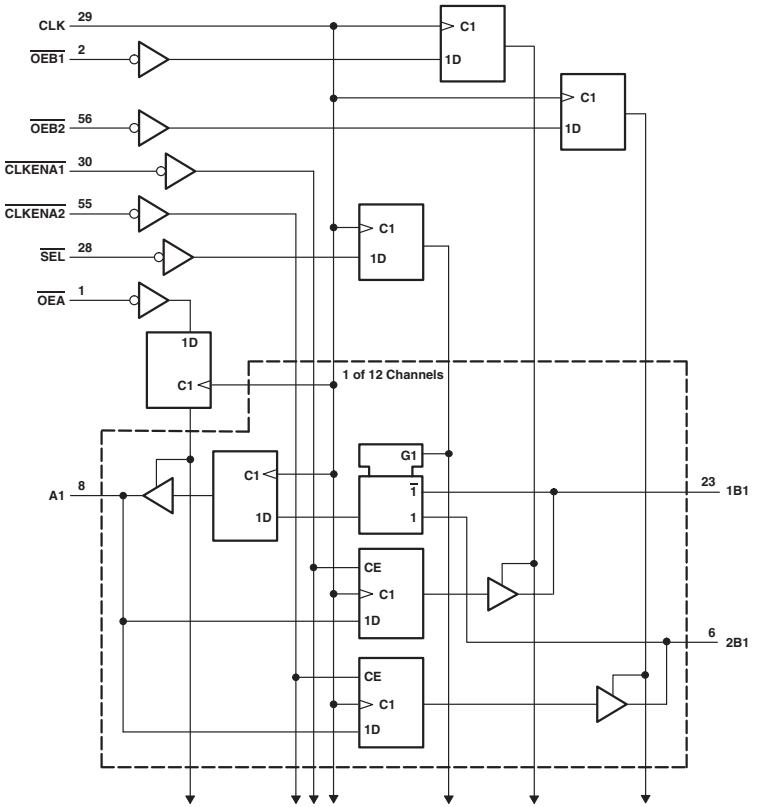
PARAMETER	MAX or MIN	ABTH	ALVCH 3V	UNIT
I_{CC}	MAX	63	0.04	mA
I_{OH}	MAX	-32	-24	mA
I_{OL}	MAX	64	24	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABTH	ALVCH 3V
t_w Pulse duration, LE1B, LE2B, LEA1B, or LEA2B high			MIN	3.3	3.3
t_{su} Setup time, data before LE1B, LE2B, LEA1B, or LEA2B ↓			MIN	1.5	1.1
t_h Hold time, data after LE1B, LE2B, LEA1B, or LEA2B ↓			MIN	1	1.5
t_{PLH}	A or B	B or A	MAX	5.6	4.3
t_{PHL}				5.9	4.3
t_{PLH}	LE	A or B	MAX	5.8	4.4
t_{PHL}				5.3	4.4
t_{PLH}	SEL (B1)	A	MAX	5.3	5.6
	SEL (B2)			6	5.6
t_{PHL}	SEL (B1)		MAX	4.4	5.6
	SEL (B2)			5.9	5.6
t_{PZH}	$\overline{OE}$	A or B	MAX	5.7	5.4
t_{PZL}				5.8	5.4
t_{PHZ}	$\overline{OE}$	A or B	MAX	6.4	4.6
t_{PLZ}				4.8	4.6

UNIT: ns

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

OUTPUT ENABLE

INPUTS			OUTPUTS	
CLK	$\overline{OEA}$	$\overline{OEB}$	A	1B,2B
↑	H	H	Z	Z
↑	H	L	Z	Active
↑	L	H	Active	Z
↑	L	L	Active	Active

A-TO-B STORAGE ($\overline{OEB}$ = L)

INPUTS				OUTPUTS	
$\overline{CLKENA1}$	$\overline{CLKENA2}$	CLK	A	1B	2B
H	H	X	X	$1B_0$†	$2B_0$†
L	X	↑	L	L	X
L	X	↑	H	H	X
X	L	↑	L	X	L
X	L	↑	H	X	H

† Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE ($\overline{OEA}$ = L)

INPUTS				OUTPUT
CLK	$\overline{SEL}$	1B	2B	A
X	H	X	X	A_0†
X	L	X	X	A_0†
↑	H	H	X	L
↑	H	L	X	H
↑	L	X	L	L
↑	L	X	H	H

† Output level before the indicated steady-state input conditions were established

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

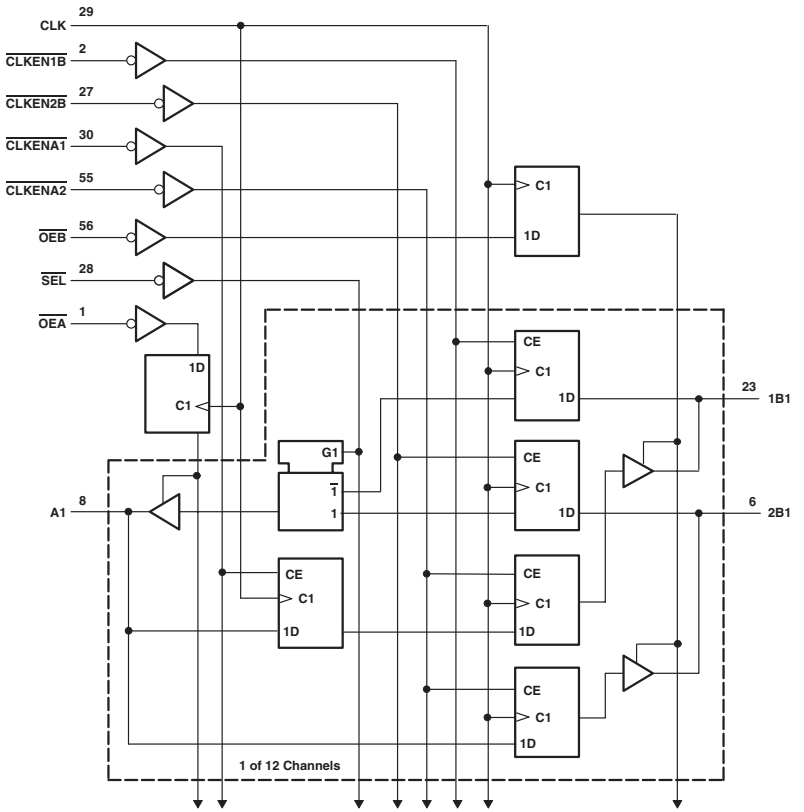
PARAMETER	MAX or MIN	ALVCH 3V	ALVCHR 3V	AVC 3V	UNIT
I_{CC}	MAX	0.04	0.04	0.04	mA
I_{OH}	MAX	-24	-12	-12	mA
I_{OL}	MAX	24	12	12	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V	ALVCHR 3V	AVC 3V
f_{max}			MIN	135	135	175
t_w Pulse duration, CLK high or low			MIN	3.3	3.3	3.5
t_{su} Setup time	A data before CLK ↑		MIN	1.7	1	1.9
	B data before CLK ↑		MIN	1.8	1.1	1.9
	$\overline{SEL}$ before CLK ↑		MIN	1.3	1.3	1.3
	$\overline{CLKENA1}$ or $\overline{CLKENA2}$ before CLK ↑		MIN	0.9	0.8	1.1
	$\overline{OE}$ before CLK ↑		MIN	1.3	1.2	1.1
t_h Hold time	A data after CLK ↑		MIN	0.6	1.2	1
	B data after CLK ↑		MIN	0.6	1	0.7
	$\overline{SEL}$ after CLK ↑		MIN	0.7	1.7	0.4
	$\overline{CLKENA1}$ or $\overline{CLKENA2}$ after CLK ↑		MIN	1.1	1.6	1
	$\overline{OE}$ after CLK ↑		MIN	0.8	1.2	0.3
t_{pd}	CLK	B	MAX	6.2	5.8	3
		A		5	5.2	2.7
t_{en}	CLK	B	MAX	6.1	5.8	3.8
		A		5.9	5.3	3.4
t_{dis}	CLK	B	MAX	6.1	6	3.7
		A		5.6	6	3.4

UNIT fmax : MHz other : ns

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

OUTPUT ENABLE

INPUTS			OUTPUTS	
CLK	$\overline{OEA}$	$\overline{OEB}$	A	1B,2B
↑	H	H	Z	Z
↑	H	L	Z	Active
↑	L	H	Active	Z
↑	L	L	Active	Active

A-TO-B STORAGE ($\overline{OEB}$ = L)

INPUTS				OUTPUTS	
$\overline{CLKENA1}$	CLKENA2	CLK	A	1B	2B
L	H	↑	L	L†	$2B_0$‡
L	H	↑	H	H†	$2B_0$‡
L	L	↑	L	L†	L
L	L	↑	H	H†	H
H	L	↑	L	$1B_0$‡	L
H	L	↑	H	$1B_0$‡	H
H	H	X	X	$1B_0$‡	$2B_0$‡

† Two CLK edges are needed to propagate data.
‡ Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE ($\overline{OEA}$ = L)

INPUTS						OUTPUT
$\overline{CLKEN1B}$	$\overline{CLKEN2B}$	CLK	$\overline{SEL}$	1B	2B	A
H	X	X	H	X	X	A_0‡
X	H	X	L	X	X	A_0‡
L	X	↑	H	H	X	L
L	X	↑	H	L	X	H
X	L	↑	L	X	L	L
X	L	↑	L	X	H	H

‡ Output level before the indicated steady-state input conditions were established

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

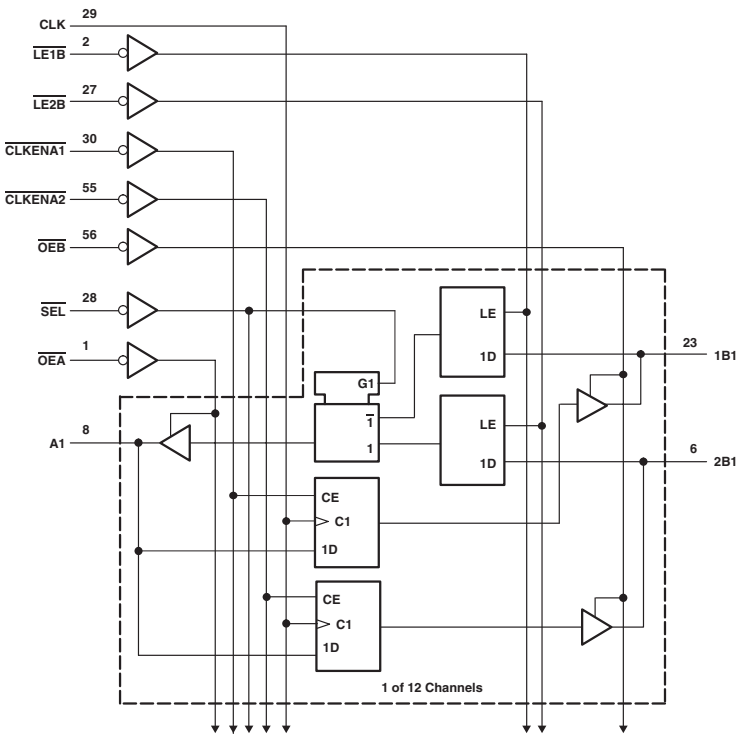
PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I_{CC}	MAX	0.04	mA
I_{OH}	MAX	-24	mA
I_{OL}	MAX	24	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
f_{max}			MIN	150
t_w Pulse duration, CLK high or low			MIN	3.3
t_{su} Setup time	A data before CLK ↑		MIN	3.1
	B data before CLK ↑		MIN	0.9
	$\overline{CLKENA1}$ or $\overline{CLKENA2}$ before CLK ↑		MIN	2.7
	$\overline{CLKEN1B}$ or $\overline{CLKEN2B}$ before CLK ↑		MIN	2.6
	$\overline{OE}$ before CLK ↑		MIN	3.2
t_h Hold time	A data after CLK ↑		MIN	0.2
	B data after CLK ↑		MIN	1.7
	$\overline{CLKENA1}$ or $\overline{CLKENA2}$ after CLK ↑		MIN	0.3
	$\overline{CLKEN1B}$ or $\overline{CLKEN2B}$ after CLK ↑		MIN	0.6
	$\overline{OE}$ after CLK ↑		MIN	0.1
t_{pd}	CLK	A or B	MAX	5.1 4.7
	$\overline{SEL}$	A	MAX	5.5
t_{en}	CLK	A or B	MAX	6 6
t_{dis}	CLK	A or B	MAX	5.8 5.8

UNIT fmax : MHz other : ns

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

OUTPUT ENABLE

INPUTS		OUTPUTS	
$\overline{OEA}$	$\overline{OEB}$	A	1B, 2B
H	X	Z	Z
L	L	Z	Active
L	H	Active	Z
L	L	Active	Active

A-TO-B STORAGE ($\overline{OEB}$ = L)

INPUTS				OUTPUTS	
$\overline{CLKENA1}$	$\overline{CLKENA2}$	CLK	A	1B	2B
H	H	X	X	$1B_0$†	$2B_0$†
L	X	↑	L	L	X
L	X	↑	H	H	X
X	L	↑	L	X	L
X	L	↑	H	A_0	H

B-TO-A STORAGE ($\overline{OEA}$ = L)

INPUTS				OUTPUTA
$\overline{LE}$	$\overline{SEL}$	1B	2B	
H	X	X	X	A_0†
H	X	X	X	A_0†
L	H	L	X	L
L	H	H	X	H
L	L	X	L	L
L	L	X	H	H

† Output level before the indicated steady-state input conditions were established

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

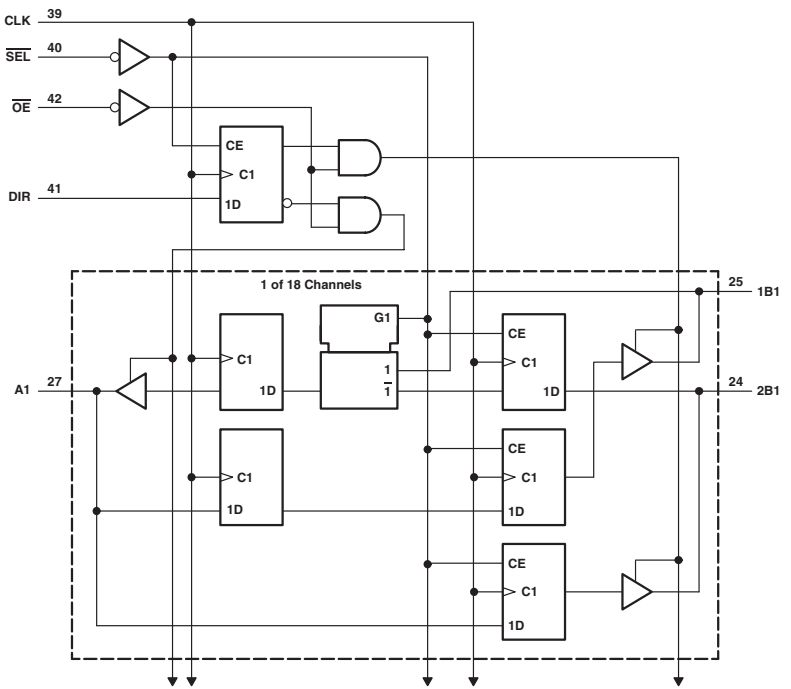
PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I_{CC}	MAX	0.04	mA
I_{OH}	MAX	-24	mA
I_{OL}	MAX	24	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
f_{max}			MIN	130
t_w Pulse duration, CLK high or low			MIN	3.3
t_{su} Setup time	A before CLK ↑		MIN	1.7
	B before $\overline{LE}$		MIN	1.3
	$\overline{CLKEN}$ before CLK ↑		MIN	1
t_h Hold time	A after CLK ↑		MIN	0.7
	B after $\overline{LE}$		MIN	1.1
	$\overline{CLKEN}$ after CLK ↑		MIN	0.9
t_{pd}	CLK	B	MAX	4.3
	B	A	MAX	4
	$\overline{LE}$			4.8
	$\overline{SEL}$			5.2
t_{en}	$\overline{OEB}$ or $\overline{OEA}$	B or A	MAX	5.1
t_{dis}	$\overline{OEB}$ or $\overline{OEA}$	B or A	MAX	4.2

UNIT fmax : MHz other : ns

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

A-TO-B STORAGE ($\overline{OE}$ = L, DIR = H)

INPUTS			OUTPUTS	
$\overline{SEL}$	CLK	A	1B	2B
H	X	X	$1B_0$†	$2B_0$†
L	↑	L	L‡	X
L	↑	H	H‡	X

† Output level before the indicated steady-state input conditions were established
‡ Two CLK edges are needed to propagate the data.

B-TO-A STORAGE ($\overline{OE}$ = L, DIR = L)

INPUTS				OUTPUT
CLK	SEL	1B	2B	A
↑	H	X	L	L§
↑	H	X	H	H§
↑	L	L	X	L
↑	L	H	X	H

§ Two CLK edges are needed to propagate the data. The data is loaded in the first register when SEL is low and propagates to the second register when SEL is high.

OUTPUT ENABLE

INPUTS			OUTPUTS	
CLK	$\overline{OE}$	DIR	A	1B, 2B
↑	H	X	Z	Z
↑	L	L	Z	Active
↑	L	H	Active	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I_{CC}	MAX	0.04	mA
I_{OH}	MAX	-24	mA
I_{OL}	MAX	24	mA

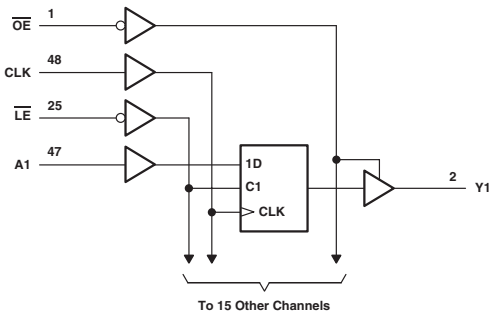
TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
f_{max}			MIN	150
t_w Pulse duration, CLK high or low			MIN	3.3
t_{su} Setup time	A data before CLK ↑		MIN	2
	B data before CLK ↑		MIN	1.8
	DIR before CLK ↑		MIN	1.7
	$\overline{SEL}$ before CLK ↑		MIN	1.8
t_h Hold time	A data after CLK ↑		MIN	0.7
	B data after CLK ↑		MIN	0.6
	DIR after CLK ↑		MIN	0.5
	$\overline{SEL}$ after CLK ↑		MIN	0.8
t_{pd}	CLK	A	MAX	5
		B		5.3
t_{en}	$\overline{OE}$	A	MAX	5.7
		B		7.4
t_{dis}	$\overline{OE}$	A	MAX	5.7
		B		6.4

UNIT fmax : MHz other : ns

16-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	$\overline{LE}$	CLK	A	Y
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	↑	L	L
L	H	↑	H	H
L	H	L or H	X	Y_0†

† Output level before the indicated steady-state input conditions were established

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVC 3V	ALVCH 3V	AVC 3V	UNIT
I_{CC}	MAX	0.04	0.04	0.04	mA
I_{OH}	MAX	-24	-24	-12	mA
I_{OL}	MAX	24	24	12	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

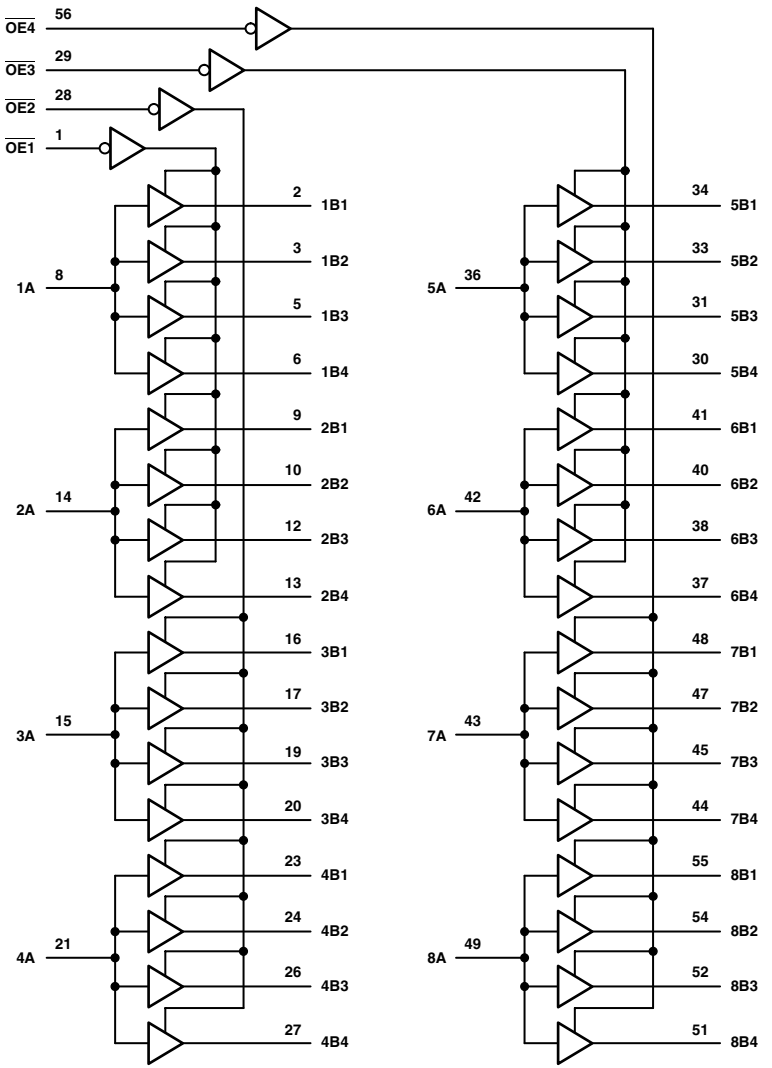
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVC 3V	ALVCH 3V	AVC 3V
f_{max}			MIN	150	150	150
t_w Pulse duration	$\overline{LE}$ low			3.3	3.3	3.3
	CLK high or low		MIN	3.3	3.3	3.3
t_{su} Setup time	Data before CLK ↑		MIN	1.5	1.5	0.7
	Data before $\overline{LE}$ ↑ CLK high		MIN	1.3	1.3	0.9
	Data before $\overline{LE}$ ↑ CLK low		MIN	1.2	1.2	1
t_h Hold time	Data after CLK ↑		MIN	0.9	0.9	0.7
	Data after $\overline{LE}$ ↑ CLK high		MIN	1.1	1.1	1.5
	Data after $\overline{LE}$ ↑ CLK low		MIN	1.1	1.1	1.3
t_{pd}	A	Y	MAX	3.3	3.3	2.5
	$\overline{LE}$			4.4	4.4	4
	CLK		MAX	4.1	4.1	3.1
t_{en}	$\overline{OE}$	Y		4.6	4.6	6.2
t_{dis}	$\overline{OE}$	Y	MAX	4.4	4.4	5.3

UNIT fmax : MHz other : ns

16344

1-BIT TO 4-BIT ADDRESS DRIVER WITH 3-STATE OUTPUTS

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS		OUTPUT
$\overline{OE}$	A	Bn
L	H	H
L	L	L
H	H	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

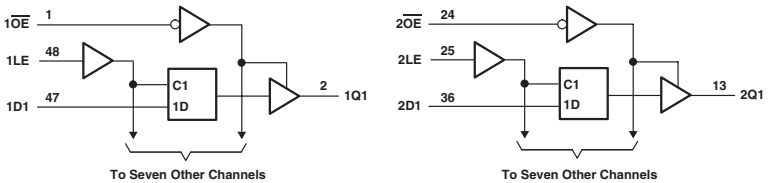
PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I_{CC}	MAX	0.04	mA
I_{OH}	MAX	-24	mA
I_{OL}	MAX	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
t_{PLH}	A	B	MAX	4
t_{PHL}				4
t_{PZH}	OE	B	MAX	5.1
t_{PZL}				5.1
t_{PHZ}	OE	B	MAX	4
t_{PLZ}				4

UNIT: ns

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_O
H	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	LVTH 3V	ALVTH 3V	AC	ACT	AHC	AHCT	LVC 3V	LVC ver.A 3V	LVCH 3V	ALVCH 3V	UNIT
I_{CC}	MAX	85	5	5	0.08	0.08	0.04	0.04	0.04	0.02	0.02	0.04	mA
I_{OH}	MAX	-32	-32	-32	-24	-24	-8	-8	-24	-24	-24	-24	mA
I_{OL}	MAX	64	64	64	24	24	8	8	24	24	24	24	mA

PARAMETER	MAX or MIN	AVC 3V	AUC 1.8V	AUC 2.3V	UNIT
I_{CC}	MAX	0.04	0.02	0.02	mA
I_{OH}	MAX	-12	-8	-9	mA
I_{OL}	MAX	12	8	9	mA

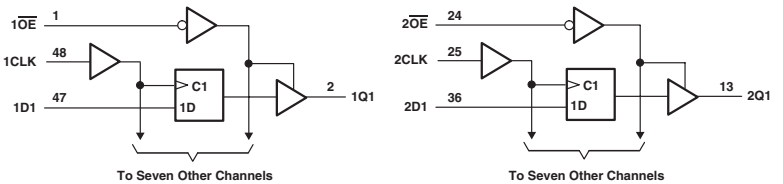
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVTH 3V	ALVTH 3V	AC	ACT	AHC	AHCT
t_w Pulse duration, LE high or low			MIN	3.3	3	1.5	4	1	5	6.5
t_{su} Setup time	Data before LE ↓, data high		MIN	1.5	1	1.4	1.5	1	4	1.5
	Data before LE ↓, data low		MIN	1.5	1	0.9	1.5	1	4	1.5
t_h Hold time	Data after LE ↓, data high		MIN	1	1	0.9	2.4	5	1	3.5
	Data after LE ↓, data low		MIN	1	1	1.4	2.4	5	1	3.5
t_{PLH}	D	Q	MAX	6.3	3.8	3.1	9.7	11.1	10.5	10.5
t_{PHL}				6.2	3.6	3.3	10.1	12.3	10.5	10.5
t_{PLH}	LE	Q	MAX	6.7	4.3	3.3	11.9	12.8	10.5	10.5
t_{PHL}				6.1	4	3.5	10.9	12.2	10.5	10.5
t_{PZH}	$\overline{OE}$	Q	MAX	6.1	4.3	4	10.8	12.1	11.5	11.5
t_{PZL}				5.6	4.3	3.4	12.8	14.2	11.5	11.5
t_{PHZ}	$\overline{OE}$	Q	MAX	8.1	5	4.9	8.8	10.7	11.5	12
t_{PLZ}				6.5	4.7	4.5	8.1	9.4	11.5	12

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 3V	LVC ver.A 3V	LVCH 3V	ALVCH 3V	AVC 3V	AUC 1.8V	AUC 2.3V
t_w Pulse duration, LE high or low			MIN	4	3.3	3.3	3.3	1.8	2.1	1.7
t_{su} Setup time	Data before LE ↓, data high		MIN	2	1.7	1.7	1.1	0.8	0.4	0.4
	Data before LE ↓, data low		MIN	2	1.7	1.7	1.1	0.8	0.4	0.4
t_h Hold time	Data after LE ↓, data high		MIN	2	1.2	1.2	1.4	1	0.7	0.6
	Data after LE ↓, data low		MIN	2	1.2	1.2	1.4	1	0.7	0.6
t_{PLH}	D	Q	MAX	7	4.2	4.2	3.6	2.8	2.4	1.9
t_{PHL}				7	4.2	4.2	3.6	2.8	2.4	1.9
t_{PLH}	LE	Q	MAX	8	4.6	4.6	3.9	3.2	2.8	2.1
t_{PHL}				8	4.6	4.6	3.9	3.2	2.8	2.1
t_{PZH}	$\overline{OE}$	Q	MAX	8	4.7	4.7	4.7	3.4	2.9	2.2
t_{PZL}				8	4.7	4.7	4.7	3.4	2.9	2.2
t_{PHZ}	$\overline{OE}$	Q	MAX	7	5.9	5.9	4.1	3.9	4.6	2.5
t_{PLZ}				7	5.9	5.9	4.1	3.9	4.6	2.5

UNIT: ns AUC:Preview

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_O
H	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	LVTH 3V	ALVTH 3V	AC	ACT	AHC	AHCT	LVC 3V	LVC ver.A 3V	LVCH 3V	ALVCH 3V	UNIT
I_{CC}	MAX	72	5	5	0.08	0.08	0.04	0.04	0.04	0.02	0.02	0.04	mA
I_{OH}	MAX	-32	-32	-32	-24	-24	-8	-8	-24	-24	-24	-24	mA
I_{OL}	MAX	64	64	64	24	24	8	8	24	24	24	24	mA

PARAMETER	MAX or MIN	AVC 3V	AUC 1.8V	AUC 2.3V	AUCH 1.8V	AUCH 2.3V	UNIT
I_{CC}	MAX	0.04	0.02	0.02	0.02	0.02	mA
I_{OH}	MAX	-12	-8	-9	-8	-9	mA
I_{OL}	MAX	12	8	9	8	9	mA

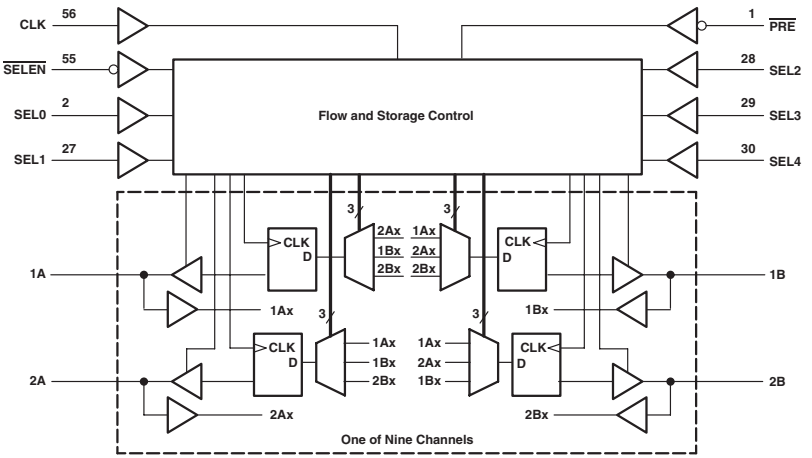
TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVTH 3V	ALVTH 3V	AC	ACT	AHC	AHCT	LVC 3V
f_{max}			MIN	150	160	250	100	65	110	110	100
t_w Pulse duration	CLK high		MIN	3.3	3	1.5	5	7.5	5	6.5	4
	CLK low			3.3	3	1.5	5	4.5	5	6.5	4
t_{su} Setup time	Data before CLK ↑, data high		MIN	1.1	1.8	1	5	4.5	3	2.5	2
	Data before CLK ↑, data low			1.1	1.8	1.5	5	4.5	3	2.5	2
t_h Hold time	Data after CLK ↑, data high		MIN	1.3	0.8	0.5	0	6.5	2	2.5	1.5
	Data after CLK ↑, data low			1.3	0.8	1	0	6.5	2	2.5	1.5
t_{PLH}	CLK	Q	MAX	6.2	4.5	3.2	10.8	12.4	11.5	11.5	7.5
t_{PHL}				5.9	4	3.2	10.6	12.2	11.5	11.5	7.5
t_{PZH}	$\overline{OE}$	Q	MAX	5.6	4.5	3.8	10.2	11.9	11.5	11.5	7.5
t_{PZL}				5.3	4.4	3.3	12.1	13.4	11.5	11.5	7.5
t_{PHZ}	$\overline{OE}$	Q	MAX	8.2	5	4.6	8.2	10.4	11.5	12	7
t_{PLZ}				6.6	4.6	4.2	7.9	9.8	11.5	12	7

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC ver.A 3V	LVCH 3V	ALVCH 3V	AVC 3V	AUC 1.8V	AUC 2.3V	AUCH 1.8V	AUCH 2.3V
f_{max}			MIN	150	150	150	200	250	250	250	250
t_w Pulse duration	CLK high		MIN	3.3	3.3	3.3	2.5	1.9	1.9	1.9	1.9
	CLK low			3.3	3.3	3.3	2.5	1.9	1.9	1.9	1.9
t_{su} Setup time	Data before CLK ↑, data high		MIN	1.9	1.9	1.9	1.4	0.6	0.6	0.6	0.6
	Data before CLK ↑, data low			1.9	1.9	1.9	1.4	0.6	0.6	0.6	0.6
t_h Hold time	Data after CLK ↑, data high		MIN	1.9	1.1	0.5	1.1	0.4	0.4	0.4	0.4
	Data after CLK ↑, data low			1.9	1.1	0.5	1.1	0.4	0.4	0.4	0.4
t_{PLH}	CLK	Q	MAX	4.5	4.5	4.2	3.3	2.8	2.2	2.8	2.2
t_{PHL}				4.5	4.5	4.2	3.3	2.8	2.2	2.8	2.2
t_{PZH}	$\overline{OE}$	Q	MAX	4.6	4.6	4.8	3.4	2.9	2.2	2.9	2.2
t_{PZL}				4.6	4.6	4.8	3.4	2.9	2.2	2.9	2.2
t_{PHZ}	$\overline{OE}$	Q	MAX	5.5	5.5	4.3	3.9	4.5	2.2	4.5	2.2
t_{PLZ}				5.5	5.5	4.3	3.9	4.5	2.2	4.5	2.2

UNIT fmax : MHz other : ns

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS		OUTPUT
CLK	SEND PORT	RECEIVE PORT
X	X	B_0†
X	L	L
X	H	H
↑	L	L
↑	H	H
H	X	B_0†
L	X	B_0†

† Output level before the indicated steady-state input conditions were established

DATA-FLOW CONTROL

INPUTS								DATA FLOW
$\overline{PRE}$	$\overline{SELEN}$	CLK	SEL0	SEL1	SEL2	SEL3	SEL4	
H	X	X	X	X	X	X	X	All outputs disabled
L	H	↑	X	X	X	X	X	No change
L	L	↑	0	0	0	0	0	None, all I/Os off
L	L	↑	0	0	0	0	1	Not used
L	L	↑	0	0	0	1	0	Not used
L	L	↑	0	0	0	1	1	Not used
L	L	↑	0	0	1	0	0	Not used
L	L	↑	0	0	1	0	1	Not used
L	L	↑	0	0	1	1	0	Not used
L	L	↑	0	0	1	1	1	Not used
L	L	↑	0	1	0	0	0	2A to 1A and 1B to 2B
L	L	↑	0	1	0	0	1	2A to 1A
L	L	↑	0	1	0	1	0	2B to 1B
L	L	↑	0	1	0	1	1	2A to 1A and 2B to 1B
L	L	↑	0	1	1	0	0	1A to 2A and 1B to 2B
L	L	↑	0	1	1	0	1	1A to 2A
L	L	↑	0	1	1	1	0	1B to 2B
L	L	↑	0	1	1	1	1	1A to 2A and 2B to 1B
L	L	↑	1	0	0	0	0	1A to 1B and 2B to 2A
L	L	↑	1	0	0	0	1	1A to 1B
L	L	↑	1	0	0	1	0	2A to 2B
L	L	↑	1	0	0	1	1	1A to 1B and 2A to 2B
L	L	↑	1	0	1	0	0	1B to 1A and 2A to 2B
L	L	↑	1	0	1	0	1	1B to 1A
L	L	↑	1	0	1	1	0	2B to 2A
L	L	↑	1	0	1	1	1	1B to 1A and 2B to 2A
L	L	↑	1	1	0	0	0	2B to 1A and 2A to 1B
L	L	↑	1	1	0	0	1	1B to 2A
L	L	↑	1	1	0	1	0	2B to 1A
L	L	↑	1	1	0	1	1	2B to 1A and 1B to 2A
L	L	↑	1	1	1	0	0	1A to 2B and 1B to 2A
L	L	↑	1	1	1	0	1	1A to 2B
L	L	↑	1	1	1	1	0	2A to 1B
L	L	↑	1	1	1	1	1	1A to 2B and 2A to 1B

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

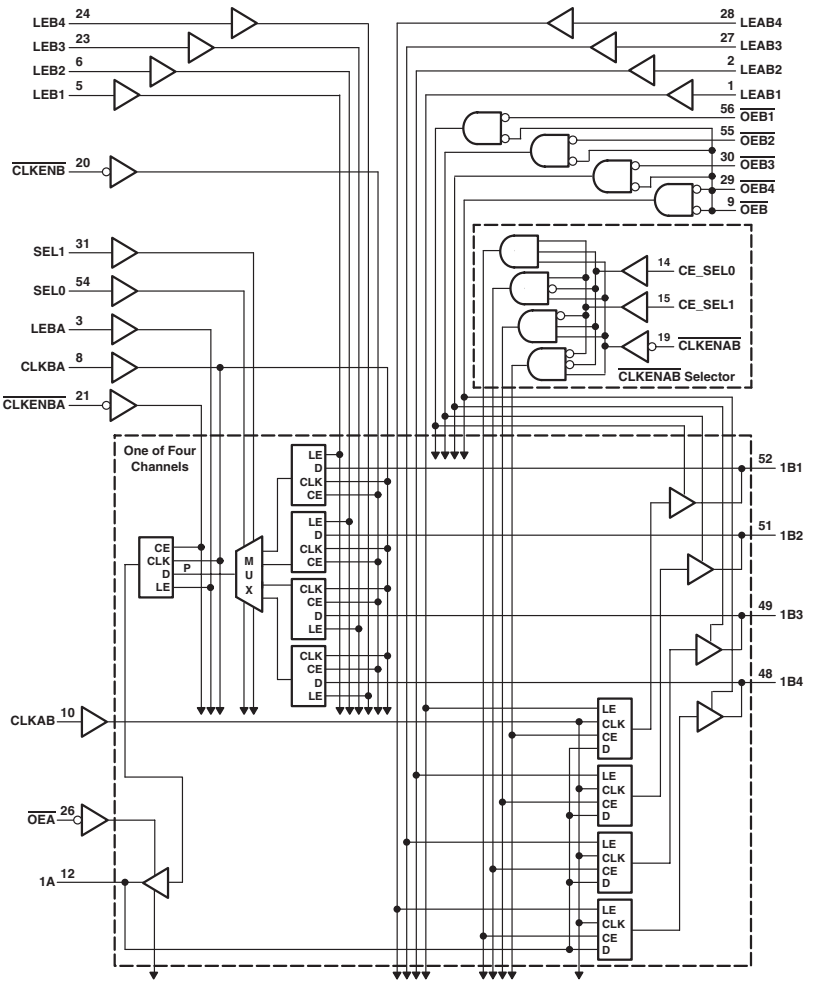
PARAMETER	MAX or MIN	ALVCH 3V	ALVC HR 3V	UNIT
I_{CC}	MAX	0.04	0.04	mA
I_{OH}	MAX	-24	-12	mA
I_{OL}	MAX	24	12	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V	ALVC HR 3V
f_{max}			MIN	120	120
t_w Pulse duration, CLK high or low			MIN	3	3
t_{su} Setup time	A or B data before CLK ↑		MIN	1.4	1.4
	$\overline{SEL}$ before CLK ↑		MIN	3.5	3.5
	$\overline{SELEN}$ before CLK ↑		MIN	1.8	1.8
	$\overline{PRE}$ before CLK ↑		MIN	0.7	0.7
t_h Hold time	A or B data after CLK ↑		MIN	1	1
	$\overline{SEL}$ after CLK ↑		MIN	0	0
	$\overline{SELEN}$ after CLK ↑		MIN	0.8	0.8
t_{pd}	CLK	A or B	MAX	5.1	6.2
t_{en}	CLK	A or B	MAX	5.7	6.8
t_{dis}	CLK	A or B	MAX	5.7	6.1
	$\overline{PRE}$			6.1	6.4

UNIT fmax : MHz other : ns

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

A-TO-B OUTPUT ENABLE

INPUTS		OUTPUT
$\overline{OEB}$	$\overline{OEBn}$	Bn
H	H	Z
H	L	Z
L	H	Z
L	L	Active

†n = 1, 2, 3, 4

A-TO-B OUTPUT ENABLE
(assuming $\overline{OEB}$ = L, $\overline{OEBn}$ = L) ‡

INPUTS								OUTPUTS			
$\overline{CLKENAB}$	CE_SEL1	CE_SEL0	CLKAB	LEAB1	LEAB2	LEAB3	LEAB4	B1	B2	B3	B4
X	X	X	H or L	H	L	L	L	A	A_0	A_0	A_0
X	X	X	H or L	H	H	H	L	A	A	A	A_0
L	X	X	L	L	L	L	L	A_0	A_0	A_0	A_0
L	L	L	↑	L	L	L	L	A	A_0	A_0	A_0
L	L	H	↑	L	L	L	L	A_0	A	A_0	A_0
L	H	L	↑	L	L	L	L	A_0	A_0	A	A_0
L	H	H	↑	L	L	L	L	A_0	A_0	A_0	A
H	X	X	↑	L	L	L	L	A_0	A_0	A_0	A_0

B-TO-A STORAGE
(after point P)

INPUTS								P
$\overline{CLKENB}$	CLKBA	LEB1	LEB2	LEB3	LEB4	SEL1	SEL0	
X	X	H	L	L	L	L	L	B1
X	X	L	H	L	L	L	H	B2
X	X	L	L	H	L	H	L	B3
X	X	L	L	L	H	H	H	B4
L	↑	L	L	L	L	L	L	B1
						L	H	B2
						H	L	B3
						H	H	B4
L	L	L	L	L	L	L	L	$B1_0$†
						L	H	$B2_0$†
						H	L	$B3_0$†
						H	H	$B4_0$†

‡ Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE
(after point P)

INPUTS					OUTPUT
$\overline{CLKENBA}$	CLKBA	LEBA	$\overline{OEA}$	B	A
X	X	X	H	X	Z
X	X	H	L	L	L
X	X	H	L	H	H
H	X	L	L	X	A_0†
L	↑	L	L	L	L
L	↑	L	L	H	H
L	L	L	L	X	A_0†

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABTH	UNIT
I_{CC}	MAX	32	mA
I_{OH}	MAX	-32	mA
I_{OL}	MAX	64	mA

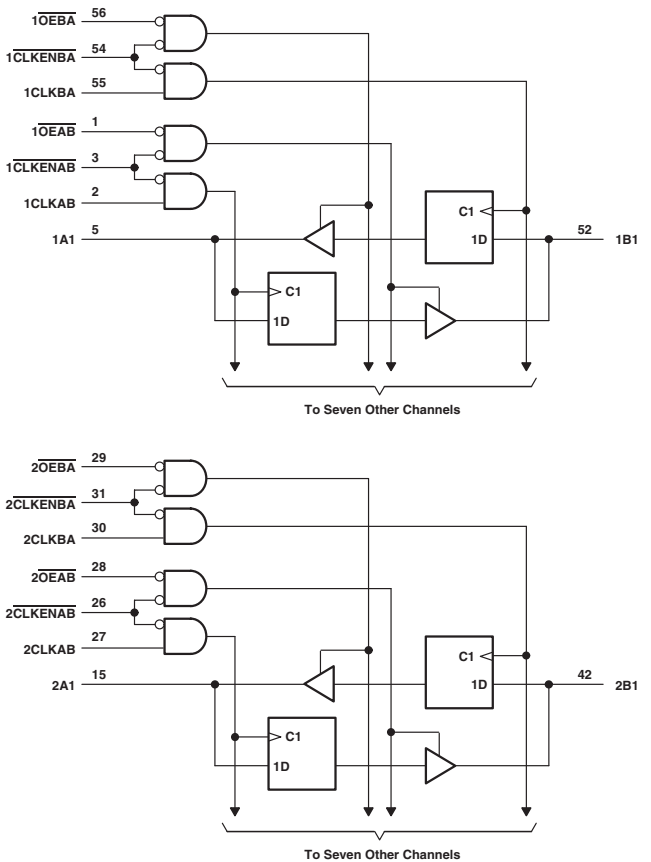
TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER			MAX or MIN	ABTH
f_{max}			MIN	160
t_w Pulse duration	CLKAB high or low		MIN	3.8
	CLKBA high or low		MIN	4.5
	LEAB1, 2, 3 or 4 high		MIN	2.2
	LEBA high		MIN	2.1
	LEB1, 2, 3 or 4 high		MIN	2.4
t_{su} Setup time	Before CLKAB ↑	A bus	MIN	2.5
		CE_SEL0/1	MIN	3.2
		$\overline{CLKENAB}$	MIN	3.2
	Before LEAB1, 2, 3, or 4 ↓	A bus	MIN	3.6
	Before CLKBA ↑	B bus	MIN	3.8
		$\overline{CLKENB}$	MIN	2.3
		$\overline{CLKENBA}$	MIN	2.5
		LEB1, 2, 3 or 4	MIN	4.3
		SEL0/1	MIN	4.5
	Before LEB1, 2, 3, or 4 ↓	B bus	MIN	3.2
	Before CLKBA ↑	B bus	MIN	4
		LEB1, 2, 3 or 4	MIN	4.4
		SEL0/1	MIN	4.3
t_h Hold time	after CLKAB ↑	A bus	MIN	0.5
		CE_SEL0/1	MIN	1.1
		$\overline{CLKENAB}$	MIN	0.5
	after LEAB1, 2, 3, or 4 ↓	A bus	MIN	1.2
	after CLKBA ↑	B bus	MIN	1.3
		$\overline{CLKENB}$	MIN	1
		$\overline{CLKENBA}$	MIN	1
		SEL0/1	MIN	0
	after LEB1, 2, 3, or 4 ↓	B bus	MIN	1.5
	after CLKBA ↑	B bus	MIN	0.4
		SEL0/1	MIN	0.1

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABTH
t_{PLH}	B	A	MAX	6.5
t_{PHL}				6.5
t_{PZH}	$\overline{OEA}$	A	MAX	5.6
t_{PZL}				5.2
t_{PHZ}	$\overline{OEA}$	A	MAX	5.9
t_{PLZ}				6.5
t_{PLH}	A	B	MAX	5.7
t_{PHL}				5.7
t_{PZH}	$\overline{OEB}$	B	MAX	6.4
t_{PZL}				6.3
t_{PHZ}	$\overline{OEB}$	B	MAX	7
t_{PLZ}				6.1
t_{PZH}	$\overline{OEB1}$, $\overline{2}$, $\overline{3}$, $\overline{4}$	B	MAX	5.8
t_{PZL}				5.6
t_{PHZ}	$\overline{OEB1}$, $\overline{2}$, $\overline{3}$, $\overline{4}$	B	MAX	6.1
t_{PLZ}				5.3
t_{PLH}	CLKBA	A	MAX	7.4
t_{PHL}				7.7
t_{PLH}	CLKAB	B	MAX	6.2
t_{PHL}				5.9
t_{PLH}	LEBA	A	MAX	5.6
t_{PHL}				5.3
t_{PLH}	LEAB1, 2, 3, 4	B	MAX	5.8
t_{PHL}				5.6
t_{PLH}	LEBA1, 2, 3, 4	A	MAX	7.2
t_{PHL}				6.8
t_{PLH}	SEL	A	MAX	7.5
t_{PHL}				6.9

UNIT fmax : MHz other : ns

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{CLKENAB}$	CLKAB	$\overline{OEAB}$	A	B
H	X	X	X	Z
X	X	H	X	Z
L	L	L	X	B0‡
L	↑	L	L	L
L	↑	L	H	H

† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{CLKENBA}$, CLKBA, and $\overline{OEBA}$.
‡ Output level before the indicated steady-state input conditions were established.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

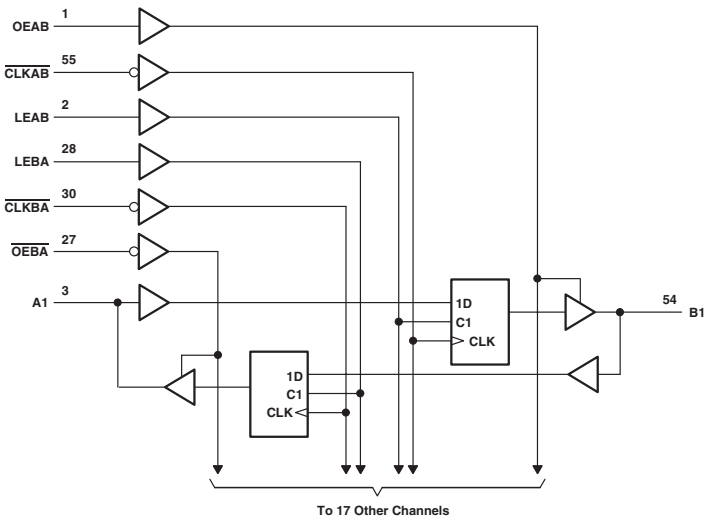
PARAMETER	MAX or MIN	ABT	ACT	UNIT
I_{CC}	MAX	35	0.08	mA
I_{OH}	MAX	-32	-24	mA
I_{OL}	MAX	64	24	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ACT
f_{max}			MIN	150	55
t_w Pulse duration, CLKAB or CLKBA high			MIN	3.3	4
t_w Pulse duration, CLKAB or CLKBA low				3.3	8.5
t_{su} Setup time, data before CLKAB ↑ or CLKBA ↑			MIN	4	6
t_h Hold time, data after CLKAB ↑ or CLKBA ↑			MIN	1	1
t_{PLH}	CLK	A or B	MAX	4.9	11.8
t_{PHL}				4.9	11.7
t_{PZH}	$\overline{OE}$	A or B	MAX	4.9	11.9
t_{PZL}				6.8	13.4
t_{PHZ}	$\overline{OE}$	A or B	MAX	5.5	9.9
t_{PLZ}				5.3	9.5
t_{PZH}	$\overline{CLKEN}$	A or B	MAX	5.7	12.5
t_{PZL}				7.2	14.3
t_{PHZ}	$\overline{CLKEN}$	A or B	MAX	5.8	11.2
t_{PLZ}				5.4	10.9

UNIT fmax : MHz other : ns

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS				OUTPUT
OEAB	LEAB	$\overline{CLKAB}$	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B_0‡
H	L	L	X	B_0§

† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, and $\overline{CLKBA}$.
‡ Output level befor the indicated steady-state input conditions were established.
§ Output level before the indicated steady-state input conditions were established, provided that $\overline{CLKAB}$ was low before LEAB went low.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

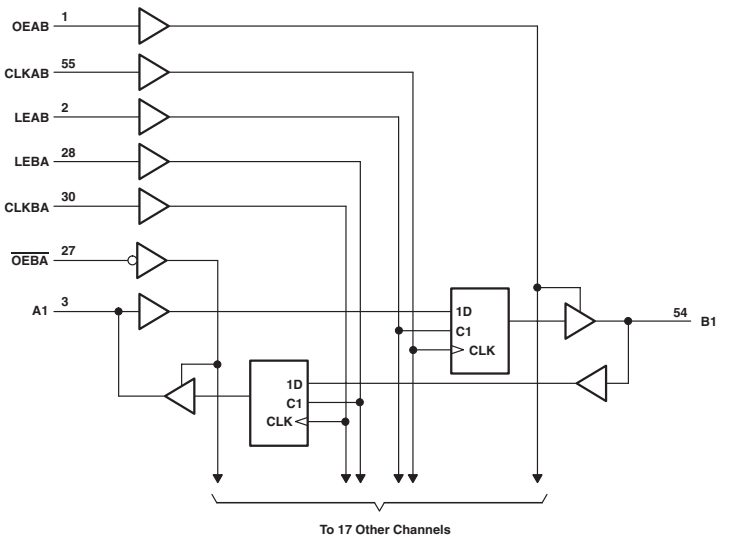
PARAMETER	MAX or MIN	ABT	LVTH 3V	ALVCH 3V	UNIT
I_{CC}	MAX	36	5	0.04	mA
I_{OH}	MAX	-32	-32	-24	mA
I_{OL}	MAX	64	64	24	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVTH 3V	ALVCH 3V
f_{max}			MIN	150	150	150
t_w Pulse duration	LEAB or LEBA high		MIN	2.5	3.3	3.3
	$\overline{CLKAB}$ or $\overline{CLKBA}$ high or low			3	3.3	3.3
t_{su} Setup time	A before $\overline{CLKAB}$ ↓		MIN	3	2.9	1.3
	B before $\overline{CLKBA}$ ↓			3	2.9	1.3
	A before LEAB ↓ or LEBA ↓ $\overline{CLK}$ high			1	1.4	1
	A before LEAB ↓ or LEBA ↓ $\overline{CLK}$ low			2.5	2.9	1.4
t_h Hold time	A after $\overline{CLKAB}$ ↓ or B after $\overline{CLKBA}$ ↓		MIN	0	0.4	1.3
	A after LEAB ↓ or B after LEBA ↓ high			2	1.6	1.5
	A after LEAB ↓ or B after LEBA ↓ low			2	1.6	1.2
t_{PLH}	A or B	B or A	MAX	4	3.7	3.9
t_{PHL}				4.9	3.7	3.9
t_{PZH}	LEAB or LEBA	B or A	MAX	5	5.1	4.7
t_{PZL}				5	5.1	4.7
t_{PHZ}	$\overline{CLKAB}$ or $\overline{CLKBA}$	B or A	MAX	5.3	5	5.5
t_{PLZ}				5.3	5	5.5
t_{PZH}	OEAB	B	MAX	5.1	4.8	4.6
t_{PZL}				5.4	4.8	4.6
t_{PHZ}	OEAB	B	MAX	6.5	5.8	5
t_{PLZ}				5.4	5.8	5
t_{PZH}	$\overline{OEBA}$	A	MAX	5.1	4.8	5.2
t_{PZL}				5.4	4.8	5.2
t_{PHZ}	$\overline{OEBA}$	A	MAX	6.5	5.8	4.3
t_{PLZ}				5.4	5.8	4.3

UNIT fmax : MHz other : ns

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS				OUTPUT
OEAB	**LEAB**	**CLKAB**	**A**	**B**
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	H	X	B_0‡
H	L	L	X	B_0§

† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, and CLKBA.
‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.
§ Output level before the indicated steady-state input conditions were established.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

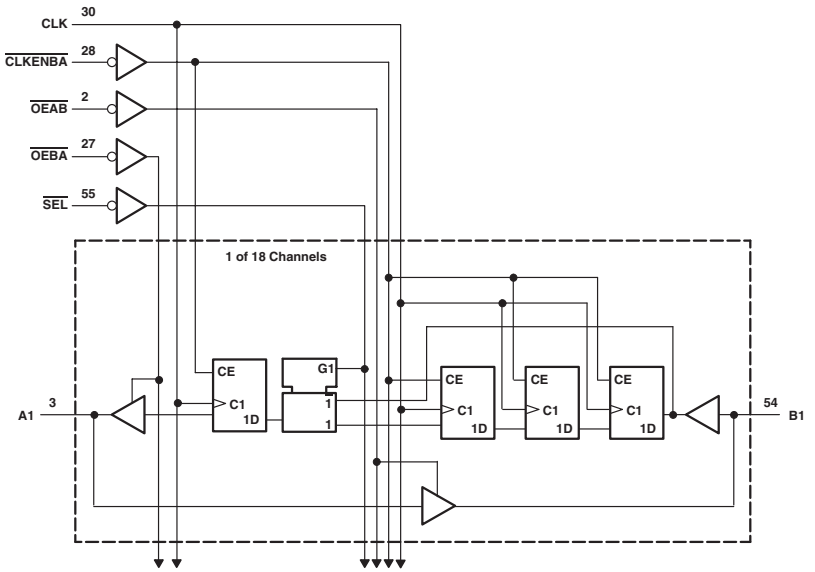
PARAMETER	MAX or MIN	ABT	LVTH 3V	ALVCH 3V	AUC 1.8V	AUC 2.3V	UNIT
I_{CC}	MAX	76	5	0.04	0.02	0.02	mA
I_{OH}	MAX	-32	-32	-24	-8	-9	mA
I_{OL}	MAX	64	64	24	8	9	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVTH 3V	ALVCH 3V	AUC 1.8V	AUC 2.3V
f_{max}			MIN	105	150	150	300	350
t_w Pulse duration	LEAB or LEBA high		MIN	3.3	3.3	3.3	1.5	1.5
	CLKAB or CLKBA high or low		MIN	4.7	3.3	3.3	1.5	1.5
t_{su} Setup time	A before CLKAB ↑		MIN	3.5	2.1	1.7	0.6	0.6
	B before CLKBA ↑		MIN	3.5	2.1	1.7	0.6	0.6
	A before LEAB ↓ or LEBA ↓ CLK high		MIN	4	2.4	1.5	0.3	0.3
	A before LEAB ↓ or LEBA ↓ CLK low		MIN	1.5	1.4	1	0.3	0.3
t_h Hold time	A after CLKAB ↑ or B after CLKBA ↑		MIN	1	1	0.7	0.9	0.9
	A after LEAB ↓ or B after LEBA ↓		MIN	2.5	1.7	1.4	1.2	1.2
t_{PLH}	A or B	B or A	MAX	3.7	3.7	3.9	2.8	2.3
t_{PHL}				4	3.7	3.9	2.8	2.3
t_{PZH}	LEAB or LEBA	B or A	MAX	5.1	5.1	4.6	3.8	3
t_{PZL}				4.4	5.1	4.6	3.8	3
t_{PHZ}	CLKAB or CLKBA	B or A	MAX	5	5.1	4.9	3.3	2.7
t_{PLZ}				4.4	5.1	4.9	3.3	2.7
t_{PZH}	OEAB	B	MAX	4.7	4.8	4.6	3.4	2.8
t_{PZL}				6.5	4.8	4.6	3.4	2.8
t_{PHZ}	OEAB	B	MAX	5.8	5.8	5	3.2	3.1
t_{PLZ}				4.9	5.8	5	3.2	3.1
t_{PZH}	$\overline{OEBA}$	A	MAX	4.7	4.8	5	3.7	3
t_{PZL}				6.5	4.8	5	3.7	3
t_{PHZ}	$\overline{OEBA}$	A	MAX	5.8	5.8	4.2	5.2	3
t_{PLZ}				4.9	5.8	4.2	5.2	3

UNIT fmax : MHz other : ns AUC:Preview

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

B-TO-A STORAGE ($\overline{OEBA}$ = L)

INPUTS				OUTPUT
$\overline{CLKENBA}$	CLK	$\overline{SEL}$	B	A
H	X	X	X	A_0†
L	↑	H	L	L
L	↑	H	H	H
L	↑	L	L	L‡
L	↑	L	H	H‡

† Output level before the indicated steady-state input conditions were established

‡ Four positive CLK edges are needed to propagate data from B to A when $\overline{SEL}$ is low.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

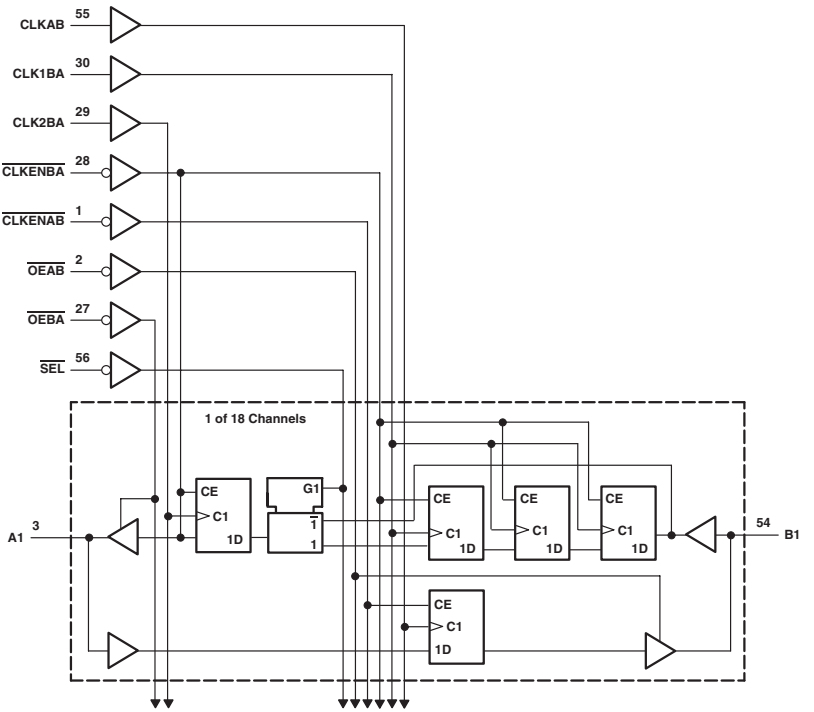
PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I_{CC}	MAX	0.04	mA
I_{OH}	MAX	-24	mA
I_{OL}	MAX	24	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
f_{max}			MIN	150
t_w Pulse duration, CLK high or low			MIN	3
t_{su} Setup time	B data before CLK ↑		MIN	1.1
	$\overline{SEL}$ before CLK ↑		MIN	2.1
	$\overline{CLKENBA}$ before CLK ↑		MIN	2
t_h Hold time	B data after CLK ↑		MIN	1.2
	$\overline{SEL}$ after CLK ↑		MIN	0.8
	$\overline{CLKENBA}$ after CLK ↑		MIN	0.3
t_{pd}	A	B	MAX	3.2
	CLK	A		5.2
t_{en}	$\overline{OEAB}$ or $\overline{OEBA}$	A or B	MAX	5.1
t_{dis}	$\overline{OEAB}$ or $\overline{OEBA}$	A or B		4.9

UNIT fmax : MHz other : ns

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

A-TO-B STORAGE ($\overline{OEAB}$ = L)

INPUTS			OUTPUT
$\overline{CLKENAB}$	CLKAB	A	B
H	X	X	B_0†
L	↑	L	L
L	↑	H	H

† Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE ($\overline{OEBA}$ = L)

INPUTS					OUTPUT
$\overline{CLKENA}$	CLK2BA	CLK1BA	$\overline{SEL}$	B	A
H	X	X	X	X	A_0†
L	↑	X	H	L	L
L	↑	X	H	H	H
L	↑	↑	L	L	L‡
L	↑	↑	L	H	H‡

† Output level before the indicated steady-state input conditions were established
‡ Three CLK1BA edges and one CLK2BA edge are needed to propagate data from B to A when $\overline{SEL}$ is low.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I_{CC}	MAX	0.04	mA
I_{OH}	MAX	-24	mA
I_{OL}	MAX	24	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

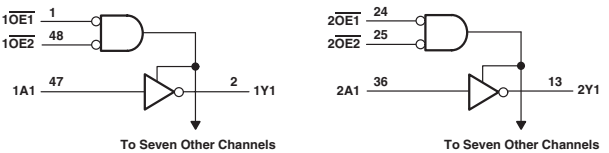
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
f_{max}			MIN	150
t_w Pulse duration, CLK high or low			MIN	3
t_{su} Setup time	A data before CLKAB ↑		MIN	1.3
	B data before CLK2BA ↑		MIN	1.7
	B data before CLK1BA ↑		MIN	1.1
	$\overline{SEL}$ before CLK2BA ↑		MIN	3.3
	$\overline{CLKENAB}$ before CLKAB ↑		MIN	1.6
	$\overline{CLKENBA}$ before CLK1BA ↑		MIN	2.1
	$\overline{CLKENBA}$ before CLK2BA ↑		MIN	2.2
t_h Hold time	A data after CLKAB ↑		MIN	0.9
	B data after CLK2BA ↑		MIN	0.6
	B data after CLK1BA ↑		MIN	1
	$\overline{SEL}$ after CLK2BA ↑		MIN	0.1
	$\overline{CLKENAB}$ after CLKAB ↑		MIN	0.3
	$\overline{CLKENBA}$ after CLK1BA ↑		MIN	0.1
	$\overline{CLKENBA}$ after CLK2BA ↑		MIN	0
t_{pd}	CLKAB or CLK2BA	A or B	MAX	4.2
t_{en}	$\overline{OEAB}$ or $\overline{OEBA}$	A or B		5.1
t_{dis}	$\overline{OEAB}$ or $\overline{OEBA}$	A or B		4.9

UNIT fmax : MHz other : ns

16540

16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
(each 8-bit section)

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ACT	AHC	AHCT	LVCH 3V	UNIT
I_{CC}	MAX	34	0.08	0.04	0.04	0.02	mA
I_{OH}	MAX	-32	-24	-8	-8	-24	mA
I_{OL}	MAX	64	24	8	8	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ACT	AHC	AHCT	LVCH 3V
t_{PLH}	A	Y	MAX	4.1	7.5	8.5	10.5	3.7
t_{PHL}				4.3	9.5	8.5	10.5	3.7
t_{PZH}	$\overline{OE}$	Y	MAX	5.1	8.9	10.5	13	4.8
t_{PZL}				5.9	10.5	10.5	13	4.8
t_{PHZ}	$\overline{OE}$	Y	MAX	5.7	11.9	10.5	13	5.9
t_{PLZ}				4.7	11.1	10.5	13	5.9

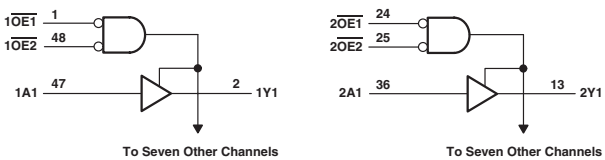
UNIT: ns

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

16541

16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
(each 8-bit section)

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

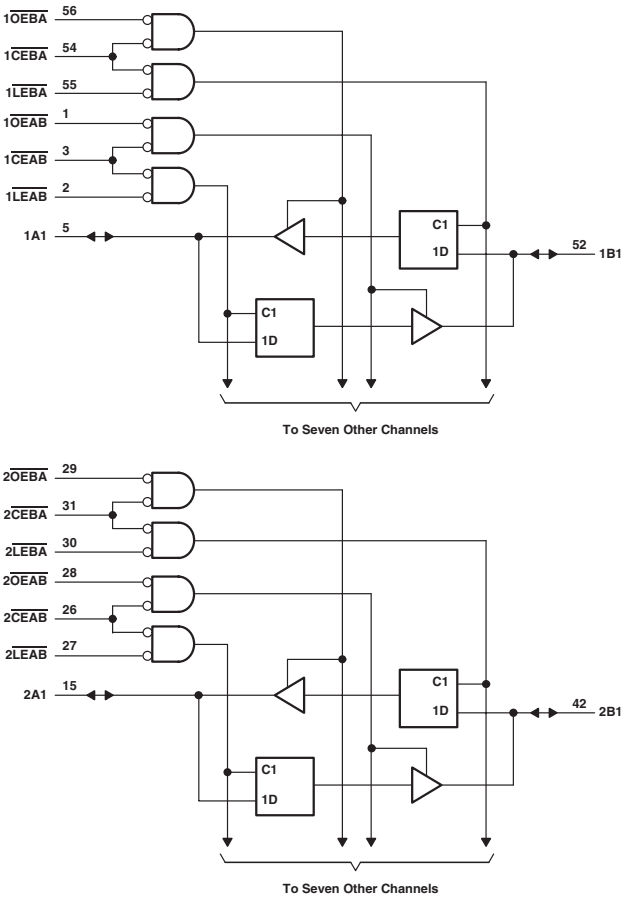
PARAMETER	MAX or MIN	ABT	LVTH 3V	ACT	AHC	AHCT	LVCH 3V	UNIT
I_{CC}	MAX	34	5	0.08	0.04	0.04	0.02	mA
I_{OH}	MAX	-32	-32	-24	-8	-8	-24	mA
I_{OL}	MAX	64	64	24	8	8	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVTH 3V	ACT	AHC	AHCT	LVCH 3V
t_{PLH}	A	Y	MAX	3.4	3.5	9	8.5	10.5	4.2
t_{PHL}				4.2	3.5	9.2	8.5	10.5	4.2
t_{PZH}	$\overline{OE}$	Y	MAX	5.2	4.6	9.7	10.5	13	5.6
t_{PZL}				6	4.6	11	10.5	13	5.6
t_{PHZ}	$\overline{OE}$	Y	MAX	5.4	5.9	11.3	10.5	13	6.8
t_{PLZ}				4.3	5.4	10.7	10.5	13	6.8

UNIT: ns

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE
(each 8-bit section)

INPUTS				OUTPUT
$\overline{CEAB}$	LEAB	$\overline{OEAB}$	A	B
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B_0‡
L	L	L	L	L
L	L	L	H	H

† A-to-B data flow is shown: B-to-A flow control is the same except that it uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.
‡ Output level before the indicated steady-state input conditions were established.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

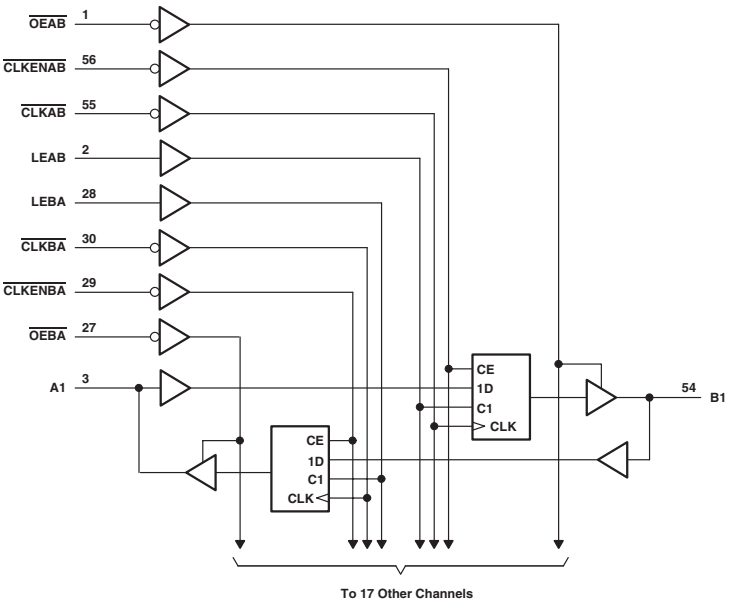
PARAMETER	MAX or MIN	ABT	LVT 3V	LVTH 3V	AC	ACT	LVCH 3V	ALVCH 3V	UNIT
I_{CC}	MAX	35	5	5	0.08	0.08	0.02	0.04	mA
I_{OH}	MAX	-32	-32	-32	-24	-24	-24	-24	mA
I_{OL}	MAX	64	64	64	24	24	24	24	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVT 3V	LVTH 3V	AC	ACT	LVCH 3V	ALVCH 3V
t_w Pulse duration, $\overline{LEAB}$ or $\overline{LEBA}$ low			MIN	4	3.3	3.3	4	7.5	3.3	3.3
t_{su} Setup time	Data before $\overline{LEAB}$ ↑ or $\overline{LEBA}$ ↑, high		MIN	1.5	0.8	0.5	1	2.5	1.1	1.2
	Data before $\overline{LEAB}$ ↑ or $\overline{LEBA}$ ↑, low		MIN	3.5	1.5	0.8	1	2.5	1.1	1.2
	Data before $\overline{CEAB}$ ↑ or $\overline{CEBA}$ ↑, high		MIN	-	0.7	0	-	-	1.1	1.2
	Data before $\overline{CEAB}$ ↑ or $\overline{CEBA}$ ↑, low		MIN	-	1.6	0.6	-	-	1.1	1.2
t_h Hold time	Data after $\overline{LEAB}$ ↑ or $\overline{LEBA}$ ↑, high		MIN	1.5	0.8	1.5	3	4	1.9	1.3
	Data after $\overline{LEAB}$ ↑ or $\overline{LEBA}$ ↑, low		MIN	2	1.2	1.2	3	4	1.9	1.3
	Data after $\overline{CEAB}$ ↑ or $\overline{CEBA}$ ↑, high		MIN	-	0.8	1.7	-	-	1.9	1.3
	Data after $\overline{CEAB}$ ↑ or $\overline{CEBA}$ ↑, low		MIN	-	1.3	1.6	-	-	1.9	1.3
t_{PLH}	A or B	B or A	MAX	3.8	4.6	3.2	8.8	10.5	5.4	4.3
t_{PHL}				5.1	4.6	3.2	9.2	11.6	5.4	4.3
t_{PLH}	$\overline{LE}$	A or B	MAX	5.2	6.3	3.9	11.5	13.8	6.1	5
t_{PHL}				5.6	6	3.9	10.9	13.5	6.1	5
t_{PZH}	$\overline{OE}$	A or B	MAX	5.2	5.8	4.3	9.6	11.4	6.3	5.3
t_{PZL}				7	6.2	4.3	11.3	13.2	6.3	5.3
t_{PHZ}	$\overline{OE}$	A or B	MAX	5.7	6.5	4.7	8.9	11.1	6.3	4.6
t_{PLZ}				4.6	5.8	4.4	8.4	9.6	6.3	4.6
t_{PZH}	$\overline{CE}$	A or B	MAX	6.2	6	4.5	9.8	11.7	6.6	5.6
t_{PZL}				7.8	6.4	4.5	11.5	13.5	6.6	5.6
t_{PHZ}	$\overline{CE}$	A or B	MAX	6.6	6.4	4.9	9.3	11.6	6.6	5.1
t_{PLZ}				5.4	5.4	4.7	8.8	10.5	6.6	5.1

UNIT: ns

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS					OUTPUT
$\overline{CLKENAB}$	$\overline{OEAB}$	LEAB	$\overline{CLKAB}$	A	B
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B_0‡
H	L	L	X	X	B_0‡
L	L	L	↓	L	L
L	L	L	↓	H	H
L	L	L	H	X	B_0‡
L	L	L	L	X	B_0§

† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, $\overline{CLKBA}$ and $\overline{CLKENBA}$.
‡ Output level before the indicated steady-state input conditions were established.
§ Output level before the indicated steady-state input conditions were established, provided that $\overline{CLKAB}$ was low before LEAB went low.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

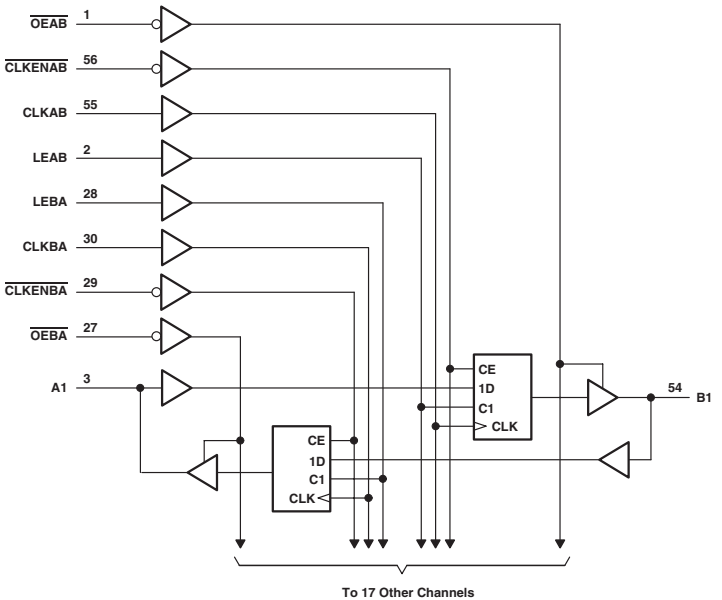
PARAMETER	MAX or MIN	ABT	ALVCH 3V	UNIT
I_{CC}	MAX	36	0.04	mA
I_{OH}	MAX	-32	-24	mA
I_{OL}	MAX	64	24	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ALVCH 3V
f_{max}			MIN	150	150
t_w Pulse duration	LEAB or LEBA high		MIN	2.5	3.3
	$\overline{CLKAB}$ or $\overline{CLKBA}$ high or low		MIN	3	3.3
t_{su} Setup time	A before $\overline{CLKAB}$ ↓ or B before $\overline{CLKBA}$ ↓		MIN	3	-
	Data before $\overline{CLK}$ ↑			-	1.2
	A before LEAB ↓ or B before LEBA ↓ , $\overline{CLK}$ high		MIN	2.5	1.1
	A before LEAB ↓ or B before LEBA ↓ , $\overline{CLK}$ low		MIN	2.5	1.5
	$\overline{CLKEN}$ after CLK ↓			2.5	-
	$\overline{CLKEN}$ after CLK ↑		MIN	2.5	0.8
t_h Hold time	A after $\overline{CLKAB}$ ↓ or B after $\overline{CLKBA}$ ↓		MIN	0	-
	Data after $\overline{CLK}$ ↑			-	1.5
	A after LEAB ↓ or B after LEBA ↓ , $\overline{CLK}$ high		MIN	2	1.6
	A after LEAB ↓ or B after LEBA ↓ , $\overline{CLK}$ low		MIN	2	1.3
	$\overline{CLKEN}$ after CLK ↓			1	-
	$\overline{CLKEN}$ after CLK ↑		MIN	-	1.4
t_{PLH}	A or B	B or A	MAX	4	4
t_{PHL}				4.9	4
t_{PLH}	LEAB or LEBA	B or A	MAX	5	4.8
t_{PHL}				5	4.8
t_{PLH}	$\overline{CLKAB}$ or $\overline{CLKBA}$	B or A	MAX	5.3	5.7
t_{PHL}				5	5.7
t_{PZH}	$\overline{OEAB}$	B	MAX	5.1	5.2
t_{PZL}				5.4	5.2
t_{PHZ}	$\overline{OEAB}$	B	MAX	6.2	4.4
t_{PLZ}				5.4	4.4
t_{PZH}	$\overline{OEBA}$	A	MAX	5.1	5.2
t_{PZL}				5.4	5.2
t_{PHZ}	$\overline{OEBA}$	A	MAX	6.2	4.4
t_{PLZ}				5.4	4.4

UNIT fmax : MHz other : ns

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS					OUTPUT
CLKENAB	$\overline{OEAB}$	LEAB	CLKAB	A	B
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B_0‡
H	L	L	X	X	B_0‡
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L	X	B_0‡
L	L	L	H	X	B_0§

† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, CLKBA and $\overline{CLKENBA}$.
‡ Output level before the indicated steady-state input conditions were established.
§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

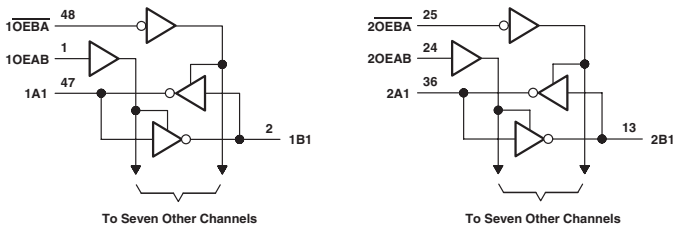
PARAMETER	MAX or MIN	ABT	ALVTH 3V	ALVCH 3V	ALVCHR 3V
I_{CC}	MAX	36	5	0.04	0.04
I_{OH}	MAX	-32	-32	-24	-12
I_{OL}	MAX	64	64	24	12

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ALVTH 3V	ALVCH 3V	ALVCHR 3V
f_{max}			MIN	150	150	150	150
t_w Pulse duration	LEAB or LEBA high		MIN	2.5	1.8	3.3	3.3
	CLKAB or CLKBA high or low		MIN	3	2.3	3.3	3.3
t_{su} Setup time	Data before CLK ↑ high		MIN	4	2.4	2.1	2.1
	Data before CLK ↑ low			4	3.8	2.1	2.1
	A before LEAB ↓ or B before LEBA ↓ , CLK high		MIN	2.5	1	1.6	1.6
	A before LEAB ↓ or B before LEBA ↓ , CLK low		MIN	1	0.6	1.1	1.1
	$\overline{CLKEN}$ before ↑ high		MIN	2.5	1.4	1.7	1.7
	$\overline{CLKEN}$ before ↑ low			2.5	1.9	1.7	1.7
t_h Hold time	Data after CLK ↑ high		MIN	0	0.5	0.8	0.8
	Data after CLK ↑ low			0	0.5	0.8	0.8
	A after LEAB ↓ or B after LEBA ↓ , $\overline{CLK}$ high		MIN	2	2	1.4	1.4
	A after LEAB ↓ or B after LEBA ↓ , $\overline{CLK}$ low		MIN	2	2.3	1.7	1.7
	$\overline{CLKEN}$ after ↑ high		MIN	0	0.6	0.6	0.6
	$\overline{CLKEN}$ after ↑ low			0	0.5	0.6	0.6
t_{PLH}	A or B	B or A	MAX	4	3.9	4.1	4.4
t_{PHL}				4.9	3.9	4.1	4.4
t_{PLH}	LEAB or LEBA	B or A	MAX	5	4.6	4.7	5.1
t_{PHL}				5.2	4.6	4.7	5.1
t_{PLH}	CLKAB or CLKBA	B or A	MAX	4.7	4.5	5	5.4
t_{PHL}				4.6	4.6	5	5.4
t_{PZH}	$\overline{OEAB}$	B	MAX	5.5	4.2	5.2	5.6
t_{PZL}				5.8	4.4	5.2	5.6
t_{PHZ}	$\overline{OEAB}$	B	MAX	6.2	5.3	4.4	4.7
t_{PLZ}				5.4	4.6	4.4	4.7
t_{PZH}	$\overline{OEBA}$	A	MAX	5.5	4.2	5.2	5.6
t_{PZL}				5.8	4.4	5.2	5.6
t_{PHZ}	$\overline{OEBA}$	A	MAX	6.2	5.3	4.4	4.7
t_{PLZ}				5.4	4.6	4.4	4.7

UNIT fmax : MHz other : ns

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS		OPERATION
$\overline{OEBA}$	OEAB	
L	L	$\overline{B}$ data to A bus
L	H	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus
H	L	Isolation
H	H	$\overline{A}$ data to B bus

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AC	ACT	UNIT
I_{CC}	MAX	0.08	0.08	mA
I_{OH}	MAX	-24	-24	mA
I_{OL}	MAX	24	24	mA

SWITCHING CHARACTERISTICS

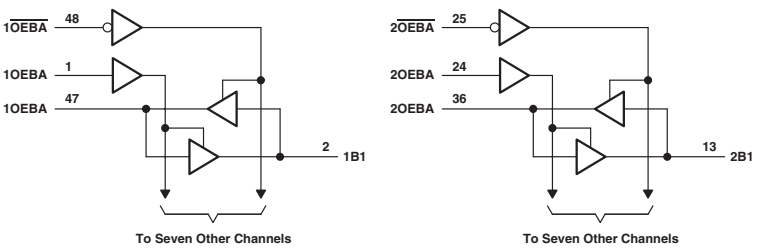
PARAMETER	INPUT	OUTPUT	MAX or MIN	AC	ACT
t_{PLH}	A	B	MAX	6.8	8.5
t_{PHL}				8.2	10.5
t_{PLH}	B	A	MAX	6.8	8.5
t_{PHL}				8.2	10.5
t_{PZH}	$\overline{OEBA}$	A	MAX	7.9	9.1
t_{PZL}				9.4	10.9
t_{PHZ}	$\overline{OEBA}$	A	MAX	9.2	11.9
t_{PLZ}				8.3	10.6
t_{PZH}	OEAB	B	MAX	7.3	8.9
t_{PZL}				9.1	10.5
t_{PHZ}	OEAB	B	MAX	9	10.8
t_{PLZ}				8	9.6

UNIT: ns

16623

16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
$\overline{OEBA}$	OEAB	
L	L	B data to A bus
L	H	B data to A bus, A data to B bus
H	L	Isolation
H	H	A data to B bus

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ACT	UNIT
I_{CC}	MAX	35	0.08	mA
I_{OH}	MAX	-32	-24	mA
I_{OL}	MAX	64	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ACT
t_{PLH}	A or B	B or A	MAX	3.6	7.7
t_{PHL}				4.3	8.6
t_{PZH}	$\overline{OEBA}$	A	MAX	4.9	9.5
t_{PZL}				6	11.1
t_{PHZ}	$\overline{OEBA}$	A	MAX	6	12
t_{PLZ}				5.4	10.7
t_{PZH}	OEAB	B	MAX	4.9	9.3
t_{PZL}				6	10.6
t_{PHZ}	OEAB	B	MAX	6	10.4
t_{PLZ}				5.4	9.5

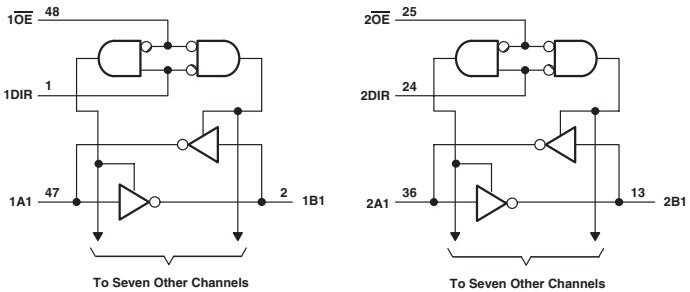
UNIT: ns

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

16640

16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	$\overline{B}$ data to A bus
L	H	$\overline{A}$ data to B bus
H	X	Isolation

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	AC	ACT	UNIT
I_{CC}	MAX	32	0.08	0.08	mA
I_{OH}	MAX	-32	-24	-24	mA
I_{OL}	MAX	64	24	24	mA

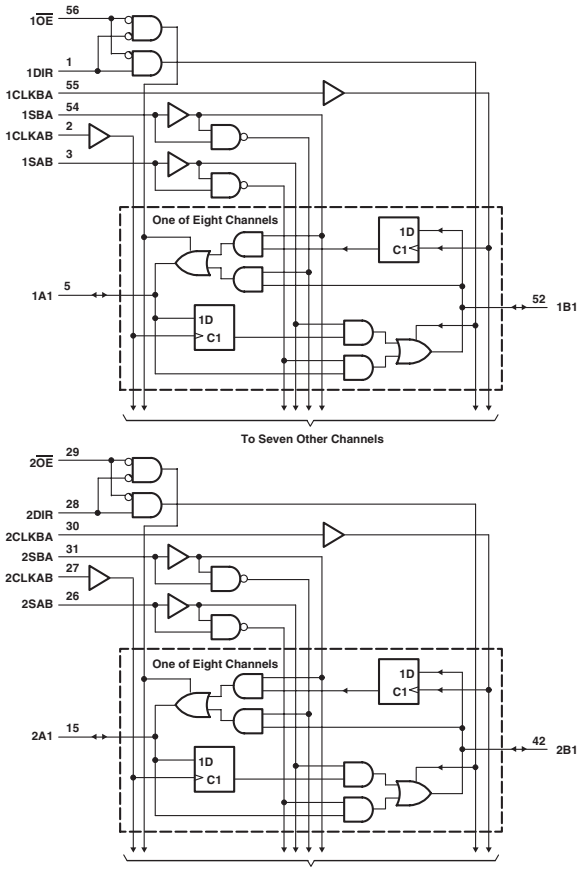
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	AC	ACT
t_{PLH}	A or B	B or A	MAX	4.3	7.3	9.1
t_{PHL}				3.9	8.6	10.5
t_{PZH}	$\overline{OE}$	A or B	MAX	5.5	8	9.8
t_{PZL}				6.3	9.9	11.5
t_{PHZ}	$\overline{OE}$	A or B	MAX	6.3	9.9	12.5
t_{PLZ}				4.2	9	11

UNIT: ns

16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified †	Store A, B unspecified †
X	X	X	↑	X	X	Unspecified †	Input	Store B, A unspecified †
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

† The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	LVT 3V	LVTH 3V	AC	ACT	LVC 3V	LVCH 3V	ALVCH 3V	AVC 3V	UNIT
I_{CC}	MAX	32	5	5	0.08	0.08	0.02	0.02	0.04	0.04	mA
I_{OH}	MAX	-32	-32	-32	-24	-24	-24	-24	-24	-12	mA
I_{OL}	MAX	64	64	64	24	24	24	24	24	12	mA

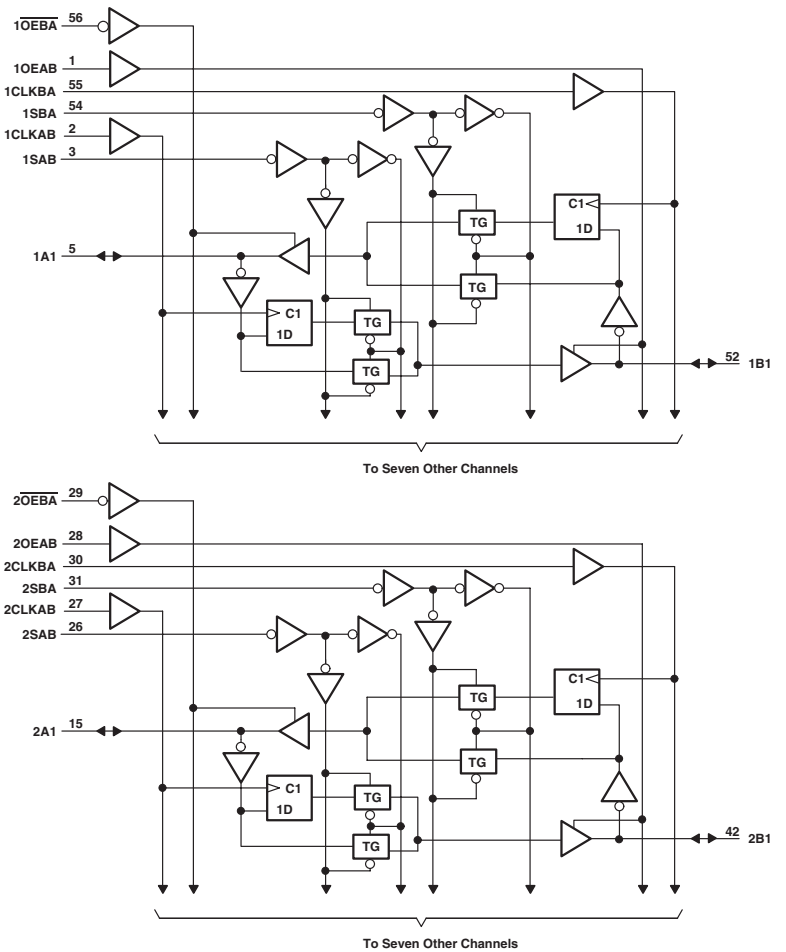
TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVT 3V	LVTH 3V	AC	ACT	LVC 3V	LVCH 3V
f_{max}			MIN	125	150	150	75	90	150	150
t_w Pulse duration	CLKAB or CLKBA high or low		MIN	4.3	3.3	3.3	6.5	5.5	3.3	3.3
t_{su} Setup time	A or B before CLKAB ↑ or CLKBA ↑, data high		MIN	3	1.3	1.2	5	4	2.7	2.9
	A or B before CLKAB ↑ or CLKBA ↑, data low		MIN	3	2.4	2	5	6	2.7	2.9
t_h Hold time	A or B after CLKAB ↑ or CLKBA ↑, data high		MIN	0	0.5	0.5	1	1.5	0.3	0.3
	A or B after CLKAB ↑ or CLKBA ↑, data low		MIN	0	0.5	0.5	1	1.5	0.3	0.3
t_{PLH}	CLKAB or CLKBA	B or A	MAX	4.9	5.7	4.2	12.1	12.2	6	6.7
t_{PHL}				4.7	5.7	4.2	11.9	12.3	6	6.7
t_{PLH}	A or B	B or A	MAX	3.9	4.7	3.4	9.5	10.6	5.2	5.7
t_{PHL}				4.6	4.7	3.4	9.7	11.4	5.2	5.7
t_{PLH}	SAB or SBA	B or A	MAX	5	6.2	4.5	12.5	15.6	6.1	7.7
t_{PHL}				5	6.2	4.5	13.1	16.7	6.1	7.7
t_{PZH}	$\overline{OE}$	A or B	MAX	5.5	5.4	4.3	10.5	11.9	6.9	6.9
t_{PZL}				5.7	5.6	4.3	12.2	13.5	6.9	6.9
t_{PHZ}	$\overline{OE}$	A or B	MAX	5.4	6.5	5.6	8.9	10.2	6.9	6.9
t_{PLZ}				4.5	5.8	5.4	8.6	9.9	6.9	6.9
t_{PZH}	DIR	A or B	MAX	5.4	5.7	4.4	10.9	15.2	7.2	7.2
t_{PZL}				5.6	5.8	4.4	12.2	13.1	7.2	7.2
t_{PHZ}	DIR	A or B	MAX	6.7	7.2	5.7	9.4	10.8	7	7
t_{PLZ}				5.9	6.6	5.2	8.8	10.4	7	7

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V	AVC 3V
f_{max}			MIN	150	350
t_w Pulse duration	CLKAB or CLKBA high or low		MIN	3.3	1.4
t_{su} Setup time	A or B before CLKAB ↑ or CLKBA ↑, data high		MIN	1.4	0.8
	A or B before CLKAB ↑ or CLKBA ↑, data low		MIN	1.4	0.8
t_h Hold time	A or B after CLKAB ↑ or CLKBA ↑, data high		MIN	0.7	0.6
	A or B after CLKAB ↑ or CLKBA ↑, data low		MIN	0.7	0.6
t_{PLH}	CLKAB or CLKBA	B or A	MAX	4.5	3.3
t_{PHL}				4.5	3.3
t_{PLH}	A or B	B or A	MAX	3.9	2.6
t_{PHL}				3.9	2.6
t_{PLH}	SAB or SBA	B or A	MAX	5.3	4
t_{PHL}				5.3	4
t_{PZH}	$\overline{OE}$	A or B	MAX	5.1	4
t_{PZL}				5.1	4
t_{PHZ}	$\overline{OE}$	A or B	MAX	4.7	4.2
t_{PLZ}				4.7	4.2
t_{PZH}	DIR	A or B	MAX	5.1	4.3
t_{PZL}				5.1	4.3
t_{PHZ}	DIR	A or B	MAX	5.3	4.3
t_{PLZ}				5.3	4.3

UNIT fmax : MHz other : ns

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS						DATA I/O †		OPERATION OR FUNCTION
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA	A1-A8	B1-B8	
L	H	L	L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	L	X	X	Input	Unspecified‡	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	L	↑	X	X	Unspecified‡	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time $\overline{B}$ data to A bus
L	L	X	L	X	H	Output	Input	Store $\overline{B}$ data to A bus
H	H	X	X	L	X	Input	Output	Real-time $\overline{A}$ data to B bus
H	H	L	X	H	X	Input	Output	Store $\overline{A}$ data to B bus
H	L	L	L	H	H	Output	Output	Store $\overline{A}$ data to B bus and Store $\overline{B}$ data to A bus

† The data-output functions may be enabled or disabled by a variety of level combinations at OEAB or $\overline{OEBA}$. Data-input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.
‡ Select control = L; clocks can occur simultaneously.
Select control = H; clocks must be staggered to load both registers.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

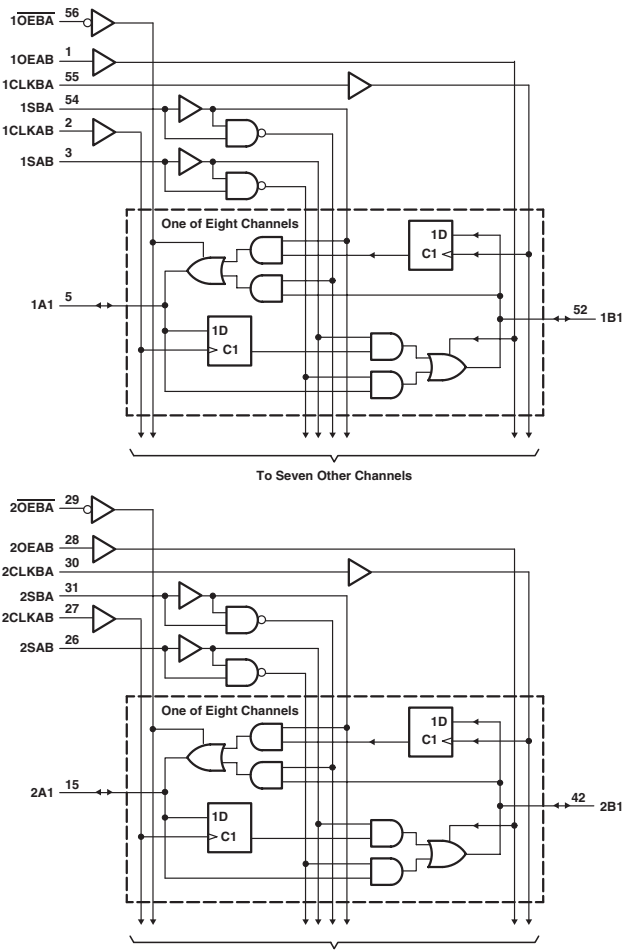
PARAMETER	MAX or MIN	ACT	UNIT
I_{CC}	MAX	0.08	mA
I_{OH}	MAX	-24	mA
I_{OL}	MAX	24	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ACT
f_{max}			MIN	90
t_w Pulse duration	CLKAB or CLKBA high or low		MIN	5.5
t_{su} Setup time	A before CLKAB ↑ or B before CLKBA ↑		MIN	5.3
t_h Hold time	A after CLKAB ↑ or B after CLKBA ↑		MIN	1
t_{PLH}	A or B	B or A	MAX	11.3
t_{PHL}				11.9
t_{PLH}	CLKAB or CLKBA	A or B	MAX	13.7
t_{PHL}				13.6
t_{PLH}	SAB or SBA	A or B	MAX	17.3
t_{PHL}				17.8
t_{PZH}	$\overline{OEBA}$	A	MAX	12.3
t_{PZL}				13.9
t_{PHZ}	$\overline{OEBA}$	A	MAX	10.6
t_{PLZ}				10.8
t_{PZH}	OEAB	B	MAX	11.9
t_{PZL}				13.5
t_{PHZ}	OEAB	B	MAX	11.4
t_{PLZ}				11.6

UNIT fmax : MHz other : ns

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified ‡	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified ‡	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	H or L	X	H	X	Input	Output	Store A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus and stored B data A bus

† The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or $\overline{OEBA}$ inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition of the clock inputs.

‡ Select control = L; clocks can occur simultaneously.
Select control = H; clocks must be staggered in order to load both registers.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

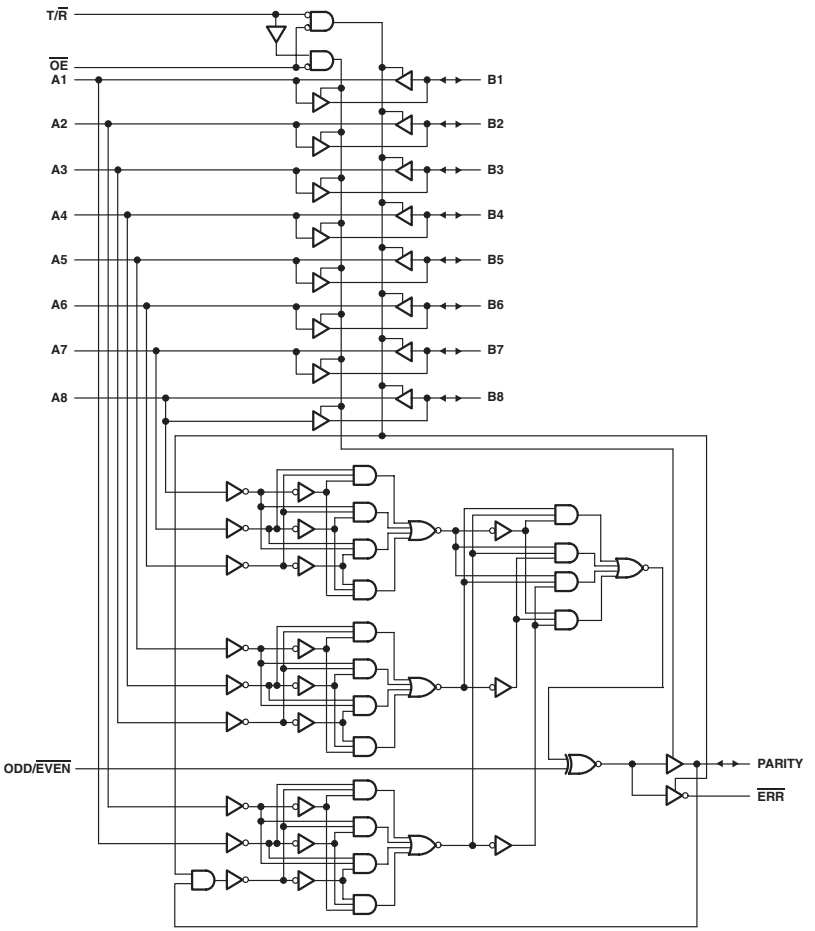
PARAMETER	MAX or MIN	ABT	LVTH 3V	AC	ACT	LVCH 3V	UNIT
I_{CC}	MAX	32	5	0.08	0.08	0.02	mA
I_{OH}	MAX	-32	-32	-24	-24	-24	mA
I_{OL}	MAX	64	64	24	24	24	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVTH 3V	AC	ACT	LVCH 3V
f_{max}			MIN	125	150	95	90	150
t_w Pulse duration	CLKAB or CLKBA high or low		MIN	4.3	3.3	5	5.5	3.3
t_{su} Setup time	A before CLKAB ↑ or B before CLKBA ↑, high		MIN	3	1.2	4.5	4.5	3
	A before CLKAB ↑ or B before CLKBA ↑, low		MIN	3	2	4.5	4.5	3
t_h Hold time	A after CLKAB ↑ or B after CLKBA ↑, high		MIN	0	0.5	0	1	0.2
	A after CLKAB ↑ or B after CLKBA ↑, low		MIN	0	0.5	0	1	0.2
t_{PLH}	CLKAB or CLKBA	A or B	MAX	4.9	4.2	12.2	12.3	6.4
t_{PHL}				4.7	4.2	12.3	12.3	6.4
t_{PLH}	A or B	B or A	MAX	3.9	3.4	9.9	10.5	6.3
t_{PHL}				4.6	3.4	10.2	11.6	6.3
t_{PLH}	SAB or SBA	A or B	MAX	5	4.5	13.8	16	7.4
t_{PHL}				5	4.5	13.8	16.9	7.4
t_{PZH}	$\overline{OEBA}$	A	MAX	5	4.3	10.7	11.7	6.3
t_{PZL}				5.3	4.3	13.2	13.4	6.3
t_{PHZ}	$\overline{OEBA}$	A	MAX	4.9	5.6	8.8	9.5	6.2
t_{PLZ}				4	5.4	8.7	9.2	6.2
t_{PZH}	OEAB	B	MAX	4.2	4.2	10.5	10.8	6.3
t_{PZL}				4.6	4.2	13	12.4	6.3
t_{PHZ}	OEAB	B	MAX	5.9	5.5	8	10.5	6.2
t_{PLZ}				5.2	5.5	7.8	9.9	6.2

UNIT fmax : MHz other : ns

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE
(each 8-bit section)

NUMBER OF A OR B INPUTS THAT ARE HIGH	INPUTS			INPUT/OUTPUT PARITY	OUTPUTS	
	$\overline{OE}$	T/$\overline{R}$	ODD/$\overline{EVEN}$		$\overline{ERR}$	OUTPUT MODE
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Don't care	H	X	X	Z	Z	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ACT	UNIT
I_{CC}	MAX	36	0.08	mA
I_{OH}	MAX	-32	-24	mA
I_{OL}	MAX	64	24	mA

SWITCHING CHARACTERISTICS

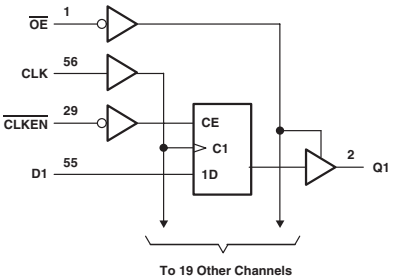
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ACT
t_{PLH}	A or B	B or A	MAX	4.1	10.7
t_{PHL}				4.3	10.6
t_{PLH}	A or B	PARITY	MAX	6.7	14.3
t_{PHL}				6.1	14.3
t_{PLH}	ODD / $\overline{EVEN}$	PARITY, $\overline{ERR}$	MAX	6.7	13.7
t_{PHL}				6.1	14.1
t_{PLH}	B	$\overline{ERR}$	MAX	6.7	14.6
t_{PHL}				6.1	14.7
t_{PLH}	PARITY	$\overline{ERR}$	MAX	6.7	13.8
t_{PHL}				6.1	14.2
t_{PZH}	$\overline{OE}$	A or B	MAX	5.6	11.3
t_{PZL}				6	13
t_{PHZ}	$\overline{OE}$	A or B	MAX	5.4	11.2
t_{PLZ}				4.3	10.5
t_{PZH}	$\overline{OE}$	PARITY, $\overline{ERR}$	MAX	5.6	11.3
t_{PZL}				6	13
t_{PHZ}	$\overline{OE}$	PARITY, $\overline{ERR}$	MAX	5.4	11.2
t_{PLZ}				4.3	10.5

UNIT: ns

16721

20-BIT FLIP-FLOP WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
(each filp-flop)

INPUTS				OUTPUT Q
$\overline{OE}$	$\overline{CLKEN}$	CLK	D	
L	H	X	H	Q_O
L	L	↑	H	H
L	L	↑	L	L
L	L	L	X	Q_O
H	X	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I_{CC}	MAX	0.04	mA
I_{OH}	MAX	-24	mA
I_{OL}	MAX	24	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
f_{max}			MIN	150
t_w Pulse duration	CLK high or low		MIN	3.3
t_{su} Setup time	Data before CLK ↑		MIN	3.1
	$\overline{CLKEN}$ before CLK ↑		MIN	2.7
t_h Hold time	Data after CLK ↑		MIN	0
	$\overline{CLKEN}$ after CLK ↑		MIN	0
t_{PLH}	CLK	Q	MAX	4.3
t_{PHL}				4.3
t_{PZH}	$\overline{OE}$	Q	MAX	4.8
t_{PZL}				4.8
t_{PHZ}	$\overline{OE}$	Q	MAX	4.4
t_{PLZ}				4.4

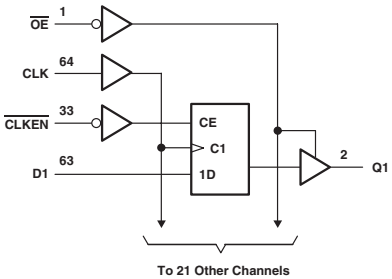
UNIT fmax : MHz other : ns

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

16722

22-BIT FLIP-FLOP WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
(each filp-flop)

INPUTS				OUTPUT
$\overline{OE}$	$\overline{CLKEN}$	CLK	D	Q
L	H	X	X	Q_O
L	L	↑	H	H
L	L	↑	L	L
L	L	L or H	X	Q_O
H	X	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AVC 3V	UNIT
I_{CC}	MAX	0.04	mA
I_{OH}	MAX	-12	mA
I_{OL}	MAX	12	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

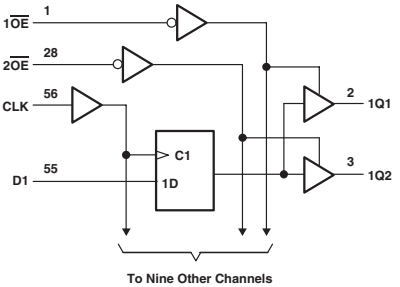
PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3V
f_{max}			MIN	150
t_w Pulse duration	CLK high or low		MIN	2.8
t_{su} Setup time	Data before CLK ↑		MIN	2.5
	$\overline{CLKEN}$ before CLK ↑		MIN	1.4
t_h Hold time	Data after CLK ↑		MIN	0
	$\overline{CLKEN}$ after CLK ↑		MIN	1.2
t_{PLH}	CLK	Q	MAX	2.6
t_{PHL}				2.6
t_{PZH}	$\overline{OE}$	Q	MAX	4.3
t_{PZL}				4.3
t_{PHZ}	$\overline{OE}$	Q	MAX	3.4
t_{PLZ}				3.4

UNIT fmax : MHz other : ns

16820

10-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH DUAL OUTPUTS

Logic Diagram



FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}_n$†	CLK	D	Q_n†
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

† n = 1, 2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I_{CC}	MAX	0.04	mA
I_{OH}	MAX	-24	mA
I_{OL}	MAX	24	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
f_{max}			MIN	150
t_w Pulse duration	CLK high or low		MIN	3.3
t_{su} Setup time	Data before CLK ↑		MIN	1.4
t_h Hold time	Data after CLK ↑		MIN	1
t_{PLH}	CLK	Q	MAX	4.8
t_{PHL}				4.8
t_{PZH}	$\overline{OE}$	Q	MAX	5
t_{PZL}				5
t_{PHZ}	$\overline{OE}$	Q	MAX	4.5
t_{PLZ}				4.5

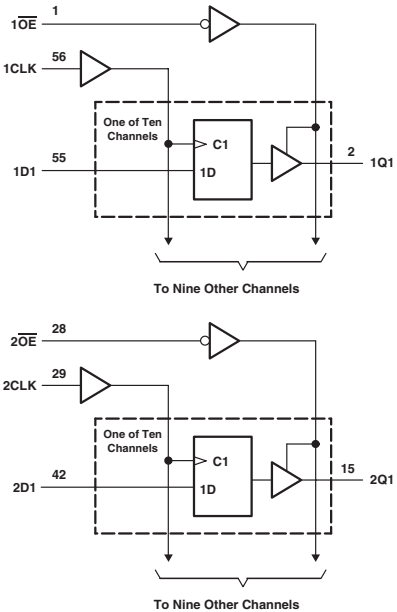
UNIT fmax : MHz other : ns

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

16821

20-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ALVTH 3V	ACT	ALVCH 3V	UNIT
I_{CC}	MAX	89	5	0.08	0.04	mA
I_{OH}	MAX	-32	-32	-24	-24	mA
I_{OL}	MAX	64	64	24	24	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

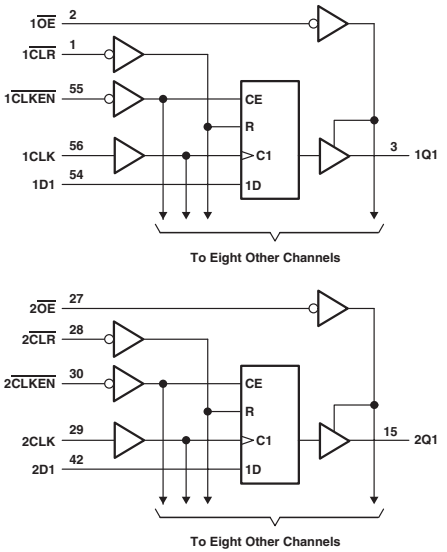
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ALVTH 3V	ACT	ALVCH 3V
f_{max}			MIN	150	150	70	150
t_w Pulse duration	CLK high or low		MIN	3.3	1.5	7	3.3
t_{su} Setup time	Data before CLK ↑, low		MIN	1.8	1.5	7.5	3.4
	Data before CLK ↑, high		MIN	1.8	1.5	7.5	3.4
t_h Hold time	Data after CLK ↑, high		MIN	1.3	1	0.5	0
	Data after CLK ↑, low		MIN	1.3	1	0.5	0
t_{PLH}	CLK	Q	MAX	6.1	3.5	13.4	4.5
t_{PHL}				5.4	3.5	14	4.5
t_{PZH}	$\overline{OE}$	Q	MAX	5.7	4.1	11.9	5.1
t_{PZL}				5.6	3.6	14.7	5.1
t_{PHZ}	$\overline{OE}$	Q	MAX	6.5	4.8	10.7	4.6
t_{PLZ}				7.1	4.8	10	4.6

UNIT fmax : MHz other : ns

16823

18-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH DUAL OUTPUTS

Logic Diagram



FUNCTION TABLE
(each 9-bit filp-flop)

INPUTS					OUTPUT
$\overline{OE}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	L	L	X	Q_0
L	H	H	X	X	Q_0
H	X	X	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ABTH	AC	ACT	ALVCH 3V	UNIT
I_{CC}	MAX	80	80	0.08	0.08	0.04	mA
I_{OH}	MAX	-32	-32	-24	-24	-24	mA
I_{OL}	MAX	64	64	24	24	24	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ABTH	AC	ACT	ALVCH 3V
f_{max}			MIN	150	150	115	90	150
t_w Pulse duration	$\overline{CLR}$ low		MIN	3.3	3.3	3.3	3.3	3.3
	CLK high or low		MIN	3.3	3.3	4.4	5.5	3.3
t_{su} Setup time	$\overline{CLR}$ inactive		MIN	1.6	1.6	0.6	0.5	0.8
	Data high before CLK ↑		MIN	1.7	1.7	5	7	1
	Data low before CLK ↑		MIN	1.7	1.7	5	7	1.3
	$\overline{CLKEN}$ low before CLK ↑		MIN	2.8	2.8	4.2	3.5	1.5
t_h Hold time	Data high after CLK ↑		MIN	1.2	1.2	1.3	0.5	0.8
	Data low after CLK ↑		MIN	1.2	1.2	1.3	0.5	0.5
	$\overline{CLKEN}$ low after CLK ↑		MIN	0.6	0.6	1.4	2.5	0.4
t_{PLH}	CLK	Q	MAX	6.8	6.8	12	12.1	4.5
t_{PHL}				6	6	12.7	12.9	4.5
t_{PLH}	$\overline{CLR}$	Q	MAX	-	-	-	-	4.6
t_{PHL}				6.1	6.7	11	12.5	4.6
t_{PZH}	$\overline{OE}$	Q	MAX	4.9	4.9	9.7	10.7	4.8
t_{PZL}				5.5	5.5	11.8	12.8	4.8
t_{PHZ}	$\overline{OE}$	Q	MAX	6.1	6.1	9.3	10.3	4.5
t_{PLZ}				8.7	8.7	8.6	9.4	4.5

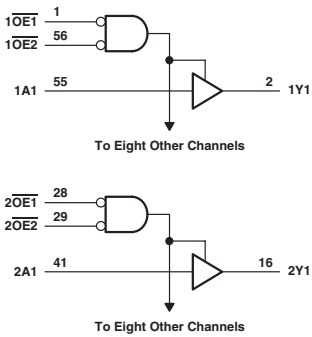
UNIT fmax : MHz other : ns

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

16825

18-BIT BUS BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
(each 9-bit section)

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

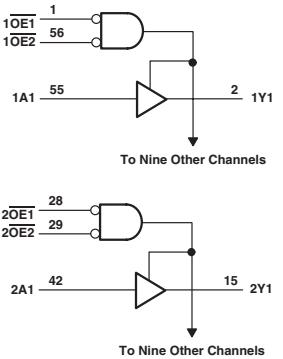
PARAMETER	MAX or MIN	ABT	ACT	ALVCH 3V	UNIT
I_{CC}	MAX	32	0.08	0.04	mA
I_{OH}	MAX	-32	-24	-24	mA
I_{OL}	MAX	64	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ACT	ALVCH 3V
t_{PLH}	A	Y	MAX	3.9	10.5	3.4
t_{PHL}				4.4	10.3	3.4
t_{PZH}	$\overline{OE}$	Y	MAX	6.1	11	4.7
t_{PZL}				6	13.2	4.7
t_{PHZ}	$\overline{OE}$	Y	MAX	6.9	11.5	4.5
t_{PLZ}				6.6	10.6	4.5

UNIT: ns

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE
(each 10-bit section)

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ALVTH 3V	ACT	ALVCH 3V	AVC 3V	UNIT
I_{CC}	MAX	32	6	0.08	0.04	0.04	mA
I_{OH}	MAX	-32	-32	-24	-24	-12	mA
I_{OL}	MAX	64	64	24	24	12	mA

SWITCHING CHARACTERISTICS

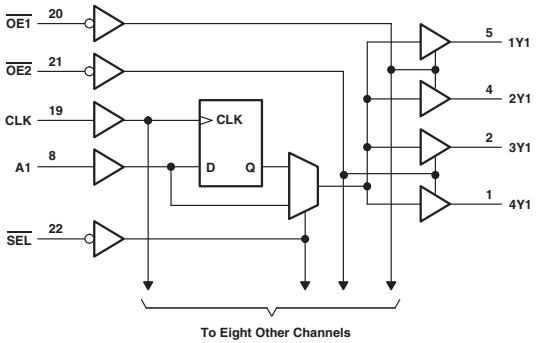
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ALVTH 3V	ACT	ALVCH 3V	AVC 3V
t_{PLH}	A	Y	MAX	3.4	3	11	3.4	1.7
t_{PHL}				4.2	2.8	10.8	3.4	1.7
t_{PZH}	$\overline{OE}$	Y	MAX	5.6	3.9	11.7	4.7	5.1
t_{PZL}				5.5	3.4	14	4.7	5.1
t_{PHZ}	$\overline{OE}$	Y	MAX	6.6	5.8	12.4	4.5	4.7
t_{PLZ}				6.1	4.6	11.5	4.5	4.7

UNIT: ns

16831

1-TO-4 ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	$\overline{SEL}$	CLK	A	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I_{CC}	MAX	0.04	mA
I_{OH}	MAX	-24	mA
I_{OL}	MAX	24	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
f_{max}			MIN	150
t_w Pulse duration	CLK high or low		MIN	3.3
t_{su} Setup time	A data before CLK ↑		MIN	1.6
t_h Hold time	A data after CLK ↑		MIN	1.1
t_{PLH}	A	Y	MAX	3.6
t_{PHL}				3.6
t_{PLH}	CLK	Y	MAX	3.9
t_{PHL}				3.9
t_{PLH}	$\overline{SEL}$	Y	MAX	4.4
t_{PHL}				4.4
t_{PZH}	$\overline{OE}$	Y	MAX	4.3
t_{PZL}				4.3
t_{PHZ}	$\overline{OE}$	Y	MAX	4.5
t_{PLZ}				4.5

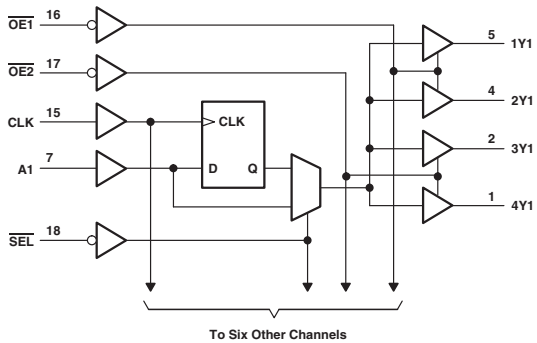
UNIT fmax : MHz other : ns

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

16832

1-TO-4 ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	$\overline{SEL}$	CLK	A	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

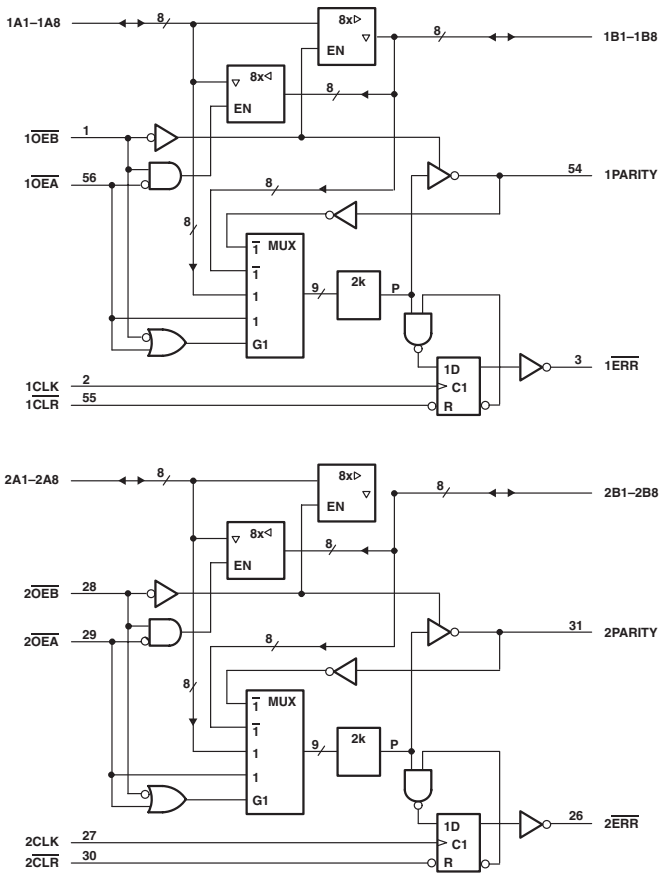
PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I_{CC}	MAX	0.04	mA
I_{OH}	MAX	-24	mA
I_{OL}	MAX	24	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
f_{max}			MIN	150
t_w Pulse duration	CLK high or low		MIN	3.3
t_{su} Setup time	A data before CLK ↑		MIN	1.6
t_h Hold time	A data after CLK ↑		MIN	1.1
t_{PLH}	A	Y	MAX	3.6
t_{PHL}				3.6
t_{PLH}	CLK	Y	MAX	3.9
t_{PHL}				3.9
t_{PLH}	$\overline{SEL}$	Y	MAX	4.4
t_{PHL}				4.4
t_{PZH}	$\overline{OE}$	Y	MAX	4.3
t_{PZL}				4.3
t_{PHZ}	$\overline{OE}$	Y	MAX	4.5
t_{PLZ}				4.5

UNIT fmax : MHz other : ns

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS						OUTPUT AND I/O				FUNCTION
$\overline{OEB}$	$\overline{OEA}$	$\overline{CLR}$	CLK	Ai Σ OF H	Bi† Σ OF H	A	B	PARITY	$\overline{ERR}$‡	
L	H	X	X	Odd Even	NA	NA	A	L H	NA	A data to B bus and generate parity
H	L	H	↑	NA	Odd Even	B	NA	NA	H L	B data to A bus and check parity
X	X	L	X	X	X	X	NA	NA	H	Check error flag register
H	H	H L H H	No↑ No↑ ↑ ↑	X X Odd Even	X	Z	Z	Z	NC H H L	Isolation§
L	L	X	X	Odd Even	NA	NA	A	H L	NA	A data to B bus and generate inverted parity

NA = not applicable, NC = no change, X = don't care
† Summation of high-level inputs includes PARITY along with Bi inputs.
‡ Output states shown assume $\overline{ERR}$ was previousiy high.
§ In this mode, $\overline{ERR}$ (when clocked) shows inverted panrity of the A bus.

ERROR-FLAG FUNCTION TABLE

INPUTS		INTERNAL TO DEVICE	OUTPUT PRE-STATE	OUTPUT	FUNCTION
$\overline{CLR}$	CLK	POINT P	$\overline{ERR}_{n-1}$†	$\overline{ERR}$	
H	↑	H	H	H	Sample
H	↑	X	L	L	
H	↑	L	X	L	
L	X	X	X	H	Clear

† State of $\overline{ERR}$ before any changes at $\overline{CLR}$, CLK, or point P

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ACT	UNIT
I_{CC}	MAX	36	0.08	mA
I_{OH}	MAX	-32	-24	mA
I_{OL}	MAX	64	24	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

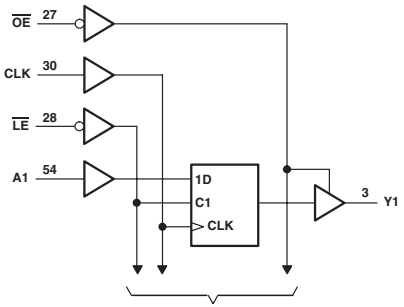
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ACT
t_w Pulse duration	CLK high or low		MIN	3	4
	$\overline{CLR}$ low			-	4
t_{su} Setup time	A data before CLK ↑, A port		MIN	4..5	-
	A data before CLK ↑, $\overline{CLR}$			1	1.5
	A data before CLK ↑, $\overline{OEA}$			5	-
t_h Hold time	A data after CLK ↑, A port or $\overline{OEA}$		MIN	0	0
t_{PLH}	A or B	B or A	MAX	4.1	10.4
t_{PHL}				4.3	10.7
t_{PLH}	A	PARITY	MAX	6.7	13.5
t_{PHL}				6.1	13.8
t_{PZH}	$\overline{OEB}$ or $\overline{OEA}$	A or B	MAX	5.6	11.2
t_{PZL}				6	13
t_{PHZ}	$\overline{OEB}$ or $\overline{OEA}$	A or B	MAX	5.4	10.8
t_{PLZ}				4.3	10.1
t_{PLH}	CLK, $\overline{CLR}$	$\overline{ERR}$	MAX	4.6	15.8
t_{PHL}	CLK			3.9	11.6
t_{PLH}	$\overline{OEB}$	PARITY	MAX	6.7	-
t_{PHL}				6.1	-
t_{PLH}	$\overline{OEA}$	PARITY	MAX	6.7	13.2
t_{PHL}				6.1	13.6
t_{PZH}	$\overline{OEB}$	PARITY	MAX	5.7	9.5
t_{PZL}				6.5	10.7
t_{PHZ}	$\overline{OEB}$	PARITY	MAX	4.7	10.2
t_{PLZ}				4.1	9.7
t_{PZH}	$\overline{OEA}$	PARITY	MAX	5.7	-
t_{PZL}				6.5	-
t_{PHZ}	$\overline{OEA}$	PARITY	MAX	4.7	-
t_{PLZ}				4.1	-

UNIT: ns

16834

16-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	$\overline{LE}$	CLK	A	Y
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	↑	L	L
L	H	↑	H	H
L	H	H	X	Y_Q†
L	H	L	X	Y_Q‡

† Output level before the indicated steady-state input conditions were established, provided that CLK is high before $\overline{LE}$ goes high
‡ Output level before the indicated steady-state input conditions were established

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVC 3V	AVC 3V	UNIT
I_{CC}	MAX	0.04	0.04	mA
I_{OH}	MAX	-24	-12	mA
I_{OL}	MAX	24	12	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVC 3V	AVC 3V
f_{max}			MIN	150	150
t_w Pulse duration	$\overline{LE}$ low		MIN	3.3	3.3
	CLK high or low		MIN	3.3	3.3
t_{su} Setup time	Data before CLK ↑		MIN	1.7	0.7
	Data before $\overline{LE}$ ↑, CLK high		MIN	1.9	1
	Data before $\overline{LE}$ ↑, CLK low			1.5	1
t_h Hold time	A data after CLK ↑		MIN	0.7	0.9
	Data after $\overline{LE}$ ↑, CLK high		MIN	0.9	1.4
	Data after $\overline{LE}$ ↑, CLK low			0.9	1.3
t_{PLH}	A	Y	MAX	3.6	2.5
t_{PHL}				3.6	2.5
t_{PLH}	$\overline{LE}$	Y	MAX	4.9	4
t_{PHL}				4.9	4
t_{PLH}	CLK	Y	MAX	4.6	3.1
t_{PHL}				4.6	3.1
t_{PZH}	$\overline{OE}$	Y	MAX	5	6.2
t_{PZL}				5	6.2
t_{PHZ}	$\overline{OE}$	Y	MAX	4.5	5.3
t_{PLZ}				4.5	5.3

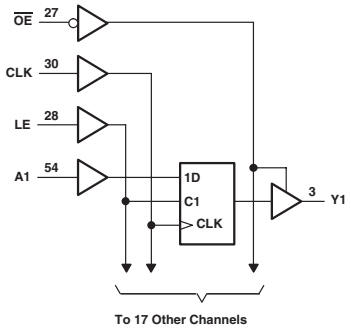
UNIT fmax : MHz other : ns

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

16835

3.3-V ABT 18-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	LE	CLK	A	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	H	X	Y_0†
L	L	L	X	Y_0‡

† Output level before the indicated steady-state input conditions were established, provided that CLK was high before LE went low.
‡ Output level before the indicated steady-state input conditions were established

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVTH 3V	ALVC 3V	ALVCH 3V	AVC 3V	UNIT
I_{CC}	MAX	5	0.04	0.04	0.04	mA
I_{OH}	MAX	-32	-24	-24	-12	mA
I_{OL}	MAX	64	24	24	12	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

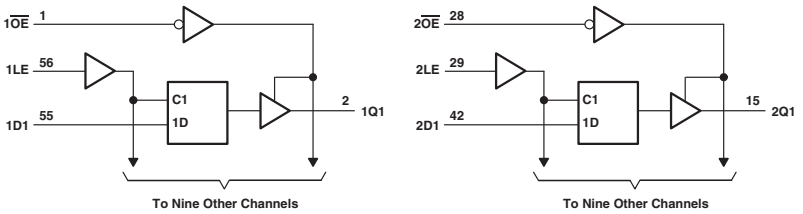
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTH 3V	ALVC 3V	ALVCH 3V	AVC 3V
f_{max}			MIN	150	150	150	150
t_w Pulse duration	LE low		MIN	3.3	3.3	3.3	3.3
	CLK high or low		MIN	3.3	3.3	3.3	3.3
t_{su} Setup time	Data before CLK ↑		MIN	2.1	1.7	1.7	0.7
	Data before LE ↓, CLK high		MIN	2.3	1.5	1.5	0.8
	Data before LE ↓, CLK low		MIN	1.5	1	1	0.5
t_h Hold time	A data after CLK ↑		MIN	1	0.7	0.7	1.3
	Data after LE ↓, CLK high		MIN	0.8	1.4	1.4	1.6
	Data after LE ↓, CLK low		MIN	0.8	1.4	1.4	1.4
t_{PLH}	A	Y	MAX	3.7	3.6	3.6	2.5
t_{PHL}				3.7	3.6	3.6	2.5
t_{PLH}	LE	Y	MAX	5.1	4.2	4.2	3.8
t_{PHL}				5.1	4.2	4.2	3.8
t_{PLH}	CLK	Y	MAX	5.1	4.5	4.5	3.1
t_{PHL}				5.1	4.5	4.5	3.1
t_{PZH}	$\overline{OE}$	Y	MAX	4.6	4.6	4.6	6.2
t_{PZL}				4.6	4.6	4.6	6.2
t_{PHZ}	$\overline{OE}$	Y	MAX	5.8	3.9	3.9	5.3
t_{PLZ}				5.8	3.9	3.9	5.3

UNIT fmax : MHz other : ns

16841

20-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
(each 10-bit latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ACT	ALVCH 3V	UNIT
I_{CC}	MAX	89	0.08	0.04	mA
I_{OH}	MAX	-32	-24	-24	mA
I_{OL}	MAX	64	24	24	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ACT	ALVCH 3V
t_w Pulse duration	LE high		MIN	4	4	3.3
	LE low			4	-	3.3
t_{su} Setup time	Data before LE ↓		MIN	1	1.5	-
	Data before LE ↑			-	-	1.1
t_h Hold time	Data after LE ↓ high		MIN	2	3	-
	Data after LE ↓ low			2	4.5	-
	Data after LE ↑		MIN	-	-	1.1
t_{PLH}	D	Q	MAX	5	11.8	3.9
t_{PHL}				5.1	12.2	3.9
t_{PLH}	LE	Q	MAX	5	12.7	4.3
t_{PHL}				5	12.7	4.3
t_{PZH}	$\overline{OE}$	Q	MAX	5.7	11.3	4.9
t_{PZL}				5.6	13.7	4.9
t_{PHZ}	$\overline{OE}$	Q	MAX	6.5	10.2	4.1
t_{PLZ}				7.1	9.6	4.1

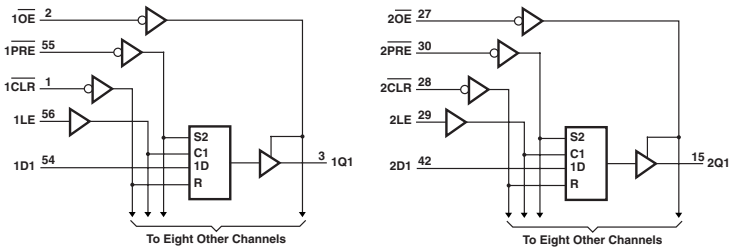
UNIT : ns

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

16843

18-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
(each 9-bit latch)

INPUTS					OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OE}$	LE	D	Q
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	L
H	H	L	H	H	H
H	H	L	L	X	Q_0
X	X	H	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIOI

PARAMETER	MAX or MIN	ABT	UNIT
I_{CC}	MAX	85	mA
I_{OH}	MAX	-32	mA
I_{OL}	MAX	64	mA

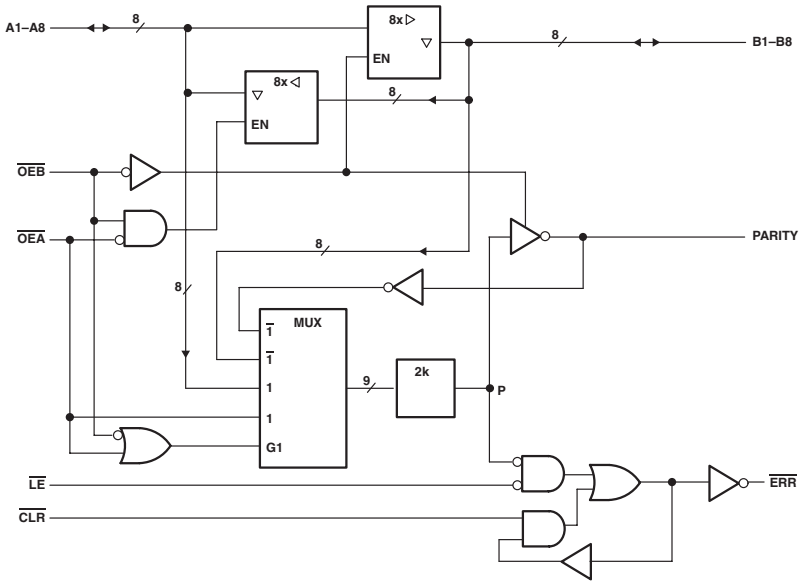
TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT
t_w Pulse duration	$\overline{CLR}$ low		MIN	3.3
	$\overline{PRE}$ low			3.3
	LE high			3.3
t_{su} Setup time	Data before LE↓, high		MIN	0.9
	Data before LE↓, low			0.6
t_h Hold time	Data after LE↓, high		MIN	1.7
	Data after LE↓, low			1.8
t_{PLH}	D	Q	MAX	4.8
t_{PHL}				4.8
t_{PLH}	LE	Q	MAX	5.9
t_{PHL}				5.3
t_{PLH}	$\overline{PRE}$	Q	MAX	6.1
t_{PHL}				5
t_{PLH}	$\overline{CLR}$	Q	MAX	5.4
t_{PHL}				6
t_{PZH}	OE	Q	MAX	5.4
t_{PZL}				5.8
t_{PHZ}	OE	Q	MAX	6.3
t_{PLZ}				5.2

UNIT: ns

DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

Logic Diagram



FUNCTION TABLE

INPUTS						OUTPUT AND I/Os				FUNCTION
$\overline{OEB}$	$\overline{OEA}$	$\overline{CLR}$	$\overline{LE}$	Ai Σ OF H	Bi† Σ OF H	A	B	PARITY	$\overline{ERR}$‡	
L	H	X	X	Odd Even	NA	NA	A	L H	NA	A data to B bus and generate parity
H	L	H	L	NA	Odd Even	B	NA	NA	H L	B data to A bus and check parity
H	L	H	H	NA	X	X	NA	NA	NC	Store error flag
X	X	L	H	X	X	X	NA	NA	H	Clear error flag register
H	H	H L X X	H H L L	X X L Odd H Even	X	Z	Z	Z	NC H H L	Isolation§ (parity check)
L	L	X	X	Odd Even	NA	NA	A	H L	NA	A data to B bus and generate inverted parity

NA = not applicable, NC = no change, X = don't care
† Summation of high-level inputs includes PARITY along with Bi inputs.
‡ Output states shown assume $\overline{ERR}$ was previously high.
§ In this mode, $\overline{ERR}$ (when clocked) shows inverted parity of the A bus.

ERROR-FLAG FUNCTION TABLE

INPUTS		INTERNAL TO DEVICE	OUTPUT	OUTPUT	FUNCTION
$\overline{CLR}$	$\overline{LE}$	POINT P	$\overline{ERR}_{n-1}$†	$\overline{ERR}$	
L	L	L H	X	L H	Pass
H	L	L X H	X L H	L L H	Sample
L	H	X	X	H	Clear
H	H	X	L H	L H	Store

† State of $\overline{ERR}$ before changes at $\overline{CLR}$, $\overline{LE}$, or point P

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	UNIT
I_{CC}	MAX	40	mA
I_{OH}	MAX	-32	mA
I_{OL}	MAX	64	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

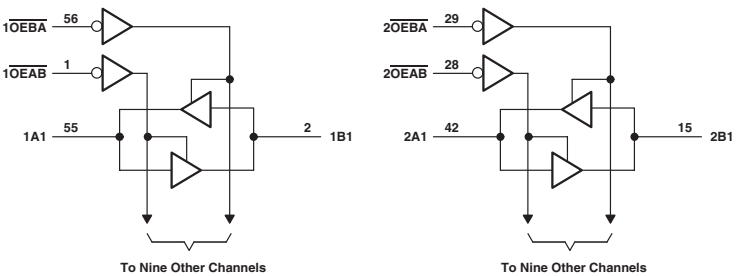
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT
t_w Pulse duration	$\overline{LE}$ high or low		MIN	8.5
	$\overline{CLR}$ low			4
t_{su} Setup time	A, B and PARITY before $\overline{LE}\downarrow$		MIN	10
	$\overline{CLR}$ before $\overline{LE}\downarrow$			0
t_h Hold time	A, B and PARITY after $\overline{LE}\downarrow$		MIN	0
	$\overline{CLR}$ after $\overline{LE}\downarrow$			0
t_{PLH}	A or B	B or A	MAX	4.1
t_{PHL}				4.3
t_{PLH}	A or $\overline{OE}$	PARITY	MAX	7.1
t_{PHL}				7.2
t_{PLH}	$\overline{CLR}$	$\overline{ERR}$	MAX	5.7
t_{PZH}	$\overline{OE}$	A or B	MAX	5.6
t_{PZL}				6
t_{PHZ}	$\overline{OE}$	A or B	MAX	5.4
t_{PLZ}				4.3
t_{PZH}	$\overline{OE}$	PARITY	MAX	5.7
t_{PZL}				6.5
t_{PHZ}	$\overline{OE}$	PARITY	MAX	4.7
t_{PLZ}				4.1
t_{PLH}	$\overline{LE}$	$\overline{ERR}$	MAX	4.8
t_{PHL}				4.9
t_{PLH}	A, B or PARITY	$\overline{ERR}$	MAX	7.2
t_{PHL}				7.4

UNIT: ns

16861

20-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
(each 10-bit section)

INPUTS		OPERATION
$\overline{OEAB}$	$\overline{OEBA}$	
L	L	Latch A and B (A = B)
L	H	A to B
H	L	B to A
H	H	Isolation

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ACT	UNIT
I_{CC}	MAX	0.08	mA
I_{OH}	MAX	-24	mA
I_{OL}	MAX	24	mA

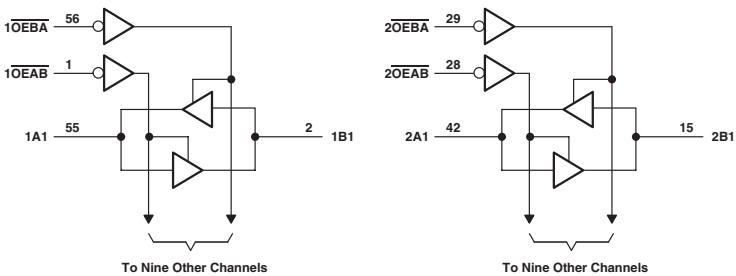
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ACT
t_{PLH}	A or B	B or A	MAX	10.4
t_{PHL}				11.1
t_{PZH}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	MAX	10
t_{PZL}				12.7
t_{PHZ}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	MAX	10.7
t_{PLZ}				10

UNIT: ns

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

Logic Diagram



FUNCTION TABLE
(each 9-bit section)

INPUTS		OPERATION
$\overline{OEAB}$	$\overline{OEBA}$	
H	L	B data to A bus
L	H	A data to B bus
H	H	Isolation

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ACT	ALVCH 3V	UNIT
I_{CC}	MAX	32	0.08	0.04	mA
I_{OH}	MAX	-32	-24	-24	mA
I_{OL}	MAX	64	24	24	mA

SWITCHING CHARACTERISTICS

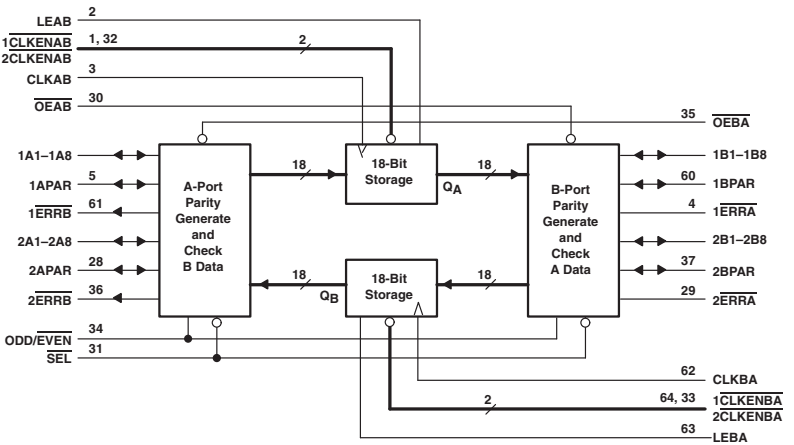
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ACT	ALVCH 3V
t_{PLH}	A or B	B or A	MAX	3.5	11.1	3.4
t_{PHL}				3.9	11.8	3.4
t_{PZH}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	MAX	5.4	10.6	4.7
t_{PZL}				4.8	13.6	4.7
t_{PHZ}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	MAX	6	11.6	4.2
t_{PLZ}				5	11	4.2

UNIT: ns

16901

18-BIT UNIVERSAL BUS TRANSCEIVER WITH PARITY GENERATORS/CHECKERS

Block Diagram



FUNCTION TABLE

INPUTS					OUTPUT
CLKENAB	OEAB	LEAB	CLKAB	A	B
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B_0‡
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L	X	B_0‡
L	L	L	H	X	B_0§

‡ Output level before the indicated steady-state input conditions were established

§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low

PARITY-ENABLE FUNCTION TABLE

INPUTS			OPERATION OR FUNCTION	
SEL	OEBA	OEAB		
L	H	L	Parity is checked on port A and is generated on port B.	
L	L	H	Parity is checked on port B and is generated on port A.	
L	H	H	Parity is checked on port B and port A.	
L	L	L	Parity is generated on port A and B if device is in FF mode.	
H	L	L	Parity funcions are disabled; device acts as a standard 18-bit registered transceiver.	Q_A data to B, Q_B data to A
H	L	H		Q_B data to A
H	H	L		Q_A data to B
H	H	H		Isolation

PARITY FUNCTION TABLE

INPUTS								OUTPUTS			
SEL	OEBA	OEAB	ODD/EVEN	Σ OF INPUTS A1-A8 = H	Σ OF INPUTS B1-B8 = H	APAR	BPAR	APAR	ERRA	BPAR	ERRB
L	H	L	L	0, 2, 4, 6, 8	N/A	L	N/A	N/A	H	L	Z
L	H	L	L	1, 3, 5, 7	N/A	L	N/A	N/A	L	H	Z
L	H	L	L	0, 2, 4, 6, 8	N/A	H	N/A	N/A	L	L	Z
L	H	L	L	1, 3, 5, 7	N/A	H	N/A	N/A	H	H	Z
L	L	H	L	N/A	0, 2, 4, 6, 8	N/A	L	L	Z	N/A	H
L	L	H	L	N/A	1, 3, 5, 7	N/A	L	H	Z	N/A	L
L	L	H	L	N/A	0, 2, 4, 6, 8	N/A	H	L	Z	N/A	L
L	L	H	L	N/A	1, 3, 5, 7	N/A	H	H	Z	N/A	H
L	H	L	H	0, 2, 4, 6, 8	N/A	L	N/A	N/A	L	H	Z
L	H	L	H	1, 3, 5, 7	N/A	L	N/A	N/A	H	L	Z
L	H	L	H	0, 2, 4, 6, 8	N/A	H	N/A	N/A	H	H	Z
L	H	L	H	1, 3, 5, 7	N/A	H	N/A	N/A	L	L	Z
L	L	H	H	N/A	0, 2, 4, 6, 8	N/A	L	H	Z	N/A	L
L	L	H	H	N/A	1, 3, 5, 7	N/A	L	L	Z	N/A	H
L	L	H	H	N/A	0, 2, 4, 6, 8	N/A	H	H	Z	N/A	H
L	L	H	H	N/A	1, 3, 5, 7	N/A	H	L	Z	N/A	L
L	H	H	L	0, 2, 4, 6, 8	0, 2, 4, 6, 8	L	L	Z	H	Z	H
L	H	H	L	1, 3, 5, 7	1, 3, 5, 7	L	L	Z	L	Z	L
L	H	H	L	0, 2, 4, 6, 8	0, 2, 4, 6, 8	H	H	Z	L	Z	L
L	H	H	L	1, 3, 5, 7	1, 3, 5, 7	H	H	Z	H	Z	H
L	H	H	H	0, 2, 4, 6, 8	0, 2, 4, 6, 8	L	L	Z	L	Z	L
L	H	H	H	1, 3, 5, 7	1, 3, 5, 7	L	L	Z	H	Z	H
L	H	H	H	0, 2, 4, 6, 8	0, 2, 4, 6, 8	H	H	Z	H	Z	H
L	H	H	H	1, 3, 5, 7	1, 3, 5, 7	H	H	Z	L	Z	L
L	L	L	L	N/A	N/A	N/A	N/A	PE†	Z	PE†	Z
L	L	L	H	N/A	N/A	N/A	N/A	PO‡	Z	PO‡	Z

† Parity output is set to the level so that the specific bus side is set to even parity.

‡ Parity output is set to the level so that the specific bus side is set to odd parity.

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVCH 3V	ALVCH 3V	UNIT
I_{CC}	MAX	0.02	0.04	mA
I_{OH}	MAX	-24	-24	mA
I_{OL}	MAX	24	24	mA

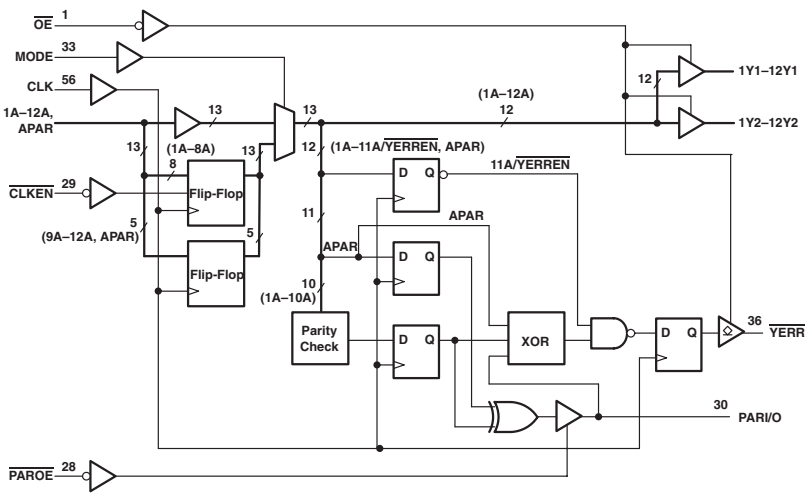
TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVCH 3V	ALVCH 3V
f_{max}			MIN	125	125
t_w Pulse duration	CLK ↑		MIN	3	3
	LE high		MIN	3	3
t_{su} Setup time	A, APAR or B, BPAR before CLK ↑		MIN	2.5	1.7
	$\overline{CLKEN}$ before CLK ↑		MIN	2.5	1.7
	A, APAR or B, BPAR before LE ↓		MIN	2	1.2
t_h Hold time	A, APAR or B, BPAR after CLK ↑		MIN	1.3	0.5
	$\overline{CLKEN}$ after CLK ↑		MIN	1.5	0.7
	A, APAR or B, BPAR after LE ↓		MIN	1.7	0.9
t_{PLH}	A or B	B or A	MAX	5.4	4.4
t_{PHL}				5.4	4.4
t_{PLH}	A or B	BPAR or APAR	MAX	7.7	6.7
t_{PHL}				7.7	6.7
t_{PLH}	APAR or BPAR	BPAR or APAR	MAX	5.7	4.7
t_{PHL}				5.7	4.7
t_{PLH}	APAR or BPAR	$\overline{ERRA}$ or $\overline{ERRB}$	MAX	8.5	7.5
t_{PHL}				8.5	7.5
t_{PLH}	ODD / $\overline{EVEN}$	$\overline{ERRA}$ or $\overline{ERRB}$	MAX	7.8	6.8
t_{PHL}				7.8	6.8
t_{PLH}	ODD / $\overline{EVEN}$	BPAR or APAR	MAX	7.5	6.5
t_{PHL}				7.5	6.5
t_{PLH}	$\overline{SEL}$	BPAR or APAR	MAX	6.1	5.1
t_{PHL}				6.1	5.1
t_{PLH}	CLKAB or CLKBA	A or B	MAX	6.1	5.1
t_{PHL}				6.1	5.1
t_{PLH}	CLKAB or CLKBA	BPAR or APAR parity feedthrough	MAX	6.6	5.6
t_{PHL}				6.6	5.6
t_{PLH}	CLKAB or CLKBA	BPAR or APAR parity generated	MAX	8.7	7.7
t_{PHL}				8.7	7.7
t_{PLH}	CLKAB or CLKBA	$\overline{ERRA}$ or $\overline{ERRB}$	MAX	8.9	7.9
t_{PHL}				8.9	7.9
t_{PLH}	LEAB or LEBA	A or B	MAX	5.8	4.8
t_{PHL}				5.8	4.8
t_{PLH}	LEAB or LEBA	BPAR or APAR parity feedthrough	MAX	6.3	5.3
t_{PHL}				6.3	5.3
t_{PLH}	LEAB or LEBA	BPAR or APAR parity generated	MAX	8.4	7.4
t_{PHL}				8.4	7.4
t_{PLH}	LEAB or LEBA	$\overline{ERRA}$ or $\overline{ERRB}$	MAX	8.5	7.5
t_{PHL}				8.5	7.5
t_{PZH}	$\overline{OEAB}$ or $\overline{OEBA}$	B, BPAR or A, APAR	MAX	6.3	5.3
t_{PZL}				6.3	5.3
t_{PHZ}	$\overline{OEAB}$ or $\overline{OEBA}$	B, BPAR or A, APAR	MAX	5.9	4.9
t_{PLZ}				5.9	4.9
t_{PZH}	$\overline{OEAB}$ or $\overline{OEBA}$	$\overline{ERRA}$ or $\overline{ERRB}$	MAX	5.9	4.9
t_{PZL}				5.9	4.9
t_{PHZ}	$\overline{OEAB}$ or $\overline{OEBA}$	$\overline{ERRA}$ or $\overline{ERRB}$	MAX	6.7	5.7
t_{PLZ}				6.7	5.7
t_{PZH}	$\overline{SEL}$	$\overline{ERRA}$ or $\overline{ERRB}$	MAX	6.5	5.5
t_{PZL}				6.5	5.5
t_{PHZ}	$\overline{SEL}$	$\overline{ERRA}$ or $\overline{ERRB}$	MAX	5.9	4.9
t_{PLZ}				5.9	4.9

UNIT fmax : MHz other : ns

3.3-V 12-BIT UNIVERSAL BUS DRIVER WITH PARITY CHECKER AND DUAL 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE

INPUTS					OUTPUTS	
$\overline{OE}$	MODE	CLKEN	CLK	A	$1Y_n$† – $8Y_n$†	$9Y_n$† – $12Y_n$†
L	L	L	↑	H	H	H
L	L	L	↑	L	L	L
L	L	H	↑	H	Y_0	H
L	L	H	↑	L	Y_0	L
L	H	X	X	H	H	H
L	H	X	X	L	L	L
H	X	X	X	X	Z	Z

† $n = 1, 2$

PARI/O FUNCTION†

INPUTS			OUTPUT
PAROE	Σ OF INPUTS 1A – 10A = H	APAR	PARI/O
L	0, 2, 4, 6, 8, 10	L	L
L	1, 3, 5, 7, 9	L	H
L	0, 2, 4, 6, 8, 10	H	H
L	1, 3, 5, 7, 9	H	L
H	X	X	Z

† This table applies to the first device of a cascaded pair of ALVCH16903 devices.

PARITY FUNCTION

INPUTS						OUTPUT
$\overline{OE}$	PAROE‡	11A/YERREN§	PARI/O	Σ OF INPUTS 1A – 10A = H	APAR	YERR
L	H	L	L	0, 2, 4, 6, 8, 10	L	H
L	H	L	L	1, 3, 5, 7, 9	L	L
L	H	L	L	0, 2, 4, 6, 8, 10	H	L
L	H	L	L	1, 3, 5, 7, 9	H	H
L	H	L	H	0, 2, 4, 6, 8, 10	L	L
L	H	L	H	1, 3, 5, 7, 9	L	H
L	H	L	H	0, 2, 4, 6, 8, 10	H	H
L	H	L	H	1, 3, 5, 7, 9	H	L
H	X	X	X	X	X	H
L	X	H	X	X	X	H

‡ When used as a single device, $\overline{PAROE}$ must be tied high.
§ Valid after appropriate number of clock pulses have set internal register.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

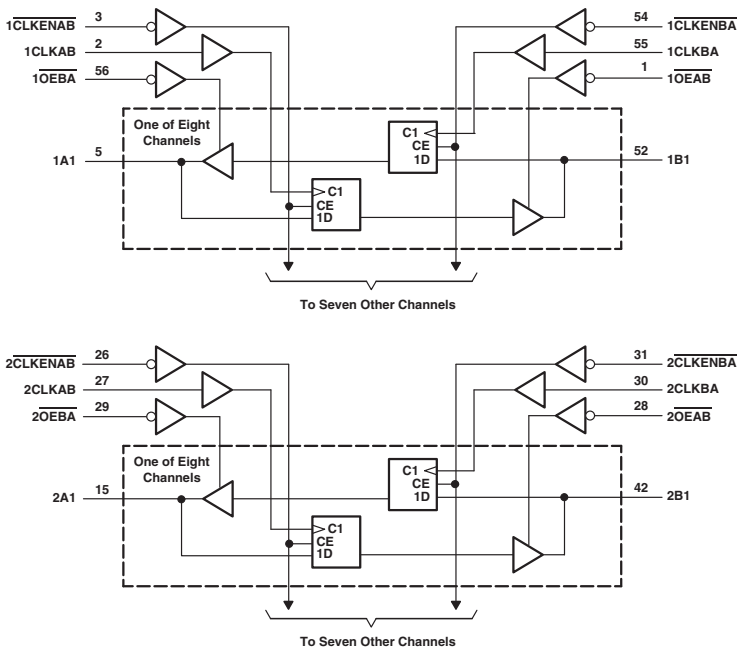
PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I_{CC}	MAX	0.04	mA
I_{OH}	MAX	-24	mA
I_{OL}	MAX	24	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	ALVCH 3V
f_{max}				MIN	125
t_w Pulse duration		CLK ↑		MIN	3
t_{su} Setup time		1A-12A before CLK ↑ , resister mode		MIN	1.45
		1A-10A before CLK ↑ , buffer mode		MIN	4.4
		APAR before CLK ↑ , resister mode		MIN	1.3
		APAR before CLK ↑ , buffer mode		MIN	3.1
		PARI/O before CLK ↑ , both mode		MIN	1.7
		11A/$\overline{YERREN}$ before CLK ↑ , buffer mode		MIN	1.6
		$\overline{CLKEN}$ before CLK ↑ , resister mode		MIN	2.2
t_h Hold time		1A-12A after CLK ↑ , resister mode		MIN	0.55
		1A-10A after CLK ↑ , buffer mode		MIN	0.25
		APAR after CLK ↑ , resister mode		MIN	0.7
		APAR after CLK ↑ , buffer mode		MIN	0.25
		PARI/O before CLK ↑ , resister mode		MIN	0.4
		PARI/O before CLK ↑ , buffer mode		MIN	0.5
		11A/$\overline{YERREN}$ after CLK ↑ , buffer mode		MIN	0.4
		$\overline{CLKEN}$ after CLK ↑ , resister mode		MIN	0.4
t_{PLH}	Buffer mode	A	Y	MAX	3.8
t_{PHL}					3.8
t_{PLH}	Both mode	CLK	$\overline{YERR}$	MAX	4.4
t_{PHL}					4.4
t_{PLH}	Both mode	CLK	PARI / O	MAX	6.6
t_{PHL}					6.6
t_{PLH}	Both mode	MODE	Y	MAX	4.9
t_{PHL}					4.9
t_{PLH}	Resister mode	CLK	Y	MAX	4.8
t_{PHL}					4.6
t_{PZH}	Both mode	$\overline{OE}$	Y	MAX	5.4
t_{PZL}					5.4
t_{PZH}	Both mode	$\overline{PAROE}$	PARI / O	MAX	4.8
t_{PZL}					4.8
t_{PHZ}	Both mode	$\overline{OE}$	Y	MAX	5
t_{PLZ}					5
t_{PHZ}	Both mode	$\overline{PAROE}$	PARI / O	MAX	3.8
t_{PLZ}					3.8
t_{PLH}	Both mode	$\overline{OE}$	$\overline{YERR}$	MAX	4
t_{PHL}					4.2

UNIT fmax : MHz other : ns

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS				OUTPUT B
$\overline{CLKENAB}$	CLKAB	$\overline{OEAB}$	A	
H	X	L	X	B_0‡
X	L	L	X	B_0‡
L	↑	L	L	L
L	↑	L	H	H
H	X	H	X	Z

† A-to-B data flow is shown; B-to-A data flow is similar but uses $\overline{CLKENBA}$, CLKBA, and $\overline{OEBA}$.
‡ Level of B before the indicated steady-state input conditions were established.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ACT	LVT 3V	LVTH 3V	LVCH 3V	ALVCH 3V	UNIT
I_{CC}	MAX	35	0.08	5	5	0.02	0.04	mA
I_{OH}	MAX	-32	-24	-32	-32	-24	-24	mA
I_{OL}	MAX	64	24	64	64	24	24	mA

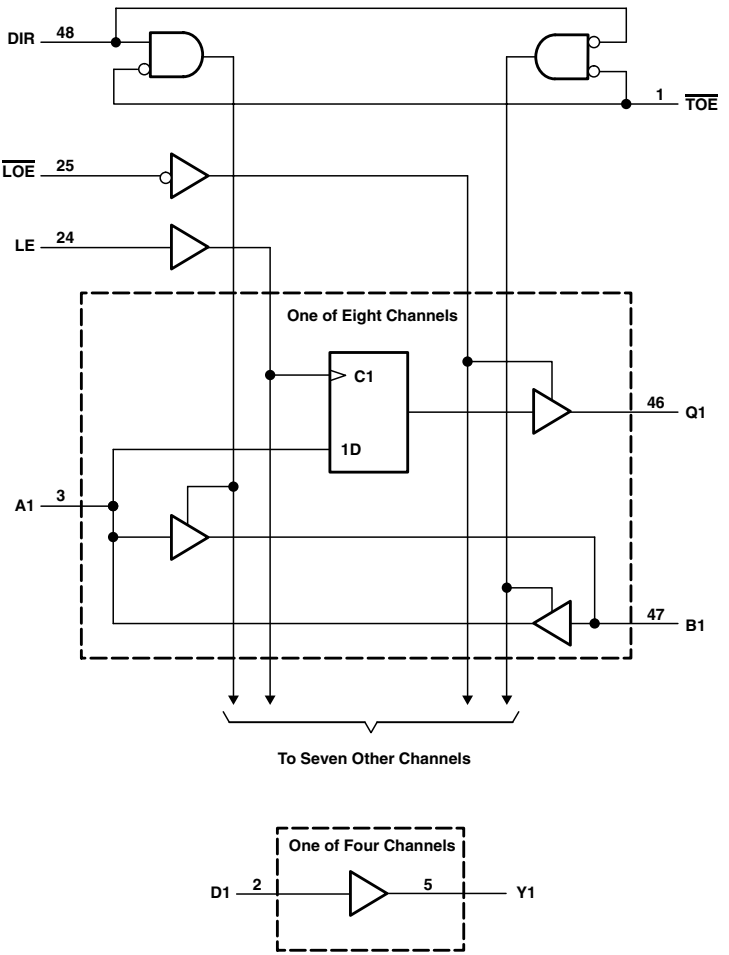
TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ACT	LVT 3V	LVTH 3V	LVCH 3V	ALVCH 3V
f_{max}			MIN	150	75	150	150	150	150
t_w Pulse duration	$\overline{CLKEN}$ high (SN74LVT: CLKEN high)		MIN	-	-	3.3	-	-	3.3
	CLK high or low			3.3	6.7	3.3	3.3	3.3	3.3
t_{su} Setup time	Data before CLK		MIN	3.5	5	2.1	1.7	2.8	1.5
	$\overline{CLKEN}$ before CLK			3	6.5	1.2	2	1.4	1
t_h Hold time	Data after CLK		MIN	1	1	0.7	0.8	0.5	0.8
	$\overline{CLKEN}$ after CLK			1	0	1.4	0.4	1.9	1.1
t_{PLH}	CLK	A or B	MAX	4.3	11.8	5.8	4.4	6.6	3.9
t_{PHL}				4.5	11.7	5.8	4.4	6.6	3.9
t_{PZH}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	MAX	4.6	11.2	5.6	4.9	6.6	4.4
t_{PZL}				6	13	6.5	4.9	6.6	4.4
t_{PHZ}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	MAX	5.5	9.4	6.3	6.2	6.7	4
t_{PLZ}				4.2	8.7	5.1	5.3	6.7	4

UNIT fmax : MHz other : ns

8-BIT BUS TRANSCEIVER AND TRANSPARENT D-TYPE LATCH WITH FOUR INDEPENDENT BUFFERS

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS		OPERATION
$\overline{TOE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	A bus and B bus Isolation

INPUTS			OUTPUT
$\overline{LOE}$	LE	A	Q
L	H	H	H
L	H	L	L
L	L	X	Q_O
H	X	X	Z

INPUT D	OUTPUT Y
L	L
H	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I_{CC}	MAX	0.03	mA
I_{OH}	MAX	-24	mA
I_{OL}	MAX	24	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
t_w Pulse duration	LE high		MIN	2
t_{su} Setup time	data before LE↓		MIN	0.9
t_h Hold time	data after LE↓		MIN	0.9
t_{PLH}	D	Y	MAX	3
t_{PHL}				3
t_{PLH}	A	Q	MAX	3
t_{PHL}				3
t_{PLH}	LE	Q	MAX	3
t_{PHL}				3
t_{PLH}	A or B	B or A	MAX	3
t_{PHL}				3
t_{PZH}	$\overline{LOE}$	Q	MAX	4.7
t_{PZL}				4.7
t_{PZH}	$\overline{TOE}$	A or B	MAX	4.4
t_{PZL}				4.4
t_{PZH}	DIR	A or B	MAX	4.7
t_{PZL}				4.7
t_{PHZ}	$\overline{LOE}$	Q	MAX	4.1
t_{PLZ}				4.1
t_{PHZ}	$\overline{TOE}$	A or B	MAX	4.1
t_{PLZ}				4.1
t_{PHZ}	DIR	A or B	MAX	4.7
t_{PLZ}				4.7

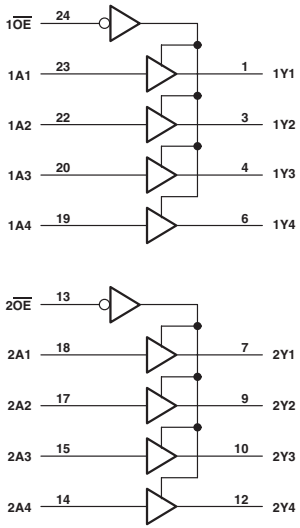
UNIT: ns

25244

25-Ω OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

- High Output Drive Current
- Distributed V_{CC} and GND Pins Minimize Noise Generated by the Simultaneous Switching of Outputs

Logic Diagram



FUNCTION TABLE
(each buffer/driver)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 BCT	SN64 BCT	UNIT
I_{CC}	MAX	119	119	mA
I_{OH}	MAX	-80	-80	mA
I_{OL}	MAX	188	188	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT	SN64 BCT
t_{PLH}	A	Y	MAX	5.5	5.5
t_{PHL}				6	6.3
t_{PZH}	$\overline{OE}$	Y	MAX	9.3	9.7
t_{PZL}				10.2	10.4
t_{PHZ}	$\overline{OE}$	Y	MAX	6.3	6.5
t_{PLZ}				8.4	9.5

UNIT: ns

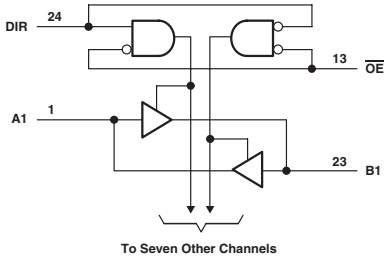
: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

25245

25-Ω OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- High Output Drive Current
- Distributed V_{CC} and GND Pins Minimize Noise Generated by the Simultaneous Switching of Outputs

Logic Diagram



FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 BCT	SN64 BCT	ABTH	UNIT
I_{CC}	MAX	125	125	20	mA
I_{OH} (A port)	MAX	-80	-80	-80	mA
I_{OH} (B port)	MAX	-3	-3	-32	mA
I_{OL} (A port)	MAX	188	188	188	mA
I_{OL} (B port)	MAX	24	24	64	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT	SN64 BCT	ABTH
t_{PLH}	A	B	MAX	5.7	5.7	3.9
t_{PHL}				7.2	7.3	4.3
t_{PLH}	B	A	MAX	5.5	5.5	3.9
t_{PHL}				6.2	6.3	4.3
t_{PZH}	$\overline{OE}$	A	MAX	9.6	9.7	6.5
t_{PZL}				10.3	10.6	6.8
t_{PHZ}	$\overline{OE}$	A	MAX	6.2	6.2	7.2
t_{PLZ}				8.3	8.8	6.4
t_{PZH}	$\overline{OE}$	B	MAX	8.9	8.9	6.5
t_{PZL}				9.7	9.9	6.8
t_{PHZ}	$\overline{OE}$	B	MAX	6.9	6.9	7.2
t_{PLZ}				7.5	7.7	6.4

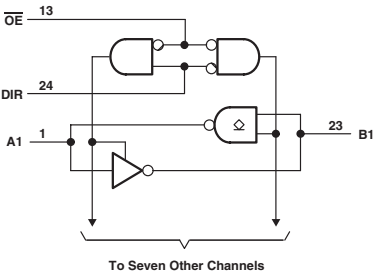
UNIT: ns

25642

25-Ω OCTAL BUS TRANSCEIVER

- High Output Drive Current
- Distributed V_{CC} and GND Pins Minimize Noise Generated by the Simultaneous Switching of Outputs

Logic Diagram



FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	$\overline{B}$ data to A bus
L	H	$\overline{A}$ data to B bus
H	X	Isolation

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 BCT	UNIT
I_{CC}	MAX	125	mA
I_{OH} (B port)	MAX	-3	mA
I_{OL} (A port)	MAX	188	mA
I_{OL} (B port)	MAX	24	mA
V_{OH} (A port)	MAX	5.5	V

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT
t_{PLH}	A	B	MAX	6.2
t_{PHL}				4
t_{PLH}	B	A	MAX	6.3
t_{PHL}				5.9
t_{PLH}	$\overline{OE}$	A	MAX	11.6
t_{PHL}				11.3
t_{PZH}	$\overline{OE}$	B	MAX	9.1
t_{PZL}				9.8
t_{PHZ}	$\overline{OE}$	B	MAX	7.3
t_{PLZ}				7.3

UNIT: ns

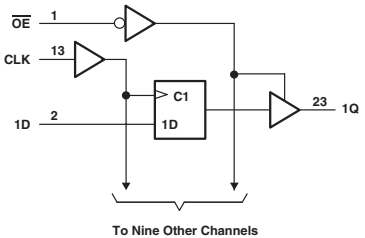
: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

29821

10-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

- 3-State Outputs
- Data Flow-Through Pinout

Logic Diagram



FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	SN74 BCT	UNIT
I_{CC}	MAX	115	35	mA
I_{OH}	MAX	-24	-24	mA
I_{OL}	MAX	48	48	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	SN74 BCT
f_{max}				-	125
t_w Pulse duration	CLK high or low		MIN	7	7
t_{su} Setup time	Data before CLK ↑		MIN	4	7
t_h Hold time	Data after CLK ↑		MIN	2	1
t_{PLH}	CLK	Q	MAX	10	12
t_{PHL}				10	10
t_{PZH}	$\overline{OE}$	Q	MAX	14	12
t_{PZL}				14	13
t_{PHZ}	$\overline{OE}$	Q	MAX	14	8
t_{PLZ}				12	8

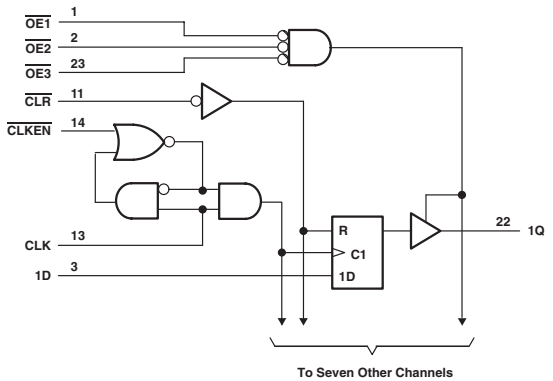
UNIT fmax : MHz other : ns

29825

8-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

- 3-State Outputs
- Data Flow-Through Pinout

Logic Diagram



FUNCTION TABLE

INPUTS					OUTPUT
$\overline{OE}$†	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	H or L	X	Q_0
H	X	X	X	X	Z

† $\overline{OE}$ = H if any of the output-enable inputs is high.
$\overline{OE}$ = L if all of the output-enable inputs are low.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 BCT	UNIT
I_{CC}	MAX	40	mA
I_{OH}	MAX	-24	mA
I_{OL}	MAX	48	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT
f_{max}			MIN	125
t_w Pulse duration	$\overline{CLK}$ low		MIN	4
	CLK high or low		MIN	4
t_{su} Setup time	Before CLK↑, data high		MIN	6
	Before CLK↑, data low		MIN	3.5
	$\overline{CLR}$		MIN	1
	$\overline{CLKEN}$ before CLK↑		MIN	8
t_h Hold time	After CLK↑, data high		MIN	1.5
	After CLK↑, data low		MIN	0
	$\overline{CLKEN}$ after CLK↑		MIN	0.5
t_{PLH}	CLK	Q	MAX	9
t_{PHL}				8.4
t_{PHL}	$\overline{CLR}$	Q	MAX	9.5
t_{PZH}	$\overline{OE}$	Q	MAX	10.3
t_{PZL}				10.2
t_{PHZ}	$\overline{OE}$	Q	MAX	9
t_{PLZ}				8.2

UNIT fmax : MHz other : ns

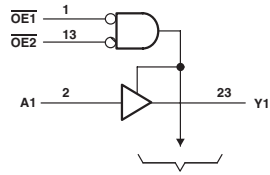
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

29827

10-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- pnp Inputs Reduce dc Loading
- 3-State Outputs
- Data Flow-Through Pinout

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
L	X	X	Z
H	H	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	SN74 BCT	UNIT
I_{CC}	MAX	40	40	mA
I_{OH}	MAX	-24	-24	mA
I_{OL}	MAX	48	48	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	SN74 BCT
t_{PLH}	A	Y	MAX	7	5.5
t_{PHL}				7.5	7.5
t_{PZH}	$\overline{OE}$	Y	MAX	15	9.1
t_{PZL}				15	12.8
t_{PHZ}	$\overline{OE}$	Y	MAX	17	8.8
t_{PLZ}				12	8.4

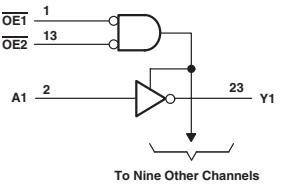
UNIT: ns

29828

10-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- pnp Inputs Reduce dc Loading
- 3-State Outputs
- Data Flow-Through Pinout

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	UNIT
I_{CC}	MAX	40	mA
I_{OH}	MAX	-24	mA
I_{OL}	MAX	48	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
t_{PLH}	A	Y	MAX	7
t_{PHL}				7.5
t_{PZH}	$\overline{OE}$	Y	MAX	15
t_{PZL}				15
t_{PHZ}	$\overline{OE}$	Y	MAX	17
t_{PLZ}				12

UNIT: ns

NOTICE : ALS IS NOT RECOMMENDED FOR NEW DESIGNS

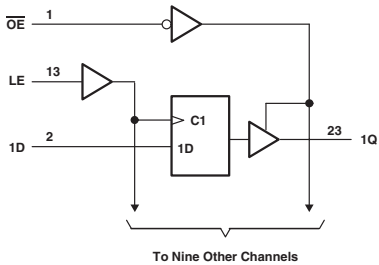
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

29841

10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

- 3-State Outputs
- Data Flow-Through Pinout

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT Q
$\overline{OE}$	LE	D	
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	SN74 BCT	UNIT
I_{CC}	MAX	85	35	mA
I_{OH}	MAX	-24	-24	mA
I_{OL}	MAX	48	48	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	SN74 BCT
t_w Pulse duration	LE high or low		MIN	6	4
t_{su} Setup time	Data before LE ↓		MIN	2.5	2
t_h Hold time	Data after LE ↓, high		MIN	4.5	1.5
	Data after LE ↓, low		MIN	4.5	3.5
t_{PLH}	D	Q	MAX	9.5	7.5
t_{PHL}				9.5	8.6
t_{PLH}	LE	Q	MAX	12	8.6
t_{PHL}				12	8.1
t_{PZH}	$\overline{OE}$	Q	MAX	14	9.2
t_{PZL}				14	12.8
t_{PHZ}	$\overline{OE}$	Q	MAX	15	6.9
t_{PLZ}				12	6.9

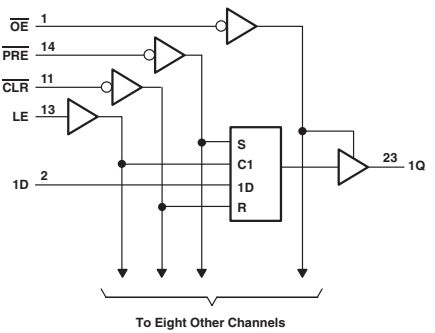
UNIT: ns

29843

9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

- 3-State Outputs
- Data Flow-Through Pinout

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS					OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OE}$	LE	D	Q
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	L
H	H	L	H	H	H
H	H	L	L	X	Q_0
X	X	H	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 BCT	UNIT
I_{CC}	MAX	35	mA
I_{OH}	MAX	-24	mA
I_{OL}	MAX	48	mA

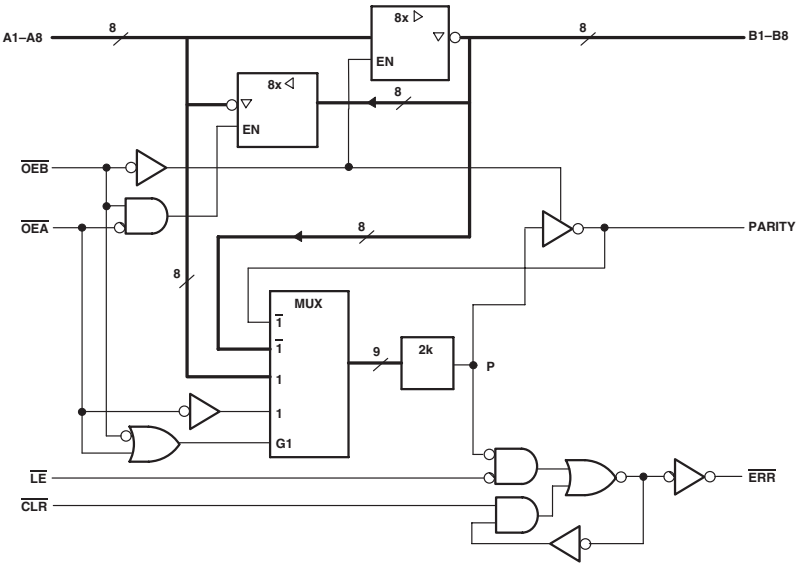
TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT
t_w Pulse duration	$\overline{PRE}$ low		MIN	7
	$\overline{CLR}$ low			5
	LE high			4
t_{su} Setup time	Data before LE ↓, high or low		MIN	1.5
	$\overline{PRE}$ or $\overline{CLR}$ inactive			2
t_h Hold time	Data after LE ↓, high or low		MIN	3.5
t_{PLH}	$\overline{D}$	Q	MAX	8
t_{PHL}				9
t_{PLH}	LE	Q	MAX	10
t_{PHL}				10
t_{PLH}	$\overline{PRE}$	Q	MAX	12
t_{PHL}				12
t_{PLH}	$\overline{CLR}$	Q	MAX	12
t_{PHL}				12
t_{PZH}	$\overline{OE}$	Q	MAX	15
t_{PZL}				15
t_{PHZ}	$\overline{OE}$	Q	MAX	8
t_{PLZ}				8

UNIT: ns

8-BIT TO 9-BIT PARITY BUS TRANSCEIVER

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS						OUTPUT AND I/O				OPERATION
$\overline{OEB}$	$\overline{OEA}$	$\overline{CLR}$	$\overline{LE}$	Ai Σ of Hs	Bi† Σ of Ls	A	B	PARITY	$\overline{ERR}$‡	
L	H	X	X	Odd Even	NA	NA	$\overline{A}$	H L	NA	$\overline{A}$ data to B bus and generate parity
H	L	X	L	NA	Odd Even	$\overline{B}$	NA	NA	H L	$\overline{B}$ data to A bus and check parity
H	L	H	H	NA	X	X	NA	NA	N-1	Store error flag
X	X	L	H	X	X	X	NA	NA	H	Clear error-flag register
H	H	H L X X	H H L L	X X L Odd H Even	X	Z	Z	Z	NC H L H	Isolation§
L	L	X	X	Odd Even	NA	NA	$\overline{A}$	L H	NA	$\overline{A}$ data to B bus and generate inverted parity

NA = not applicable, NC = no change, X = don't care
† Summation of high-level inputs includes PARITY along with Bi inputs.
‡ Output states Shown assume $\overline{ERR}$ was previously high.
§ In this mode, $\overline{ERR}$, when enabled, shows inverted parity of the A bus.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	SN74 BCT	UNIT
I_{CC}	MAX	100	80	mA
I_{OH}	MAX	-24	-24	mA
I_{OL}	MAX	48	48	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	SN74 BCT
t_w Pulse duration	$\overline{LE}$ high		MIN	10	-
	$\overline{LE}$ low		MIN	10	10
	$\overline{CLR}$ low		MIN	10	10
t_{su} Setup time	Before $\overline{LE}$ ↓, Bi and PARITY		MIN	10	18
	Before LE ↓, $\overline{CLR}$ high		MIN	15	-
t_h Hold time	Bi and PARITY after $\overline{LE}$ ↓		MIN	3	8
t_{PLH}	A or B	B or A	MAX	8	8
t_{PHL}				8	8
t_{PLH}	A	PARITY	MAX	15	15
t_{PHL}				18	15
t_{PZH}	$\overline{OEA}$ or $\overline{OEB}$	A or B	MAX	17	17
t_{PZL}				17	19
t_{PHZ}	$\overline{OEA}$ or $\overline{OEB}$	A or B	MAX	15	15
t_{PLZ}				8	17
t_{PHL}	$\overline{LE}$	$\overline{ERR}$	MAX	12	9
t_{PLH}	$\overline{CLR}$	$\overline{ERR}$	MAX	12	15
t_{PLH}	$\overline{OEA}$	PARITY	MAX	17	15
t_{PHL}				19	16
t_{PLH}	Bi / PARITY	$\overline{ERR}$	MAX	20	20
t_{PHL}				20	15

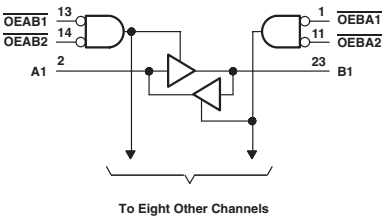
UNIT: ns

29863

9-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- True Outputs

Logic Diagram



FUNCTION TABLE

INPUTS				OPERATION
$\overline{OEAB1}$	$\overline{OEAB2}$	$\overline{OEBA1}$	$\overline{OEBA2}$	
L	L	L	L	Latch A and B
L	L	H	X	A to B
L	L	X	H	
H	X	L	L	B to A
X	H	L	L	
H	X	H	X	Isolation
H	X	X	H	
X	H	X	H	
X	H	H	X	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	SN74 BCT	UNIT
I_{CC}	MAX	65	45	mA
I_{OH}	MAX	-24	-24	mA
I_{OL}	MAX	48	48	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	SN74 BCT
t_{PLH}	A or B	B or A	MAX	8	5
t_{PHL}				8	7.5
t_{PZH}	$\overline{OEAB}$ or $\overline{OEBA}$	A or B	MAX	15	8.4
t_{PZL}				15	12.6
t_{PHZ}	$\overline{OEAB}$ or $\overline{OEBA}$	A or B	MAX	17	8.8
t_{PLZ}				12	8.1

UNIT: ns

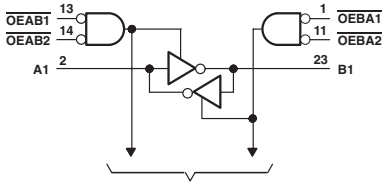
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

29864

9-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

- Inverted Outputs

Logic Diagram



FUNCTION TABLE

INPUTS				OPERATION
$\overline{OEAB1}$	$\overline{OEAB2}$	$\overline{OEBA1}$	$\overline{OEBA2}$	
L	L	L	L	Latch A and B
L	L	H	X	$\overline{A}$ to B
L	L	X	H	
H	X	L	L	$\overline{B}$ to A
X	H	L	L	
H	X	H	X	Isolation
H	X	X	H	
X	H	X	H	
X	H	H	X	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

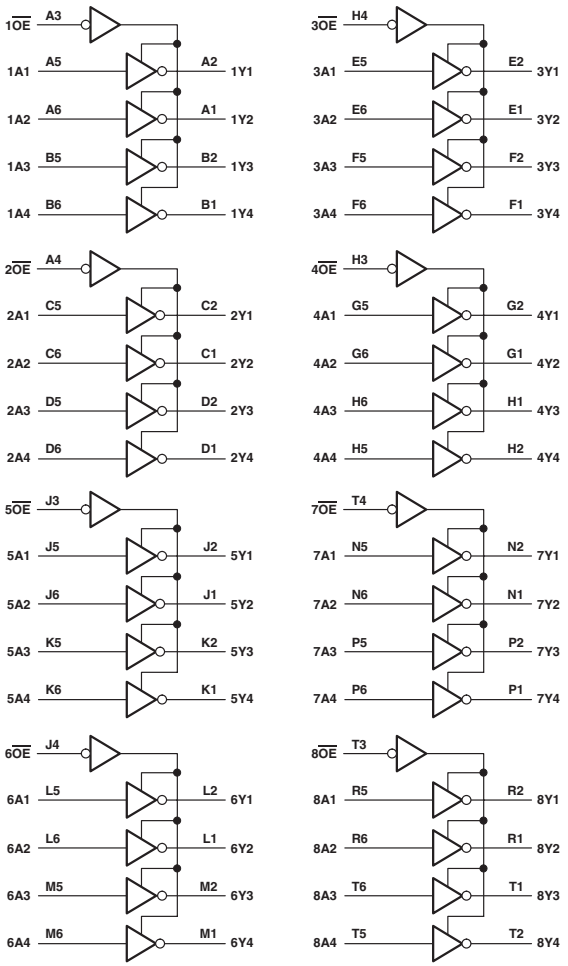
PARAMETER	MAX or MIN	SN74 BCT	UNIT
I_{CC}	MAX	45	mA
I_{OH}	MAX	-24	mA
I_{OL}	MAX	48	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT
t_{PLH}	A or B	B or A	MAX	6.1
t_{PHL}				4.8
t_{PZH}	$\overline{OEAB}$ or $\overline{OEBA}$	A or B	MAX	8.4
t_{PZL}				12.5
t_{PHZ}	$\overline{OEAB}$ or $\overline{OEBA}$	A or B	MAX	8.4
t_{PLZ}				8.2

UNIT: ns

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

(each 4bit buffer/drirer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

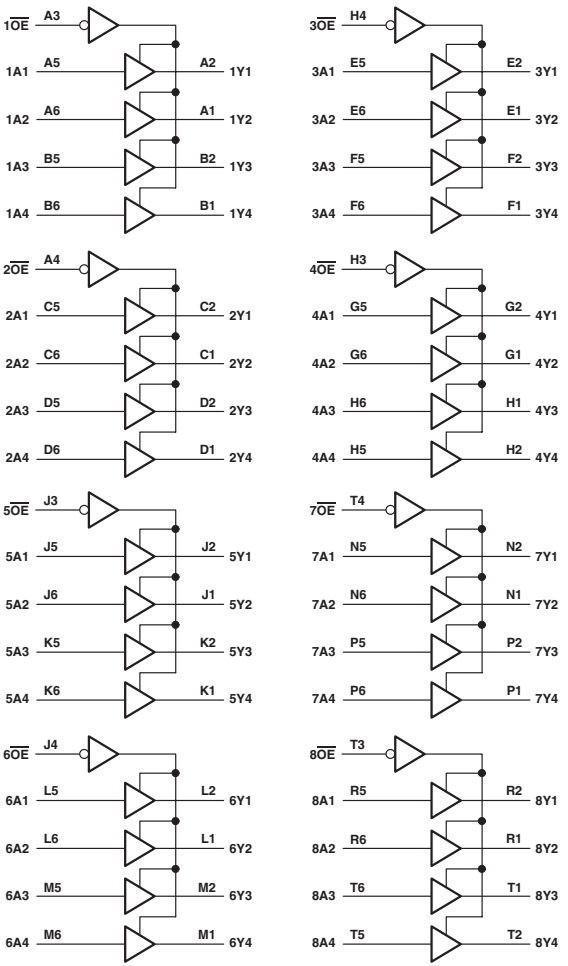
PARAMETER	MAX or MIN	LVCZ 3V	LVT	UNIT
I_{CC}	MAX	0.2	10	mA
I_{OH}	MAX	-24	-32	mA
I_{OL}	MAX	24	64	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVCZ 3V	LVT
t_{PLH}	A	Y	MAX	4.2	3.5
t_{PHL}			MAX	4.2	3.5
t_{PZH}	$\overline{OE}$	Y	MAX	4.7	4
t_{PZL}			MAX	4.7	4.4
t_{PHZ}	$\overline{OE}$	Y	MAX	5.9	4.5
t_{PLZ}			MAX	5.9	4.2

UNIT:ns

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVT 3V	LVTH 3V	ALVTH 3V	LVC 3V	LVCH 3V	LVCZ 3V	ALVCH 3V	AUC 1.8V	AUC 2.3V	AUCH 1.8V	AUCH 2.3V	UNIT
I_{CC}	MAX	10	10	5	0.04	0.04	0.2	0.08	0.04	0.04	0.04	0.04	mA
I_{OH}	MAX	-32	-32	-32	-24	-24	-24	-24	-8	-9	-8	-9	mA
I_{OL}	MAX	64	64	64	24	24	24	24	8	9	8	9	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVT 3V	LVTH 3V	ALVTH 3V	LVC 3V	LVCH 3V	LVCZ 3V	ALVCH 3V	AUC 1.8V
t_{PLH}	A	Y	MAX	3.2	3.2	2.4	4.1	4.1	4.1	3	1.8
t_{PHL}				3.2	3.2	2.5	4.1	4.1	4.1	3	1.8
t_{PZH}	$\overline{OE}$	Y	MAX	4	4	3.8	4.6	4.6	4.6	4.4	2.5
t_{PZL}				4	4	2.9	4.6	4.6	4.6	4.4	2.5
t_{PHZ}	$\overline{OE}$	Y	MAX	4.5	4.5	4.2	5.8	5.8	5.8	4.1	4.0
t_{PLZ}				4.2	4.2	3.6	5.8	5.8	5.8	4.1	4.0

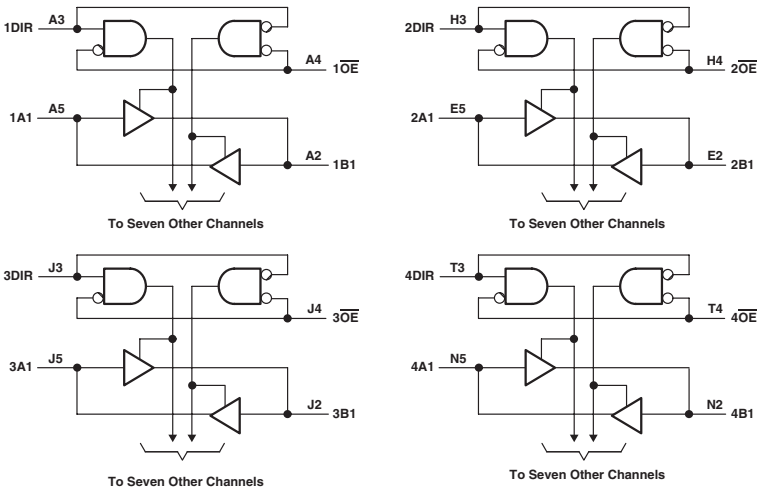
PARAMETER	INPUT	OUTPUT	MAX or MIN	AUC 2.3V	AUCH 1.8V	AUCH 2.3V
t_{PLH}	A	Y	MAX	1.8	1.8	1.8
t_{PHL}				1.8	1.8	1.8
t_{PZH}	$\overline{OE}$	Y	MAX	1.9	2.5	1.9
t_{PZL}				1.9	2.5	1.9
t_{PHZ}	$\overline{OE}$	Y	MAX	2	4.0	2
t_{PLZ}				2	4.0	2

UNIT: ns

32245

32-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
(each 9-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ABTH	LVTH 3V	LVC 3V	LVCH 3V	LVCHR 3V	LVCR 3V	LVCZ 3V	ALVCH 3V	AUC 1.8V	AUC 2.3V	UNIT
I_{CC}	MAX	20	20	10	0.02	0.04	0.04	0.02	0.12	0.08	0.04	0.04	mA
I_{OH}	MAX	-32	-32	-32	-24	-24	-12	-12	-24	-24	-8	-9	mA
I_{OL}	MAX	64	64	64	24	24	12	12	24	24	8	9	mA

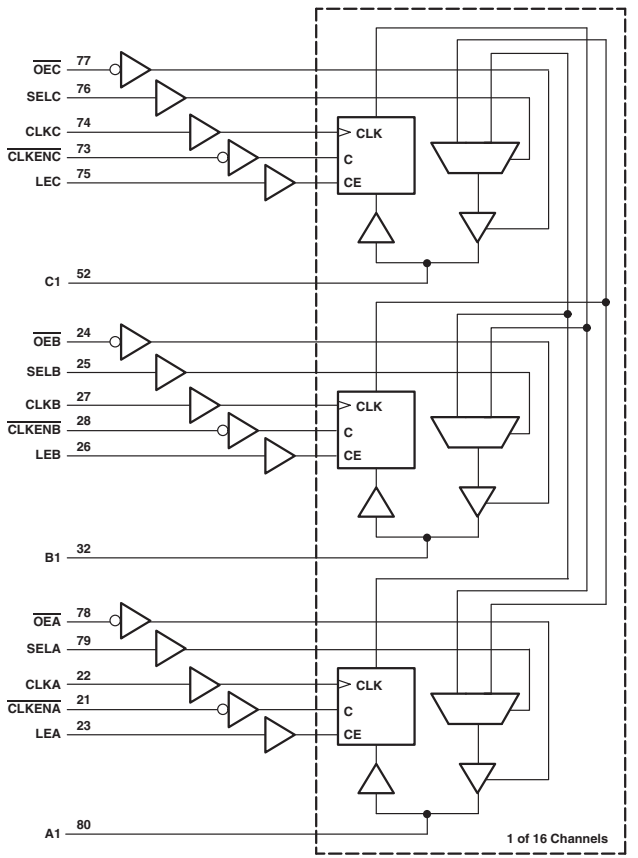
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ABTH	LVTH 3V	LVC 3V	LVCH 3V	LVCHR 3V	LVCR 3V	LVCZ 3V
t_{PLH}	A or B	B or A	MAX	5	5	3.3	4	4	4.8	4.8	4.0
t_{PHL}				5.2	5.2	3.3	4	4	4.8	4.8	4.0
t_{PZH}	$\overline{OE}$	B or A	MAX	7.3	7.3	4.5	5.5	5.5	6.3	6.3	5.6
t_{PZL}				8.1	8.1	4.6	5.5	5.5	6.3	6.3	5.6
t_{PHZ}	$\overline{OE}$	B or A	MAX	6.5	6.5	5.1	6.6	6.6	7.4	7.4	6.6
t_{PLZ}				6.9	6.9	5.1	6.6	6.6	7.4	7.4	6.6

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V	AUC 1.8V	AUC 2.3V
t_{PLH}	A or B	B or A	MAX	3	2.0	1.9
t_{PHL}				3	2.0	1.9
t_{PZH}	$\overline{OE}$	B or A	MAX	4.4	3.1	2.6
t_{PZL}				4.4	3.1	2.6
t_{PHZ}	$\overline{OE}$	B or A	MAX	4.1	4.8	2.9
t_{PLZ}				4.1	4.8	2.9

UNIT: ns

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE
STORAGE†

INPUTS				OUTPUT
$\overline{CLKENA}$	CLKA	LEA	A	
H	X	L	X	Q_0‡
L	↑	L	L	L
L	↑	L	H	H
X	H	L	X	Q_0‡
X	L	L	X	Q_0‡
X	X	H	L	L
X	X	H	H	H

† A-port register shown, B and C ports are similar but use $\overline{CLKENB}$, $\overline{CLKENC}$, CLKB, CLKC, LEB, and LEC.
‡ Output level before the indicated steady-state input conditions were established.

A-PORT OUTPUT

INPUTS		OUTPUT A
$\overline{OEA}$	SELA	
H	X	Z
L	H	Output of C register
L	L	Output of B register

B-PORT OUTPUT

INPUTS		OUTPUT B
$\overline{OEB}$	SELB	
H	X	Z
L	H	Output of A register
L	L	Output of C register

C-PORT OUTPUT

INPUTS		OUTPUT C
$\overline{OEC}$	SELC	
H	X	Z
L	H	Output of B register
L	L	Output of A register

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

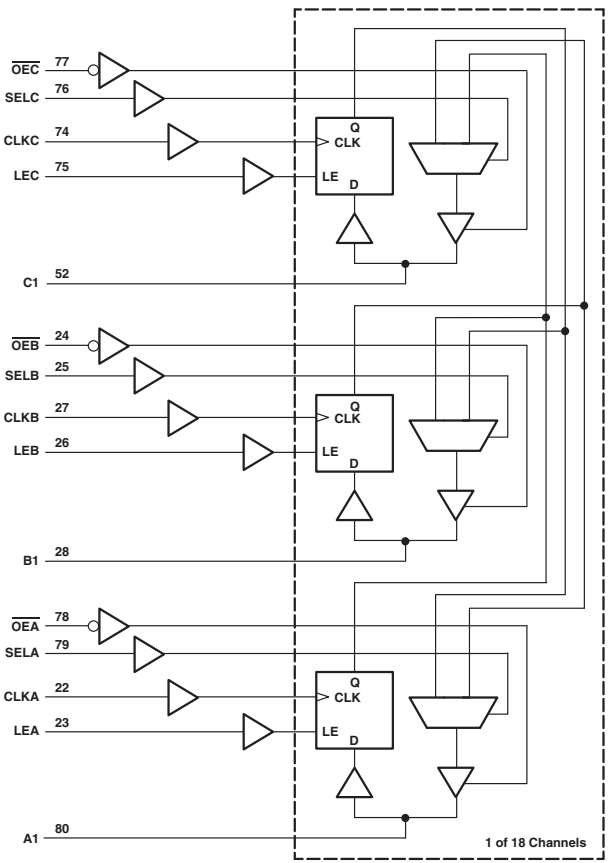
PARAMETER	MAX or MIN	ABTH	UNIT
I_{CC}	MAX	40	mA
I_{OH}	MAX	-32	mA
I_{OL}	MAX	64	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABTH
f_{max}			MIN	150
t_w Pulse duration	LE high		MIN	3.3
	CLK high or low		MIN	3.3
t_{su} Setup time	A, B, or C before CLK ↑		MIN	2.4
	A or B before LE ↓		MIN	2.1
	$\overline{CLKEN}$ before CLK ↑		MIN	3.2
t_h Hold time	A, B, or C after CLK ↑		MIN	1.4
	A or B after LE ↓		MIN	2.1
	$\overline{CLKEN}$ after CLK ↑		MIN	1.1
t_{PLH}	A, B, or C	C, B, or A	MAX	6.1
t_{PHL}				6.6
t_{PLH}	SEL	A, B, or C	MAX	6.5
t_{PHL}				6.5
t_{PLH}	LE	A, B, or C	MAX	7.5
t_{PHL}				6.9
t_{PLH}	CLK	A, B, or C	MAX	7.5
t_{PHL}				6.7
t_{PZH}	$\overline{OE}$	A, B, or C	MAX	6.4
t_{PZL}				6.8
t_{PHZ}	$\overline{OE}$	A, B, or C	MAX	6
t_{PLZ}				6.1

UNIT fmax : MHz other : ns

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE
STORAGE†

INPUTS			OUTPUT
CLKA	LEA	A	
↑	L	L	L
↑	L	H	H
H	L	X	Q_0‡
L	L	X	Q_0‡
X	H	L	L
X	H	H	H

† A-port register shown, B and C ports are similar but use CLKB, CLKC, LEB, and LEC.
‡ Outpu level befor the indicated steady-state input conditions were established.

A-PORT OUTPUT

INPUTS		OUTPUT A
$\overline{OEA}$	SELA	
H	X	Z
L	H	Output of C register
L	L	Output of B register

B-PORT OUTPUT

INPUTS		OUTPUT B
$\overline{OEB}$	SELB	
H	X	Z
L	H	Output of A register
L	L	Output of C register

C-PORT OUTPUT

INPUTS		OUTPUT C
$\overline{OEC}$	SELC	
H	X	Z
L	H	Output of B register
L	L	Output of A register

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABTH	UNIT
I_{CC}	MAX	45	mA
I_{OH}	MAX	-32	mA
I_{OL}	MAX	64	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

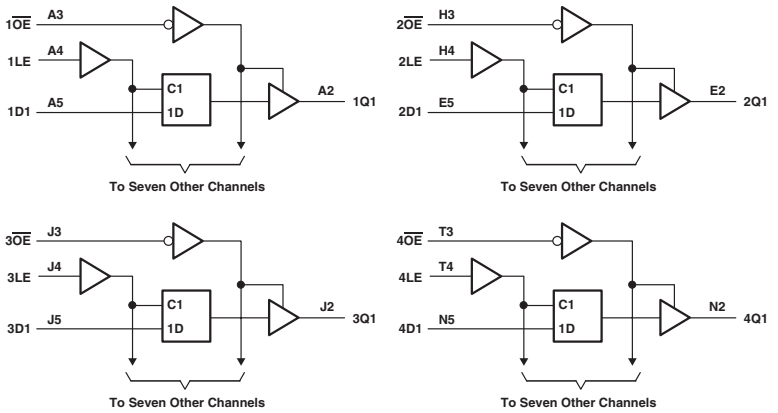
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABTH
f_{max}			MIN	150
t_w Pulse duration	LE high		MIN	3.3
	CLK high or low		MIN	3.3
t_{su} Setup time	A, B, or C before CLK↑		MIN	2.4
	A, B, or C before LE↓		MIN	2.1
t_h Hold time	A, B, or C after CLK↑		MIN	1.4
	A, B, or C after LE↓		MIN	2.1
t_{PLH}	A, B, or C	C, B, or A	MAX	6.1
t_{PHL}				6.6
t_{PLH}	SEL	A, B, or C	MAX	6.5
t_{PHL}				6.5
t_{PLH}	LE	A, B, or C	MAX	7.5
t_{PHL}				6.9
t_{PLH}	CLK	A, B, or C	MAX	7.4
t_{PHL}				6.7
t_{PZH}	$\overline{OE}$	A, B, or C	MAX	6.8
t_{PZL}				7.1
t_{PHZ}	$\overline{OE}$	A, B, or C	MAX	6.2
t_{PLZ}				6

UNIT fmax : MHz other : ns

32373

32-BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

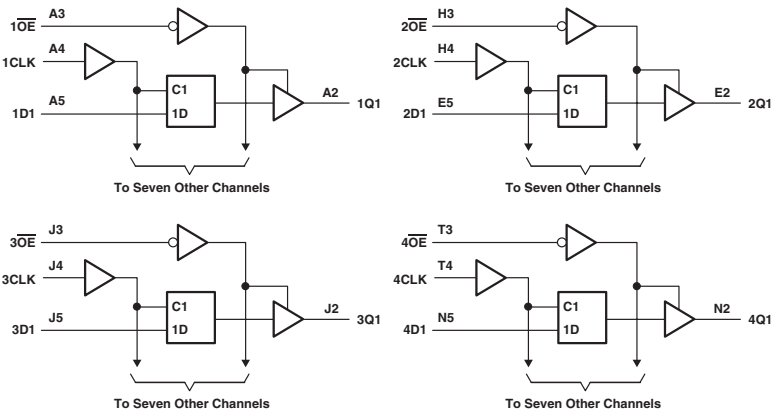
PARAMETER	MAX or MIN	LVTH 3V	ALVTH 3V	LVC 3V	LVCH 3V	UNIT
I_{CC}	MAX	10	5	0.04	0.04	mA
I_{OH}	MAX	-32	-32	-24	-24	mA
I_{OL}	MAX	64	64	24	24	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTH 3V	ALVTH 3V	LVC 3V	LVCH 3V
t_w Pulse duration, LE high or low			MIN	3	1.5	3.3	3.3
t_{su} Setup time	Data before LE ↓ , data high		MIN	1	1.4	1.7	1.7
	Data before LE ↓ , data low		MIN	1	0.9	1.7	1.7
t_h Hold time	Data after LE ↓ , data high		MIN	1	0.9	1.2	1.2
	Data after LE ↓ , data low		MIN	1	1.4	1.2	1.2
t_{PLH}	D	Q	MAX	3.8	3.1	4.2	4.2
t_{PHL}				3.6	3.3	4.2	4.2
t_{PLH}	LE	Q	MAX	4.3	3.3	4.6	4.6
t_{PHL}				4	3.5	4.6	4.6
t_{PZH}	$\overline{OE}$	Q	MAX	4.3	4	4.7	4.7
t_{PZL}				4.3	3.4	4.7	4.7
t_{PHZ}	$\overline{OE}$	Q	MAX	5	4.9	5.9	5.9
t_{PLZ}				4.7	4.5	5.9	5.9

UNIT: ns

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVTH 3V	ALVTH 3V	LVC 3V	LVCH 3V	ALVCH 3V	AUC 1.8V	AUC 2.3V	AUCH 1.8V	AUCH 2.3V	UNIT
I_{CC}	MAX	10	5	0.04	0.04	0.08	0.04	0.04	0.04	0.04	mA
I_{OH}	MAX	-32	-32	-24	-24	-24	-8	-9	-8	-9	mA
I_{OL}	MAX	64	64	24	24	24	8	9	8	9	mA

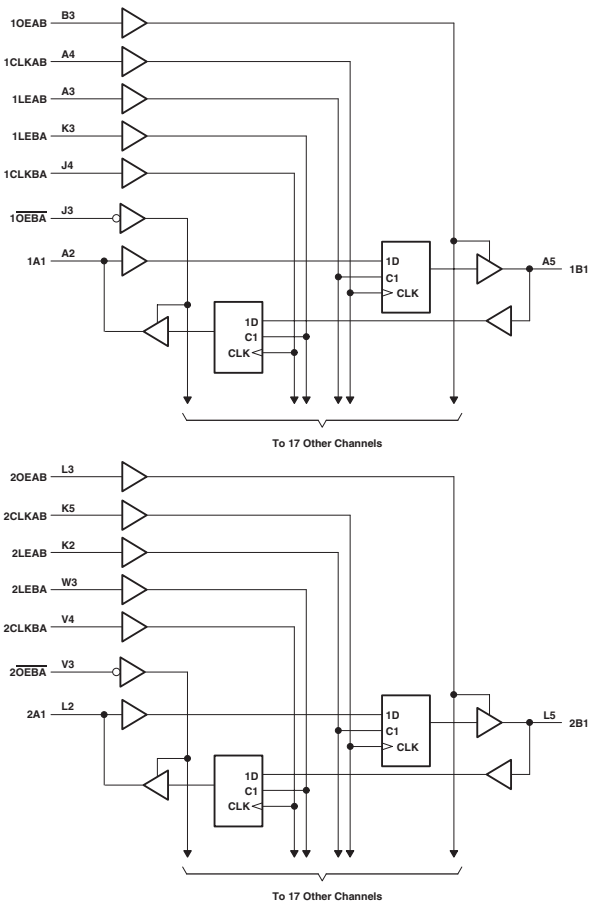
TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTH 3V	ALVTH 3V	LVC 3V	LVCH 3V	ALVCH 3V	AUC 1.8V	AUC 2.3V
f_{max}				160	250	150	150	150	250	250
t_w Pulse duration, CLK high or low			MIN	3	1.5	3.3	3.3	3.3	1.9	1.9
t_{su} Setup time	Data before CLK ↑, data high		MIN	1.8	1	1.9	1.9	1.9	0.6	0.6
	Data before CLK ↑, data low		MIN	1.8	1.5	1.9	1.9	1.9	0.6	0.6
t_h Hold time	Data after CLK ↑, data high		MIN	0.8	0.5	1.9	1.1	0.5	0.4	0.4
	Data after CLK ↑, data low		MIN	0.8	1	1.9	1.1	0.5	0.4	0.4
t_{PLH}	CLK	Q	MAX	4.5	3.2	4.5	4.5	4.2	2.8	2.2
t_{PHL}				4	3.2	4.5	4.5	4.2	2.8	2.2
t_{PZH}	$\overline{OE}$	Q	MAX	4.5	3.8	4.6	4.6	4.8	2.9	2.2
t_{PZL}				4.4	3.3	4.6	4.6	4.8	2.9	2.2
t_{PHZ}	$\overline{OE}$	Q	MAX	5	4.6	5.5	5.5	4.3	4.5	2.2
t_{PLZ}				4.6	4.2	5.5	5.5	4.3	4.5	2.2

PARAMETER	INPUT	OUTPUT	MAX or MIN	AUCH 1.8V	AUCH 2.3V
f_{max}				250	250
t_w Pulse duration, CLK high or low			MIN	1.9	1.9
t_{su} Setup time	Data before CLK ↑, data high		MIN	0.6	0.6
	Data before CLK ↑, data low		MIN	0.6	0.6
t_h Hold time	Data after CLK ↑, data high		MIN	0.4	0.4
	Data after CLK ↑, data low		MIN	0.4	0.4
t_{PLH}	CLK	Q	MAX	2.8	2.2
t_{PHL}				2.8	2.2
t_{PZH}	$\overline{OE}$	Q	MAX	2.9	2.2
t_{PZL}				2.9	2.2
t_{PHZ}	$\overline{OE}$	Q	MAX	4.5	2.2
t_{PLZ}				4.5	2.2

UNIT fmax : MHz other : ns

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE†

INPUTS				OUTPUT
OEAB	LEAB	CLKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	H	X	B_0‡
H	L	L	X	B_0§

† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, and CLKBA.
‡ Output level before the indicated steady-state input conditions were established
§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

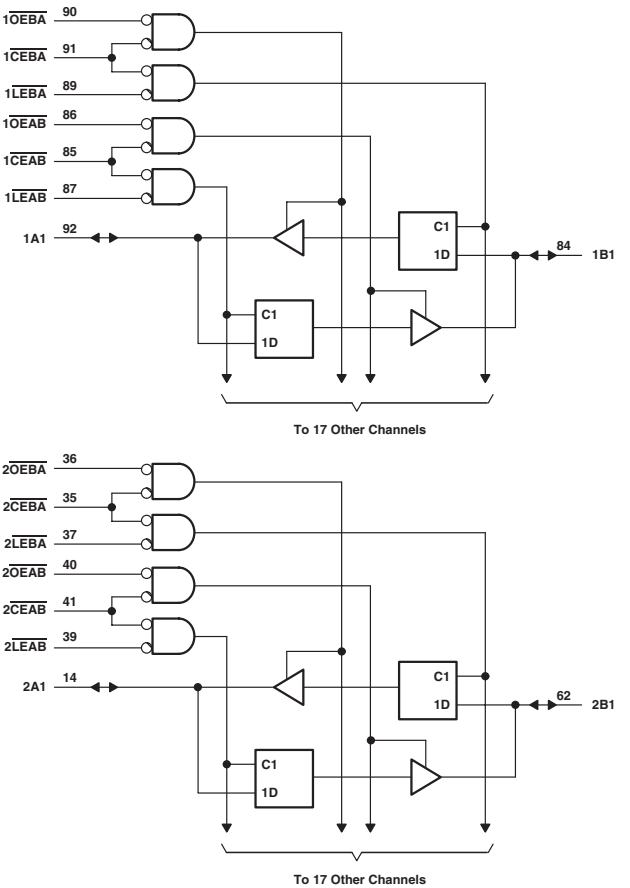
PARAMETER	MAX or MIN	ABTH	ALVCH 3V	UNIT
I_{CC}	MAX	90	0.08	mA
I_{OH}	MAX	-32	-24	mA
I_{OL}	MAX	64	24	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABTH	ALVCH 3V
f_{max}			MIN	150	150
t_w Pulse duration	LEAB or LEBA high		MIN	3.3	3.3
	CLKAB or CLKBA high or low		MIN	3.3	3.3
t_{su} Setup time	A before CLKAB ↑		MIN	3.5	1.7
	B before CLKBA ↑		MIN	3.5	1.7
	A before LEAB ↓ or LEBA ↓ CLK high		MIN	1.6	1.5
	A before LEAB ↓ or LEBA ↓ CLK low		MIN	1.6	1
t_h Hold time	A after CLKAB ↑ or B after CLKBA ↑		MIN	0	0.7
	A after LEAB ↓ or B after LEBA ↓		MIN	1.6	1.4
t_{PLH}	A or B	B or A	MAX	4.8	3.9
t_{PHL}				5.4	3.9
t_{PZH}	LEAB or LEBA	B or A	MAX	5.3	4.6
t_{PZL}				5.5	4.6
t_{PHZ}	CLKAB or CLKBA	B or A	MAX	5.3	4.9
t_{PLZ}				5.4	4.9
t_{PZH}	OEAB	B	MAX	5.6	4.6
t_{PZL}				6	4.6
t_{PHZ}	OEAB	B	MAX	5.9	5
t_{PLZ}				5.6	5
t_{PZH}	$\overline{OEBA}$	A	MAX	5.6	5
t_{PZL}				6	5
t_{PHZ}	$\overline{OEBA}$	A	MAX	5.9	4.2
t_{PLZ}				5.6	4.2

UNIT fmax : MHz other : ns

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS				OUTPUT
CEAB	LEAB	OEAB	A	Y
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B_0‡
L	L	L	L	L
L	L	L	H	H

† A-to-B data flow is shown: B-to-A flow conditions is the same that it uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.
‡ Outoput level before the indicated steady-state input conditions were established

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABTH	UNIT
I_{CC}	MAX	20	mA
I_{OH}	MAX	-32	mA
I_{OL}	MAX	64	mA

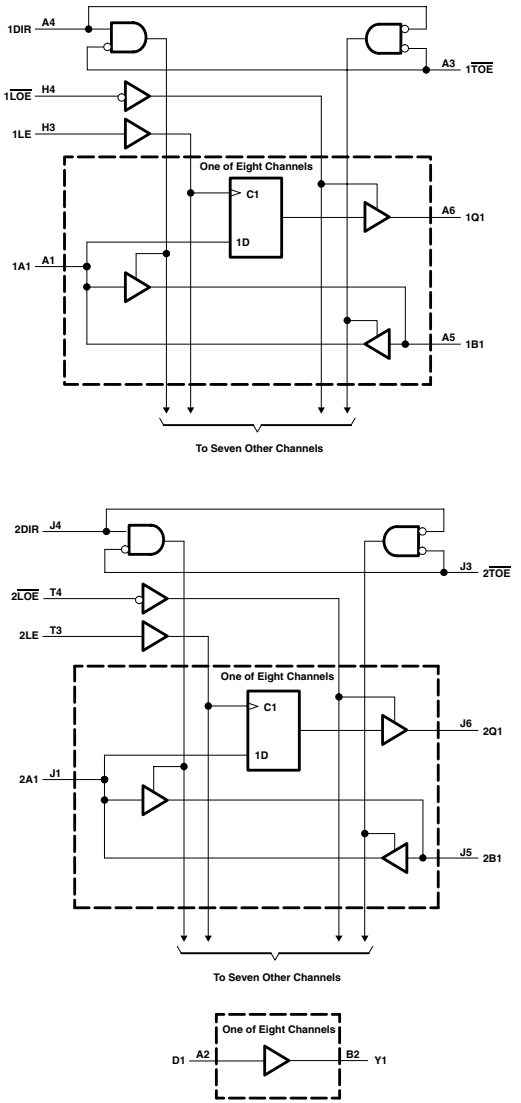
TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABTH
t_w Pulse duration, $\overline{LEAB}$ or $\overline{LEBA}$ low			MIN	3.3
t_{su} Setup time	Data before $\overline{LEAB}$ ↑ or $\overline{LEBA}$ ↑		MIN	2.1
	Data before $\overline{CEAB}$ ↑ or $\overline{CEBA}$ ↑		MIN	1.7
t_h Hold time	Data after $\overline{LEAB}$ ↑ or $\overline{LEBA}$ ↑		MIN	0.6
	Data after $\overline{CEAB}$ ↑ or $\overline{CEBA}$ ↑		MIN	0.9
t_{PLH}	A or B	B or A	MAX	5.9
t_{PHL}				5.7
t_{PLH}	$\overline{LE}$	A or B	MAX	7.5
t_{PHL}				6.6
t_{PZH}	$\overline{CE}$	A or B	MAX	8
t_{PZL}				8.8
t_{PHZ}	$\overline{CE}$	A or B	MAX	7.1
t_{PLZ}				7.5
t_{PZH}	$\overline{OE}$	A or B	MAX	7.3
t_{PZL}				8.1
t_{PHZ}	$\overline{OE}$	A or B	MAX	6.5
t_{PLZ}				6.9

UNIT: ns

16-BIT BUS TRANSCEIVER AND TRANSPARENT D-TYPE LATCH WITH EIGHT INDEPENDENT BUFFERS

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS		OPERATION
$\overline{TOE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	A bus and B bus Isolation

INPUTS			OUTPUT
$\overline{LOE}$	LE	A	Q
L	H	H	H
L	H	L	L
L	L	X	Q_O
H	X	X	Z

INPUT D	OUTPUT Y
L	L
H	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I_{CC}	MAX	0.06	mA
I_{OH}	MAX	-24	mA
I_{OL}	MAX	24	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

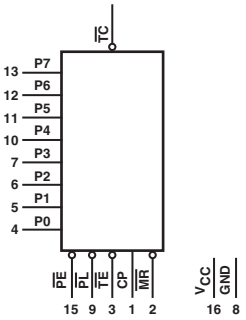
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
t_w Pulse duration	LE high		MIN	2
t_{su} Setup time	data before LE ↓		MIN	0.9
t_h Hold time	data after LE ↓		MIN	0.9
t_{PLH}	D	Y	MAX	3
t_{PHL}				3
t_{PLH}	A	Q	MAX	3
t_{PHL}				3
t_{PLH}	LE	Q	MAX	3
t_{PHL}				3
t_{PLH}	A or B	B or A	MAX	3
t_{PHL}				3
t_{PZH}	$\overline{LOE}$	Q	MAX	4.7
t_{PZL}				4.7
t_{PZH}	$\overline{TOE}$	A or B	MAX	4.4
t_{PZL}				4.4
t_{PZH}	DIR	A or B	MAX	4.7
t_{PZL}				4.7
t_{PHZ}	$\overline{LOE}$	Q	MAX	4.1
t_{PLZ}				4.1
t_{PHZ}	$\overline{TOE}$	A or B	MAX	4.1
t_{PLZ}				4.1
t_{PHZ}	DIR	A or B	MAX	4.7
t_{PLZ}				4.7

UNIT: ns

40103

8-STAGE SYNCHRONOUS DOWN COUNTERS

Function Diagram



FUNCTION TABLE

CONTROL INPUTS					
$\overline{MR}$	$\overline{PL}$	$\overline{PE}$	$\overline{TE}$	PRESET MODE	ACTION
L	X	X	L	Synchronous	Inhibit Counter
X	H	X	L		Cownt Down
X	X	L	L		Preset On Next Positive Clock Transition
H	L	L	L	Asynchronously	Preset Asychronously
H	L	H	L		Clear to Maximum Count

: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	0.16	0.16	mA
I_{OH}	MAX	-4	-4	mA
I_{OL}	MAX	4	4	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
t_w	CP		MIN	50	53
	$\overline{PL}$			38	65
	$\overline{MR}$			38	53
t_{su}	P to CP		MIN	30	36
	$\overline{PE}$ to CP			22	30
	$\overline{TE}$ to CP			45	60
t_h	P to CP		MIN	5	5
	$\overline{TE}$ to $\overline{CP}$			0	0
	$\overline{PE}$ to $\overline{CP}$			2	2
t_{PLH}	CP	$\overline{TC}$ (Async Preset)	MAX	90	90
t_{PHL}				90	90
t_{PLH}	CP	$\overline{TC}$ (Sync Preset)	MAX	90	95
t_{PHL}				90	95
t_{PLH}	$\overline{TE}$	$\overline{TC}$	MAX	60	75
t_{PHL}				60	75
t_{PLH}	$\overline{PL}$	$\overline{TC}$	MAX	83	102
t_{PHL}				83	102
t_{PLH}	$\overline{MR}$	$\overline{TC}$	MAX	83	83
t_{PHL}				83	83

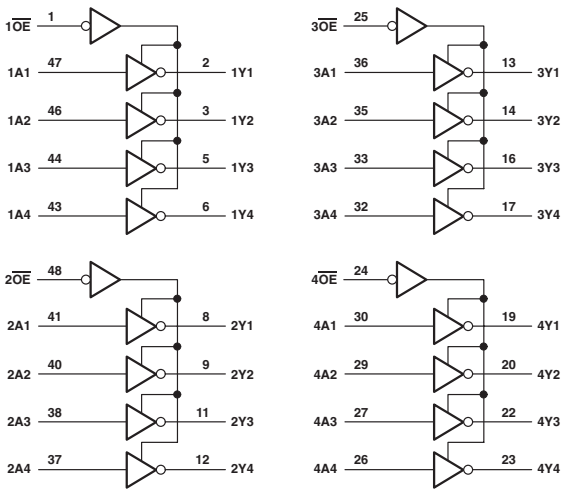
UNIT : ns

162240

3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- SN74LVT162240, SN74LVTH162240: Output Ports Have Equivalent 22-Ω Series Resistors

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVT 3V	LVTH 3V	UNIT
I_{CC}	MAX	5	5	mA
I_{OH}	MAX	-12	-12	mA
I_{OL}	MAX	12	12	mA

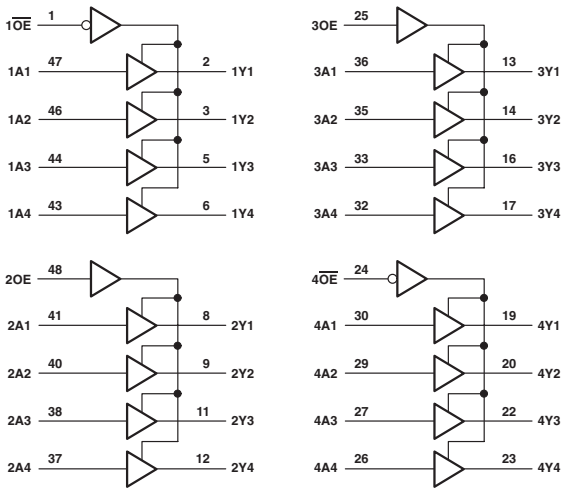
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVT 3V	LVTH 3V
t_{PLH}	A	Y	MAX	4	4
t_{PHL}				4	4
t_{PZH}	$\overline{OE}$	Y	MAX	4.8	4.8
t_{PZL}				4.7	4.7
t_{PHZ}	$\overline{OE}$	Y	MAX	4.7	4.7
t_{PLZ}				4.5	4.5

UNIT: ns

: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUT
$1\overline{OE}$, $4\overline{OE}$	1A, 4A	1Y, 4Y
L	H	H
L	L	L
H	X	Z

INPUTS		OUTPUT
2OE, 3OE	2A, 3A	2Y, 3Y
H	H	H
H	L	L
L	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVTH 3V	UNIT
I_{CC}	MAX	5	mA
I_{OH}	MAX	-12	mA
I_{OL}	MAX	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTH 3V
t_{PLH}	A	Y	MAX	4.1
t_{PHL}				4.1
t_{PZH}	$\overline{OE}$ or OE	Y	MAX	4.9
t_{PZL}				4.8
t_{PHZ}	$\overline{OE}$ or OE	Y	MAX	5.3
t_{PLZ}				4.9

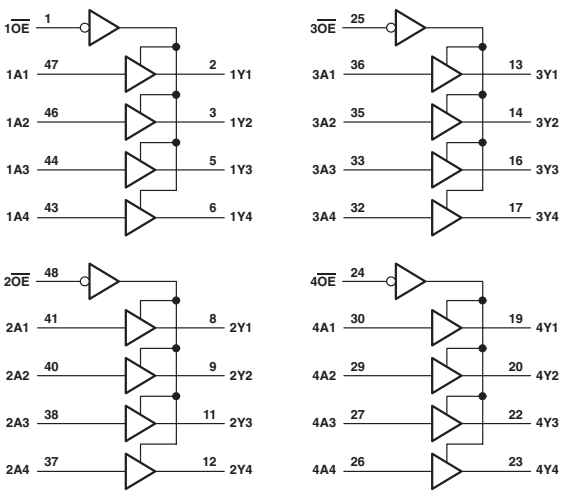
UNIT: ns

162244

16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- SN74ABT162244: Output Ports Have Equivalent 25-Ω Series Resistors
- SN74LVT162244A, LVTH162244: Output Ports Have Equivalent 22-Ω Series Resistors
- SN74ALVTH162244: Output Ports Have Equivalent 30-Ω Series Resistors
- SN74LVC162244A: Output Ports Have Equivalent 26-Ω Series Resistors
- SN74LVCH162244A: Output Ports Have Equivalent 26-Ω Series Resistors
- SN74ALVCH162244: Output Ports Have Equivalent 26-Ω Series Resistors

Logic Diagram



FUNCTION TABLE
(each 4-bit buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	LVT 3V	LVTH 3V	ALVTH 3V	LVC 3V	LVCH 3V	ALVCH 3V	UNIT
I_{CC}	MAX	30	5	5	5	0.02	0.02	0.04	mA
I_{OH}	MAX	-12	-12	-12	-12	-12	-12	-12	mA
I_{OL}	MAX	12	12	12	12	12	12	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVT 3V	LVTH 3V	ALVTH 3V	LVC 3V	LVCH 3V	ALVCH 3V
t_{PLH}	A	Y	MAX	3.9	4	4	3.3	4.4	4.4	4.2
t_{PHL}				4.8	3.6	3.6	3.3	4.4	4.4	4.2
t_{PZH}	$\overline{OE}$	Y	MAX	5.4	5.1	5.1	4.9	5.5	5.5	5.6
t_{PZL}				5.1	4.5	4.5	3.3	5.5	5.5	5.6
t_{PHZ}	$\overline{OE}$	Y	MAX	4.6	5	5	4.9	6.3	6.3	5.5
t_{PLZ}				4.5	5	5	4.3	6.3	6.3	5.5

UNIT: ns

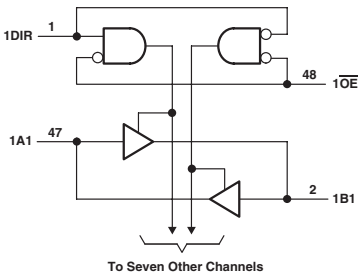
: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

162245

16-BIT TRANSCEIVER WITH 3-STATE OUTPUTS

- SN74ABT162245, SN74ABTH162245: A-Port Outputs Have Equivalent 25-Ω Series Resistors
- SN74LVT162245A, SN74LVTH162245: A-Port Outputs Have Equivalent 22-Ω Series Resistors
- SN74ALVTH162245: A-Port Outputs Have Equivalent 30-Ω Series Resistors
- SN74LVCR162245: All Outputs Have Equivalent 26-Ω Series Resistors

Logic Diagram



FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ABTH	LVT 3V	LVTH 3V	ALVTH 3V	UNIT
I_{CC}	MAX	32	32	5	5	5	mA
I_{OH} (A port)	MAX	-12	-12	-12	-12	-12	mA
I_{OH} (B port)	MAX	-32	-32	-32	-32	-32	mA
I_{OL} (A port)	MAX	12	12	12	12	12	mA
I_{OL} (B port)	MAX	64	64	64	64	64	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ABTH	LVT 3V	LVTH 3V	ALVTH 3V
t_{PLH}	A	B	MAX	3.9	3.9	3.3	3.3	3.1
t_{PHL}				4.2	4.2	3.3	3.3	3
t_{PLH}	B	A	MAX	4.6	4.6	4	4	3.7
t_{PHL}				5.1	5.1	3.4	3.4	3.4
t_{PZH}	$\overline{OE}$	B	MAX	6.3	6.3	4.6	4.6	3.8
t_{PZL}				6.4	6.4	4.6	4.6	3.4
t_{PHZ}	$\overline{OE}$	B	MAX	6.3	6.3	5.2	5.2	4.7
t_{PLZ}				5.2	5.2	5.1	5.1	4.8
t_{PZH}	$\overline{OE}$	A	MAX	7.1	7.1	5.3	5.3	4.7
t_{PZL}				7	7	5.1	5.1	3.9
t_{PHZ}	$\overline{OE}$	A	MAX	6.6	6.6	5.6	5.6	5
t_{PLZ}				5.7	5.7	5.5	5.5	4.9

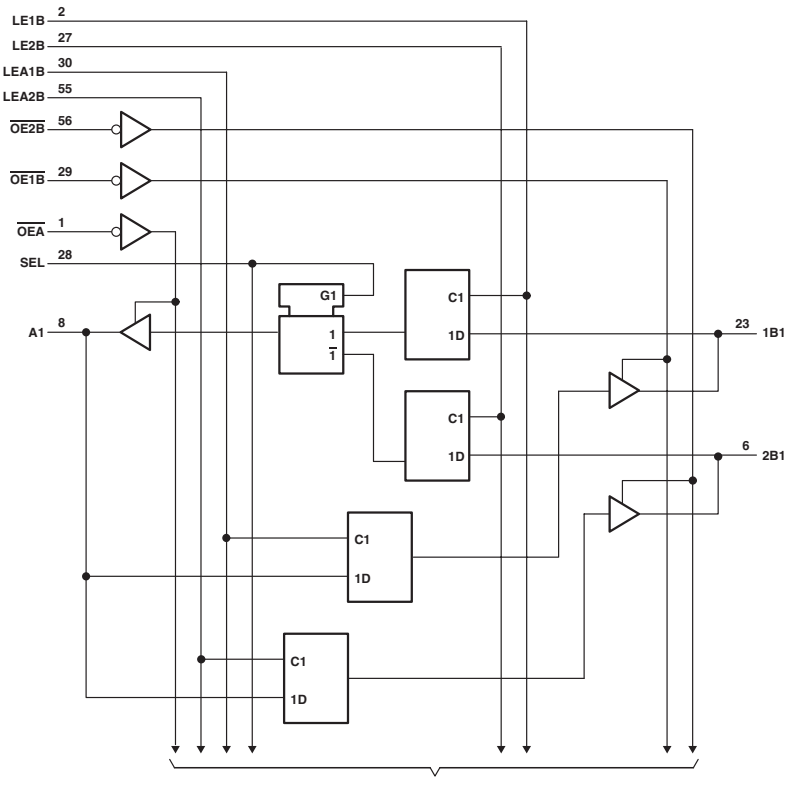
UNIT: ns

162260

12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCH WITH 3-STATE OUTPUTS

- SN74ABTH162260: B-Port Outputs Have Equivalent 25-Ω Series Resistors
- SN74ALVCH162260: B-Port Outputs Have Equivalent 26-Ω Series Resistors

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

B TO A ($\overline{OEB}$ = H)

INPUTS						OUTPUT
1B	2B	SEL	LE1B	LE2B	$\overline{OEA}$	A
H	X	H	H	X	L	H
L	X	H	H	X	L	L
X	X	H	L	X	L	A_0
X	H	L	X	H	L	H
X	L	L	X	H	L	L
X	X	L	X	L	L	A_0
X	X	X	X	X	H	Z

A TO B ($\overline{OEA}$ = H)

INPUTS					OUTPUTS	
A	LEA1B	LEA2B	$\overline{OE1B}$	$\overline{OE2B}$	1B	2B
H	H	H	L	L	H	H
L	H	H	L	L	L	L
H	H	L	L	L	H	$2B_0$
L	H	L	L	L	L	$2B_0$
H	L	H	L	L	$1B_0$	H
L	L	H	L	L	$1B_0$	L
X	L	L	L	L	$1B_0$	$2B_0$
X	X	X	H	H	Z	Z
X	X	X	L	H	Active	Z
X	X	X	H	L	Z	Active
X	X	X	L	L	Active	Active

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABTH	ALVCH 3V	UNIT
I_{CC}	MAX	63	0.04	mA
I_{OH} (A port)	MAX	-32	-24	mA
I_{OH} (B port)	MAX	-32	-12	mA
I_{OL} (A port)	MAX	64	24	mA
I_{OL} (B port)	MAX	12	12	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABTH	ALVCH 3V
f_{max}				-	150
t_w Pulse duration, LE1B, LE2B, LEA1B, or LEA2B high			MIN	3.3	3.3
t_{su} Setup time, data before LE1B, LE2B, LEA1B, or LEA2B ↓			MIN	1.5	1.1
t_h Hold time, data after LE1B, LE2B, LEA1B, or LEA2B ↓			MIN	1	1.5
t_{PLH}	A	B	MAX	6.1	4.9
t_{PHL}				7.1	4.9
t_{PLH}	B	A	MAX	6	4.3
t_{PHL}				6.2	4.3
t_{PLH}	LE	A	MAX	6.3	4.4
t_{PHL}				5.8	4.4
t_{PLH}	LE	B	MAX	6.1	5
t_{PHL}				7.1	5
t_{PLH}	SEL (1B)	A	MAX	5.6	5.6
	SEL (2B)			6.3	5.6
t_{PHL}	SEL (1B)		MAX	5	5.6
	SEL (2B)			6.2	5.6
t_{PZH}	$\overline{OE}$	A	MAX	6.3	5.4
t_{PZL}				6.5	5.4
t_{PZH}	$\overline{OE}$	B	MAX	6.3	6
t_{PZL}				8.2	6
t_{PHZ}	$\overline{OE}$	A	MAX	6.7	4.6
t_{PLZ}				5.2	4.6
t_{PHZ}	$\overline{OE}$	B	MAX	7.5	5.1
t_{PLZ}				6.2	5.1

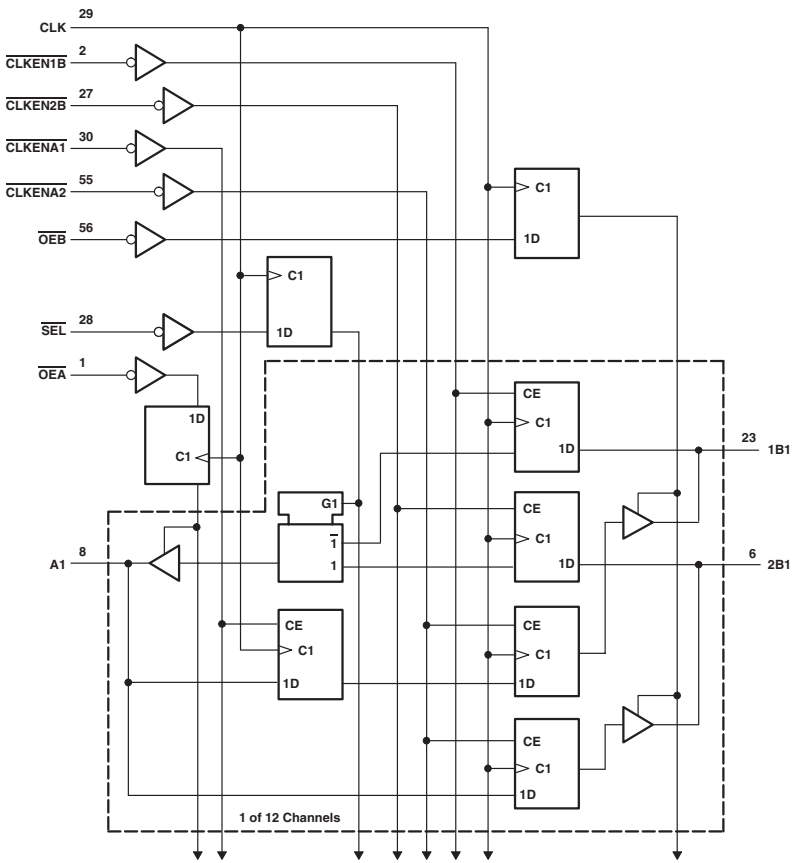
UNIT fmax : MHz other : ns

162268

12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

- SN74ALVCH162268: B-Port Outputs Have Equivalent 26-Ω Series Resistors

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

OUTPUT ENABLE

INPUTS			OUTPUTS	
CLK	$\overline{OEA}$	$\overline{OEB}$	A	1B, 2B
↑	H	H	Z	Z
↑	H	L	Z	Active
↑	L	H	Active	Z
↑	L	L	Active	Active

A-TO-B STORAGE ($\overline{OEB}$ = L)

INPUTS				OUTPUTS	
CLKENA1	CLKENA2	CLK	A	1B	2B
H	H	X	X	$1B_0$‡	$2B_0$‡
L	X	↑	L	L†	X
L	X	↑	H	H†	X
X	L	↑	L	X	L
X	L	↑	H	X	H

† Two CLK edges are needed to propagate data.
‡ Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE ($\overline{OEA}$ = L)

INPUTS						OUTPUT
CLKEN1B	CLKEN2B	CLK	SEL	1B	2B	A
H	X	X	H	X	X	A_0‡
X	H	X	L	X	X	A_0‡
L	X	↑	H	H	X	L
L	X	↑	H	L	X	H
X	L	↑	L	X	L	L
X	L	↑	L	X	H	H

‡ Output level before the indicated steady-state input conditions were established

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I_{CC}	MAX	0.04	mA
I_{OH} (A port)	MAX	-24	mA
I_{OH} (B port)	MAX	-12	mA
I_{OL} (A port)	MAX	24	mA
I_{OL} (B port)	MAX	12	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
f_{max}			MIN	150
t_w Pulse duration, CLK high or low			MIN	3.3
t_{su} Setup time	A data before CLK ↑		MIN	3.4
	B data before CLK ↑		MIN	1
	$\overline{SEL}$ before CLK ↑		MIN	1.3
	$\overline{CLKENA1}$ or $\overline{CLKENA2}$ before CLK ↑		MIN	2.8
	$\overline{CLKENB1}$ or $\overline{CLKENB2}$ before CLK ↑		MIN	2.5
	$\overline{OE}$ before CLK ↑		MIN	3.2
t_h Hold time	A data after CLK ↑		MIN	0.2
	B data after CLK ↑		MIN	1.3
	$\overline{SEL}$ after CLK ↑		MIN	1
	$\overline{CLKENA1}$ or $\overline{CLKENA2}$ after CLK ↑		MIN	0.4
	$\overline{CLKENB1}$ or $\overline{CLKENB2}$ after CLK ↑		MIN	0.5
	$\overline{OE}$ after CLK ↑		MIN	0.2
t_{pd}	CLK	B	MAX	5.4
		A (1B)		4.8
		A (2B)		4.8
		A (SEL)		5.8
t_{en}	CLK	B	MAX	6.1
		A		5.1
t_{dis}	CLK	B	MAX	5.9
		A		5

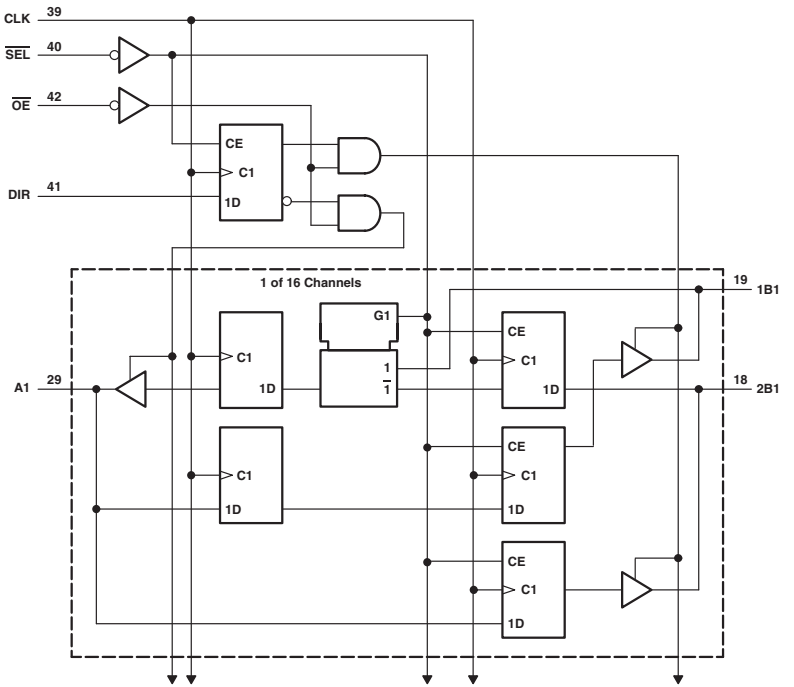
UNIT fmax : MHz other : ns

162280

16-BIT TO 32-BIT REGISTERED BUS EXCHANGER WITH BYTE MASKS AND 3-STATE OUTPUTS

- SN74ALVCHG162280: A-Port Outputs Have Equivalent 50-Ω Series Resistors
- B-Port Outputs Have Equivalent 20-Ω Series Resistors

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

A-TO-B STORAGE ($\overline{OE}$ = L, DIR = H)

INPUTS			OUTPUTS	
$\overline{SEL}$	CLK	A	1B	2B
H	X	X	$1B_0$†	$2B_0$†
L		L	L‡	X
L		H	H‡	X

† Output level before indicated steady-state input conditions were established
‡ Two CLK edges are needed to propagate the data.

B-TO-A STORAGE ($\overline{OE}$ = L, DIR = L)

INPUTS				OUTPUT
CLK	$\overline{SEL}$	1B	2B	A
↑	H	X	L	L§
↑	H	X	H	H§
↑	L	L	X	L
↑	L	H	X	H

§ Two CLK edges are needed to propagate the data. The data is loaded in the first register when $\overline{SEL}$ is low and propagates to the second register when $\overline{SEL}$ is high.

C-TO-D STORAGE ($\overline{OE}$ = L)

INPUTS			OUTPUT	
$\overline{SEL}$	CLK	C	1D	2D
H	X	X	$1B_0$†	$2B_0$†
L	↑	L	L‡	L
L	↑	H	H‡	H

† Output level before indicated steady-state input conditions were established
‡ Two CLK edges are needed to propagate the data.

OUTPUT ENABLE

INPUTS			OUTPUT		
CLK	$\overline{OE}$	DIR	A	1B, 2B	1D, 2D
↑	H	X	Z	Z	Z
↑	L	H	Z	Active	Active
↑	L	L	Active	Z	Active

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCHG 3V	UNIT
I_{CC}	MAX	0.04	mA
I_{OH} (A to B)	MAX	8	mA
I_{OH} (B to A)	MAX	6	mA
I_{OL} (A to B)	MAX	8	mA
I_{OL} (B to A)	MAX	6	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCHG 3V
f_{max}			MIN	160
t_w Pulse duration, CLK high or low			MIN	2.3
t_{su} Setup time	A data before CLK ↑, high or low		MIN	1.4
	B data before CLK ↑, high or low		MIN	2
	C data before CLK ↑, high or low		MIN	1.3
	DIR before CLK ↑, high or low		MIN	2
	$\overline{SEL}$ before CLK ↑, high or low		MIN	2
t_h Hold time	A data after CLK ↑, high or low		MIN	0.3
	B data after CLK ↑, high or low		MIN	0.3
	C data after CLK ↑, high or low		MIN	0.3
	DIR after CLK ↑, high or low		MIN	0.3
	$\overline{SEL}$ after CLK ↑, high or low		MIN	0.3
t_{pd}	CLK	A	MAX	5
		B		7.4
		D		7.2
t_{en}	CLK	A	MAX	6.2
		B		9.4
	$\overline{OE}$	A	MAX	6
		B		9.5
		D		7.9
t_{dis}	CLK	A	MAX	6.4
		B		7.8
	$\overline{OE}$	A	MAX	5
		B		7.6
		D		6.7

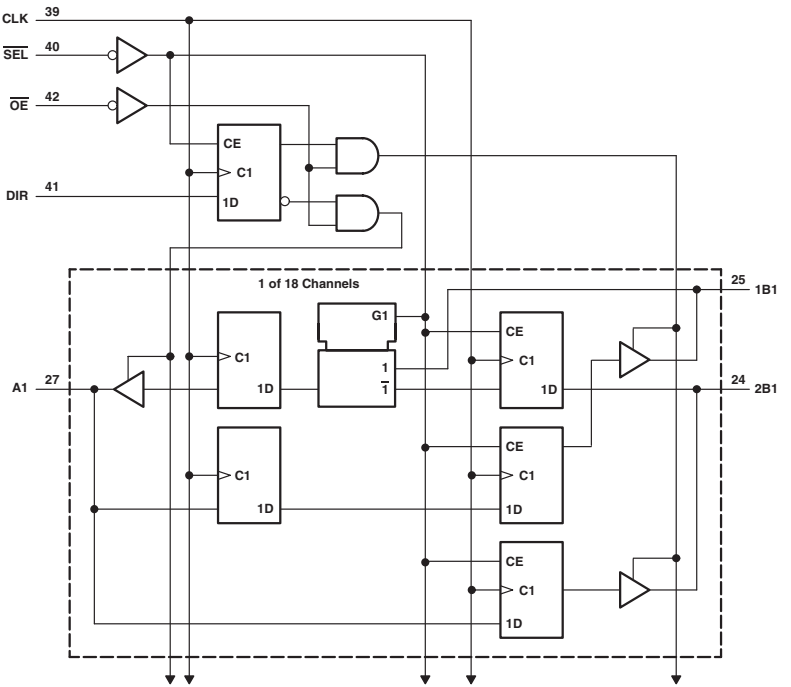
UNIT fmax : MHz other : ns

162282

18-BIT TO 36-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

- SN74ALVCHG162282: A-Port Outputs Have Equivalent 50-Ω Series Resistors
- B-Port Outputs Have Equivalent 20-Ω Series Resistors

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

A-TO-B STORAGE
($\overline{OE}$ = L, DIR = H)

INPUTS			OUTPUTS	
$\overline{SEL}$	CLK	A	1B	2B
H	X	X	$1B_0$†	$2B_0$†
L	↑	L	L‡	L
L	↑	H	H‡	H

† Output level before indicated steady-state input conditions were established
‡ Two CLK edges are needed to propagate the data.

B-TO-A STORAGE
($\overline{OE}$ = L, DIR = L)

INPUTS				OUTPUT
CLK	$\overline{SEL}$	1B	2B	A
↑	H	X	L	L§
↑	H	X	H	H§
↑	L	L	X	L
↑	L	H	X	H

§ Two CLK edges are needed to propagate the data. The data is loaded in the first register when $\overline{SEL}$ is low and proparates to the second register when $\overline{SEL}$ is high.

OUTPUT ENABLE

INPUTS			OUTPUTS	
CLK	$\overline{OE}$	DIR	A	1B, 2B
↑	H	X	Z	Z
↑	L	H	Z	Active
↑	L	L	Active	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCHG 3V	UNIT
I_{CC}	MAX	0.04	mA
I_{OH} (A to B)	MAX	8	mA
I_{OH} (B to A)	MAX	6	mA
I_{OL} (A to B)	MAX	8	mA
I_{OL} (B to A)	MAX	6	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCHG 3V
f_{max}			MIN	160
t_w Pulse duration, CLK high or low			MIN	2.3
t_{su} Setup time	A data before CLK ↑		MIN	1.5
	B data before CLK ↑		MIN	2
	DIR before CLK ↑		MIN	2
	$\overline{SEL}$ before CLK ↑		MIN	2
t_h Hold time	A data after CLK ↑		MIN	0.3
	B data after CLK ↑		MIN	0.3
	DIR after CLK ↑		MIN	0.3
	$\overline{SEL}$ after CLK ↑		MIN	0.3
t_{pd}	CLK	A	MAX	5
		B		7.4
t_{en}	CLK	A	MAX	6.3
		B		9.4
	$\overline{OE}$	A	MAX	6
		B		9.5
t_{dis}	CLK	A	MAX	6.4
		B		7.8
	$\overline{OE}$	A	MAX	5
		B		7.6

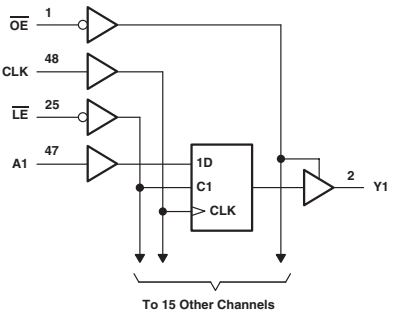
UNIT fmax : MHz other : ns

162334

16-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

- SN74ALVC162334: Output Ports Have Equivalent 26-Ω Series Resistors
- SN74ALVCH162334: Output Port Has Equivalent 26-Ω Series Resistors

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	$\overline{LE}$	CLK	A	Y
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	↑	L	L
L	H	↑	H	H
L	H	L or H	X	Y_0†

† Output level before the indicated steady-state input conditions were established

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVC 3V	ALVCH 3V	UNIT
I_{CC}	MAX	0.04	0.04	mA
I_{OH}	MAX	-12	-12	mA
I_{OL}	MAX	12	12	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVC 3V	ALVCH 3V
f_{max}			MIN	150	150
t_w Pulse duration	$\overline{LE}$ low			3.3	3.3
	CLK high or low		MIN	3.3	3.3
t_{su} Setup time	Data before CLK ↑		MIN	1.5	1.5
	Data before $\overline{LE}$ ↑ CLK high		MIN	1.3	1.3
	Data before $\overline{LE}$ ↑ CLK low		MIN	1.2	1.2
t_h Hold time	Data after CLK ↑		MIN	0.9	0.9
	Data after $\overline{LE}$ ↑ CLK high		MIN	1.1	1.1
	Data after $\overline{LE}$ ↑ CLK low		MIN	1.1	1.1
t_{pd}	A	Y	MAX	3.9	3.9
	$\overline{LE}$			5	5
	CLK		MAX	4.9	4.9
t_{en}	$\overline{OE}$	Y		5.4	5.4
t_{dis}	$\overline{OE}$	Y	MAX	5	5

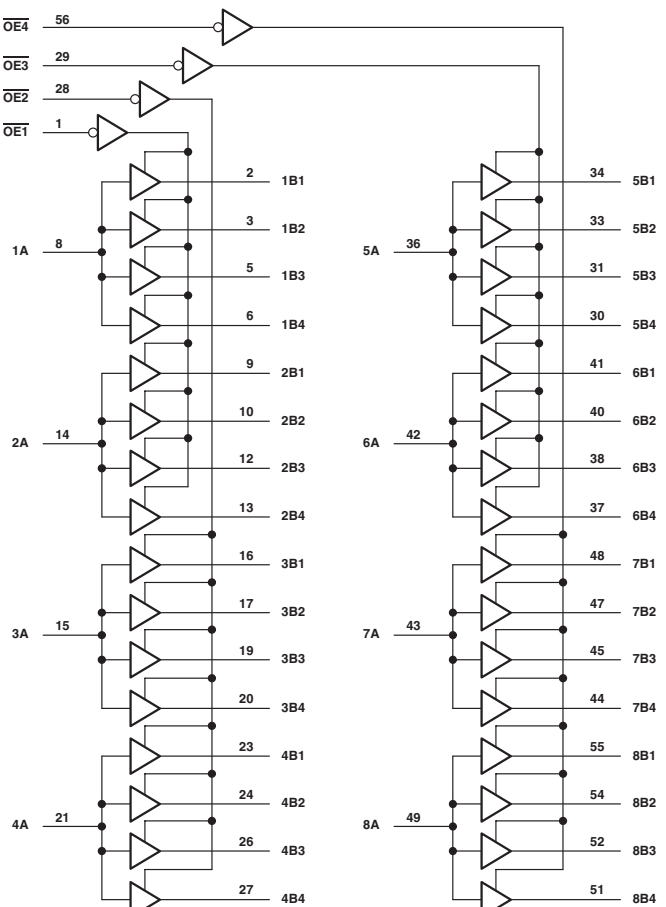
UNIT fmax : MHz other : ns

162344

1-BIT TO 4-BIT ADDRESS DRIVER WITH 3-STATE OUTPUTS

- SN74ALVCH162344: Output Ports Have Equivalent 26-Ω Series Resistors

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS		OUTPUT
$\overline{OE}$	A	Bn
L	H	H
L	L	L
H	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I_{CC}	MAX	0.04	mA
I_{OH}	MAX	-12	mA
I_{OL}	MAX	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
t_{PLH}	A	B	MAX	4.4
t_{PHL}				4.4
t_{PZH}	$\overline{OE}$	B	MAX	5.7
t_{PZL}				5.7
t_{PHZ}	$\overline{OE}$	B	MAX	4.5
t_{PLZ}				4.5

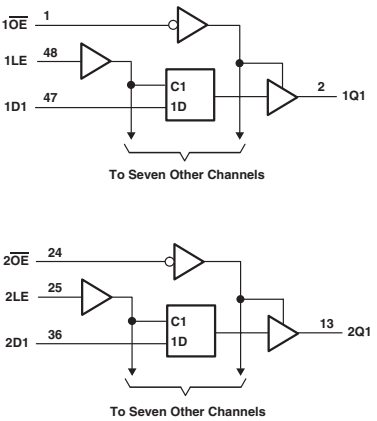
UNIT: ns

162373

3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

- SN74LVTH162373: Output Ports Have Equivalent 22-Ω Series Resistors

Logic Diagram



FUNCTION TABLE
(each 8-bit section)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVTH 3V	ALVCH 3V	UNIT
I_{CC}	MAX	5	0.04	mA
I_{OH}	MAX	-12	-12	mA
I_{OL}	MAX	12	12	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTH 3V	ALVC 3V
t_w Pulse duration, LE high or low			MIN	3	3.3
t_{su} Setup time	Data before LE↓, data high		MIN	1	1.1
	Data before LE↓, data low		MIN	1	1.1
t_h Hold time	Data after LE↓, data high		MIN	1	1.1
	Data after LE↓, data low		MIN	1	1.1
t_{PLH}	D	Q	MAX	4.6	4
t_{PHL}				4	4
t_{PLH}	LE	Q	MAX	5.1	4.2
t_{PHL}				4.6	4.2
t_{PZH}	$\overline{OE}$	Q	MAX	5.4	5
t_{PZL}				4.9	5
t_{PHZ}	$\overline{OE}$	Q	MAX	5.4	4.5
t_{PLZ}				5.1	4.5

UNIT: ns

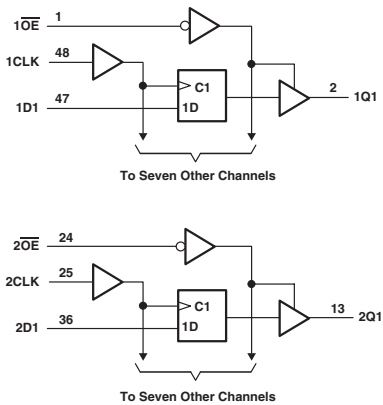
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

162374

3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

- SN74LVTH162374: Output Ports Have Equivalent 22-Ω Series Resistors
- SN74ALVCH162374: Output Ports Have Equivalent 26-Ω Series Resistors

Logic Diagram



FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVTH 3V	ALVCH 3V	UNIT
I_{CC}	MAX	5	0.04	mA
I_{OH}	MAX	-12	-12	mA
I_{OL}	MAX	12	12	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTH 3V	ALVCH 3V
f_{max}				160	150
t_w Pulse duration, CLK high or low			MIN	3	3.3
t_{su} Setup time	Data before CLK ↑, data high		MIN	1.8	1.9
	Data before CLK ↑, data low		MIN	1.8	1.9
t_h Hold time	Data after CLK ↑, data high		MIN	0.8	0.5
	Data after CLK ↑, data low		MIN	0.8	0.5
t_{PLH}	CLK	Q	MAX	5.3	4.6
t_{PHL}				4.9	4.6
t_{PZH}	$\overline{OE}$	Q	MAX	5.6	5.2
t_{PZL}				4.9	5.2
t_{PHZ}	$\overline{OE}$	Q	MAX	5.4	4.5
t_{PLZ}				5	4.5

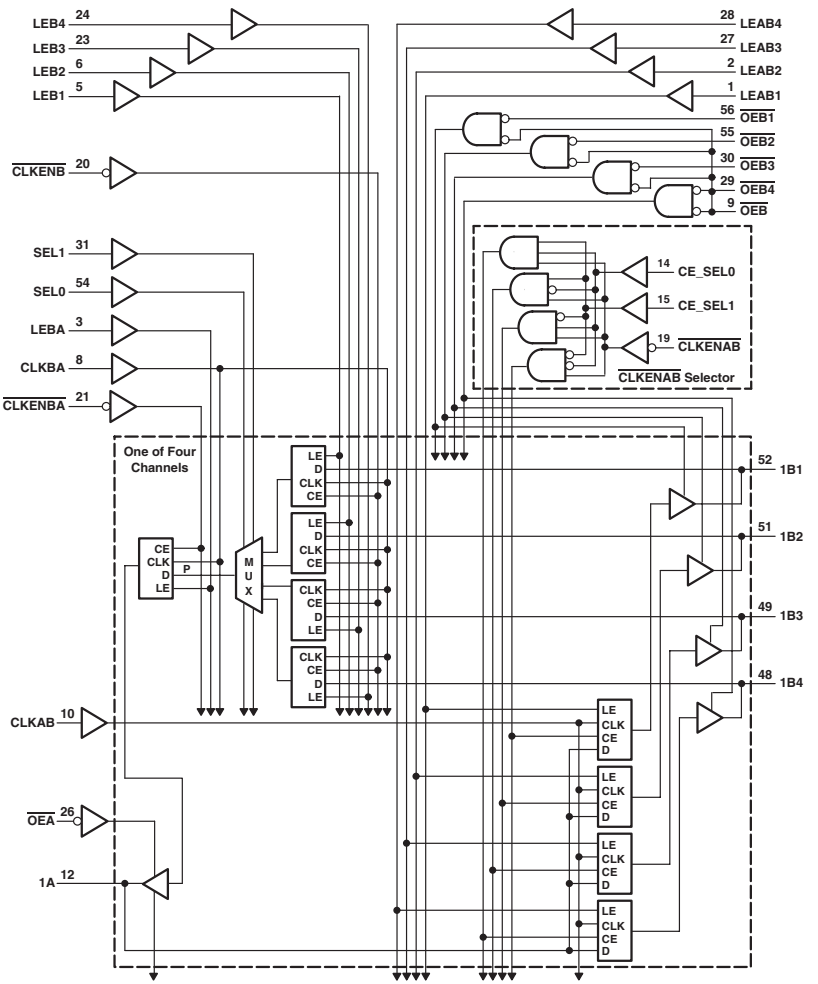
UNIT fmax : MHz other : ns

162460

4-TO-1 MULTIPLEXED/DEMULTIPLEXED REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

- SN74ABTH162460: B-Port Outputs Have Equivalent 25-Ω Series Resistors

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

A-TO-B OUTPUT ENABLE

INPUTS		OUTPUT
$\overline{OEB}$	$\overline{OEBn}$	Bn
H	H	Z
H	L	Z
L	H	Z
L	L	Active

†n = 1, 2, 3, 4

A-TO-B STORAGE
(assuming $\overline{OEB}$ = L, $\overline{OEBn}$ = L)

INPUTS								OUTPUTS			
$\overline{CLKENAB}$	CE_SEL1	CE_SEL0	CLKAB	LEAB1	LEAB2	LEAB3	LEAB4	B1	B2	B3	B4
X	X	X	H or L	H	L	L	L	A	A_0	A_0	A_0
X	X	X	H or L	H	H	H	L	A	A	A	A_0
L	X	X	L	L	L	L	L	A_0	A_0	A_0	A_0
L	L	L	↑	L	L	L	L	A	A_0	A_0	A_0
L	L	H	↑	L	L	L	L	A_0	A	A_0	A_0
L	H	L	↑	L	L	L	L	A_0	A_0	A	A_0
L	H	H	↑	L	L	L	L	A_0	A_0	A_0	A
H	X	X	↑	L	L	L	L	A_0	A_0	A_0	A_0

B-TO-A STORAGE
(after point P)

INPUTS								P
$\overline{CLKENB}$	CLKBA	LEB1	LEB2	LEB3	LEB4	SEL1	SEL0	
X	X	H	L	L	L	L	L	B1
X	X	L	H	L	L	L	H	B2
X	X	L	L	H	L	H	L	B3
X	X	L	L	L	H	H	H	B4
L	↑	L	L	L	L	L	L	B1
						L	H	B2
						H	L	B3
						H	H	B4
L	L	L	L	L	L	L	L	$B1_0$†
						L	H	$B2_0$†
						H	L	$B3_0$†
						H	H	$B4_0$†

† Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE
(after point P)

INPUTS					OUTPUT
$\overline{CLKENBA}$	CLKBA	LEBA	$\overline{OEA}$	B	A
X	X	X	H	X	X
X	X	H	L	L	L
X	X	H	L	H	H
H	X	L	L	X	A_0†
L	↑	L	L	L	L
L	↑	L	L	H	H
L	L	L	L	X	A_0†

ELECTRICAL CHARACTERISTICS AND
RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABTH	UNIT
I_{CC}	MAX	32	mA
I_{OH} (A port)	MAX	-32	mA
I_{OH} (B port)	MAX	-12	mA
I_{OL} (A port)	MAX	64	mA
I_{OL} (B port)	MAX	12	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER			MAX or MIN	ABTH
f_{max}			MIN	160
t_w Pulse duration	CLKAB high or low		MIN	3.8
	CLKBA high or low		MIN	4.5
	LEAB1, 2, 3 or 4 high		MIN	2.8
	LEBA high		MIN	2.8
	LEB1, 2, 3 or 4 high		MIN	3
t_{su} Setup time	Before CLKAB ↑	A bus	MIN	2.5
		CE_SEL0/1	MIN	3.2
		$\overline{CLKENAB}$	MIN	3.2
	Before LEAB1, 2, 3, or 4 ↓ A bus		MIN	3.6
	Before CLKBA ↑	B bus	MIN	3.8
		$\overline{CLKENB}$	MIN	2.3
		$\overline{CLKENBA}$	MIN	2.5
		LEB1, 2, 3 or 4	MIN	4.3
		SEL0/1	MIN	4.5
	Before LEB1, 2, 3, or 4 ↓ B bus		MIN	3.2
	Before CLKBA ↑	B bus	MIN	4
		LEB1, 2, 3 or 4	MIN	4.4
		SEL0/1	MIN	4.3
t_h Hold time	after CLKAB ↑	A bus	MIN	0.5
		CE_SEL0/1	MIN	1.1
		$\overline{CLKENAB}$	MIN	0.5
	after LEAB1, 2, 3, or 4 ↓ A bus		MIN	1.2
	after CLKBA ↑	B bus	MIN	1.3
		$\overline{CLKENB}$	MIN	1
		$\overline{CLKENBA}$	MIN	1
		SEL0/1	MIN	0
	after LEB1, 2, 3, or 4 ↓ B bus		MIN	1.5
	after CLKBA ↑	B bus	MIN	0.4
		SEL0/1	MIN	0.1

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABTH
t_{PLH}	B	A	MAX	6.5
t_{PHL}				6.5
t_{PZH}	$\overline{OEA}$	A	MAX	5.6
t_{PZL}				5.5
t_{PHZ}	$\overline{OEA}$	A	MAX	5.9
t_{PLZ}				6.5
t_{PLH}	A	B	MAX	6.2
t_{PHL}				6.5
t_{PZH}	$\overline{OEB}$	B	MAX	6.8
t_{PZL}				6.3
t_{PHZ}	$\overline{OEB}$	B	MAX	6.2
t_{PLZ}				5.8
t_{PZH}	$\overline{OEB1}$, $\overline{2}$, $\overline{3}$, $\overline{4}$	B	MAX	6.6
t_{PZL}				6.2
t_{PHZ}	$\overline{OEB1}$, $\overline{2}$, $\overline{3}$, $\overline{4}$	B	MAX	5.3
t_{PLZ}				4.9
t_{PLH}	CLKBA	A	MAX	7.4
t_{PHL}				7.7
t_{PLH}	CLKAB	B	MAX	6.5
t_{PHL}				6.5
t_{PLH}	LEBA	A	MAX	5.8
t_{PHL}				5.8
t_{PLH}	LEAB1, 2, 3, 4	B	MAX	6.2
t_{PHL}				6.2
t_{PLH}	LEBA1, 2, 3, 4	A	MAX	7.2
t_{PHL}				6.8
t_{PLH}	SEL	A	MAX	7.5
t_{PHL}				6.9

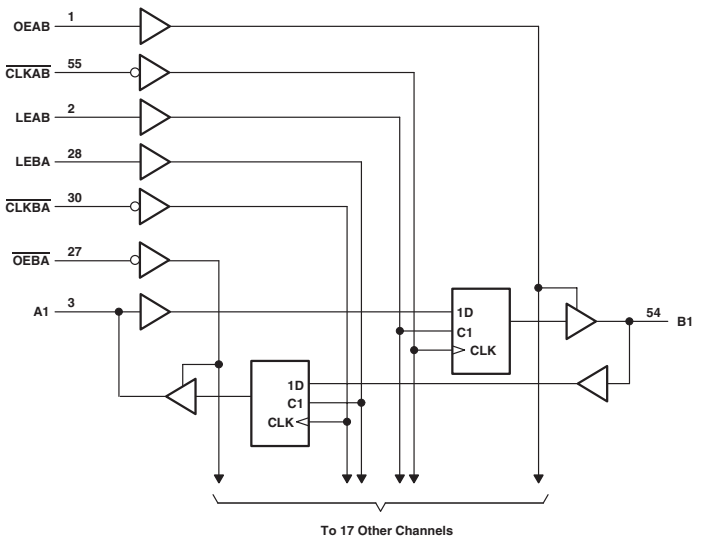
UNIT fmax : MHz other : ns

162500

18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

- SN74ABT162500: B-Port Outputs Have Equivalent 25-Ω Series Resistors

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS				OUTPUT
OEAB	LEAB	$\overline{CLKAB}$	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B_0‡
H	L	L	X	B_0§

‡ Output level before the indicated steady-state input conditions were established.
§ Output level before the indicated steady-state input conditions were established, provided that $\overline{CLKAB}$ was low before LEAB went low.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	UNIT
I_{CC}	MAX	36	mA
I_{OH} (A port)	MAX	-32	mA
I_{OH} (B port)	MAX	-12	mA
I_{OL} (A port)	MAX	64	mA
I_{OL} (B port)	MAX	12	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

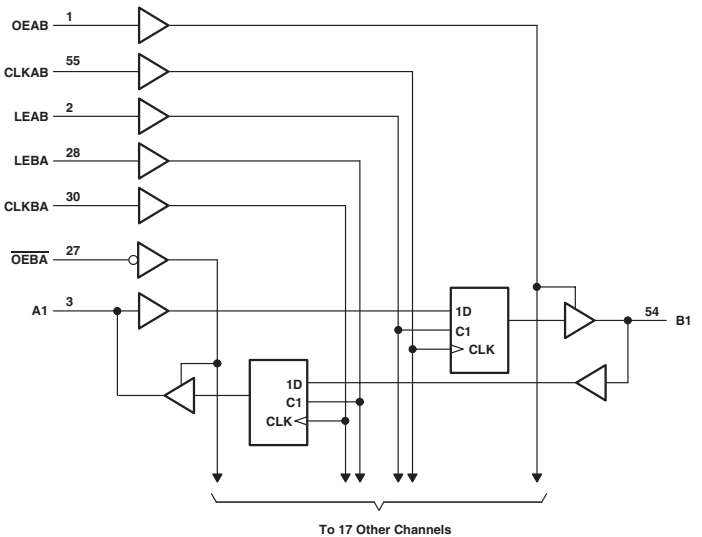
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT
f_{max}			MIN	150
t_w Pulse duration	LEAB or LEBA high		MIN	2.5
	$\overline{CLKAB}$ or $\overline{CLKBA}$ high or low		MIN	3
t_{su} Setup time	A before $\overline{CLKAB}$ ↓		MIN	3.3
	B before $\overline{CLKBA}$ ↓		MIN	3.3
	A before LEAB ↓ or LEBA ↓ $\overline{CLK}$ high		MIN	1
	A before LEAB ↓ or LEBA ↓ $\overline{CLK}$ low		MIN	2.5
t_h Hold time	A after $\overline{CLKAB}$ ↓ or B after $\overline{CLKBA}$ ↓		MIN	0
	A after LEAB ↓ or B after LEBA ↓		MIN	2
t_{PLH}	A or B	B or A	MAX	4.8
t_{PHL}				5.7
t_{PZH}	LEAB or LEBA	B or A	MAX	5.6
t_{PZL}				5.9
t_{PHZ}	$\overline{CLKAB}$ or $\overline{CLKBA}$	B or A	MAX	5.9
t_{PLZ}				6
t_{PZH}	OEAB	B	MAX	5.3
t_{PZL}				5.4
t_{PHZ}	OEAB	B	MAX	6.5
t_{PLZ}				5.8
t_{PZH}	$\overline{OEBA}$	A	MAX	5.3
t_{PZL}				5.4
t_{PHZ}	$\overline{OEBA}$	A	MAX	6.5
t_{PLZ}				5.8

UNIT fmax : MHz other : ns

18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- SN74ABT162501: B-Port Outputs Have Equivalent 25-Ω Series Resistors

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE†

INPUTS				OUTPUT
OEAB	LEAB	CLKAB	A	Y
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	H	X	B_0‡
H	L	L	X	B_0§

† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, and CLKBA

‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low

§ Outoput level before the indicated steady-state input conditions were established

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	UNIT
I_{CC}	MAX	36	mA
I_{OH} (A port)	MAX	-32	mA
I_{OH} (B port)	MAX	-12	mA
I_{OL} (A port)	MAX	64	mA
I_{OL} (B port)	MAX	12	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT
f_{max}			MIN	150
t_w Pulse duration	LEAB or LEBA high		MIN	3
	CLKAB or CLKBA high or low		MIN	3.3
t_{su} Setup time	A before CLKAB ↑		MIN	4.3
	B before CLKBA ↑		MIN	4.3
	A before LEAB ↓ or LEBA ↓ CLK high		MIN	2.5
	A before LEAB ↓ or LEBA ↓ CLK low		MIN	1
t_h Hold time	A after CLKAB ↑ or B after CLKBA ↑		MIN	0
	A after LEAB ↓ or B after LEBA ↓		MIN	2
t_{PLH}	A or B	B or A	MAX	4.8
t_{PHL}				5.7
t_{PZH}	LEAB or LEBA	B or A	MAX	5.6
t_{PZL}				5.9
t_{PHZ}	CLKAB or CLKBA	B or A	MAX	5.5
t_{PLZ}				5.3
t_{PZH}	OEAB	B	MAX	5.3
t_{PZL}				5.4
t_{PHZ}	OEAB	B	MAX	6.5
t_{PLZ}				5.8
t_{PZH}	$\overline{OEBA}$	A	MAX	5.3
t_{PZL}				5.4
t_{PHZ}	$\overline{OEBA}$	A	MAX	6.5
t_{PLZ}				5.8

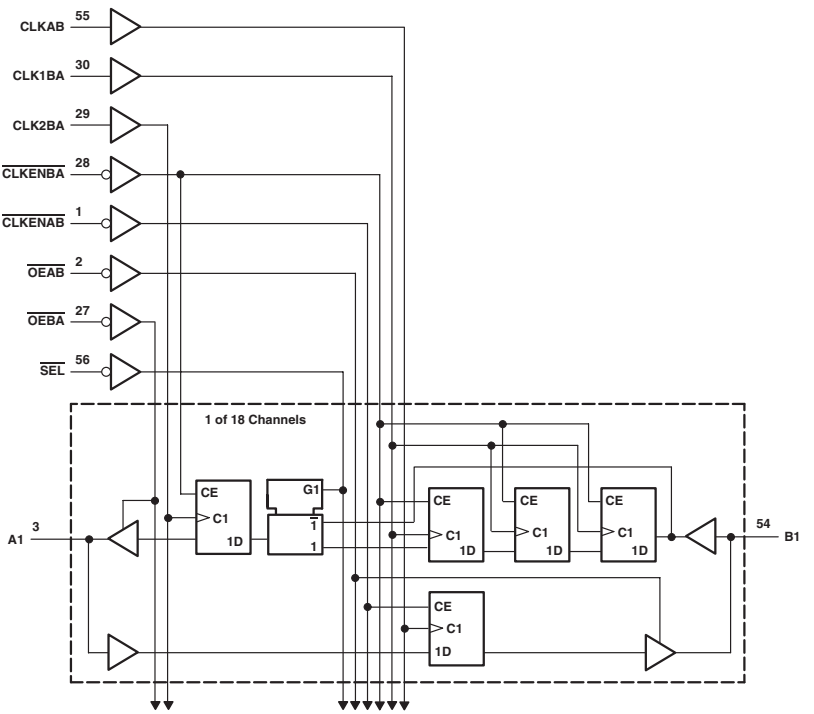
UNIT fmax : MHz other : ns

162525

18-BIT REGISTERED BUS TRANSCEIVER WITH 3-STATE OUTPUTS

- SN74ALVCH162525: B-Port Outputs Have Equivalent 26-Ω Series Resistors

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

A-TO-B STORAGE($\overline{OEAB}$ = L)

INPUTS			OUTPUT
CLKNAB	OLKAB	A	B
H	X	X	B_0†
L	↑	L	L
L	↑	H	H

† Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE ($\overline{OEBA}$ = L)

INPUTS					OUTPUT
$\overline{CLKENBA}$	$\overline{CLK2BA}$	CLK1BA	SEL	B	A
H	X	X	X	X	A_0†
L	↑	X	H	L	L
L	↑	X	H	H	H
L	↑	↑	L	L	L‡
L	↑	↑	L	H	H‡

† Output level before the indicated steady-state input conditions were established

‡ Three CLK1BA edges and one $\overline{CLK2BA}$ edge are needed to propagate data from B to A when $\overline{SEL}$ is low.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I_{CC}	MAX	0.04	mA
I_{OH} (A port)	MAX	-24	mA
I_{OH} (B port)	MAX	-12	mA
I_{OL} (A port)	MAX	24	mA
I_{OL} (B port)	MAX	12	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
f_{max}			MIN	150
t_w Pulse duration, CLK high or low			MIN	3
t_{su} Setup time	A data before CLKAB ↑		MIN	1.3
	B data before CLK2BA ↑		MIN	1.7
	B data before CLK1BA ↑		MIN	1.1
	$\overline{SEL}$ before CLK2BA ↑		MIN	3.3
	$\overline{CLKENAB}$ before CLKAB ↑		MIN	1.6
	$\overline{CLKENBA}$ before CLK1BA ↑		MIN	2.1
	$\overline{CLKENBA}$ before CLK2BA ↑		MIN	2.2
t_h Hold time	A data after CLKAB ↑		MIN	0.9
	B data after CLK2BA ↑		MIN	0.6
	B data after CLK1BA ↑		MIN	1
	$\overline{SEL}$ after CLK2BA ↑		MIN	0.1
	$\overline{CLKENAB}$ after CLKAB ↑		MIN	0.3
	$\overline{CLKENBA}$ after CLK1BA ↑		MIN	0.1
	$\overline{CLKENBA}$ after CLK2BA ↑		MIN	0
t_{pd}	CLKAB	B	MAX	4.7
	CLK2BA	A		4.2
t_{en}	$\overline{OEBA}$	A	MAX	5.1
	$\overline{OEAB}$	B		5.7
t_{dis}	$\overline{OEBA}$	A	MAX	4.9
	$\overline{OEAB}$	B		4.9

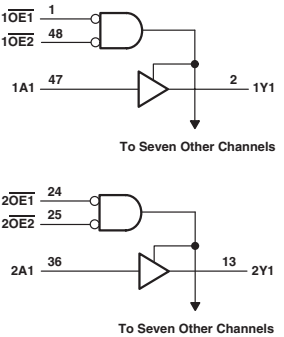
UNIT fmax : MHz other : ns

162541

3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- SN74LVTH162541: Output Ports Have Equivalent 22-Ω Series Resistors

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE
(each 8-bit section)

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVTH 3V	UNIT
I_{CC}	MAX	5	mA
I_{OH}	MAX	-12	mA
I_{OL}	MAX	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTH 3V
t_{PLH}	A	Y	MAX	4.1
t_{PHL}				4.1
t_{PZH}	$\overline{OE}$	Y	MAX	5
t_{PZL}				4.8
t_{PHZ}	$\overline{OE}$	Y	MAX	5.9
t_{PLZ}				5.4

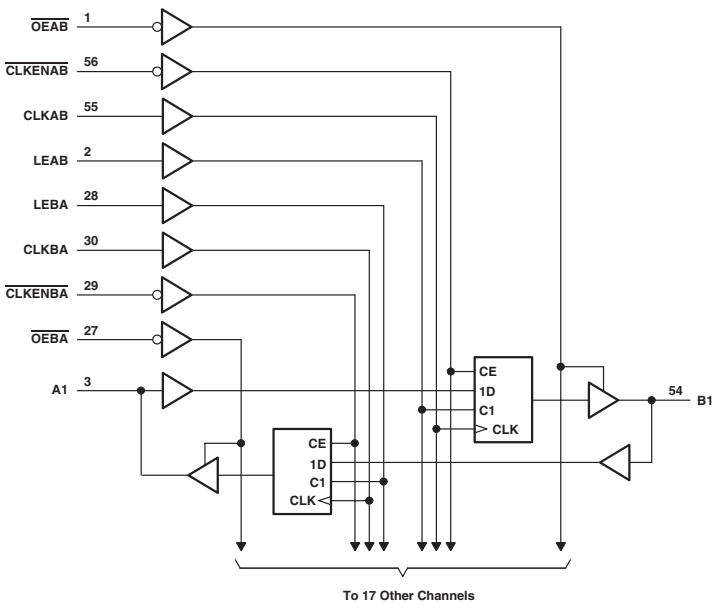
UNIT: ns

162601

18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

- SN74ABT162601: B-Port Outputs Have Equivalent 25-Ω Series Resistors
- SN74ALVCH162601: B-Port Outputs Have Equivalent 26-Ω Series Resistors

Logic Diagram



: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

FUNCTION TABLE

INPUTS					OUTPUT
CLKENAB	$\overline{OEAB}$	$\overline{LEAB}$	CLKAB	A	B
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B_0‡
H	L	L	X	X	B_0†
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L	X	B_0‡
L	L	L	H	X	B_0§

† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CLKENBA}$.
‡ Output level before the indicated steady-state input conditions were established.
§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ALVCH 3V	UNIT
I_{CC}	MAX	36	0.04	mA
I_{OH} (A port)	MAX	-32	-24	mA
I_{OH} (B port)	MAX	-12	-12	mA
I_{OL} (A port)	MAX	64	24	mA
I_{OL} (B port)	MAX	12	12	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ALVCH 3V
f_{max}			MIN	150	150
t_w Pulse duration	LEAB or LEBA high		MIN	2.5	3.3
	CLKAB or CLKBA high or low		MIN	3	3.3
t_{su} Setup time	Data before CLK ↑		MIN	4.3	2.1
	A before LEAB ↓ or B before LEBA ↓ , CLK high		MIN	2.5	1.6
	A before LEAB ↓ or B before LEBA ↓ , CLK low		MIN	1	1.1
	$\overline{CLKEN}$ before ↑		MIN	2.7	1.7
t_h Hold time	Data after CLK ↑		MIN	0	0.8
	A after LEAB ↓ or B after LEBA ↓ , CLK high		MIN	0.5	1.4
	A after LEAB ↓ or B after LEBA ↓ , CLK low		MIN	0.5	1.7
	$\overline{CLKEN}$ after ↑		MIN	0	0.6
t_{PLH}	A	B	MAX	4.8	4.5
t_{PHL}				5.7	4.5
t_{PLH}	B	A	MAX	4	4.1
t_{PHL}				4.9	4.1
t_{PLH}	LEBA	A	MAX	5	4.7
t_{PHL}				5	4.7
t_{PLH}	LEAB	B	MAX	5.6	5.1
t_{PHL}				5.9	5.1
t_{PLH}	CLKBA	A	MAX	5.3	5
t_{PHL}				5	5
t_{PLH}	CLKAB	B	MAX	5.5	5.5
t_{PHL}				5.3	5.5
t_{PZH}	$\overline{OEBA}$	A	MAX	5.1	5.2
t_{PZL}				5.4	5.2
t_{PZH}	$\overline{OEAB}$	B	MAX	6.1	5.7
t_{PZL}				5.7	5.7
t_{PHZ}	$\overline{OEBA}$	A	MAX	6.2	4.4
t_{PLZ}				5.4	4.4
t_{PHZ}	$\overline{OEAB}$	B	MAX	5.4	4.8
t_{PLZ}				5.2	4.8

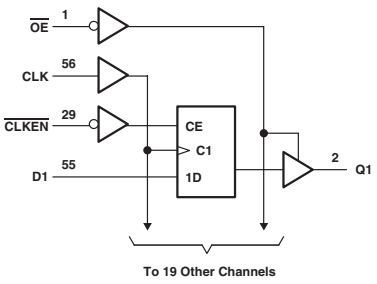
UNIT fmax : MHz other : ns

162721

3.3-V 20-BIT FLIP-FLOP WITH 3-STATE OUTPUTS

- SN74ALVCH162721: Output Ports Have Equivalent 26-Ω Series Resistors

Logic Diagram



FUNCTION TABLE
(each flip-flop)

INPUTS				OUTPUT
$\overline{OE}$	$\overline{CLKEN}$	CLK	D	Q
L	H	X	X	Q_0
L	L	↑	H	H
L	L	↑	L	L
L	L	L or H	X	Q_0
H	X	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I_{CC}	MAX	0.04	mA
I_{OH}	MAX	-12	mA
I_{OL}	MAX	12	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
f_{max}			MIN	150
t_w Pulse duration	CLK high or low		MIN	3.3
t_{su} Setup time	Data before CLK ↑		MIN	3.1
	$\overline{CLKEN}$ before CLK ↑		MIN	2.7
t_h Hold time	Data after CLK ↑		MIN	0
	$\overline{CLKEN}$ after CLK ↑		MIN	0
t_{PLH}	CLK	Q	MAX	5.3
t_{PHL}				5.3
t_{PZH}	OE	Q	MAX	5.8
t_{PZL}				5.8
t_{PHZ}	OE	Q	MAX	5
t_{PLZ}				5

UNIT fmax : MHz other : ns

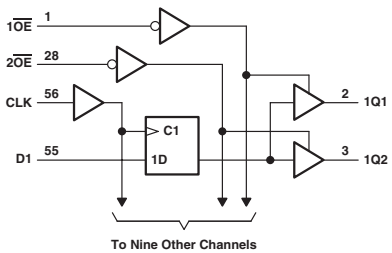
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

162820

3.3-V 10-BIT FLIP-FLOP WITH DUAL OUTPUTS AND 3-STATE OUTPUTS

- SN74ALVCH162820: Output Ports Have Equivalent 26-Ω Series Resistors

Logic Diagram



FUNCTION TABLE
(each flip flop)

INPUTS			OUTPUT
$\overline{OE}n$†	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

† n = 1,2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I_{CC}	MAX	0.04	mA
I_{OH}	MAX	-12	mA
I_{OL}	MAX	12	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
f_{max}			MIN	150
t_w Pulse duration	CLK high or low		MIN	3.3
t_{su} Setup time	Data before CLK ↑		MIN	1.4
t_h Hold time	Data after CLK ↑		MIN	1
t_{PLH}	CLK	Q	MAX	5.4
t_{PHL}				5.4
t_{PZH}	$\overline{OE}$	Q	MAX	5.6
t_{PZL}				5.6
t_{PHZ}	$\overline{OE}$	Q	MAX	5
t_{PLZ}				5

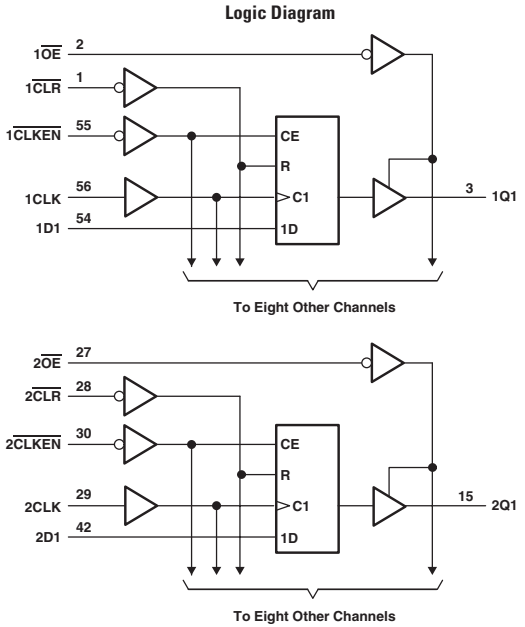
UNIT fmax : MHz other : ns

162823

18-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

- SN74ABT162823A: Output Ports Have Equivalent 25-Ω Series Resistors

Logic Diagram



FUNCTION TABLE

INPUTS					OUTPUT
$\overline{OE}$	$\overline{CLR}$	$\overline{CLENK}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	L	L	X	Q_0
L	H	H	X	X	Q_0
H	X	X	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	UNIT
I_{CC}	MAX	80	mA
I_{OH}	MAX	-12	mA
I_{OL}	MAX	12	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT
f_{max}			MIN	150
t_w Pulse duration	$\overline{CLR}$ low		MIN	3.3
	CLK high or low		MIN	3.3
t_{su} Setup time	$\overline{CLR}$ inactive		MIN	1.6
	Data before CLK ↑		MIN	2
	$\overline{CLKEN}$ low before CLK ↑		MIN	2.8
t_h Hold time	Data after CLK ↑		MIN	1.2
	$\overline{CLKEN}$ low after CLK ↑		MIN	0.6
t_{PLH}	CLK	Q	MAX	7.5
t_{PHL}				6.7
t_{PHL}	$\overline{CLR}$	Q	MAX	7
t_{PZH}	$\overline{OE}$	Q	MAX	5.9
t_{PZL}				7
t_{PHZ}	$\overline{OE}$	Q	MAX	6.6
t_{PLZ}				9

UNIT fmax : MHz other : ns

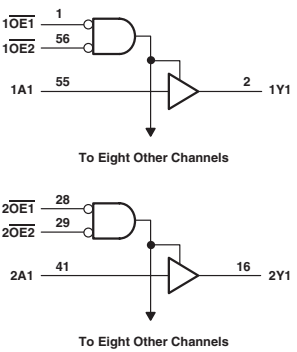
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

162825

18-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- SN74ABT162825: Output Ports Have Equivalent 25-Ω Series Resistors

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	UNIT
I_{CC}	MAX	32	mA
I_{OH}	MAX	-12	mA
I_{OL}	MAX	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT
t_{PLH}	A	Y	MAX	3.9
t_{PHL}				4.7
t_{PZH}	$\overline{OE}$	Y	MAX	6.9
t_{PZL}				6.3
t_{PHZ}	$\overline{OE}$	Y	MAX	6.6
t_{PLZ}				6.3

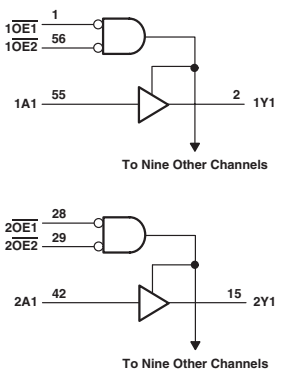
UNIT: ns

162827

20-BIT BUS BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- SN74ABT162827A: Output Ports Have Equivalent 25-Ω Series Resistors
- SN74ALVTH162827: Output Ports Have Equivalent 30-Ω Series Resistors
- SN74ALVCH162827: Output Ports Have Equivalent 26-Ω Series Resistors

Logic Diagram



FUNCTION TABLE
(each flip flop)

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ALVTH 3V	ALVCH 3V	UNIT
I_{CC}	MAX	32	5.5	0.04	mA
I_{OH}	MAX	-12	-12	-12	mA
I_{OL}	MAX	12	12	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ALVTH 3V	ALVCH 3V
t_{PLH}	A	Y	MAX	3.9	3.9	3.8
t_{PHL}				4.7	3.7	3.8
t_{PZH}	$\overline{OE}$	Y	MAX	6.9	5.6	5.1
t_{PZL}				6.3	4.1	5.1
t_{PHZ}	$\overline{OE}$	Y	MAX	6.6	6.3	4.7
t_{PLZ}				6.3	5.1	4.7

UNIT: ns

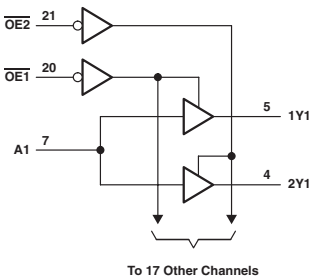
: **OBSOLETED or NOT RECOMMENDED NEW DESIGNS**

162830

1-BIT TO 2-BIT ADDRESS DRIVER WITH 3-STATE OUTPUTS

- SN74ALVCH162830, SN74ALVCHS162830: Output Ports Have Equivalent 26-Ω Series Resistors

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{OE1}$	$\overline{OE2}$	A	1Yn	2Yn
L	H	H	H	Z
L	H	L	L	Z
H	L	H	Z	H
H	L	L	Z	L
L	L	H	H	H
L	L	L	L	L
H	H	X	Z	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	ALVCHS 3V	UNIT
I_{CC}	MAX	0.04	0.04	mA
I_{OH}	MAX	-12	-12	mA
I_{OL}	MAX	12	12	mA

SWITCHING CHARACTERISTICS

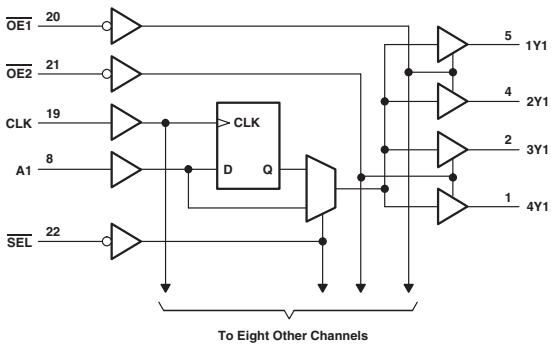
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V	ALVCHS 3V
t_{PLH}	A	Y	MAX	3.5	3.5
t_{PHL}				3.5	3.5
t_{PZH}	$\overline{OE}$	Y	MAX	4.8	4.8
t_{PZL}				4.8	4.8
t_{PHZ}	$\overline{OE}$	Y	MAX	5.2	5.2
t_{PLZ}				5.2	5.2

UNIT: ns

162831

1-BIT TO 4-BIT ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS

● SN74ALVC162831, SN74ALVCH162831: Output Ports Have Equivalent 26-Ω Series Resistors



FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	$\overline{SEL}$	CLK	A	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVC 3V	ALVCH 3V	UNIT
I_{CC}	MAX	0.04	0.04	mA
I_{OH}	MAX	-12	-12	mA
I_{OL}	MAX	12	12	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVC 3V	ALVCH 3V
f_{max}			MIN	150	150
t_w Pulse duration	CLK high or low		MIN	3.3	3.3
t_{su} Setup time	A data before CLK ↑		MIN	1.6	1.6
t_h Hold time	A data after CLK ↑		MIN	1.1	1.1
t_{PLH}	A	Y	MAX	4.3	4.3
t_{PHL}				4.3	4.3
t_{PLH}	CLK	Y	MAX	4.7	4.7
t_{PHL}				4.7	4.7
t_{PLH}	$\overline{SEL}$	Y	MAX	4.8	4.8
t_{PHL}				4.8	4.8
t_{PZH}	$\overline{OE}$	Y	MAX	5.1	5.1
t_{PZL}				5.1	5.1
t_{PHZ}	$\overline{OE}$	Y	MAX	5.1	5.1
t_{PLZ}				5.1	5.1

UNIT fmax : MHz other : ns

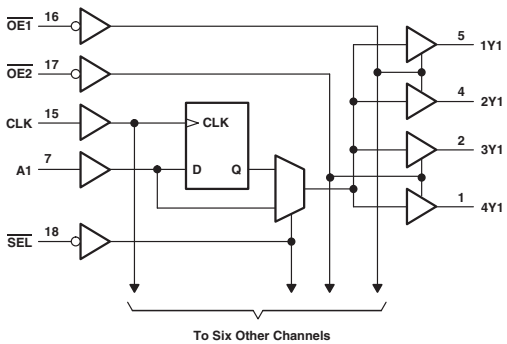
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

162832

1-BIT TO 4-BIT ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS

- SN74ALVCH162832: Output Ports Have Equivalent 26-Ω Series Resistors

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	$\overline{SEL}$	CLK	A	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I_{CC}	MAX	0.04	mA
I_{OH}	MAX	-12	mA
I_{OL}	MAX	12	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
f_{max}			MIN	150
t_w Pulse duration	CLK high or low		MIN	3.3
t_{su} Setup time	A data before CLK ↑		MIN	1.6
t_h Hold time	A data after CLK ↑		MIN	1.1
t_{PLH}	A	Y	MAX	4.3
t_{PHL}				4.3
t_{PLH}	CLK	Y	MAX	4.7
t_{PHL}				4.7
t_{PLH}	$\overline{SEL}$	Y	MAX	4.8
t_{PHL}				4.8
t_{PZH}	$\overline{OE}$	Y	MAX	5.1
t_{PZL}				5.1
t_{PHZ}	$\overline{OE}$	Y	MAX	5.1
t_{PLZ}				5.1

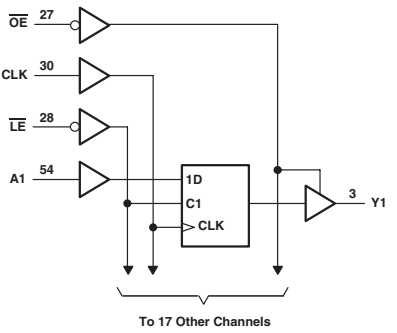
UNIT fmax : MHz other : ns

162834

18-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

- SN74ALVC162834: Outputs Have Equivalent 26-Ω Series Resistors

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUT
OE	LE	CLK	A	Y
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	↑	L	L
L	H	↑	H	H
L	H	H	X	Y_0†
L	H	L	X	Y_0‡

† Output level before the indicated steady-state input conditions were established, provided that CLK is high before LE goes high
‡ Output level before the indicated steady-state input conditions were established

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVC 3V	ALVCF 3V	UNIT
I_{CC}	MAX	0.04	0.04	mA
I_{OH}	MAX	-12	-18	mA
I_{OL}	MAX	12	18	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVC 3V	ALVCF 3V
f_{max}			MIN	150	150
t_w Pulse duration	LE low		MIN	3.3	3.3
	CLK high or low		MIN	3.3	3.3
t_{su} Setup time	Data before CLK ↑		MIN	1.7	1.0
	Data before LE ↑, CLK high		MIN	1.9	1.5
	Data before LE ↑, CLK low		MIN	1.5	1.0
t_h Hold time	A data after CLK ↑		MIN	0.7	0.6
	Data after LE ↑, CLK high		MIN	0.9	1.4
	Data after LE ↑, CLK low		MIN	0.9	1.4
t_{PLH}	A	Y	MAX	4.2	3.5
t_{PHL}				4.2	3.5
t_{PLH}	LE	Y	MAX	5.8	4.6
t_{PHL}				5.8	4.6
t_{PLH}	CLK	Y	MAX	5.4	3.5
t_{PHL}				5.4	3.5
t_{PZH}	OE	Y	MAX	5.9	5.0
t_{PZL}				5.9	5.0
t_{PHZ}	OE	Y	MAX	5	4.2
t_{PLZ}				5	4.2

UNIT fmax : MHz other : ns

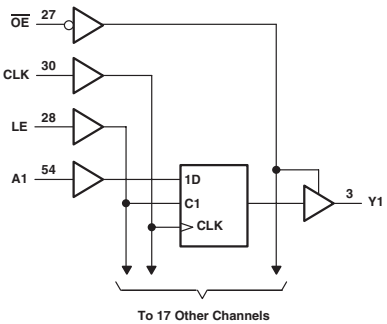
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

162835

18-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

- SN74ALVC162835, SN74ALVCH162835: Output Port Has Equivalent 26-Ω Series Resistors

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	LE	CLK	A	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	L or H	X	Y_0†

† Output level before the indicated steady-state input conditions were established

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVC 3V	ALVCF 3V	ALVCH 3V	UNIT
I_{CC}	MAX	0.04	0.04	0.04	mA
I_{OH}	MAX	-12	-18	-12	mA
I_{OL}	MAX	12	18	12	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVC 3V	ALVCF 3V	ALVCH 3V
f_{max}			MIN	150	150	150
t_w Pulse duration	LE low		MIN	3.3	3.3	3.3
	CLK high or low		MIN	3.3	3.3	3.3
t_{su} Setup time	Data before CLK ↑		MIN	1.7	1.0	1.7
	Data before LE ↓, CLK high		MIN	1.5	1.5	1.5
	Data before LE ↓, CLK low		MIN	1	1.0	1
t_h Hold time	A data after CLK ↑		MIN	0.7	0.6	0.7
	Data after LE ↓, CLK high		MIN	1.4	1.4	1.4
	Data after LE ↓, CLK low		MIN	1.4	1.4	1.4
t_{PLH}	A	Y	MAX	4.2	3.5	4.2
t_{PHL}				4.2	3.5	4.2
t_{PLH}	LE	Y	MAX	5.1	4.6	5.1
t_{PHL}				5.1	4.6	5.1
t_{PLH}	CLK	Y	MAX	5.4	3.5	5.4
t_{PHL}				5.4	3.5	5.4
t_{PZH}	$\overline{OE}$	Y	MAX	5.5	5.0	5.5
t_{PZL}				5.5	5.0	5.5
t_{PHZ}	$\overline{OE}$	Y	MAX	4.5	4.2	4.5
t_{PLZ}				4.5	4.2	4.5

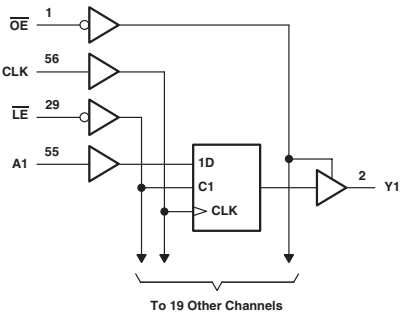
UNIT fmax : MHz other : ns

162836

20-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

- SN74ALVC162836, SN74ALVCH162836: Output Port Has Equivalent 26-Ω Series Resistors

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	$\overline{LE}$	CLK	A	Y
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	↑	L	L
L	H	↑	H	H
L	H	L or H	X	Y_0†

† Output level before the indicated steady-state input conditions were established

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVC 3V	ALVCH 3V	UNIT
I_{CC}	MAX	0.04	0.04	mA
I_{OH}	MAX	-12	-12	mA
I_{OL}	MAX	12	12	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVC 3V	ALVCH 3V
f_{max}			MIN	150	150
t_w Pulse duration	$\overline{LE}$ low		MIN	3.3	3.3
	CLK high or low		MIN	3.3	3.3
t_{su} Setup time	Data before CLK ↑		MIN	1.5	1.5
	Data before $\overline{LE}$ ↓, CLK high		MIN	1.3	1.3
	Data before $\overline{LE}$ ↓, CLK low		MIN	1.2	1.2
t_h Hold time	A data after CLK ↑		MIN	0.9	0.9
	Data after $\overline{LE}$ ↓, CLK high		MIN	1.1	1.1
	Data after $\overline{LE}$ ↓, CLK low		MIN	1.1	1.1
t_{PLH}	A	Y	MAX	4	4
t_{PHL}				4	4
t_{PLH}	$\overline{LE}$	Y	MAX	5.1	5.1
t_{PHL}				5.1	5.1
t_{PLH}	CLK	Y	MAX	5	5
t_{PHL}				5	5
t_{PZH}	$\overline{OE}$	Y	MAX	5.5	5.5
t_{PZL}				5.5	5.5
t_{PHZ}	$\overline{OE}$	Y	MAX	5.1	5.1
t_{PLZ}				5.1	5.1

UNIT fmax : MHz other : ns

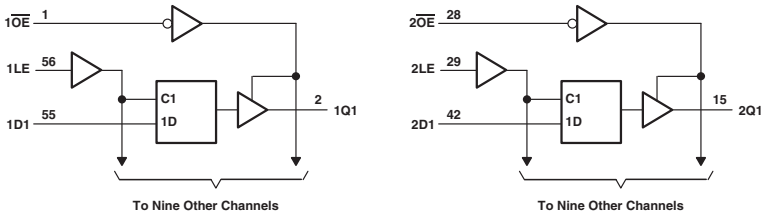
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

162841

20-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

- SN74ABT162841: Output Ports Have Equivalent 25-Ω Series Resistors
- SN74ALVCH162841: Output Ports Have Equivalent 26-Ω Series Resistors

Logic Diagram



FUNCTION TABLE
(each 10-bit latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ALVCH 3V	UNIT
I_{CC}	MAX	89	0.04	mA
I_{OH}	MAX	-12	-12	mA
I_{OL}	MAX	12	12	mA

TIMING REQUIREMENTS AND SWITCHING CHARACTERISTICS

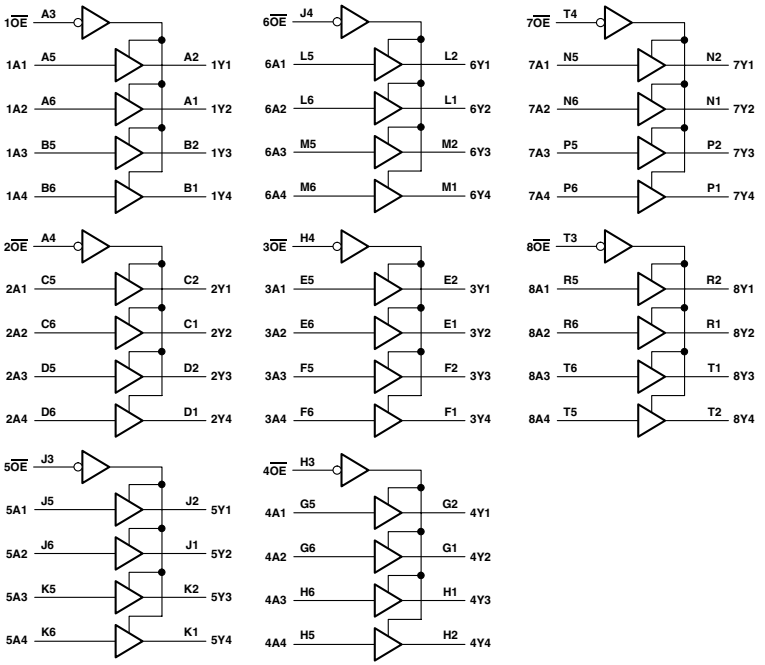
PARAMETER		INPUT	OUTPUT	MAX or MIN	ABT	ALVCH 3V
t_w	Pulse duration	LE highor low		MIN	4	3.3
t_{su}	Setup time	Data before LE ↓		MIN	0.8	-
		Data before LE ↑			-	1.1
t_h	Hold time	Data after LE ↓		MIN	1.8	-
		Data after LE ↑		MIN	-	1.1
t_{PLH}		D	Q	MAX	5.2	4.3
t_{PHL}					6	4.3
t_{PLH}		LE	Q	MAX	5.4	4.7
t_{PHL}					5.8	4.7
t_{PZH}		$\overline{OE}$	Q	MAX	5.7	5.3
t_{PZL}					6.5	5.3
t_{PHZ}		$\overline{OE}$	Q	MAX	6.5	4.4
t_{PLZ}					7.1	4.4

UNIT : ns

322244

32-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

Logic Diagram



ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVCH 3V	UNIT
I_{CC}	MAX	0.04	mA
I_{OH}	MAX	-12	mA
I_{OL}	MAX	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVCH 3V
t_{PLH}	A	Y	MAX	4.4
t_{PHL}				4.4
t_{PZH}	$\overline{OE}$	Y	MAX	5.5
t_{PZL}				5.5
t_{PHZ}	$\overline{OE}$	Y	MAX	6.3
t_{PLZ}				6.3

UNIT: ns

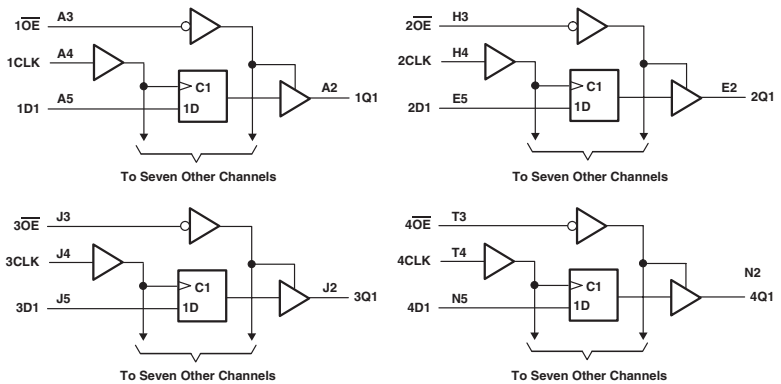
: OBSOLETED or NOT RECOMMENDED NEW DESIGNS

322374

3.3-V ABT 32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP

- Output Ports Have Equivalent 22-Ω Series Resistors

Logic Diagram



FUNCTION TABLE

(each 8bit flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVTH 3V	UNIT
I_{CC}	MAX	10	mA
I_{OH}	MAX	-12	mA
I_{OL}	MAX	12	mA

TIMING REQUREMENTS AND SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTH 3V
f_{max}				160
t_w Pulse duration, CLK high or low			MIN	3
t_{su} Setup time	Data before CLK↑, data high		MIN	1.8
	Data before CLK↑, data low		MIN	1.8
t_h Hold time	Data after CLK↑, data high		MIN	0.8
	Data after CLK↑, data low		MIN	0.8
t_{PLH}	CLK	Q	MAX	5.3
t_{PHL}				4.9
t_{PZH}	$\overline{OE}$	Q	MAX	5.6
t_{PZL}				4.9
t_{PHZ}	$\overline{OE}$	Q	MAX	5.4
t_{PLZ}				5

UNIT fmax : MHz other : ns

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