Multilayer PCB Stackup Planning

by Barry Olney | In-Circuit Design Pty Ltd |Australia

This Application Note details tried and proven techniques for planning high speed Multilayer PCB Stackup configurations.

Planning the multilayer PCB stackup configuration is one of the most important aspects in achieving the best possible performance of a product. A poorly designed substrate, with inappropriately selected materials, can degrade the electrical performance of signal transmission increasing emissions and crosstalk and can also make the product more susceptible to external noise. These issues can cause intermittent operation due to timing glitches and interference dramatically reducing the products performance and long term reliability.

In contrast, a properly built PCB substrate can effectively reduce electromagnetic emissions, crosstalk and improve the signal integrity providing a low inductance power distribution network. And, looking from a fabrication point of view, can also improved manufacturability of the product.

Suppressing the noise at the source rather than trying to elevate the problems once the product has been built makes sense. Having the project completed 'Right First Time' on time and to budget means that you cut costs by reducing the design cycle, have a shorter time to market and an extended product life cycle.

Boards containing copper planes allow signals to be routed in either microstrip or stripline controlled impedance transmission line configurations creating much less radiation than the indiscriminate traces on a two layer board. The signals are tightly coupled to the planes (either ground or power) reducing crosstalk and improving signal integrity.

Planes, in multilayer PCB's, provide significant reduction in radiated emission over two layer PCBs. As a rule of thumb, a four layer board will produce 15 dB less radiation than a two layer board.

When selecting a multilayer stackup we should consider the following:

- A signal layer should always be adjacent to a plane. This limits the number of signal layers embedded between planes to two and top and bottom (outer) layers to one signal.
- Signal layers should be tightly coupled (<10 MIL) to their adjacent planes
- A power plane (as well as a ground) can be used for the return path of the signal.
- Determine the return path of the signals (which plane will be used). Fast rise time signals take the path of least inductance which is normally the closest plane.
- Cost (the boss's most important design parameter).

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Soldermask – Affects on Impedance

Since PCB's are normally covered in Soldermask then the affects of the conformal coating should be considered when calculating impedance. Generally, soldermask will reduce the impedance by 2 to 3 ohms on thin traces. As the trace thickness increases the soldermask has less affect.

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UNITS: MIL — Total Board Thickness: 88.6

Layer		Material	Dielectric		Copper	Trace		Current	Impedance	Edge Coupled	Broadside Coupled	
Number	Name	Type	Constant	Thickness	Thickness	Clearance	Width	(Amps)	Characteristic(Zo)	Differential(Zdiff)	Differential(Zdbs)	Description
1	Top	Conductive			1.4	4	4	0.31	55.64	93.54		Signal
		Dielectric	4.3	3								Prepreg
2	GND	Conductive			1.4							Plane
		Dielectric	4.3	6								Core

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UNITS: MIL — Total Board Thickness: 88.6

Layer		Material	Dielectric		Copper	Trace		Current	Impedance	Edge Coupled	Broadside Coupled	
Number	Name	Type	Constant	Thickness	Thickness	Clearance	Width	(Amps)	Characteristic(Zo)	Differential(Zdiff)	Differential(Zdbs)	Description
		Dielectric	3.3	0.5								Soldermask
1	Top	Conductive			1.4	4	4	0.31	53.53	89.98		Signal
		Dielectric	4.3	3								Prepreg
2	GND	Conductive			1.4							Plane
		Dielectric	4.3	6								Core

Figure 1 – Affects of Soldermask coating

Figure 1 illustrates the affect of soldermask coating on microstrip impedance. This example is of commonly used liquid photoimageable soldermask having a thickness of 0.5 MIL and a Dielectric Constant of 3.3.

The soldermask drops the microstrip characteristic impedance by 2 ohms and the differential impedance by 3.5 ohms. So, if you don't consider soldermask then the calculation could be out by as much as 3 to 4%.

Dielectric Materials

The most popular Dielectric material is FR4 and may be in the form of core or prepreg (pre-impregnated) material.

The core material is thin dielectric (cured fibreglass epoxy resin) with copper foil bonded to both sides. For instance: Isola's FR406 materials - include 5, 8, 9.5, 14, 18, 21, 28, 35, 39, 47, 59 and 93 MIL cores. The copper thickness is typically ½ to 2 oz (17 to 70 um).

The prepreg material is thin sheets of fibreglass impregnated with uncured epoxy resin which hardens when heated and pressed during the PCB fabrication process. Isola's FR406 materials – include 1.7, 2.3, 3.9 and 7.1 MIL prepregs that may be combined to achieve the desired prepreg thickness.

The most common stackup called the 'Foil Method' is to have prepreg with copper foils bonded to the outside on the outer most layers (top and bottom) then core alternating with prepreg throughout the substrate. An alternate stackup is called the 'Caped Method' which is the opposite of the Foil Method and was used by old-school military contractors.

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Let's take a look at the most common multilayer configurations.

4 Layer Stackup

A typical four layer board stackup is shown below. The Characteristic and Differential Impedances of the substrate are calculated using the ICD Stackup Planner (available for download @ www.icd.com.au).

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UNITS: MIL — Total Board Thickness: 61.2

Layer		Material	Dielectric		Copper	Trace		Current	Impedance	Edge Coupled	Broadside Coupled	
Number	Name	Type	Constant	Thickness	Thickness	Clearance	Width	(Amps)	Characteristic(Zo)	Differential(Zdiff)	Differential(Zdbs)	Description
		Dielectric	3.3	0.5								Soldermask
1	Top	Conductive			0.7	15	15	0.49	51.93	90.98		Signal
		Dielectric	4.3	9								Prepreg
2	GND	Conductive			1.4							Plane
		Dielectric	4.3	39								Core
3	VCC	Conductive			1.4							Plane
		Dielectric	4.3	9								Prepreg
4	Bottom	Conductive			0.7	15	15	0.49	51.93	90.98		Signal
		Dielectric	3.3	0.5								Soldermask

Figure 2 - 4 Layer Stackup

It is common to see four layer boards stacked evenly. That is, four evenly spaced layers with the planes in the centre. Although, this certainly makes the board symmetrical it doesn't help the EMC.

Also, another common mistake is to have the planes closely coupled in the centre with large dielectrics between the signal layers and planes. This certainly creates good inter-plane capacitance but again doesn't help with signal integrity, crosstalk or EMC – which is why we opt for a four layer PCB over a two layer.

To improve the EMC performance of a four layer board, it is best to space the signal layers as close to the planes as possible (< 10 MIL), and use a large core (~ 40 MIL) between the power and ground plane keeping the overall thickness of the substrate to ~ 62 MIL. The close trace to plane coupling will decrease the crosstalk between traces and allow us to maintain the impedance at an acceptable value.

A good range of impedance (Zo) is from 50 to 60 ohms. Keep in mind that lower impedance will increase the dI/dt and dramatically increase the current drawn (not good for the PDN) and higher impedance will emit more EMI and also make the design more susceptible to outside interference.

6 Layer Stackup

A six layer board is basically a four layer board with two extra signal layers added between the planes. This improves the EMI dramatically as it provides two buried layers for high-speed signals and two surface layers for routing low speed signals.

The signal layers should be placed very close to there adjacent planes and the desired board thickness (62 MIL) made up by the use of a thicker centre core. It is always a

compromise between trace impedance, trace width and prepreg/core thickness and it is best to use a stackup calculator to provide quick ‘what if’ analysis of the possibilities.

The ICD Stackup Planner calculates characteristic impedance plus edge coupled and broadside coupled differential impedance. The latter for embedded dual stripline layers only. Differential pairs are becoming common place in high speed design reducing noise by using differential mode signalling.

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UNITS: MIL

Total Board Thickness: 63

Layer		Material	Dielectric		Copper	Trace		Current	Impedance	Edge Coupled	Broadside Coupled	
Number	Name	Type	Constant	Thickness	Thickness	Clearance	Width	(Amps)	Characteristic(Zo)	Differential(Zdiff)	Differential(Zdbs)	Description
		Dielectric	3.3	0.5								Soldermask
1	Top	Conductive			0.7	12	12	0.42	50.81	89.45		Signal
		Dielectric	4.3	7								Prepreg
2	GND	Conductive			1.4							Plane
		Dielectric	4.3	15								Core
3	Inner 3	Conductive			1.4	12	12	0.69	52.65	88.5	66.91	Signal
		Dielectric	4.3	12								Prepreg
4	Inner 4	Conductive			1.4	12	12	0.69	52.65	88.5	66.91	Signal
		Dielectric	4.3	15								Core
5	VCC	Conductive			1.4							Plane
		Dielectric	4.3	7								Prepreg
6	Bottom	Conductive			0.7	12	12	0.42	50.81	89.45		Signal
		Dielectric	3.3	0.5								Soldermask

Figure 3 - 6 Layer Stackup

8 Layer Stackup

To improve EMC performance, add two more planes to the six layer stackup. It is not recommended to have more then two adjacent signal layers between the planes as this creates impedance discontinuities (~20 ohms difference in impedance of signal layers) and increases crosstalk between these signal layers.

In the case below, two plane layers are added to the centre of the substrate. This allows tight coupling between the centre planes and isolates each signal plane reducing coupling hence crosstalk dramatically. This configuration is commonly used for high speed signals of DDR2 and DDR3 designs where crosstalk due to tight routing is an issue. <u>If you are risk aversive – then this is the stackup to use.</u>

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UNITS: MIL

Total Board Thickness: 60.4

Layer		Material	Dielectric		Copper	Trace		Current	Impedance	Edge Coupled	Broadside Coupled	
Number	Name	Type	Constant	Thickness	Thickness	Clearance	Width	(Amps)	Characteristic(Zo)	Differential(Zdiff)	Differential(Zdbs)	Description
		Dielectric	3.3	0.5								Soldermask
1	Top	Conductive			0.7	5	5	0.22	50.05	87.69		Signal
		Dielectric	4.3	3								Prepreg
2	GND	Conductive			1.4							Plane
		Dielectric	4.3	8								Core
3	Inner 3	Conductive			1.4	12	5	0.37	51.96	90.66		Signal
		Dielectric	4.3	8								Prepreg
4	VDD	Conductive			0.7							Plane
		Dielectric	4.3	14								Core
5	GND	Conductive			0.7							Plane
		Dielectric	4.3	8								Prepreg
6	Inner 6	Conductive			1.4	12	5	0.37	51.96	90.66		Signal
		Dielectric	4.3	8								Core
7	VCC	Conductive			1.4							Plane
		Dielectric	4.3	3								Prepreg
8	Bottom	Conductive			0.7	5	5	0.22	50.05	87.69		Signal
		Dielectric	3.3	0.5								Soldermask

Figure 4 - 8 Layer Stackup

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10 Layer Stackup

A ten layer board should be used when six routing layers and four planes are required and EMC is of concern.

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UNITS: MIL Total Board Thickness: 62

Layer		Material	Dielectric		Copper	Trace		Current	Impedance	Edge Coupled	Broadside Coupled	
Number	Name	Type	Constant	Thickness	Thickness	Clearance	Width	(Amps)	Characteristic(Zo)	Differential(Zdiff)	Differential(Zdbs)	Description
		Dielectric	3.3	0.5								Soldermask
1	Top	Conductive			1.4	7	4	0.31	53.53	98.54		Signal
		Dielectric	4.3	3								Prepreg
2	GND	Conductive			1.4							Plane
		Dielectric	4.3	5								Core
3	Inner 3	Conductive			1.4	7	4	0.31	50.69	90.13	66.78	Signal
		Dielectric	4.3	5								Prepreg
4	Inner 4	Conductive			1.4	7	4	0.31	50.69	90.13	66.78	Signal
		Dielectric	4.3	5								Core
5	VDD	Conductive			1.4							Plane
		Dielectric	4.3	12								Prepreg
6	GND	Conductive			1.4							Plane
		Dielectric	4.3	5								Core
7	Inner 7	Conductive			1.4	7	4	0.31	50.69	90.13	66.78	Signal
		Dielectric	4.3	5								Prepreg
8	Inner 8	Conductive			1.4	7	4	0.31	50.69	90.13	66.78	Signal
		Dielectric	4.3	5								Core
9	VCC	Conductive			1.4							Plane
		Dielectric	4.3	3								Prepreg
10	Bottom	Conductive			1.4	7	4	0.31	53.53	98.54		Signal
		Dielectric	3.3	0.5								Soldermask

Figure 5 - 10 Layer Stackup

Figure 5 above demonstrates a typical 10 layer stackup. This stackup is ideal because of the tight coupling of the signal and return planes, the shielding of the high speed signal layers, the existence of multiple ground planes, as well as a tightly coupled power/ground plane pair in the center of the board. High speed signals normally would be routed on the signal layers buried between planes (layers 3-4 and 7-8 in this case). However, care should be taken to route these signal orthogonally, with respect to each other, to avoid coupling (crosstalk) between adjacent layers.

12 Layer Stackup

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UNITS: MIL Total Board Thickness: 59.4

Layer		Material	Dielectric		Copper	Trace		Current	Impedance	Edge Coupled	Broadside Coupled	
Number	Name	Type	Constant	Thickness	Thickness	Clearance	Width	(Amps)	Characteristic(Zo)	Differential(Zdiff)	Differential(Zdbs)	Description
		Dielectric	3.3	0.5								Soldermask
1	Top	Conductive			0.7	4	4	0.19	55.93	94.02		Signal
		Dielectric	4.3	3								Prepreg
2	GND	Conductive			0.7							Plane
		Dielectric	4.3	5								Core
3	Inner 3	Conductive			0.7	4	4	0.19	53.25	88.28	72.66	Signal
		Dielectric	4.3	5								Prepreg
4	Inner 4	Conductive			0.7	4	4	0.19	53.25	88.28	72.66	Signal
		Dielectric	4.3	5								Core
5	VDD	Conductive			0.7							Plane
		Dielectric	4.3	5								Prepreg
6	Inner 6	Conductive			0.7	4	4	0.19	53.25	88.28	72.66	Signal
		Dielectric	4.3	5								Core
7	Inner 7	Conductive			0.7	4	4	0.19	53.25	88.28	72.66	Signal
		Dielectric	4.3	5								Prepreg
8	GND	Conductive			0.7							Plane
		Dielectric	4.3	5								Core
9	Inner 9	Conductive			0.7	4	4	0.19	53.25	88.28	72.66	Signal
		Dielectric	4.3	5								Prepreg
10	Inner 10	Conductive			0.7	4	4	0.19	53.25	88.28	72.66	Signal
		Dielectric	4.3	5								Core
11	VCC	Conductive			0.7							Plane
		Dielectric	4.3	3								Prepreg
12	Bottom	Conductive			0.7	4	4	0.19	55.93	94.02		Signal
		Dielectric	3.3	0.5								Soldermask

Figure 6 - 12 Layer Stackup

Twelve layers is the largest number of layers that can usually be conveniently fabricated in a 62MIL thick board. Occasionally you will see 14 to 16 layer boards fabricated as a 62MIL thick board, but the numbers of fabricators capable of producing them are limited to those that can produce HDI boards.

High layer count boards (ten plus) require thin dielectrics (typically 5MIL or less on a 62MIL thick board) and therefore they automatically have tight coupling between layers. When properly stacked and routed they can meet all of our high speed requirements and will have excellent EMC performance and signal integrity. The above twelve layer stackup provides shielding on six of the internal layers.

14 Layer Stackup

The fourteen layer stackup below is used when eight routing (signal) layers are required plus special shield of critical nets is required. Layers 6 and 9 provide isolation for sensitive signals while layers 3 & 4 and 11 & 12 provide shielding for high speed signals.

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UNITS: MIL — Total Board Thickness: 88.6

Layer		Material	Dielectric		Copper	Trace		Current	Impedance	Edge Coupled	Broadside Coupled	
Number	Name	Type	Constant	Thickness	Thickness	Clearance	Width	(Amps)	Characteristic(Zo)	Differential(Zdiff)	Differential(Zdbs)	Description
		Dielectric	3.3	0.5								Soldermask
1	Top	Conductive			1.4	4	4	0.31	53.53	89.98		Signal
		Dielectric	4.3	3								Prepreg
2	GND	Conductive			1.4							Plane
		Dielectric	4.3	6								Core
3	Inner 3	Conductive			1.4	7	4	0.31	50.78	90.29	48.55	Signal
		Dielectric	4.3	3								Prepreg
4	Inner 4	Conductive			1.4	7	4	0.31	50.78	90.29	48.55	Signal
		Dielectric	4.3	6								Core
5	VDD	Conductive			1.4							Plane
		Dielectric	4.3	7								Prepreg
6	Inner 6	Conductive			1.4	10	4	0.31	52.87	91.42		Signal
		Dielectric	4.3	7								Core
7	VCC	Conductive			1.4							Plane
		Dielectric	4.3	5								Prepreg
8	GND	Conductive			1.4							Plane
		Dielectric	4.3	7								Core
9	Inner 9	Conductive			1.4	10	4	0.31	52.87	91.42		Signal
		Dielectric	4.3	7								Prepreg
10	VSS	Conductive			1.4							Plane
		Dielectric	4.3	6								Core
11	Inner 11	Conductive			1.4	7	4	0.31	50.78	90.29	48.55	Signal
		Dielectric	4.3	3								Prepreg
12	Inner 12	Conductive			1.4	7	4	0.31	50.78	90.29	48.55	Signal
		Dielectric	4.3	6								Core
13	VCC	Conductive			1.4							Plane
		Dielectric	4.3	3								Prepreg
14	Bottom	Conductive			1.4	4	4	0.31	53.53	89.98		Signal
		Dielectric	3.3	0.5								Soldermask

Figure 7 - 14 Layer Stackup

16 Layer Stackup

A sixteen layer PCB provides ten layers of routing and is normally used for extremely dense designs. Generally, you see 16 layer PCB's where the routing technology used in the EDA application doesn't have ability to route the design to completion. "If it won't route - just keep adding layers". Although this is a common saying it is not good practice.

If a board won't route to completion then there may be a number of reasons. Poor placement is often the course. Open routing channels, reduce the number of crossovers in the rats nets, place vias on a 25 MIL grid to allow through routing and basically help the router as much as possible.

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UNITS: MIL											Total Board Thickness: 75.6	
Layer		Material	Dielectric		Copper	Trace		Current	Impedance	Edge Coupled	Broadside Coupled	
Number	Name	Type	Constant	Thickness	Thickness	Clearance	Width	(Amps)	Characteristic(Zo)	Differential(Zdiff)	Differential(Zdbs)	Description
		Dielectric	3.3	0.5								Soldermask
1	Top	Conductive			1.4	4	4	0.31	53.53	89.98		Signal
		Dielectric	4.3	3								Prepreg
2	GND	Conductive			0.7							Plane
		Dielectric	4.3	5								Core
3	Inner 3	Conductive			0.7	7	4	0.19	49.86	91.26	54.43	Signal
		Dielectric	4.3	3								Prepreg
4	Inner 4	Conductive			0.7	7	4	0.19	49.86	91.26	54.43	Signal
		Dielectric	4.3	5								Core
5	VDD	Conductive			0.7							Plane
		Dielectric	4.3	5								Prepreg
6	Inner 6	Conductive			0.7	7	4	0.19	49.86	91.26	54.43	Signal
		Dielectric	4.3	3								Core
7	Inner 7	Conductive			0.7	7	4	0.19	49.86	91.26	54.43	Signal
		Dielectric	4.3	5								Prepreg
8	VCC	Conductive			0.7							Plane
		Dielectric	4.3	5								Core
9	GND	Conductive			0.7							Plane
		Dielectric	4.3	5								Prepreg
10	Inner 10	Conductive			0.7	7	4	0.19	49.86	91.26	54.43	Signal
		Dielectric	4.3	3								Core
11	Inner 11	Conductive			0.7	7	4	0.19	49.86	91.26	54.43	Signal
		Dielectric	4.3	5								Prepreg
12	VSS	Conductive			0.7							Plane
		Dielectric	4.3	5								Core
13	Inner 13	Conductive			0.7	7	4	0.19	49.86	91.26	54.43	Signal
		Dielectric	4.3	3								Prepreg
14	Inner 14	Conductive			0.7	7	4	0.19	49.86	91.26	54.43	Signal
		Dielectric	4.3	5								Core
15	VCC	Conductive			0.7							Plane
		Dielectric	4.3	3								Prepreg
16	Bottom	Conductive			1.4	4	4	0.31	53.53	89.98		Signal
		Dielectric	3.3	0.5								Soldermask

Figure 8 - 16 Layer Stackup

There is really no limit to the number of layers that can be fabricated in a multilayer PCB (please check the capabilities of your fabricator first though). Of course, the board thickness increases as the layer count goes up to accommodate the minimum thickness of materials used. Also the aspect ratio (board thickness to smallest hole diameter) has to be considered. Generally this is 10:1 for boards thicker then 100MIL. For example, a 200 MIL thick substrate has a minimum hole size of 20 MIL.

Determining the Layer Count

The technology rules are based on the minimum pitch of the SMT components employed and are basically the largest trace, clearance and via allowable whilst minimising PCB fabrication costs. Technology of 4/4 MIL (trace/clearance) and Vias of 20/8 MIL (pad/hole) are generally required for complex high speed design incorporating ball grid arrays (BGA). However, if you can use less demanding dimensions then this will reduce cost and improved fabrication yield.

Once these rules have been established, calculate the stackup required for the desired characteristic impedance (Zo) and the differential impedance (Zdiff) as per the component datasheets. Generally, 50 ohm Zo and 100 ohm Zdiff are used. Keep in mind that lower impedance will increase the dI/dt and dramatically increase the current drawn (not good for the PDN) and higher impedance will emit more EMI and also make the design more susceptible to outside interference. So, a good range of Zo is 50 – 60 ohms.

The total number of layers required for a given design is dependent on the complexity of the design. Factors include: the number of signal nets that must break out from a BGA; the number of power supplies required by the BGA's; component density and package types.

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Experienced designers get a feel for it after a while but a good way to check if you have enough layers is to autoroute the board. With no tweaking, the router needs to complete at least 85% of the routes to indicate the selected stackup is routable. You may have to re-evaluate the placement a couple of times to get the best results.

How do you calculate the characteristic and differential impedance of the entire stackup using the established design rules?

Well this one I have made easy for you. In-Circuit Design Pty Ltd has developed a Stackup Planner. This new release builds on the familiar ease of use of the popular In-Circuit Design online Impedance Calculator that has been utilized by tens of thousands of Engineers and PCB Designers world wide since 1996. You can download an evaluation copy from www.icd.com.au

For those who are new to multilayer PCB stackup planning, standard 2 to 16 layer stackups have been provided that are commonly used. However, you can edit, rename and save a favourite custom stackup to use again.

The generic stackups use default values for all variables that can be adjusted to achieve the desired Characteristic (Zo), Edge Coupled (Zdiff) and Broadside Coupled (Zdbs) Impedance. The Dielectric Constant (also called Relative Permittivity), Dielectric Thickness, Copper Thickness, Trace Width and Trace can be varied. The 2011 release also calculates trace current.

For further information, please contact Barry Olney | +61 4123 14441 | b.olney@icd.com.au

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EMC and the Printed Circuit Board - Montrose

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