# Four or more layer PCB design for beginners using EAGLE

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### 1 Introduction

With microcontrollers and other Integrated Circuit (IC)'s getting smaller and smaller Printed Circuit Board (PCB) design gets more and more difficult. 2 layer PCB design is getting common for small companies and hobbyists but 4 layer or more is a bit daring for those used to 2 layers. When designing a circuit with a Ball Grid Array (BGA) that has 100 or more pins a 4 layer circuit board is necessary, but more layers can make designing easier. With prices of 4 layer boards getting lower it can be a better idea to route a board thats hard to do in 2 layers in 4 layers as it can save a lot of time. This document will explain the basics of routing PCBs with 4 or more layers with Cadsoft Eagle.

### 2 PCB techniques

When designing with more than 2 layers some new PCB techniques can be used to make routing easier. two common techniques are blind Vertical Interconnect Access (via)s and buried vias.



Figure 1: Image licensed under GFDL, CC-BY 3.0, Author: M adler, <u>Source</u>.

- 1. Trough hole via
- 2. Blind via
- 3. Buried via

Normally a via goes through the PCB, from the top layer to the bottom layer. A blind via is a via that starts at the top or bottom via but does not go fully through. So in an 8 layer PCB it goes from layer one (the top layer) to layer 2 or from layer 8 (the bottom layer) to layer 7. It is possible to use blind vias that go through multiple layers but not all PCB manufacturers can do this.

Buried vias are the opposite and are vias in internal layers. For example, a via from layer 3 to layer 7 in an 8 layer PCB. The advantage of blind and buried vias that you can still place PCB tracks on layers that the via does not reach. This means you can place more PCB traces and vias in less space and make the PCB smaller thus cheaper to produce. A smaller PCB also means that high speed routing like Random Access Memory (RAM) databusses can be shorter making higher speeds possible.

Microvias are small vias drilled with a laser instead of a normal drill. Most blind vias are made this way. The drill size of a microvia is around 0.1mm with most PCB manufactures. This small size means they can be used on a pad of a BGA package or Quad-Flat No-leads package (QFN) package. This makes routing much easier. Warning: the failure rate of PCBs with microvias on BGA pads is a bit higher then placing a via next to the pad. Never place a normal via on a BGA pad, this will make the failure rates much higher!

Most 2 layer PCB boards are routed with 0.2mm or 0.15mm clearance and trace as this is the default design rules most PCB manufacturers use. With dense boards and BGA devices with a small pitch this can be too big and 0.125 or 0.1mm clearance/trace thickness is used but even smaller is possible. For example, Sierra circuits can make 2 mil (50um) laser drilled holes and do 1 mil (25um) clearance/trace thickness if required.

### 3 Setup Eagle for multilayer boards

To use Eagle for multilayer PCBs the design rules have to be setup first. Design rules like clearance, trace thickness and hole size are different per PCB and wont be explained here. But for Eagle it is required to setup the design rules for the layers first, else it is impossible to route multilayer boards. To do this in Eagle, click on the Design Rule Check (DRC) button and then on the Layers tab.

1	Nr	Copper	Isolation
	1	0.035mm	
	16	0.035mm	1.5mm
16		1	otal: 1.57mm
	Setup	(1*16)	
ayers are combined through eit <b>suried</b> and <b>through</b> vias are d <b>suried</b> and <b>through</b> vias are d <b>simulation</b> via the defined by writing <b>scample:</b> [2:1+((2*3)+(4) ores. The cores are combined to syer 1 to 2.	ther core or prepr lefined by writing g [t::b], w *16) )] is a mult hrough a prepres	regmaterial. <b>a</b> * <b>b</b> combines layers <i>a</i> and <i>b</i> with a () hich defines a blind via from top to layer <i>t</i> and fro layer setup with two cores, combining layers 2/3 and buried vias are produced through the result	core, while <b>a+b</b> does the same with <i>prepreg</i> . on bottom to layer <i>b</i> . and 4/16, respectively, with buried vias going through both ing stack. Finally layer 1 is added, with blind vias going from

Figure 2: Image licensed under CC-BY 3.0, Author: Rik te Winkel

By default the Layers are setup for a 2 layer design. Normally a PCB manufacturer can provide an image or PDF with the copper thickness, isolation and other info. This can be helpful when setting up the Layers part of the DRC but it is not necessary. The settings for copper and isolation thickness and core material are for visuals only and wont influence the final PCB.

For a 2 layer design the default Layers settings are (1 \* 16), this means that there are 2 layers, layer 1 and layer 16 and in between them is core material. For a 4 layer board the following setting can be used: (1 \* 2 \* 3 \* 4). To use buried vias it gets a bit more difficult. A 6 layer board with buried vias possible from layer 2 to 5 is possible with this setting: (1 \* (2 \* 3 \* 4 \* 5) \* 6). A via is possible between layers in '()', so from layer 1 to 6 and layer 2 to 5. In Eagle it looks like this:

A blind via is defined with [depth: and :depth]. For a 6 layer PCB like above with blind vias from layer 1 to 2 and layer 5 to 6 the command is as following: [2 : (1 \* (2 \* 3 \* 4 \* 5) \* 6) : 5].

### 4 Making a design plan

With extensive PCB's that require 4 or more layers it is a very good idea to make a design plan. A design plan is nothing more then a description on how you are going to route the PCB. Are

	Unitarite States	Resulty Shopes	- Sobbyl	1.000	
1	Nr	Copper			Isolation
2	1 0.035mr	n		0.2	mm
3	2 0.035m	n		0.1	Smm
	3 0.035mm	n		0.1	
	4 0.035m	n		0.0	Email
4	5 0.035mm	n		0.1	200
5	6 0.035m	n		0.2	mm
6				Total: 1.71	mm
	Setup (1*(2*	3*4*5)*6)			
yers are combined through ei <b>pried</b> and <b>through</b> vias are ( <b>ind</b> vias are defined by writin <b>cample:</b> [2:1+((2+3)+(4 res. The cores are combined yer 1 to 2.	ther core or prepregmate defined by writing ( ) . g [t::b], which def *16))] is a multilayer se through a prepreg and bur	rial. <b>a*b</b> combines laye ines a blind via from top tup with two cores, con ied vias are produced t	rs a and b wit o to layer t an nbining layers through the re	th a <i>core</i> , while d from bottom 2/3 and 4/16, esulting stack.	• a+b does the same with prepreg. to layer b. respectively, with buried vias going through both Finally layer 1 is added, with blind vias going from

Figure 3: Image licensed under CC-BY 3.0, Author: Rik te Winkel

File Lavers	Clearance	Distance	Sizes	Restring	Shanes	Sunniv	Marke	Misc	
	Creation rec	Cistorice	0.000	recourty	Unopes -	Sobby)	1.03.0	1.00	
		N	r		Copper				Isolation
2			1 0.035n	nm				0.2mm	
3			2 0.035n	nm				0.15mm	
		3	3 0.035n	nm				0.1300	
			4 0.035n	nm				U.Smm	
4			5 0.035m	nm				0.15mm	
5			5 0.035n	nm			_	0.2mm	
6		- 1					Total:	1.71mm	
		Set	up [2:(1	*(2* <b>\$</b> *4*5)*(	5):5]				
Layers are combined and through the second s	ned through eit <b>ugh</b> vias are d fined by writing + ( (2*3) + (4* are combined ti	her core or pro efined by writi ) [t::b] *16) )] is a m hrough a prepr	epreg mat ng () , which de ultilayer s reg and bi	erial. <b>a*b</b> co ). efines a blind etup with two uried vias are	mbines layer via from top o cores, comi produced th	s a and b wi to layer tar bining layers rough the r	th a <i>core,</i> nd from bo 2/3 and 4 esulting st	while <b>a+b</b> d ittom to laye 4/16, respect ack. Finally l	does the same with <i>prepreg.</i> or <i>b.</i> tively, with buried vias going through both layer 1 is added, with blind vias going from
								unde D	Salart Cancal Annly

Figure 4: Image licensed under CC-BY 3.0, Author: Rik te Winkel

there any high speed signals, what will be routed first, things to keep in mind. All those points make up the design plan. This section explains the most common points in a design plan.

#### 4.1 PCB stack-up

A PCB stack-up is a description for all the layers. Are there layers used as a power plane, are there layers for analog signals, etcetera. An example of a 6 layer PCB stack-up:

- Layer 1, normal traces
- Layer 2, 3.3V plane
- Layer 3, RAM and FLASH routing, high speed.
- Layer 4, RAM and FLASH routing, high speed.
- Layer 5, GND plane
- Layer 6, normal traces

#### 4.2 Digital and analog lines

Digital and analog are two very different things and in PCB design it can be wise to route it like this. A design with an microcontroller or Field Programmable Gate Array (FPGA) and an external Analog to Digital Converter (ADC) can be difficult especially if the ADC is 16 or more bits. Keeping the digital and analog grounds separated, putting a ground layer between digital and analog signals or dedicating a whole layer for the analog routing can make the difference between a working ADC or an ADC with too much noise. Texas Instruments has a great app note on mixed signal routing that can be found <u>here</u>.

#### 4.3 High speed and differential lines

When routing high speed signals some extra attention is required. External RAM, fast ADC's, Digital to Analog Converter (DAC)'s or a fast serial bus like Universal Serial Bus (USB). When you get over 100Mhz a PCB trace is more then just a bit of copper. It acts like a resistor, coil, capacitor and antenna all at the same time. When routing a parallel bus like an external RAM IC the difference between 2 traces can make it possible that one bit reaches the IC faster then the other, messing up the timing. The higher the speeds the more important this gets. Crosstalk is when the information on one signal can be seen on the signal next to it. When traces act like antennas it is possible that one trace picks up data from the other. Keeping high speed signals close to a ground plane and placing a ground trace next to the LSB from a parallel bus are good ways to avoid crosstalk. Sometimes reserving one layer for high speed routing and placing a ground layer above and underneath it are necessary for very fast signals, 500 Mhz or more.

### 5 Tips and tricks for PCB design in Eagle

Since Eagle 6.0 Eagle can do differential routing using an User Language Program (ULP). This are small scripts to make working with Eagle easier. An ULP to check the length and resistance of traces is also available, useful for high speed routing or analog and high power routing when resistance counts. To make BGA routing easier an ULP for BGA escape routing is available to in Eagle 6.0 or higher. To use an ULP just type '*Run ULPName*' in the PCB or Schematic editor in the white command line on the top. Just typing '*Run*' will open a window with all the ULP's available. For the explanation a PCB with an BGA256 micro-controller and a RAM IC will be routed. This is a non working example just to show how all the ULP's work. This is an image of the PCB file before any routing is done:



Figure 5: Image licensed under CC-BY 3.0, Author: Rik te Winkel

#### 5.1 BGA Escape routing

BGA escape routing is something that can consume a lot of time and most bigger CAD programs have ways to let the autorouter give it a go. Most of the times this works quite good. To do this in Eagle the ULP 'route-BGA' is used. If the BGA you want to route is called 'IC1' then the command to run is 'run route-BGA IC1'. In the pop up window the settings can be altered is required. The ULP will use the current DRC rules so make sure they are OK. In the example PCB the PCB looks like this after running the route-BGA ULP:



Figure 6: Image licensed under CC-BY 3.0, Author: Rik te Winkel

#### 5.2 High speed routing

Eagle also has an ULP that checks the length of all traces and calculates the resistance and maximum theoretical frequency for all traces. This can be useful to check if all traces for an parallel data bus like a RAM or ADC IC are not too different in length. The ULP is called *'length-freq-ri'*. to run this ULP the command is *'run length-freq-ri'*. A pop up windows will appear showing the length, resistance, maximum current and maximum frequency.

After letting the autorouter have a go on the example PCB the PCB is fully routed and looks like this:



Figure 7: Image licensed under CC-BY 3.0, Author: Rik te Winkel

After running the *'length-freq-ri'* command the pop up window shows up and looks like this. The shortest data wire is 21 mm long and the longest data wire 79mm, acceptable for a 100Mhz RAM IC.

ist of signals with length and its max. frequency / current xported from //who.nxp.com/Users I/NXP34109/Data/eagle/Eagletest/Testfile.brd it 6/7/2012 2:03:48 PM											
Cu thickness = 0.035 mm											
Signal	f max. [MHz]	I [mm]	A [mm2]	R [mOhm]	w min [mm]	w max [mm]	Imax [A]				
N\$32	13783.54	21.751	0.005	70.95	0.152	0.152	0.50				
N\$30	13708.51	21.870	0.005	71.34	0.152	0.152	0.50				
N\$34	13606.50	22.034	0.005	71.88	0.152	0.152	0.50				
N\$31	13485.26	22.232	0.005	72.52	0.152	0.152	0.50				
N\$29	13458.30	22.276	0.005	72.67	0.152	0.152	0.50				
N\$33	13202.31	22.708	0.005	74.08	0.152	0.152	0.50				
N\$27	13002.55	23.057	0.005	75.21	0.152	0.152	0.50				
N\$28	10829.96	27.682	0.005	90.30	0.152	0.152	0.50				
N\$16	8861.93	33.830	0.005	110.36	0.152	0.152	0.50				
N\$21	8806.22	34.044	0.005	111.06	0.152	0.152	0.50				
N\$9	8694.14	34.483	0.005	112.49	0.152	0.152	0.50				
N\$37	8519.61	35.189	0.005	114.79	0.152	0.152	0.50				
N\$39	8387.72	35.743	0.005	116.60	0.152	0.152	0.50				
N\$38	8260.29	36.294	0.005	118.39	0.152	0.152	0.50				
N\$23	8223.32	36.457	0.005	118.93	0.152	0.152	0.50				
N\$22	8171.55	36.688	0.005	119.68	0.152	0.152	0.50				
N\$8	8114.67	36.945	0.005	120.52	0.152	0.152	0.50				
N\$26	8105.46	36.987	0.005	120.66	0.152	0.152	0.50				
N\$24	8006.63	37.444	0.005	122.15	0.152	0.152	0.50				
N\$7	7913.99	37.882	0.005	123.58	0.152	0.152	0.50				
N\$25	7805.23	38.410	0.005	125.30	0.152	0.152	0.50				
NS4	7412.80	40.444	0.005	131.93	0.152	0.152	0.50				
N\$5	7182.18	41.742	0.005	136.17	0.152	0.152	0.50				
N\$13	6598.63	45.434	0.005	148.21	0.152	0.152	0.50				
N\$12	6381.50	46.980	0.005	153.25	0.152	0.152	0.50				
N\$10	6159.05	48.676	0.005	158.79	0.152	0.152	0.50				
N\$11	6033.29	49.691	0.005	162.10	0.152	0.152	0.50				
N\$17	6019.12	49.808	0.005	162.48	0.152	0.152	0.50				
N\$35	5788.66	51.791	0.005	168.95	0.152	0.152	0.50				
N\$6	5580.57	53.722	0.005	175.25	0.152	0.152	0.50				
N\$2	5547.55	54.042	0.005	176.29	0.152	0.152	0.50				
N\$15	5320.47	56.348	0.005	183.81	0.152	0.152	0.50				
N\$18	5138.46	58.344	0.005	190.32	0.152	0.152	0.50				
N\$14	4738.51	63.269	0.005	206.39	0.152	0.152	0.50				
N\$20	4648.13	64.499	0.005	210.40	0.152	0.152	0.50				
N\$36	4609.42	65.041	0.005	212.17	0.152	0.152	0.50				
N\$3	4273.37	70.155	0.005	228.85	0.152	0.152	0.50				
N\$19	3806.30	78.764	0.005	256.94	0.152	0.152	0.50				
N\$1	3792.98	79.041	0.005	257.84	0.152	0.152	0.50				
+3V3	2038.28	147.085	0.005	479.81	0.152	0.152	0.50				
GND	1956.58	153.226	0.005	499.84	0.152	0.152	0.50				

Figure 8: Image licensed under CC-BY 3.0, Author: Rik te Winkel

#### 5.3 Differential routing

For high speed routing differential signals are sometimes used. A differential signal is a complementary signal transferred over 2 wires or PCB traces. For a digital signal this means that when a digital 1 is send the positive trace will be high and the negative trace will be low and when a digital 0 is send it will be the opposite. The advantage of this is that this method is better protected against noise and a lower voltage can be used. Some busses using differential signals are:

- USB
- Ethernet over twisted pair
- PCI Express
- RS485

The same technique can be used for analog signals as well, in balanced audio for example. More information about differential signals can be found <u>here</u>.

Eagle also supports basic differential routing. To make a pair of traces a differential pair the both should have the same name with \_N and \_P at the end. For example ' $USB_N$ ' and ' $USB_P$ '. When you try to route this signal it will be seen as a differential pair and will be routed as one. This means then both traces will be routed at the same time as visible in this image: One of



Figure 9: Image licensed under CC-BY 3.0, Author: Rik te Winkel

the two traces is selected but both will be routed at the same time. To route only one of the two traces, click on the trace to route it and when both traces are selected press escape to only route one of the two traces.

### 6 The actual routing

After making a design plan and looking for things like high speed signals etcetera, it's time to start routing. PCB design is something that can't be learned from books, experience is very important. Going from 2 to 4 layers can make routing easier but it is something to get used to. Don't expect your first PCB to be perfect and don't be afraid to start over.

#### 6.1 What first?

There is no common rule on the order in routing the PCB but it is common practise to route the PCB in 'blocks'. If you have some RAM, Flash, some analog stuff and a FPGA, route it in those blocks. Route the RAM first, then the flash and then the analog part. Routing a bit of RAM, then some flash, then half the analog stuff and then finishing the RAM will most likely result in a bad PCB design. Personally I prefer to do the critical analog routing first, high speed/precision ADC and DAC stuff and power supply traces for high power signals. Then the critical digital routing like RAM, Flash, USB etcetera. After that the non critical stuff and the power supply at last. Of course, this is what I do and not what you have to do. I sometimes route in a different order if I see that it would make the PCB easier to route.

#### 6.2 Supply layers

On a two layer boards it is almost impossible to reserve 1 layer just for a ground plane unless it is a very simple design. On a four layer board reserving one layer for the ground and one for the Vcc is common for a lot of designs. Most of the time the bottom layer will be used for ground, the top layer for the Vcc some other routing and the two internal layers for all the rest. On 6 or 8 layer boards reserving 2 layer for the ground and Vcc is something done in almost all cases. With 8 layer boards it is possible to reserve more then 2 layer for the power in case your design has multiple Vcc voltages, 1.8 and 3.3V for example. If microvia's are no problem and you are working with BGA packages it can be a good idea to use layer 2 for the Vcc. In that way you can access the Vcc layer with a microvia under a BGA pad.

#### 6.3 Component placement

When using BGA packages the only way to effectively place decoupling capacitors is on the bottom of the PCB underneath the BGA. Placing all decoupling capacitors on the bottom can save some space on the top, meaning the PCB can get a bit smaller. Sometimes placing high speed devices like RAM IC's on the bottom can be a good idea as the RAM device can be placed closer to the BGA and the traces can be shorter. of course, placing components on the bottom to is a very effective way to make a PCB smaller. As with 2 layer PCB's, place decoupling capacitors close to the IC, place stuff that belongs to each other close to each other and don't place buttons and connectors on hard to reach places. For example, place an IC for Ethernet close to the Ethernet connector and don't forget that an Ethernet connector is quite big and a pin header next to an Ethernet connector might be hard to reach.

### 7 Tips and tricks

For high speed PCB designs you can get a lot of problems extra. Data that gets lost, one data line acting as an antenna effecting other data lines nearby and other problems. When you also have some high speed or high precision analog parts on the PCB it only gets worse. In this section some tips and tricks are explained that can help when designing high speed PCB's.

High speed signals can, especially on long traces, act like an antenna. Placing a ground plane close to these traces helps against this effect. Making traces shorter and thinner also helps, don't forget, thin traces have a higher resistance. It is also a good practise to keep high speed signals away from the edges of the PCB.

The LSB line of a parallel bus is usually the most used line with the most changes between 1 and 0. it can be wise to route a ground trace next to the LSB line as a form of shielding. When the parallel databus is connected to a second PCB via an IO connector and flat-cable it can be necessary to place some ground lines between the data lines on the flat-cable to prevent crosstalk. On IO connectors it is always a good idea to place multiple ground and voltage lines, when a connector is new the resistance is very low but after a couple of years the resistance will get higher.

All components can act like a resistor, capacitor and inductor to. In general, smaller components are better, a 0402 resistor will behave less like an inductor then a 0805 resistor. There are special resistors when even a small inductance is not allowed that are designed to have an inductance as low as possible. Capacitors have the same problems. Because of these parasitic properties every decoupling capacitor can have problems at a certain frequency. For sensitive parts like an analog ADC or DAC try using different package sizes for decoupling. For example, place 0402 0.1uF's close to the VCC pins and one or two 0603 10uF's close to the IC. The 0.1uF should be places as close as possible to the IC.

### 8 Manufacturing the board

4 and 8 layer boards are standard stuff for most PCB manufacturers nowadays. Prices per PCB are very dependent on clearance, extras like microvia's, amount of PCB's and lead time. For hobbyists these prices are still high compared to the cheap 2 layer services available in China but start to get better.

#### 8.1 Costs for extra options

Extras like microvia's, buried via's or very low clearances will cost more. The prices can differ a lot per PCB manufacturer and it's smart to check with multiple manufacturers what their prices are. In general, buried via's or microvia's will add about 10 to 30% to the price. Going from 0.15mm clearance to 0.125mm or 0.1mm costs about 10 to 15 % extra, smaller than that can be expensive and prices differ a lot between different PCB manufacturers. A lot is possible but the prices will rise proportionally.

#### 8.2 More then 8 layers?

Most motherboards for PC's and mobile phones nowadays have more then 8 layers, 12 or 16 layers are common on that business but more is possible. For small quantities this is very expensive, going from 8 to 12 layers can easily double the price but for very high density this can be necessary. Up to 32 layers is possible with quite some PCB manufacturers but higher is possible at some PCB manufacturers.

#### 8.3 Let the professionals route

Sometimes it can be cheaper or faster to let the PCB design be done externally. External PCB design companies have people that know everything of PCB design so high density multilayer designs is daily business for them. In general, the easier the PCB design the lower the price. If a PCB is possible to route with 6 layer but they can use 8 layers the price will be lower but of course the price of manufacturing the PCB will be higher. <u>Gendreau Microsystems</u> is a company that can do PCB design and they have an online price calculator on their website.

#### 8.4 Example prices

A lot of PCB manufacturers have online price calculators on their websites. For this example I used the online tool from Wurth, you can find it <u>here</u>. For an 8 layer PCB with 0.125mm clearance and 0.15mm drill holes that is 100\*160mm in size is a bit over  $\leq 450$  for one PCB or about  $\leq 830$  for 10 PCB's. Going from 1 to 10 PCB's doesnt even double the price and most of the times when you need 1 or 2 PCB's getting 5 PCB's is not that much more in price but having an extra PCB can be a big time saver in case something goes wrong with the first PCB.

A 4 layer PCB with the same specifications is about  $\in 130$  each or  $\in 330$  for 10 pieces. For a hobbyist these prices are to high in most cases. For small PCB's, smaller then 7.5 by 7.5cm there are two cheaper manufacturers. <u>batchPCB</u> offers 0.15 clearance and trace thickness with 4 layer PCB's for 8 dollars per square inch + 10 dollars setup fee. You get 1 or 2 PCB's but it can take a while before they arrive. <u>DorkbotPDX</u> uses the same design rules but a slightly different pricing. 4 layer PCB's are 10 dollars per square inch but they don't have any setup fee. For that you get 3 PCB's in purple instead of green. The last option is <u>Iteadstudio</u>, they have one affordable option, 10 pieces of 10\*10cm 4 layer boards for \$ 99. For all three the same downsides apply, only 0.15mm clearance and trace thickness and it will take a while before they arrive. If this is no problem the prices are affordable compared to the bigger companies.

### 9 Online tools and examples

#### 9.1 Online tools

There are some online tools to calculate the resistance of a trace, the impedance, the maximum current and more. As Eagle can't do all of this these online tools can be handy in some cases: To calculate the resistance of a trace: <u>Resistance</u>.

To calculate the maximum current for a trace: <u>Current</u>.

To calculate the impedance of a trace or a differential pair: <u>Impedance</u>.

On <u>this site</u> an overview can be found of frequencies and their wavelength,  $\frac{1}{4}$  wavelength,  $\frac{1}{20}$  wavelength and  $\frac{1}{100}$  wavelength. The  $\frac{1}{4}$  and  $\frac{1}{20}$  wavelength are ones to look out for. It is possible to calculate these wavelengths with this <u>online tool</u> but it doesn't support  $\frac{1}{20}$  wavelengths. If you calculate the  $\frac{1}{20}$  wavelength you can calculate the full wavelength and divide that by 20.

#### 9.2 Online examples and documentation

There is a lot of information that can be found for special designs like high speed or high precision designs. Some useful websites: The website of Henry Ott, a ElectroMagnetic Compatibility (EMC) consultant, has a page with a lot of tips and tricks, mostly for keeping EMC low:

Henry Ott Tech Tips

MicroBuilder, who made some ARM dev boards in the past, has some general tips on their website:

Microbuilder OSHW Design Checklist

NXP has 2 app notes that can help, one for BGA design and one for ESD design.

A guide to designing for ESD

PCB layout guidelines for BGA packages

Gendreau Microsystems, a company that does PCB design, has some examples on their website with a small explanation. <u>PCB Design Examples</u>

### 10 References

- [1] Microbuilder OSHW Design Checklist
- [2] <u>NXP Semiconductors</u>
- [3] <u>NXP App note AN10897</u>
- [4] <u>NXP App note AN10778</u>
- [5] <u>Henry Ott Consultants</u>
- [6] <u>Gendreau Microsystems Inc</u>
- [7] <u>Screaming circuits</u>
- [8] <u>Sierra Circuits</u>
- [9] <u>EEWeb</u>
- [10] <u>Wurth Elektronik</u>
- [11] <u>TI Seminar, high resolution PCB layout</u>

### Acronyms

ADC Analog to Digital Converter.
BGA Ball Grid Array.
DAC Digital to Analog Converter.
DRC Design Rule Check.
EMC ElectroMagnetic Compatibility.
FPGA Field Programmable Gate Array.
IC Integrated Circuit.
PCB Printed Circuit Board.
QFN Quad-Flat No-leads package.
RAM Random Access Memory.
ULP User Language Program.
USB Universal Serial Bus.
via Vertical Interconnect Access.

### Glossary

clearance the space between 2 traces on a PCB.

- **crosstalk** the phenomenon that data from one trace can be seen on another trace, happens when traces act like antenna's.
- **decoupling capacitors** a capacitor used as a small localised energy reservoir to decouple a part of the circuit from the power supply.

differential a complementary signal transferred over 2 wires or PCB traces.

high density a PCB with a lot of components in a small space, a mobile phone for example.

trace a line of copper on a PCB.

**wavelength** the distance over which a sine wave repeats at a certain frequency. in electronics a trace as long as the wavelength of the frequency of the signal on it is a very good antenna and can cause crosstalk.