Product Selection Guides

XILINX
ALL PROGRAMMABLE™

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Important: Verify all data in this document with the device data sheets found at www.xilinx.com

		Zynq™-7000 All Programmable SoC									
	Device Name	Z-7010		Z-7020		Z-7030			Z-7045		
	Part Number	XC7Z010		XC7Z020		XC7Z030			XC7Z045		
Processing System	Processor Core	Dual ARM® Cortex™-A9 MPCore™ with CoreSight™									
	Processor Extensions	NEON™ & Single / Double Precision Floating Point for each processor									
	Maximum Frequency	800 MHz				1 GHz					
	L1 Cache	32 KB Instruction, 32 KB Data per processor									
	L2 Cache	512 KB									
	On-Chip Memory	256 KB									
	External Memory Support[1]	DDR3, DDR2, LPDDR2									
	External Static Memory Support[1]	2x Quad-SPI, NAND, NOR									
	DMA Channels	8 (4 dedicated to Programmable Logic)									
	Peripherals	2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO									
	Peripherals w/ built-in DMA[1]	2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO									
	Security[2]	AES and SHA 256b Decryption and Authentication for Secure Boot									
	Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only)	2x AXI 32b Master, 2x AXI 32b Slave, 4x AXI 64b/32b Memory AXI 64b ACP 16 Interrupts									
Programmable Logic	Xilinx 7 Series Programmable Logic Equivalent	Artix™-7 FPGA		Artix™-7 FPGA		Kintex™-7 FPGA			Kintex™-7 FPGA		
	Programmable Logic Cells (Approximate ASIC Gates[3])	28K Logic Cells (~430K)		85K Logic Cells (~1.3M)		125K Logic Cells (~1.9M)			350K Logic Cells (~5.2M)		
	Look-Up Tables (LUTs)	17,600		53,200		78,600			218,600		
	Flip-Flops	35,200		106,400		157,200			437,200		
	Extensible Block RAM (# 36 Kb Blocks)	240 KB (60)		560 KB (140)		1,060 KB (265)			2,180 KB (545)		
	Programmable DSP Slices (18x25 MACCs)	80		220		400			900		
	Peak DSP Performance (Symmetric FIR)	100 GMACs		276 GMACs		593 GMACs			1,334 GMACs		
	PCI Express® (Root Complex or Endpoint)	—		—		Gen2 x4			Gen2 x8		
	Agile Mixed Signal (AMS) / XADC[1]	2x 12 bit, MSPS ADCs with up to 17 Differential Inputs									
	Security[2]	AES and SHA 256b Decryption and Authentication for Secure Programmable Logic Configuration									
Speed Grades	Commercial (0C to 85C)	-1									
	Extended (0C to 100C)	-2, -3									
	Industrial (-40C to 100C)	-1, -2									
Packages	Package Type[4]	**CLG225[1]**	**CLG400**	**CLG400**	**CLG484**	**FBG484**	**FBG676**	**FFG676**	**FBG676**	**FFG676**	**FFG900**
	Size (mm)	13x13	17x17	17x17	19x19	23x23	27x27	27x27	27x27	27x27	31x31
	Pitch (mm)	0.8	0.8	0.8	0.8	1.0	1.0	1.0	1.0	1.0	1.0
	Processing System User I/Os (excludes DDR dedicated I/Os)[5]	32	54	54	54	54	54	54	54	54	54
	Multi-Standards and Multi-Voltage SelectIO™ Interfaces (1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V)	54	100	125	200	100	100	100	100	100	212
	Multi-Standards and Multi-Voltage High Performance SelectIO Interfaces (1.2V, 1.35V, 1.5V, 1.8V)	—	—	—	—	63	150	150	150	150	150
	Serial Transceivers	—	—	—	—	4	4	4	8	8	16
	Maximum Transceiver Speed (Speed Grade Dependant)	N/A	N/A	N/A	N/A	6.6 Gb/s	6.6 Gb/s	12.5 Gb/s	6.6 Gb/s	12.5 Gb/s	12.5 Gb/s

XMP087 (v1.6.1)

Notes: 1. Z-7010 in CLG225 has restrictions on PS peripherals, Memory interfaces and I/Os. Please refer to the Technical Reference Manual for more details.

2. Security block is shared by the Processing System and the Programmable Logic.

3. Equivalent ASIC gate count is dependent of the function implemented. The assumption is 1 Logic Cell = ~15 ASIC Gates.

4. Devices in the same package are pin-to-pin compatible. FBG676 and FFG676 are also pin-to-pin compatible.

5. Static memory interface combined with the usage of many peripherals could require more than 54 I/Os. In that case, the designer can use the Programmable Logic SelectIO interface.

6. Preliminary product information. Subject to change. Please contact your Xilinx representative for the latest information.

Virtex-7 FPGAs
Optimized for Highest System Performance and Capacity

			(1.0V, 0.9V)		(1.0V, 0.9V)							(1.0V)	
	Part Number		XC7V585T	XC7V2000T	XC7VX330T	XC7VX415T	XC7VX485T	XC7VX550T	XC7VX690T	XC7VX980T	XC7VX1140T	XC7VH580T	XC7VH870T
	EasyPath™ Cost Reduction Solutions[1]		XCE7V585T	XCE7V2000T	XCE7VX330T	XCE7VX415T	XCE7VX485T	XCE7VX550T	XCE7VX690T	XCE7VX980T	XCE7VX1140T	—	—
Logic Resources	Slices		91,050	305,400	51,000	64,400	75,900	86,600	108,300	153,000	178,000	90,700	136,900
	Logic Cells		582,720	1,954,560	326,400	412,160	485,760	554,240	693,120	979,200	1,139,200	580,480	876,160
	CLB Flip-Flops		728,400	2,443,200	408,000	515,200	607,200	692,800	866,400	1,224,000	1,424,000	725,600	1,095,200
Memory Resources	Maximum Distributed RAM (Kb)		6,938	21,550	4,388	6,525	8,175	8,725	10,888	13,838	17,700	8,850	13,275
	Block RAM/FIFO w/ ECC (36 Kb each)		795	1,292	750	880	1,030	1,180	1,470	1,500	1,880	940	1,410
	Total Block RAM (Kb)		28,620	46,512	27,000	31,680	37,080	42,480	52,920	54,000	67,680	33,840	50,760
Clocking	CMTs (1 MMCM + 1 PLL)		18	24	14	12	14	20	20	18	24	12	18
I/O Resources	Maximum Single-Ended I/O		850	1,200	700	600	700	600	1,000	900	1,100	600	650
	Maximum Differential I/O Pairs		408	576	336	288	336	288	480	432	528	288	312
Embedded IP Resources	DSP48E1 Slices		1,260	2,160	1,120	2,160	2,800	2,880	3,600	3,600	3,360	1,680	2,520
	PCI Express Gen2		3	4	—	—	4	—	—	—	—	—	—
	PCI Express Gen3		—	—	2	2	—	2	3	3	4	2	3
	Agile Mixed Signal (AMS) / XADC		1	1	1	1	1	1	1	1	1	1	1
	Configuration AES / HMAC Blocks		1	1	1	1	1	1	1	1	1	1	1
	GTX 12.5 Gb/s Transceivers[2]		36	36	—	—	56	—	—	—	—	—	—
	GTH 13.1 Gb/s Transceivers[3]		—	—	28	48	—	80	80	72	96	48	72
	GTZ 28.05 Gb/s Transceivers		—	—	—	—	—	—	—	—	—	8	16
Speed Grades	Commercial		-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2
	Extended[4]		-2L, -3	-2L, -2G	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L	-2L, -2G	-2L, -2G	-2L, -2G
	Industrial		-1, -2	-1	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1	-1	—	—
	Package[5]	Area	Available User I/O: 3.3V SelectI/O™ Pins, 1.8V SelectI/O Pins (GTX, GTH Transceivers)									1.8V SelectIO Pins (GTH, GTZ)	
	Flip chip, fine pitch BGA (1.0 mm ball spacing)												
	FFG1157	35 x 35 mm	0, 600 (20, 0)		0, 600 (0, 20)	0, 600 (0, 20)	0, 600 (20, 0)		0, 600 (0, 20)				
Footprint Compatible	FFG1761	42.5 x 42.5 mm	100, 750 (36, 0)		50, 650 (0, 28)		0, 700 (28, 0)		0, 850 (0, 36)				
	FHG1761	45 x 45 mm		0, 850 (36, 0)									
	FLG1925	45 x 45 mm		0, 1200 (16, 0)									
	FFG1158	35 x 35 mm				0, 350 (0, 48)	0, 350 (48, 0)	0, 350 (0, 48)	0, 350 (0, 48)				
Footprint Compatible	FFG1926	45 x 45 mm							0, 720 (0, 64)	0, 720 (0, 64)			
	FLG1926	45 x 45 mm									0, 720 (0, 64)		
	FFG1927	45 x 45 mm				0, 600 (0, 48)	0, 600 (56, 0)	0, 600 (0, 80)	0, 600 (0, 80)				
Footprint Compatible	FFG1928	45 x 45 mm								0, 480 (0, 72)			
	FLG1928	45 x 45 mm									0, 480 (0, 96)		
Footprint Compatible	FFG1930	45 x 45 mm					0, 700 (24, 0)		0, 1000 (0, 24)	0, 900 (0, 24)			
	FLG1930	45 x 45 mm									0, 1100 (0, 24)		
	Ceramic flip chip, fine pitch BGA (1.0 mm ball spacing)												
	HCG1155	35 x 35 mm										400 (24, 8)	
	HCG1931	45 x 45 mm										600 (48, 8)	650 (48, 8)
	HCG1932	45 x 45 mm										300 (48, 8)	300 (72, 16)

XMP084 (v4.6)

Notes: 1. EasyPath™ solutions provide a fast and conversion-free path for cost reduction.
2. 12.5 Gb/s support in "-3E", "-2GE" speed/temperature grade; 10.3125 Gb/s support in "2C", "-2LE", and "-2I" speed grade.
3. 13.1 Gb/s support in "-3E". "-2GE" speed grade; 11.3 Gb/s support in "2C" , "-2LE" and "-2I" speed/temperature grades.
4. -2G only applies to Stacked Silicon Interconnect devices and supports 12.5G GTX, 13.1G GTH, 28.05G GTZ with -2 fabric.
5. Leaded package options ("FFxxxx"/"FLxxxx"/"FHxxxx"/"HCxxxx") available for all packages.

Kintex-7 FPGAs
Optimized for Best Price-Performance
(1.0V, 0.9V)

	Part Number		XC7K70T	XC7K160T	XC7K325T	XC7K355T	XC7K410T	XC7K420T	XC7K480T
	EasyPath™ Cost Reduction Solutions(1)		—	—	—	XCE7K355T	XCE7K410T	XCE7K420T	XCE7K480T
Logic Resources	Slices		10,250	25,350	50,950	55,650	63,550	65,150	74,650
	Logic Cells		65,600	162,240	326,080	356,160	406,720	416,960	477,760
	CLB Flip-Flops		82,000	202,800	407,600	445,200	508,400	521,200	597,200
Memory Resources	Maximum Distributed RAM (Kbits)		838	2,188	4,000	5,088	5,663	5,938	6,788
	Block RAM/FIFO w/ ECC (36Kbits each)		135	325	445	715	795	835	955
	Total Block RAM (Kbits)		4,860	11,700	16,020	25,740	28,620	30,060	34,380
Clock Resources	CMTs (1 MMCM + 1 PLL)		6	8	10	6	10	8	8
I/O Resources	Maximum Single-Ended I/O		300	400	500	300	500	400	400
	Maximum Differential I/O Pairs		144	192	240	144	240	192	192
Embedded Hard IP Resources	DSP48E1 Slices		240	600	840	1,440	1,540	1,680	1,920
	PCI Express®(2)		1	1	1	1	1	1	1
	Agile Mixed Signal (AMS) / XADC		1	1	1	1	1	1	1
	Configuration AES / HMAC Blocks		1	1	1	1	1	1	1
	GTX 12.5 Gb/s Transceivers		8	8	16	24	16	32	32
Speed Grades	Commercial		-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2
	Extended		-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3
	Industrial		-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2
	Package(4)	Dimensions (mm)	Available User I/O: 3.3V SelectIO™ Pins, 1.8V SelectIO Pins (GTX Transceivers)						
	FBG484	23 x 23	185, 100 (4)	185, 100 (4)					
Footprint Compatible	FBG676	27 x 27	200, 100 (8)	250, 150 (8)	250, 150 (8)		250, 150 (8)		
	FFG676	27 x 27		250, 150 (8)	250, 150 (8)		250, 150 (8)		
Footprint Compatible	FBG900	31 x 31			350, 150 (16)		350, 150 (16)		
	FFG900	31 x 31			350, 150 (16)		350, 150 (16)		
	FFG901	31 x 31				300, 0 (24)		380, 0 (28)	380, 0 (28)
	FFG1156	35 x 35						400, 0 (32)	400, 0 (32)

XMP085 (v3.5)

FBG 1.0mm Lidless flip-chip; **FFG**: 1.0mm Flip-chip fine-pitch

Notes: 1. EasyPath™ solutions provide a fast and conversion-free path for cost reduction.
2. Hard block supports PCI Express Base 2.1 specification at Gen1 and Gen2 data rates. Gen3 supported with soft IP.
3. Leaded package options ("FBxxx" or "FFxxx") available for the following Kintex-7 devices: XC7K160T, XC7K325T, XC7K355T, XC7K410T, XC7K420T, XC7K480T
4. Preliminary product information, subject to change. Please contact your Xilinx representative for the latest information.

Artix™-7 FPGAs
Optimized for Lowest Cost and Lowest Power Applications
(1.0V, 0.9V)

			Artix-7 SL FPGAs (Advance)				Artix-7 SLT FPGAs (Advance)				Artix-7 T FPGAs	
	Part Number		XC7A20SL	XC7A35SL	XC7A50SL	XC7A75SL	XC7A20SLT	XC7A35SLT	XC7A50SLT	XC7A75SLT	XC7A100T	XC7A200T
Logic Resources	Slices		2,500	5,142	8,200	11,194	2,500	5,142	8,200	11,194	15,850	33,650
	Logic Cells		16,000	32,909	52,480	71,642	16,000	32,909	52,480	71,642	101,440	215,360
	CLB Flip-Flops		20,000	41,136	65,600	89,552	20,000	41,136	65,600	89,552	126,800	269,200
Memory Resources	Maximum Distributed RAM (Kbits)		208	453	688	974	208	453	688	974	1,188	2,888
	Block RAM/FIFO w/ ECC (36Kbits each)		30	65	95	125	30	65	95	125	135	365
	Total Block RAM (Kbits)		1,080	2,340	3,420	4,500	1,080	2,340	3,420	4,500	4,860	13,140
Clock Resources	CMTs (1 MMCM + 1 PLL)		3	3	4	4	3	3	4	4	6	10
I/O Resources	Maximum Single-Ended I/O		216	216	300	300	216	216	300	300	300	500
	Maximum Differential I/O Pairs		54	54	72	72	54	54	72	72	144	240
Embedded Hard IP Resources	DSP48E1 Slices		60	120	180	240	60	120	180	240	240	740
	PCI Express®[1]		—	—	—	—	1	1	1	1	1	1
	Agile Mixed Signal (AMS) / XADC		1	1	1	1	1	1	1	1	1	1
	Configuration AES / HMAC Blocks		1	1	1	1	1	1	1	1	1	1
	GTP Transceivers (6.6 Gb/s Max Rate)		—	—	—	—	4	4	8	8	8	16
Speed Grades	Commercial		-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2
	Extended		-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3
	Industrial		-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2
	Package[2, 3]	Dimensions (mm)	Available User I/O: 3.3V SelectI/O™ HR I/O, 3.3V SelectI/O™ HD I/O Pins (GTP Transceivers)								Available User I/O: 3.3V SelectI/O™ HR I/O Pins (GTP Transceivers)	
	CPG236	10 x 10	48, 52	48, 52								
	CSG325	15 x 15	108, 108	108, 108								
	CSG484	19 x 19			144, 156	144, 156						
	CPG237	10 x 10					48, 52 (1)	48, 52 (1)				
	CSG326	15 x 15					108, 77 (4)	108, 77 (4)	108, 77 (4)	108, 77 (4)		
	CSG485	19 x 19					108, 108 (4)	108, 108 (4)	126, 108 (6)	126, 108 (6)		
	FGG677	27 x 27							144, 156 (8)	144, 156 (8)		
	CSG324	15 x 15									210 (0)	
	FTG256	17 x 17									170 (0)	
	SBG484	19 x 19										285 (4)
Footprint Compatible	FGG484	23 x 23									285 (4)	
	FBG484	23 x 23										285 (4)
Footprint Compatible	FGG676	27 x 27									300 (8)	
	FBG676	27 x 27										400 (8)
	FFG1156	35 x 35										500 (16)

XMP086 (v4.2)

CPG: 0.5mm Wire-bond chip-scale; **CSG**: 0.8mm Wire-bond chip-scale; **FTG**: 1.0mm Wire-bond fine-pitch; **SBG**: 0.8mm Lidless flip-chip; **FGG**: 1.0mm Wire-bond fine-pitch; **FBG** 1.0mm Lidless flip-chip; **FFG**: 1.0mm Flip-chip fine-pitch

Notes: 1. Supports PCI Express Base 2.1 specification at Gen1 and Gen2 data rates.
2. Leaded package option available for all packages.
3. Device migration is available within the Artix-7 family for like packages but is not supported between other 7 series families.

			Virtex-6 LXT FPGAs Optimized for High-Performance Logic and DSP with Low-Power Serial Connectivity (1.0V, 0.9V)							Virtex-6 SXT FPGAs Optimized for Ultra High-Performance DSP with Low-Power Serial Connectivity (1.0V, 0.9V)		Virtex-6 HXT FPGAs Optimized for Communications Systems that Require Highest-Bandwidth Serial Connectivity (1.0V)			
	Part Number		XC6VLX75T	XC6VLX130T	XC6VLX195T	XC6VLX240T	XC6VLX365T	XC6VLX550T	XC6VLX760	XC6VSX315T	XC6VSX475T	XC6VHX250T	XC6VHX255T	XC6VHX380T	XC6VHX565T
	EasyPath™ FPGA Cost Reduction Solutions[1]		XCE6VLX75T	XCE6VLX130T	XCE6VLX195T	XCE6VLX240T	XCE6VLX365T	XCE6VLX550T	XCE6VLX760	XCE6VSX315T	XCE6VSX475T	XCE6VHX250T	XCE6VHX255T	XCE6VHX380T	XCE6VHX565T
Logic Resources	Slices[2]		11,640	20,000	31,200	37,680	56,880	85,920	118,560	49,200	74,400	39,360	39,600	59,760	88,560
	Logic Cells[3]		74,496	128,000	199,680	241,152	364,032	549,888	758,784	314,880	476,160	251,904	253,440	382,464	566,784
	CLB Flip-Flops		93,120	160,000	249,600	301,440	455,040	687,360	948,480	393,600	595,200	314,880	316,800	478,080	708,480
Memory Resources	Maximum Distributed RAM (Kb)		1,045	1,740	3,040	3,650	4,130	6,200	8,280	5,090	7,640	3,040	3,050	4,570	6,370
	Block RAM/FIFO w/ECC (36 Kb each)		156	264	344	416	416	632	720	704	1,064	504	516	768	912
	Total Block RAM (Kb)		5,616	9,504	12,384	14,976	14,976	22,752	25,920	25,344	38,304	18,144	18,567	27,648	32,832
Clock Resources	Mixed-Mode Clock Managers (MMCM)		6	10	10	12	12	18	18	12	18	12	12	18	18
I/O Resources[4,5]	Maximum Single-Ended I/O		360	600	600	720	720	1,200	1,200	720	840	320	480	720	720
	Maximum Differential I/O Pairs		180	300	300	360	360	600	600	360	420	160	240	360	360
Embedded Hard IP Resources[6]	DSP48E1 Slices		288	480	640	768	576	864	864	1,344	2,016	576	576	864	864
	PCI Express® Interface Blocks		1	2	2	2	2	2	—	2	2	4	2	4	4
	10/100/1000 Ethernet MAC Blocks		4	4	4	4	4	4	—	4	4	4	2	4	4
	GTX Low-Power Transceivers		12	20	20	24	24	36	—	24	36	48	24	48	48
	GTH High-Speed Transceivers		—	—	—	—	—	—	—	—	—	—	24	24	24
Speed Grades	Commercial		-L1, -1, -2, -3	-L1, -1, -2, -3	-L1, -1, -2, -3	-L1, -1, -2, -3	-L1, -1, -2, -3	-L1, -1, -2	-L1, -1, -2	-L1, -1, -2, -3	-L1, -1, -2	-1, -2, -3	-1, -2, -3	-1, -2, -3	-1, -2
	Extended		—	—	—	—	—	-2	-2	—	-2	—	—	-2	-2
	Industrial		-L1, -1, -2	-L1, -1, -2	-L1, -1, -2	-L1, -1, -2	-L1, -1, -2	-L1, -1	-L1, -1	-L1, -1, -2	-L1, -1	-1, -2	-1, -2	-1, -2	-1
Configuration	Configuration Memory (Mb)		26.3	43.8	61.6	73.9	96.1	144.1	184.9	104.5	156.7	79.9	79.9	119.8	160.7
	Package[7]	Area	Available User I/O: SelectIO™ Interface Pins[4, 5] (GTX Low-Power Transceivers, GTH High-Speed Transceivers)												
FFA Packages (FF): Flip-chip, fine-pitch BGA (1.0 mm ball spacing)															
	FF484	23 x 23 mm	240 (8, 0)	240 (8, 0)											
	FF784	29 x 29 mm	360 (12, 0)	400 (12, 0)	400 (12, 0)	400 (12, 0)									
	FF1156	35 x 35 mm		600 (20, 0)	600 (20, 0)	600 (20, 0)	600 (20, 0)			600 (20, 0)	600 (20, 0)				
	FF1759	42.5 x 42.5 mm				720 (24, 0)	720 (24, 0)	840 (36, 0)		720 (24, 0)	840 (36, 0)				
	FF1760	42.5 x 42.5 mm						1,200 (0, 0)	1,200 (0, 0)						
	FF1154	35 x 35 mm										320 (48, 0)		320 (48, 0)	
	FF1155	35 x 35 mm											440 (24, 12)	440 (24, 12)	
	FF1923	45 x 45 mm											480 (24, 24)	720 (40, 24)	720 (40, 24)
	FF1924	45 x 45 mm												640 (48, 24)	640 (48, 24)

XMP068 (v1.2)

Notes: 1. EasyPath FPGAs provide a conversion-free, low-risk path for volume production.

2. A single Virtex-6 FPGA CLB comprises two slices, each containing four 6-input LUTs and eight flip-flops (twice the number found in a Virtex-4 FPGA slice), for a total of eight 6-input LUTs and 16 flip-flops per CLB.

3. Virtex-6 FPGA logic cell ratings reflect the increased logic capacity offered by the 6-input LUT architecture.

4. Digitally Controlled Impedance (DCI) is available on I/Os of all devices.

5. Supported I/O standards include: HT, LVCMOS (1.2V, 1.5V, 1.8V, 2.5V), HSTL I (1.2V,1.5V,1.8V), HSTL II (1.5V,1.8V), HSTL III (1.5V,1.8V), LVDS, Extended LVDS, RSDS, Bus LVDS, LVPECL, SSTL I (1.8V, 2.5V), SSTL II (1.8V, 2.5V), and SSTL (1.5V).

6. One System Monitor block is included in all devices.

7. All products are available Pb-free and RoHS-Compliant (FFG).

5. Supported I/O standards include: HT, LVDS, LVDSEXT, RSDS, BLVDS, ULVDS, LVPECL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVTTL, PCI33, PCI66, PCI-X, GTL, GTL+, HSTL I (1.2V, 1.5V, 1.8V), HSTL II (1.5V, 1.8V), HSTL III (1.5V, 1.8V), HSTL IV (1.5V, 1.8V), SSTL2 I, SSTL II, SSTL18 I, and SSTL18 II.

			Spartan-6 LX FPGAs Optimized for Lowest-Cost Logic, DSP, and Memory (1.2V, 1.0V)								Spartan-6 LXT FPGAs Optimized for Lowest-Cost Logic, DSP, and Memory with High-Speed Serial Connectivity (1.2V)				
	Part Number		XC6SLX4	XC6SLX9	XC6SLX16	XC6SLX25	XC6SLX45	XC6SLX75	XC6SLX100	XC6SLX150	XC6SLX25T	XC6SLX45T	XC6SLX75T	XC6SLX100T	XC6SLX150T
Logic Resources	Slices[1]		600	1,430	2,278	3,758	6,822	11,662	15,822	23,038	3,758	6,822	11,662	15,822	23,038
	Logic Cells[2]		3,840	9,152	14,579	24,051	43,661	74,637	101,261	147,443	24,051	43,661	74,637	101,261	147,443
	CLB Flip-Flops		4,800	11,440	18,224	30,064	54,576	93,296	126,576	184,304	30,064	54,576	93,296	126,576	184,304
Memory Resources	Maximum Distributed RAM (Kb)		75	90	136	229	401	692	976	1,355	229	401	692	976	1,355
	Block RAM (18 Kb each)		12	32	32	52	116	172	268	268	52	116	172	268	268
	Total Block RAM (Kb) [3]		216	576	576	936	2,088	3,096	4,824	4,824	936	2,088	3,096	4,824	4,824
Clock Resources	Clock Management Tiles (CMT) [4]		2	2	2	2	4	6	6	6	2	4	6	6	6
I/O Resources	Maximum Single-Ended Pins		132	200	232	266	358	408	480	576	250	296	348	498	540
	Maximum Differential Pairs		66	100	116	133	179	204	240	288	125	148	174	249	270
Embedded Hard IP Resources	DSP48A1 Slices [5]		8	16	32	38	58	132	180	180	38	58	132	180	180
	Endpoint Block for PCI Express®		—	—	—	—	—	—	—	—	1	1	1	1	1
	Memory Controller Blocks		0	2	2	2	2	4	4	4	2	2	4	4	4
	GTP Low-Power Transceivers		—	—	—	—	—	—	—	—	2	4	8	8	8
Speed Grades	Commercial[10]		-1L, -2, -3	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-2, -3, -3N	-2, -3, -3N	-2, -3, -3N	-2, -3, -3N	-2, -3, -3N
	Industrial[10]		-1L, -2, -3	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-2, -3, -3N	-2, -3, -3N	-2, -3, -3N	-2, -3, -3N	-2, -3, -3N
Configuration	Configuration Memory (Mb)		2.7	2.7	3.7	6.4	11.9	19.6	26.5	33.8	6.4	11.9	19.6	26.5	33.8
	Package	Body Area	Maximum User I/O: SelectIO™ Interface Pins (GTP Transceivers)[6]												
	Chip Scale Packages (CPG): Pb-free, wire-bond, chip scale BGA (0.5 mm ball spacing)														
	CPG196[7]	8 x 8 mm	106	106	106										
	TQFP Packages (TQG): Pb-free, thin QFP (0.5 mm lead spacing)														
	TQG144[7]	20 x 20 mm	102	102											
	Chip Scale Packages (CSG): Pb-free, wire-bond, chip scale BGA (0.8 mm ball spacing)														
	CSG225[8]	13 x 13 mm	132	160	160										
	CSG324	15 x 15 mm		200	232	226	218				190 (2)	190 (4)			
	CSG484[9]	19 x 19 mm					320	328	338	338		296 (4)	292 (4)	296 (4)	296 (4)
	BGA Packages (FTG): Pb and Pb-free, wire-bond, fine-pitch thin BGA (1.0 mm ball spacing)														
	FT(G)256	17 x 17 mm		186	186	186									
	BGA Packages (FGG): Pb and Pb-free, wire-bond, fine-pitch BGA (1.0 mm ball spacing)														
	FG(G)484[9]	23 x 23 mm				266	316	280	326	338	250 (2)	296 (4)	268 (4)	296 (4)	296 (4)
	FG(G)676	27 x 27 mm					358	408	480	498			348 (8)	376 (8)	396 (8)
	FG(G)900	31 x 31 mm								576				498 (8)	540 (8)

XMP071 (v1.2)

Notes:
1. Each slice contains four LUTs and eight flip-flops.
2. Spartan-6 FPGA logic cell ratings reflect the increased logic capacity offered by the new 6-input LUT architecture.
3. Block RAM are fundamentally 18Kb in size. Each block can also be used as two independent 9 Kb blocks.
4. Each CMT contains two DCMs and one PLL.
5. Each DSP48A1 slice contains an 18x18 multiplier, an adder, and an accumulator.
6. The LX device pinouts are not compatible with the LXT device pinouts.
7. CPG196 and TQG144 do not have memory controller support. -3N is not available for these packages.
8. CSG225 has X8 memory controller support in the LX9 and LX16 devices. There is no memory controller in the LX4 devices.
9. Devices in the FG(G)484 and CSG484 packages have support for two memory controllers.
10. Devices with -3N speed grade do not support MCB functionality

		Virtex-5 LX FPGAs Optimized for High-Performance Logic (1.0V)							Virtex-5 LXT FPGAs Optimized for High-Performance Logic with Low-Power Serial Connectivity (1.0V)							
	Part Number	XC5VLX30	XC5VLX50	XC5VLX85	XC5VLX110	XC5VLX155	XC5VLX220	XC5VLX330	XC5VLX20T	XC5VLX30T	XC5VLX50T	XC5VLX85T	XC5VLX110T	XC5VLX155T	XC5VLX220T	XC5VLX330T
	EasyPath™ FPGA Cost Reduction Solutions[1]	—	—	XCE5VLX85	XCE5VLX110	XCE5VLX155	XCE5VLX220	XCE5VLX330	—	—	—	XCE5VLX85T	XCE5VLX110T	XCE5VLX155T	XCE5VLX220T	XCE5VLX330T
Logic Resources	Slices[2]	4,800	7,200	12,960	17,280	24,320	34,560	51,840	3,120	4,800	7,200	12,960	17,280	24,320	34,560	51,840
	Logic Cells[3]	30,720	46,080	82,944	110,592	155,648	221,184	331,776	19,968	30,720	46,080	82,944	110,592	155,648	221,184	331,776
	CLB Flip-Flops	19,200	28,800	51,840	69,120	97,280	138,240	207,360	12,480	19,200	28,800	51,840	69,120	97,280	138,240	207,360
Memory Resources	Maximum Distributed RAM (Kb)	320	480	840	1,120	1,640	2,280	3,420	210	320	480	840	1,120	1,640	2,280	3,420
	Block RAM/FIFO w/ECC (36 Kb each)	32	48	96	128	192	192	288	26	36	60	108	148	212	212	324
	Total Block RAM (Kb)	1,152	1,728	3,456	4,608	6,912	6,912	10,368	936	1,296	2,160	3,888	5,328	7,632	7,632	11,664
Clock Resources	Digital Clock Managers (DCM)	4	12	12	12	12	12	12	2	4	12	12	12	12	12	12
	Phase-Locked Loop (PLL)/PMCD	2	6	6	6	6	6	6	1	2	6	6	6	6	6	6
I/O Resources[4,5]	Maximum Single-Ended Pins	400	560	560	800	800	800	1,200	172	360	480	480	680	680	680	960
	Maximum Differential I/O Pairs	200	280	280	400	400	400	600	86	180	240	240	340	340	340	480
Embedded Hard IP Resources[6]	DSP48E Slices	32	48	48	64	128	128	192	24	32	48	48	64	128	128	192
	PowerPC® 440 Processor Blocks	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	Endpoint Blocks for PCI Express®	—	—	—	—	—	—	—	1	1	1	1	1	1	1	1
	10/100/1000 Ethernet MAC Blocks	—	—	—	—	—	—	—	2	4	4	4	4	4	4	4
	RocketIO™ GTP Low-Power Transceivers	—	—	—	—	—	—	—	4	8	12	12	16	16	16	24
	RocketIO GTX High-Speed Transceivers	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Speed Grades	Commercial	-1, -2, -3	-1, -2, -3	-1, -2, -3	-1, -2, -3	-1, -2, -3	-1, -2	-1, -2	-1, -2	-1, -2, -3	-1, -2, -3	-1, -2, -3	-1, -2, -3	-1, -2, -3	-1, -2	-1, -2
	Industrial	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1
Configuration	Configuration Memory (Mb)	8.4	12.6	21.9	29.1	41.1	53.2	79.8	6.3	9.4	14.1	23.4	31.2	43.1	55.2	82.7
Package[7]	Area	Available User I/O: SelectIO™ Interface Pins[4,5] (GTP/GTX Serial Transceivers)														
FFA Packages (FF): Flip-chip, fine-pitch BGA (1.0 mm ball spacing)																
FF324	19 x 19 mm	220	220													
FF676	27 x 27 mm	400	440	440	440											
FF1153	35 x 35 mm		560	560	800	800										
FF1760	42.5 x 42.5 mm				800	800	800	1,200								
FF323	19 x 19 mm								172 (4)	172 (4)						
FF665	27 x 27 mm									360 (8)	360 (8)					
FF1136	35 x 35 mm										480 (12)	480 (12)	640 (16)	640 (16)		
FF1738	42.5 x 42.5 mm												680 (16)	680 (16)	680 (16)	960 (24)
FF1156	35 x 35 mm															
FF1759	42.5 x 42.5 mm															

XMP069 (v1.1)

Notes: 1. EasyPath FPGAs provide a conversion-free, low-risk path for volume production.

2. A single Virtex-5 FPGA CLB comprises two slices, each containing four 6-input LUTs and four flip-flops (twice the number found in a Virtex-4 FPGA slice), for a total of eight 6-input LUTs and eight flip-flops per CLB.

3. Virtex-5 FPGA logic cell ratings reflect the increased logic capacity offered by the 6-input LUT architecture.

4. Digitally Controlled Impedance (DCI) is available on I/Os of all devices.

5. Supported I/O standards include: HT, LVDS, LVDSEXT, RSDS, BLVDS, ULVDS, LVPECL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVTTL, PCI33, PCI66, PCI-X, GTL, GTL+, HSTL I (1.2V, 1.5V, 1.8V), HSTL II (1.5V, 1.8V), HSTL III (1.5V, 1.8V), HSTL IV (1.5V, 1.8V), SSTL2 I, SSTL2 II, SSTL18 I, and SSTL18 II.

6. One System Monitor block is included in all devices.

7. All products are available Pb-free and RoHS-Compliant (FFG).

			Virtex-5 SXT FPGAs Optimized for DSP with Low-Power Serial Connectivity (1.0V)				**Virtex-5 FXT FPGAs** Optimized for Embedded Processing with High-Speed Serial Connectivity (1.0V)					**Virtex-5 TXT FPGAs** Optimized for Ultra-High Bandwidth (1.0V)	
	Part Number		XC5VSX35T	XC5VSX50T	XC5VSX95T	XC5VSX240T	XC5VFX30T	XC5VFX70T	XC5VFX100T	XC5VFX130T	XC5VFX200T	XC5VTX150T	XC5VTX240T
	EasyPath™ FPGA Cost Reduction Solutions[1]		—	XCE5VSX50T	XCE5VSX95T	XCE5VSX240T	—	XCE5VFX70T	XCE5VFX100T	XCE5VFX130T	XCE5VFX200T	XCE5VTX150T	XCE5VTX240T
Logic Resources	Slices[2]		5,440	8,160	14,720	37,440	5,120	11,200	16,000	20,480	30,720	23,200	37,440
	Logic Cells[3]		34,816	52,224	94,208	239,616	32,768	71,680	102,400	131,072	196, 608	148,480	239,616
	CLB Flip-Flops		21,760	32,640	58,880	149,760	20,480	44,800	64,000	81,920	122,880	92,800	149,760
Memory Resources	Maximum Distributed RAM (Kb)		520	780	1,520	4,200	380	820	1,240	1,580	2,280	1,500	2,400
	Block RAM/FIFO w/ECC (36 Kb each)		84	132	244	516	68	148	228	298	456	228	324
	Total Block RAM (Kb)		3,024	4,752	8,784	18,576	2,448	5,328	8,208	10,728	16,416	8,208	11,664
Clock Resources	Digital Clock Managers (DCM)		4	12	12	12	4	12	12	12	12	12	12
	Phase-Locked Loop (PLL)/PMCD		2	6	6	6	2	6	6	6	6	6	6
I/O Resources[4,5]	Maximum Single-Ended Pins		360	480	640	960	360	640	680	840	960	680	680
	Maximum Differential I/O Pairs		180	240	320	480	180	320	340	420	480	340	340
Embedded Hard IP Resources[6]	DSP48E Slices		192	288	640	1,056	64	128	256	320	384	80	96
	PowerPC® 440 Processor Blocks		—	—	—	—	1	1	2	2	2	—	—
	Endpoint Blocks for PCI Express®		1	1	1	1	1	3	3	3	4	1	1
	10/100/1000 Ethernet MAC Blocks		4	4	4	4	4	4	4	6	8	4	4
	RocketIO™ GTP Low-Power Transceivers		8	12	16	24	—	—	—	—	—	—	—
	RocketIO GTX High-Speed Transceivers		—	—	—	—	8	16	16	20	24	40	48
Speed Grades	Commercial		-1, -2, -3	-1, -2, -3	-1, -2	-1, -2	-1, -2, -3	-1, -2, -3	-1, -2, -3	-1, -2, -3	-1, -2	-1, -2	-1, -2
	Industrial		-1, -2	-1, -2	-1, -2	-1	-1, -2	-1, -2	-1, -2	-1, -2	-1	-1, -2	-1, -2
Configuration	Configuration Memory (Mb)		13.4	20.0	35.8	79.7	13.6	27.1	39.4	49.3	70.9	43.4	65.8
Package[7]		Area	Available User I/O: SelectIO™ Interface Pins[4, 5] (GTP/GTX Serial Transceivers)										
FFA Packages (FF): Flip-chip, fine-pitch BGA (1.0 mm ball spacing)													
FF324		19 x 19 mm											
FF676		27 x 27 mm											
FF1153		35 x 35 mm											
FF1760		42.5 x 42.5 mm											
FF323		19 x 19 mm											
FF665		27 x 27 mm	360 (8)	360 (8)			360 (8)	360 (8)					
FF1136		35 x 35 mm		480 (12)	640 (16)			640 (16)	640 (16)				
FF1738		42.5 x 42.5 mm				960 (24)			680 (16)	840 (20)	960 (24)		
FF1156		35 x 35 mm										360 (40)	
FF1759		42.5 x 42.5 mm										680 (40)	680 (48)

XMP069 (v1.1)

Notes: 1. EasyPath FPGAs provide a conversion-free, low-risk path for volume production.

2. A single Virtex-5 FPGA CLB comprises two slices, each containing four 6-input LUTs and four flip-flops (twice the number found in a Virtex-4 FPGA slice), for a total of eight 6-input LUTs and eight flip-flops per CLB.

3. Virtex-5 FPGA logic cell ratings reflect the increased logic capacity offered by the new 6-input LUT architecture.

4. Digitally Controlled Impedance (DCI) is available on I/Os of all devices.

5. Supported I/O standards include: HT, LVDS, LVDSEXT, RSDS, BLVDS, ULVDS, LVPECL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVTTL, PCI33, PCI66, PCI-X, GTL, GTL+, HSTL I (1.2V, 1.5V, 1.8V), HSTL II (1.5V, 1.8V), HSTL III (1.5V, 1.8V), HSTL IV (1.5V, 1.8V), SSTL2 I, SSTL2 II, SSTL18 I, and SSTL18 II.

6. One System Monitor block included in all devices.

7. All products are available Pb-free and RoHS-Compliant (FFG).

			CoolRunner™-II Family					
	Part Number		XC2C32A	XC2C64A	XC2C128	XC2C256	XC2C384	XC2C512
Logic Resources	System Gates		750	1,500	3,000	6,000	9,000	12,000
	Macrocells		32	64	128	256	384	512
	Product Terms Per Macrocell		56	56	56	56	56	56
Clock Resources	Global Clocks		3	3	3	3	3	3
	Product Term Clocks Per Function Block		16	16	16	16	16	16
I/O Resources	Maximum I/O		33	64	100	184	240	270
	Input Voltage Compatible		1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3
	Output Voltage Compatible		1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3
Speed Grades	Min. Pin-to-Pin Logic Delay (ns)		3.8	4.6	5.7	5.7	7.1	7.1
	Commercial Speed Grades (Fastest to Slowest)		-4, -6	-5, -7	-6, -7	-6, -7	-7, -10	-7, -10
	Industrial Speed Grades (Fastest to Slowest)		-6	-7	-7	-7	-10	-7[1], -10
	Package[2]	Area[3]	Maximum User I/Os					
	QFN Packages (QFG): Quad, flat, no-lead (0.5 mm lead spacing)							
	QF32[4]	5 x 5 mm	21					
	QF48[4]	7 x 7 mm		37				
	VQFP Packages (VQ): Very thin QFP (VQ44: 0.8 mm lead spacing, VQ100: 0.5 mm lead spacing)							
	VQ44	12 x 12 mm	33	33				
	VQ100	16 x 16 mm		64	80	80		
	Chip Scale Packages (CP): Wire-bond, chip-scale, BGA (0.5 mm ball spacing)							
	CP56	6 x 6 mm	33	45				
	CP132	8 x 8 mm			100	106		
	TQFP Packages (TQ): Thin QFP (0.5 mm lead spacing)							
	TQ100	16 x 16 mm						
	TQ144	22 x 22 mm			100	118	118	
	PQFP Packages (PQ): Wire-bond, plastic, QFP (0.5 mm lead spacing)							
	PQ208	30.6 x 30.6 mm				173	173	173
	FGA Packages (FG): Wire-bond, fine-pitch, BGA (1.0 mm ball spacing)							
	FT256	17 x 17 mm				184	212	212
	FBGA Packages (FG): Wire-bond, fine-line, BGA (1.0 mm ball spacing)							
	FG324	23 x 23 mm					240	270

XMP073 (v2.0)

Notes: 1. -7 speed grade is only available in FT(G)256 package.
2. All packages are available in Pb-Free and RoHS6 compliant versions.
3. Area dimensions for lead-frame product are inclusive of the leads.
4. Only available in RoHS6 compliant and Halogen-free packages.

Xilinx Configuration Memory Cross-Reference

Platform Flash/XL Flash Memory	
Virtex®-6 FPGAs	
XC6VLX75T	XCF32P
XC6VLX130T	XCF128X
XC6VLX195T	XCF128X
XC6VLX240T	XCF128X
XC6VLX365T	XCF128X
XC6VLX760	(2)XCF128X + CPLD
XC6VLX550T	(2)XCF128X + CPLD
XC6VSX315T	XCF128X
XC6VSX475T	(2)XCF128X + CPLD
XC6VHX250T	XCF128X
XC6VHX255T	XCF128X
XC6VHX380T	XCF128X
XC6VHX565T	(2)XCF128X + CPLD
Virtex-5 FPGAs	
XC5VLX30	XCF08P
XC5VLX50	XCF16P
XC5VLX85	XCF32P
XC5VLX110	XCF32P
XC5VLX155	XCF128X
XC5VLX220	XCF128X
XC5VLX330	XCF128X
XC5VLX20T	XCF08P
XC5VLX30T	XCF16P
XC5VLX50T	XCF16P
XC5VLX85T	XCF32P
XC5VLX110T	XCF32P
XC5VLX155T	XCF128X
XC5VLX220T	XCF128X
XC5VLX330T	XCF128X
XC5VSX35T	XCF16P
XC5VSX50T	XCF32P
XC5VSX95T	XCF128X or XCF32P(1)
XC5VSX240T	XCF128X
XC5VFX30T	XCF16P
XC5VFX70T	XCF32P
XC5VFX100T	XCF128X
XC5VFX130T	XCF128X
XC5VFX200T	XCF128X
XC5VTX150T	XCF128X
XC5VTX240T	XCF128X

Platform Flash/XL Flash Memory	
Spartan®-6 FPGAs	
XC6SLX4	XCF04S
XC6SLX9	XCF04S
XC6SLX16	XCF04S
XC6SLX25	XCF08P
XC6SLX25T	XCF08P
XC6SLX45	XCF16P
XC6SLX45T	XCF16P
XC6SLX75	XCF32P
XC6SLX75T	XCF32P
XC6SLX100	XCF32P
XC6SLX100T	XCF32P
XC6SLX150	XCF32P(1)
XC6SLX150T	XCF32P(1)
Virtex-4 FPGAs	
XC4VLX15	XCF08P
XC4VLX25	XCF08P
XC4VLX40	XCF16P
XC4VLX60	XCF32P
XC4VLX80	XCF32P
XC4VLX100	XCF32P
XC4VLX160	XCF32P + XCF08P
XC4VLX200	XCF32P + XCF32P
XC4VFX12	XCF08P
XC4VFX20	XCF08P
XC4VFX40	XCF16P
XC4VFX60	XCF32P
XC4VFX100	XCF32P
XC4VFX140	XCF32P + XCF16P
XC4VSX25	XCF16P
XC4VSX35	XCF16P
XC4VSX55	XCF32P

Platform Flash/XL Flash Memory	
Spartan-3A FPGAs	
XC3S50A	XCF01S
XC3S200A	XCF02S
XC3S400A	XCF02S
XC3S700A	XCF04S
XC3S1400A	XCF08P
Spartan-3A DSP FPGAs	
XC3SD1800A	XCF08P
XC3SD3400A	XCF16P
Spartan-3E FPGAs	
XC3S100E	XCF01S
XC3S250E	XCF02S
XC3S500E	XCF04S
XC3S1200E	XCF04S
XC3S1600E	XCF08P
Spartan-3 FPGAs	
XC3S50	XCF01S
XC3S200	XCF01S
XC3S400	XCF02S
XC3S1000	XCF04S
XC3S1500	XCF08P
XC3S2000	XCF08P
XC3S4000	XCF16P
XC3S5000	XCF16P

Notes: 1. Assumes typical compression benchmarks; compression should be confirmed using ISE® tools

Platform Flash Family Packages and Features

Part Number	XCF01S	XCF02S	XCF04S	XCF08P	XCF16P	XCF32P	XCF128X
Density	1 Mb	2 Mb	4 Mb	8 Mb	16 Mb	32 Mb	128 Mb
JTAG Programmable	Yes	Yes	Yes	Yes	Yes	Yes	Indirect
Serial Configuration	Yes	Yes	Yes	Yes	Yes	Yes	No
SelectMAP Configuration	—	—	—	Yes	Yes	Yes	Yes
Compression	—	—	—	Yes	Yes	Yes	No
Design Rev	—	—	—	Yes	Yes	Yes	Yes
V_{CC} (V)	3.3	3.3	3.3	1.8	1.8	1.8	1.8
V_{CCO} (V)	1.8-3.3	1.8-3.3	1.8-3.3	1.8-3.3	1.8-3.3	1.8-3.3	2.5-3.3
V_{CCJ} (V)	2.5-3.3	2.5-3.3	2.5-3.3	2.5-3.3	2.5-3.3	2.5-3.3	N/A
Clock (MHz)	33	33	33	40	40	40	50
Standard Package	VO20	VO20	VO20	FS48	FS48	FS48	FT64
Pb-Free Package	VOG20	VOG20	VOG20	FSG48	FSG48	FSG48	FTG64
	—	—	—	VOG48	VOG48	VOG48	—

Notes: 1. The iMPACT software tool supports XCF128X JTAG programming indirectly via the Virtex-5 or Virtex-6 FPGA JTAG port.

2. For more information regarding design-in considerations of Platform Flash PROMs, refer to UG161, *Platform Flash User Guide* .

XMP074 (v1.0)

Configuration Hardware Products

Platform Cable USB II - State-of-the-art Xilinx cable with industry-leading performance recommended for new designs. For in-system programming using Xilinx® iMPACT programming software connected via a simple four-wire header to the FPGA, PROM, or CPLD device on target board.

	Xilinx Download Cable Chart
Part Number	Platform Cable USB II
	HW-USB-II-G
Connection to PC	USB 1.1 (Basic Speed) or USB 2.0 (High-Speed)
I/O Voltage Support	1.5V, 1.8V, 2.5V, 3.3V, and 5V
Multiple Cable Management	Yes (Users can easily name and control individual cables through Xilinx iMPACT software)
Input Power Requirements	Bus Powered (+5VDC)
Configuration Modes	JTAG (IEEE Std 1149.1), Slave Serial, IEEE Std 1532, Direct SPI with automatic PROG_B control, Indirect programming of SPI and parallel flash memory devices (1)
Stand-Alone Programming Support	Download cable only
OS Support	Windows XP Professional (32 and 64 bit) Windows Vista (32 and 64 bit)
Xilinx Device Support	All Xilinx FPGAs, CPLDs, Platform Flash PROMs, XC18V00 PROMs, and System ACE™ Tool
Third-Party Flash Memory Support	Direct programming of specific SPI Flash memory devices (1) Indirect programming of specific SPI and parallel flash memory devices (1)
Device and Board Interface	Ribbon cable or flying wires (shipped with both)
RoHS Compliant	Yes
Miscellaneous	Improved target interface protection FPGA-based for feature growth Target system MUX control (PGND) for dynamic JTAG bus sharing
Maximum Target Clock Speed	12 MHz

Notes: 1. See XAPP951 for a list of SPI devices that Xilinx supports via direct programming and XAPP974 for a list of SPI devices that Xilinx supports via indirect programming

Key Configuration Solutions Application Notes

Design Guides for Configuration
Platform Flash XL User Guide - UG438
Platform Flash PROM User Guide - UG161
Bulletproof Configuration Best Practices Guide for Spartan®-3A FPGAs - XAPP986

Configuration Application Notes for In-System Programming and Remote Update
Xilinx In-System Programtming Using an Embedded Microcontroller, a microprocessor solution -XAPP058
Embedded In-System Programming, JTAG ACE Player Solution - XAPP424
Multiple-Boot with Platform Flash PROMs and Spartan-3E FPGAs - XAPP483
A CPLD-Based Configuration and Revision Manager for Xilinx Platform Flash PROMs and FPGAs - XAPP693
Updating a Platform Flash PROM Design Revision In-System Using SVF - XAPP972
Low-Profile In-System Programming Using XCF32P Platform Flash PROMs - XAPP975
MultiBoot with Virtex-5 FPGAs and Platform Flash XL - XAPP1100

Configuration Application Notes for Data Storage
Data storage with Platform Flash XCF02S/XCF04S PROMs - XAPP544

Configuration Application Note for Code Storage
MicroBlaze™ Processor Platform Flash/PROM Boot Loader and User Data Storage - XAPP482

Configuration Application Note for PCI/PCI-X
Dynamic Bus Mode Reconfiguration of PCI-X and PCI Designs - XAPP938

Configuration Application Notes for 3rd Party Flash Memory
A best-practices example using BPI flash for Virtex®-5 FPGAs configuration - XAPP973
A best-practices example using SPI flash for Spartan-3A FPGAs configuration - XAPP974

**To download these application notes, visit the 'Documentation' section at www.xilinx.com/products/design_resources/config_sol/

System ACE Technology

For multiple FPGA configuration and for designs utilizing system-level features, use the System ACE solution.

	System ACE Tool CF
Memory Density	Up to 8 Gb
Number of Components	2
Minimum Board Specifications	25 cm
Compression	No
FPGA Configuration Mode	JTAG
Multiple Designs	Unlimited
Software Storage	Yes
Removable	Yes
IRL Hooks	Yes
Maximum Configuration Speed	30 Mb/s
Nonvolatile Media	CompactFlash

Pb-free solutions are available. For more information about Pb-free solutions, visit www.xilinx.com/pbfree.

XMP074 (v1.0)

ISE Design Suite Device Support	ISE® WebPACK™ Tool	ISE Design Suite Logic Edition Embedded Edition DSP Edition System Edition
Virtex® FPGAs	Virtex-4 FPGAs LX: XC4VLX15, XC4VLX25 SX: XC4VSX25 FX: XC4VFX12	Virtex-4 FPGAs LX: All SX: All FX: All
	Virtex-5 FPGAs LX: XC5VLX30, XC5VLX50 LXT: XC5VLX20T - XC5VLX50T FXT: XC5VFX30T	Virtex-5 FPGAs LX: All LXT: All SXT: All FXT: All
	Virtex-6 FPGAs XCLX75T	Virtex-6 FPGAs All
	Virtex-7 FPGAs None	Virtex-7 FPGAs All
Kintex® FPGAs	Kintex-7 FPGAs XC7K70T, XC7K160T	Kintex-7 FPGAs All
Artix® FPGAs	Artix-7 FPGAs: XC7A100T, XC7A200T	Artix-7 FPGAs: All
Zynq™ Extensible Processing Platform	Zynq-7000 EPP: XC7Z010, XC7Z020, XC7Z030	Zynq-7000 EPP: All
Spartan® FPGAs	Spartan-3 FPGAs XC3S50 - XC3S1500 Spartan-3A FPGAs All Spartan-3AN FPGAs All Spartan-3A DSP FPGAs XC3SD1800A Spartan-3E FPGAs All Spartan-6 FPGAs XC6SLX4 - XC6SLX75T XA (Xilinx Automotive) Spartan-3 FPGAs All XA (Xilinx Automotive) Spartan-6 FPGAs All	Spartan-3 FPGAs: All Spartan-3A FPGAs: All Spartan-3AN FPGAs: All Spartan-3 DSP FPGAs: All Spartan-3E FPGAs: All Spartan-6 FPGAs: All XA (Xilinx Automotive)
CoolRunner™ XPLA3 CoolRunner-II CPLDs	All	
XC9500™ Series	All (Except 9500XV Family)	

ISE Design Suite Comparison Table	ISE WebPACK Tool (Device Limited)	Logic Edition	Embedded Edition	DSP Edition	System Edition
ISE Foundation™ Tools with ISE Simulator (ISim)	√	√	√	√	√
PlanAhead™ Design Analysis Tool	√	√	√	√	√
ChipScope™ Pro Logic Analyzer		√	√	√	√
ChipScope Pro Serial I/O Toolkit		√	√	√	√
Embedded Development Kit (EDK)	√*	√*	√	√*	√
Software Development Kit (SDK)	√	√	√	√	√
System Generator for DSP				√	√

* Device Limited to Zynq-7000 EPP – Z7010, Z7020, Z7030 devices only

Targeted Stand-Alone Products	Usage
Software Development Kit (SDK)	Embedded software developers who do not require ISE tools
ChipScope Pro and ChipScope Pro Serial I/O Toolkit	Lab Environments
Embedded Development Kit (EDK)	ISE WebPACK Tool Users
System Generator for DSP	

ISE Design Suite Operating System Support	Windows XP Professional 32/64-Bit*	Windows 7 Professional 32/64-Bit*	Windows Server 2008	Red Hat Enterprise Linux 5 WS32/64-bit Red Hat Enterprise Linux 6 WS32/65-bit	SUSE Linux Enterprise 11 32/64-bit
ISE Design Entry and Implementation Tools	√	√	√	√	√
ISE Simulator (ISim)	√	√	√	√	√
ISE WebPACK	√	√	√	√	√
ChipScope Pro and ChipScope Pro Serial I/O Toolkit	√	√	√	√	√
Embedded Development Kit (EDK) and Platform Studio	√	√	√	√	√
Software Development Kit (SDK)	√	√	√	√	√
System Generator for DSP	√	√	√	√	√

XMP075 (v3.0)

*US and Japanese: Full Support. Chinese: Limited Support.

		Zynq™-7000Q All Programmable SoC				
	Device Name	Z-7020		Z-7030		Z-7045
	Part Number	XQ7Z020		XQ7Z030		XQ7Z045
Processing System	Processor Core	Dual ARM® Cortex™-A9 MPCore™ with CoreSight™				
	Processor Extensions	NEON™ & Single / Double Precision Floating Point for each processor				
	Maximum Frequency	733 MHz				
	L1 Cache	32 KB Instruction, 32 KB Data per processor				
	L2 Cache	512 KB				
	On-Chip Memory	256 KB				
	External Memory Support	DDR3, DDR2, LPDDR2				
	External Static Memory Support	2x Quad-SPI, NAND, NOR				
	DMA Channels	8 (4 dedicated to Programmable Logic)				
	Peripherals	2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO				
	Peripherals w/ Built-in DMA	2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO				
	Security[1]	AES and SHA 256b Decryption and Authentication for Secure Boot				
	Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only)	2x AXI 32b Master, 2x AXI 32b Slave, 4x AXI 64b/32b Memory AXI 64b ACP 16 Interrupts				
Programmable Logic	Xilinx 7 Series Programmable Logic Equivalent	Artix™-7Q FPGA		Kintex™-7Q FPGA		Kintex™-7Q FPGA
	Programmable Logic Cells (Approximate ASIC Gates[2])	85K Logic Cells (~1.3M)		125K Logic Cells (~1.9M)		350K Logic Cells (~5.2M)
	Look-Up Tables (LUTs)	53,200		78,600		218,600
	Flip-Flops	106,400		157,200		437,200
	Extensible Block RAM (36 Kb Blocks)	560 KB (140)		1,060 KB (265)		2,180 KB (545)
	Programmable DSP Slices (18x25 MACCs)	220		400		900
	PCI Express® (Root Complex or Endpoint)	—		x4 Gen2		x8 Gen2
	Analog Mixed Signal (AMS) / XADC	2x 12 bit, MSPS ADCs with up to 17 Differential Inputs				
	Security[1]	AES and SHA 256b Decryption and Authentication for Secure Programmable Logic Configuration				
Speed Grades	Q-Temp (–40°C to 125°C)	-1				
	Industrial (–40°C to 100°C)	-1, -2				
Packages	Package Type[3]	**CL400**	**CL484**	**RB484[5]**	**RF676**	**RF676**
	Size (mm)	17x17	19x19	23x23	27x27	27x27
	Pitch (mm)	0.8	0.8	1.0	1.0	1.0
	Processing System User I/Os (excludes DDR dedicated I/Os)[4]	54	54	54	54	54
	Multi-Standards and Multi-Voltage SelectIO™ Interfaces (1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V)	125	200	100	100	100
	Multi-Standards and Multi-Voltage High Performance SelectIO Interfaces (1.2V, 1.35V, 1.5V, 1.8V)	—	—	63	150	150
	Serial Transceivers	—	—	4	4	8
	Maximum Transceiver Speed (Speed Grade Dependent)	N/A	N/A	6.6 Gb/s	10.3125 Gb/s	10.3125 Gb/s

XMP092 (v1.0)

Notes: 1. Security block is shared by the Processing System and the Programmable Logic.

2. Equivalent ASIC gate count is dependent of the function implemented. The assumption is 1 Logic Cell = ~15 ASIC Gates.

3. Devices in the same package are pin-to-pin compatible.

4. Static memory interface combined with the usage of many peripherals could require more than 54 I/Os. In that case, the designer can use the Programmable Logic SelectIO interface.

5. RB484 is a ruggedized version of FB484 (4-corner lid added).

6. Preliminary product information. Subject to change. Please contact your Xilinx representative for the latest information.

		Virtex-7Q T FPGAs				
	Part Number	XQ7V585T	XQ7VX330T	XQ7VX485T	XQ7VX690T	XQ7VX980T
Logic Resources	Slices[1]	91,050	51,000	75,900	108,300	153,000
	Logic Cells[2]	582,720	326,400	485,760	693,120	979,200
	CLB Flip-Flops	728,400	408,000	607,200	866,400	1,224,000
Memory Resources	Maximum Distributed RAM (Kb)	6,938	4,388	8,175	10,888	13,838
	Block RAM/FIFO w/ ECC (36 Kb each)	795	750	1,030	1,470	1,500
	Total Block RAM (Kb)	28,620	27,000	37,080	52,920	54,000
Clock Resources	Mixed Mode Clock Managers (MMCM)	18	14	14	20	18
I/O Resources	Maximum Single-Ended I/O[3]	850	700	700	1,000	900
	Maximum Differential I/O Pairs	408	336	336	480	432
Embedded Hard IP Resources	DSP48E1 Slices	1,260	1,120	2,800	3,600	3,600
	PCI Express® Gen 2 Interface Blocks	3	–	4	–	–
	PCI Express Gen 3 Interface Blocks	–	2	–	3	3
	Analog Front End (XADC) / SysMon Blocks	1	1	1	1	1
	Configuration AES / HMAC Blocks	1	1	1	1	1
	GTX 10.3125 Gb/s Transceivers[4]	36	–	28	–	–
	GTH 11.3 Gb/s Transceivers[5]	–	28	–	36	24
Speed Grades	Extended Temp (0° to +100°C)	-2L	-2L	-2L	–	-2L
	Industrial Temp (–40° to +100°C)	-1, -2	-1, -2	-1, -2	-1, -2	-1
	Military Temp (–55° to +125°C)	-1	-1	-1	–	–
Package	**Dimensions (mm)**	**Available User I/O: 3.3V SelectIO™ Pins, 1.8V SelectIO Pins (GTX, GTH Transceivers)**				
RF1157	35 x 35	0, 600 (20, 0)	0, 600 (0, 20)		0, 600 (0, 20)	
RF1761	42.5 x 42.5	100, 750 (36, 0)	50, 650 (0,28)	0, 700 (28,0)	0, 850 (0,36)	
RF1930	45 x 45			0, 700 (24,0)	0, 1000(0,24)	0,900 (0,24)

XMP091 (v1.0)

Notes: 1. A single Virtex-7 FPGA CLB comprises two slices, with each containing four 6-input LUTs and eight Flip-Flops, for a total of eight 6-LUTs and 16 Flip-Flops per CLB.

2. Virtex-7 FPGA logic cell ratings reflect the increased logic capacity offered by the 6-input LUT architecture.
3. Refer to data sheet for details on I/O standards support.
4. 10.3125 Gb/s support in -2 speed grade.
5. 11.3 Gb/s support in -2 speed grade.
6. This is *preliminary product information, subject to change* . Please contact A&D Marketing for the latest information.

			Kintex-7Q T FPGAs	
	Part Number		XQ7K325T	XQ7K410T
Logic Resources	Slices		50,950	63,550
	Logic Cells		326,080	406,720
	CLB Flip-Flops		407,600	508,400
Memory Resources	Maximum Distributed RAM (Kb)		4,000	5,663
	Block RAM/FIFO w/ ECC (36 Kb each)		445	795
	Total Block RAM (Kb)		16,020	28,620
Clock Resources	Mixed Mode Clock Managers (MMCM)		10	10
I/O Resources	Maximum Single-Ended I/O		500	500
	Maximum Differential I/O Pairs		240	240
Embedded Hard IP Resources	DSP48E1 Slices		840	1,540
	PCI Express®[(1)]		1	1
	Analog Front End (XADC) / SysMon Blocks		1	1
	Configuration AES / HMAC Blocks		1	1
	GTX 10.3125 Gb/s Transceivers		16	16
Speed Grades	Extended Temp (0° to +100°C)		-2L	-2L
	Industrial Temp (–40° to +100°C)		-1, -2	-1, -2
	Military Temp (–55° to +125°C)		-1	-1
	Package	**Dimensions (mm)**	**Available User I/O: 3.3V SelectIO™ Pins, 1.8V SelectIO Pins (GTX Transceivers)**	
	RF676	27 x 27	250, 150 (8)	250, 150 (8)
	RF900	31 x 31	350, 150 (16)	350, 150 (16)

XMP090 (v1.0)

Notes: 1. Supports PCI Express Base 2.1 specification at Gen1 and Gen2 data rates.
2. This is *preliminary product information, subject to change.* Please contact A&D Marketing for the latest information.

		Artix-7Q T FPGAs	
	Part Number	XQ7A100T	XQ7A200T
Logic Resources	Slices	15,850	33,650
	Logic Cells	101,440	215,360
	CLB Flip-Flops	126,800	269,200
Memory Resources	Maximum Distributed RAM (Kb)	1,188	2,888
	Block RAM/FIFO w/ ECC (36 Kb each)	135	365
	Total Block RAM (Kb)	4,860	13,140
Clock Resources	Mixed Mode Clock Managers (MMCM)	6	10
I/O Resources	Maximum Single-Ended I/O	285	400
	Maximum Differential I/O Pairs	137	192
Embedded Hard IP Resources	DSP48E1 Slices	240	740
	PCI Express®[1]	1	1
	Analog Front End (XADC) / SysMon Blocks	1	1
	Configuration AES / HMAC Blocks	1	1
	GTP 5.4/ 6.6 Gb/s Transceivers	4	8
Speed Grades	Industrial Temp (–40° to 100°C)	-1, -2	-1, -2
	Military Temp (–55° to 125°C)	-1	-1
Package[2]	**Dimensions (mm)**	**Available User I/O: 3.3V SelectIO™ Pins (GTP Transceivers)**	
CS324	15 x 15	210 (0)	
FG484	23 x 23	285 (4)	
RB484[3]	23 x 23		285 (4)
RB676[3]	27 x 27		400 (8)
RS484[4]	19 x 19		285 (4)

XMP089 (v1.0)

Notes: 1. Supports PCI Express Base 2.1 specification at Gen1 and Gen2 data rates.
2. Design migration is available within the Artix-7Q family for like packages, but is not supported between other 7 Series families. (**CS:** 0.8 mm wire-bond chip-scale. **FG:** 1.0 mm wire-bond fine-pitch.)
3. RB484 & RB676 are ruggedized versions (4-corner lid added) of FB484 and FB676 packages. (**FB:** 1.0 mm flip-chip bare-die.)
4. RS484 is a ruggedized version (4-corner lid added) of SB484 package. Feasibility of this lid is in process. (**SB:** 0.8 mm flip-chip bare-die.)
5. This is *preliminary product information, subject to change.* Please contact A&D Marketing for the latest information.

			Defense-Grade FPGAs			
			Spartan®-6Q FPGAs			
	Part Number		XQ6SLX75	XQ6SLX150	XQ6SLX75T	XQ6SLX150T
Logic Resources	Logic Cells		75,000	147,000	75,000	147,000
	CLB Flip-Flops		93,000	184,000	93,000	184,000
Memory Resources	Maximum Distributed RAM (Kb)		692	1,355	692	1,355
	Block RAM (18 Kb each)		172	268	172	268
	Total Block RAM (Kb)		3,096	4,824	3,096	4,824
Clock Resources	Clock Management Tiles (CMT)		6	6	6	6
Embedded Hard IP Resources	DSP48A1 Slices		132	180	132	180
	Interface Blocks for PCI Express®		—	—	1	1
	Memory Controller Blocks		2	2	4	4
	GTP Low-Power Transceivers		—	—	8	8
Miscellaneous	Speed Grades: Extended (Q: -40°C - 125°C)		—	-2	-2	-2
	Speed Grades: Industrial (I: -40°C - 100°C)		-L1, -2	-L1, -2	-2, -3	-2, -3
	Package	Area	Maximum SelectIO™ Interface Pins (GTP Serial Transceivers)			
	CS(G)484[1,2,3]	19 x 19 mm	328	338	292 (4)	296 (4)
	FG484[2,3]	23 x 23 mm	270	338	268 (4)	296 (4)
	FG(G)676[1]	27 x 27 mm			348 (8)	396 (8)

XMP076 (v2.3)

Notes: 1. Pb-free (additional G) not available for Spartan-6 Q-temp devices.
2. Devices in the CS(G)484 and FG484 support two memory controllers.
3. Due to the GTP transceivers in the LXT devices, pinouts for the LX and LXT devices are not compatible.

		Defense-Grade FPGAs													
		Virtex®-5Q FPGAs													
	Part Number	XQ5VLX30T	XQ5VLX85	XQ5VLX110	XQ5VLX110T	XQ5VLX155T	XQ5VLX220T	XQ5VLX330T	XQ5VSX50T	XQ5VSX95T	XQ5VSX240T	XQ5VFX70T	XQ5VFX100T	XQ5VFX130T	XQ5VLX200T
Logic Resources	Slices[2]	4,800	12,960	17,280	17,280	24,320	34,560	51,840	8,160	14,720	37,440	11,200	16,000	20,480	30,720
	Logic Cells[3]	30,720	82,944	110,592	110,592	155,648	221,184	331,776	52,224	94,208	239,616	71,680	102,400	131,072	196,608
	CLB Flip-Flops	19,200	51,840	69,120	69,120	97,280	138,240	207,360	32,640	58,880	149,670	44,880	64,000	81,920	122,880
Memory Resources	Maximum Distributed RAM (Kb)	320	840	1,120	1,120	1,640	2,280	3,420	780	1,520	4,200	820	1,240	1,580	2,280
	Block RAM/FIFO w/ECC (36 Kb each)	36	96	128	148	212	212	324	132	244	516	148	228	298	456
	Total Block RAM (Kb)	1,296	3,456	4,608	5,328	7,632	7,632	11,664	4,752	8,784	18,576	5,328	8,208	10,728	16,416
Clock Resources	Digital Clock Manager (DCM)	4	12	12	12	12	12	12	12	12	12	12	12	12	12
I/O Resources	Phase-Locked Loop/PMCD	2	6	6	6	6	6	6	6	6	6	6	6	6	6
	Maximum Single-Ended Pins	360	560	800	680	680	680	960	480	640	960	640	680	840	960
	Maximum Differential I/O Pairs	180	280	400	340	340	340	480	240	320	480	320	340	420	480
Embedded Hard IP Resources	DSP48E Slices	32	48	64	64	128	128	192	288	640	1,056	128	256	320	384
	PowerPC® 440 Processor Blocks	—	—	—	—	—	—	—	—	—	—	1	2	2	2
	Interface Blocks for PCI Express®	1	—	—	1	1	1	1	1	1	1	3	3	3	4
	10/100/1000 Ethernet MAC Blocks	4	—	—	4	4	4	4	4	4	4	4	4	6	8
	RocketIO™ GTP Low-Power Transceivers	8	—	—	16	16	16	24	12	16	24	—	—	—	—
	RocketIO GTX High-Speed Transceivers	—	—	—	—	—	—	—	—	—	—	16	16	20	24
Configuration	Configuration Memory (Mb)	9.4	21.9	29.1	31.2	43.1	55.2	82.7	20	35.8	79.7	27.1	39.4	49.3	70.9
Miscellaneous	Speed Grades	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1	-1	-1, -2	-1	-1	-1, -2	-1, -2	-1, -2	-1
	Manufacturing Grades	I	I	I	I	I	I	I	I	I	I	I, M[7]	I, M[7]	I	I
Package	Area	Available User I/O: SelectIO™ Interface Pins[4] (GTP/GTX Serial Transceivers)													
EF676	27 x 27 mm		440	440											
EF1153	35 x 35 mm			800											
FF323	19 x 19 mm	172 (4)													
EF665	27 x 27 mm								360 (8)			360 (8)			
EF1136	35 x 35 mm				640 (16)	640 (16)				640 (16)		640 (16)	640 (16)		
EF1738	42.5 x 42.5 mm						680 (16)	960 (24)					680 (16)	840 (20)	
FF1738	42.5 x 42.5 mm										960 (24)				960 (24)

XMP076 (v2.3)

Notes: 1. A single Virtex-5Q FPGA CLB comprises two slices, with each containing four 6-input LUTs and four flip-flops (twice the number found in a Virtex-4 FPGA slice), for a total of eight 6-LUTs and eight flip-flops per CLB.

2. Virtex-5 FPGA logic cell ratings reflect the increased logic capacity offered by the new 6-input LUT architecture.

3. Digitally Controlled Impedance (DCI) is available on I/Os of all devices.

4. I/O standards supported: HT, LVDS, LVDSEXT, RSDS, BLVDS, ULVDS, LVPECL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVTTL, PCI33, PCI66, PCI-X, GTL, GTL+, HSTL I (1.2V,1.5V,1.8V), HSTL II (1.5V,1.8V), HSTL III (1.5V,1.8V), HSTL IV (1.5V,1.8V), SSTL2 I, SSTL2 II, SSTL18 I, and SSTL18 II.

5. One system monitor block included in all devices.

6. Available I/O for each device-package combination: number of SelectIO interface pins (number of RocketIO transceivers).

7. M-grade available only in -1 speed grade and EF1136 package.

Manufacturing Grades

http://www.xilinx.com/products/milaero/rpt003.pdf

Grade	Description	Temperature
V	Xilinx V-Grade Flow[1] Military Ceramic	T_j = –55°C to +125°C
H	Flip-Chip Radiation Tolerant Ceramic	T_j = –55°C to +125°C
B	SMD Radiation Tolerant and Non-RT SMD Military Ceramic	T_j = –55°C to +125°C
N	Military Plastic	T_j = –55°C to +125°C
M	Military Ceramic or Plastic	T_j = –55°C to +125°C
I	Industrial Plastic	T_j = -40°C to +100°C

Notes: 1. Per ADQ0007

		Defense-Grade FPGAs												
		Virtex®-4Q FPGAs								Virtex-II Pro XQ FPGAs		Virtex-II XQ FPGAs		
	Part Number	XQ4VLX25	XQ4VLX40	XQ4VLX60	XQ4VLX100	XQ4VLX160	XQ4VSX55	XQ4VFX60	XQ4VFX100	XQ2VP40	XQ2VP70	XQ2V1000	XQ2V3000	XQ2V6000
	Core Voltage	1.2V	1.2V	1.2V	1.2V	1.2V	1.2V	1.2V	1.2V	1.5V	1.5V	1.5V	1.5V	1.5V
Logic Resources	Slices[1]	10,752	18,432	26,624	49,152	67,584	24,576	25,280	42,176	19.392	33,088	5,120	14,336	33,792
	Logic Cells	24,192	41,472	59.904	110,592	152,064	55,296	56,880	94,896	44,632	74,448	11,520	32,256	76,032
	CLB Flip-Flops	21,504	36,864	53,248	98,304	135,168	49,152	50,560	84,352	38,784	66,176	10,240	28,672	67,584
Memory Resources	Maximum Distributed RAM (Kb)	168	288	416	768	1,056	384	395	659	606	1,034	160	448	1,056
	Block RAM/FIFO w/ECC (36 Kb each)	72	96	160	240	288	320	232	376	192	328	40	96	144
	Total Block RAM (Kb)	1,296	1,728	2,880	4,320	5,184	5,760	4,176	6,768	3,456	5,904	720	1,728	2,592
Clock Resources	Digital Clock Manager (DCM)	8	8	8	12	12	8	12	12	8	8	8	12	12
I/O Resources	Maximum Single-Ended I/Os	448	640	640	960	960	640	576	768	804	996	432	720	1,104
	Maximum Differential I/O Pairs	224	320	320	480	480	320	228	384	396	492	216	360	552
	Digitally Controlled Impedance	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Embedded Hard IP Resources	DSP Slices	48	64	64	96	96	512	128	160	—	—	—	—	—
	18 x 18 Multipliers	—	—	—	—	—	—	—	—	192	328	40	96	144
	RocketIO™ Transceivers	—	—	—	—	—	—	16	20	8 or 12	20	—	—	—
	PowerPC® Processor Blocks	—	—	—	—	—	—	2	2	2	2	—	—	—
Miscellaneous	Speed Grades	-10	-10	-10	-10	-10	-10	-10	-10	-5	-5	-4	-4	-4
	Configuration Memory (Mb)	4.8	12.3	17.7	30.7	40.3	22.7	21	33	15.5	25.6	4.1	10.5	21.9
	Manufacturing Grades	M	I, M	M	I	I	M	I, M	I	N	N	N	M, N, B	M
	Packages	SF363, FF668	FF668	‘668, FF1148, EF6	FF1148	FF1148	FF1148	EF672, FFG1152*	FF1152	FF1152, FG676	FF1704	FG456, BG575	CG717, BG728	CF1144

XMP076 (v2.3)

Notes: 1. Each slice comprises two 4-input logic function generators (LUTs), two storage elements, wide-function multiplexers, and carry logic.

Manufacturing Grades
http://www.xilinx.com/products/milaero/rpt003.pdf

Grade	Description	Temperature
V	Device Xilinx V-Grade Flow[1] Military Ceramic	T_J = –55°C to +125°C
H	Device Flip-Chip Radiation Tolerant Ceramic	T_J = –55°C to +125°C
B	SMD Radiation Tolerant and Non-RT SMD Military Ceran	T_J = –55°C to +125°C
N	Military Plastic	T_J = –55°C to +125°C
M	Military Ceramic or Plastic	T_J = –55°C to +125°C
I	Industrial Plastic	T_J = –40°C to +100°C

Notes: 1. Per ADQ0007.

		Space-Grade Devices							
		Virtex®-5QV FPGAs	Virtex-4QV FPGAs				Virtex-II XQR FPGAs	Virtex XQR FPGAs	
	Part Number	XQR5VFX130	XQR4VLX200	XQR4VSX55	XQR4VFX60	XQR4VFX140	XQR2V3000	XQVR300	XQVR600
	Core Voltage	1.0V	1.2V	1.2V	1.2V	1.2V	1.5V	2.5V	2.5V
Logic Resources	Slices[1]	20,480	89,088	24,576	25,280	63,168	14,336	3,072	6,912
	Logic Cells	130,000	200,448	55,296	56,880	142,128	32,256	6,912	15,552
	CLB Flip-Flops	81920	178,176	49,152	50,560	126,336	28,672	6,144	13,824
Memory Resources	Maximum Distributed RAM (Kb)	1580	1,392	384	395	987	448	1,711	3,523
	Block RAM/FIFO w/ECC (36 Kb each)	298	—	—	—	—	—	—	—
	Block RAM/FIFO (18 Kb each)	596	336	320	232	552	96	—	—
	Block RAM (4 Kb each)	—	—	—	—	—	—	16	24
	Total Block RAM (Kb)	10,728	6,048	5,760	4,176	9,936	1,728	64	96
Clock Resources	Digital Clock Manager (DCM)	12	12	8	12	20	12	–	—
	Phase Lock Loop (PLL)	6	—	—	—	—	—	—	—
	Delay Lock Loop (DLL)	—	—	—	—	—	—	4	4
I/O Resources	Maximum Single-Ended I/Os	836	960	640	576	896	720	316	316
	Maximum Differential I/O Pairs	414	480	320	288	448	360	–	—
	Digitally Controlled Impedance	Yes	Yes	Yes	Yes	Yes	Yes	—	—
Embedded Hard IP Resources	Enhanced DSP Slices (DSP48E)	320	—	—	—	—	—	—	—
	DSP Slices	—	96	512	128	192	—	—	—
	18 x 18 Multipliers	—	—	—	—	—	96	—	—
	10/100/100 Ethernet MAC Blocks	6	—	—	4	4	—	—	—
	PowerPC® Processor Blocks	—	—	—	2	2	—	—	—
	Multi-Gigabit Serial Trasceivers (MGT)	18	—	—	—	—	—	—	—
Miscellaneous	Speed Grades	-1	-10	-10	-10	-10	-4	-4	-4
	Configuration Memory (Mb)	49.2	51.4	22.7	21.0	47.9	10.5	1.7	3.5
	Manufacturing Grades	V	V	V	V	V	M, V	M, V, B	M, V, B
	Total Ionizing Dose (krad(Si))	1000	300	300	300	300	200	100	100
	SEL Immunity (MeV-cm2/mg)	>125	>125	>125	>125	>125	>160	>125	>125
Package[2]	Area	Available User I/Os							
CGA Packages (CG): Ceramic column grid array (1.27 mm ball spacing)									
CG717[3]	35 x 35 mm						516		
CFA Packages (CF): Flip-chip, ceramic column grid array (1.0 mm ball spacing)									
CF1144[4]	35 x 35 mm				576				
CF1140[5]	35 x 35 mm			640					
CF1509[6]	40 x 40 mm		960			768			
CF1752[7]	45 x 45 mm	836							
CQFP Packages (CB): Ceramic, brazed, quad flat pack (0.025 inch lead spacing)									
CB228	1.55 x 1.55 in							162	162

XMP077 (v2.1)

Notes: 1. Each slice comprises two 4-input logic function generators (LUTs), two storage elements, wide-function multiplexers, and carry logic.

2. For information on DSCC SMD availability, contact Xilinx.
3. The BG728 and CG717 packages are footprint/pin compatible.
4. The CF1144 and FF1152 packages are footprint/pin compatible.
5. The CF1140 and FF1148 packages are footprint/pin compatible.
6. For the XQR4VLX200, the CF1509 and FF1513 packages are footprint/pin compatible. For the XQR4VFX140, the CF1509 and the FF1517 are footprint/pin compatible.
7. The CF1752 and FF1738 are footprint/pin compatible.

Manufacturing Grades
http://www.xilinx.com/products/milaero/rpt003.pdf

Grade	Description	Temperature
V	Device Xilinx V-Grade Flow[1] Military Ceramic	T_C = –55°C to +125°C
H	Device Flip-Chip Radiation Tolerant Ceramic	T_j = –55°C to +125°C
B	SMD Radiation Tolerant and Non-RT SMD Military Ceramic	T_C = –55°C to +125°C
N	Military Plastic	T_j = –55°C to +125°C
M	Military Ceramic or Plastic	T_j = –55°C to +125°C (Plastic), T_C = –55°C to +125°C (Ceramic)
I	Industrial Plastic	T_j = –40°C to +100°C

Notes: 1. Per ADQ0007.

		Defense-Grade Configuration PROMs				**Space-Grade Devices** Radiation Tolerant Configuration PROMs	
Part Number		XQ1701L	XQ17V16	XQ18VQ4	XQF32P	XQR1701L	XQR17V16
Core Voltage[1]		3.3V	3.3V	3.3V	3.3V	3.3V	3.3V
Storage Bits		1M	16M	4M	32M	1M	16M
Manufacturing Grades		M, N	M, N	N	M	M, V	M, V
Total Ionizing Dose (krad)		—	—	—	—	50	50
Packages		CC44, VQ44	CC44, VQ44	VQ44	VQ48	CC44	CC44
Package[2]	Area						
CC44	0.69 x 0.69 in						
VQ44	12 x 12 mm						
VQ48	20 x 20 mm						

Notes: 1. Xilinx configuration PROMs have adjustable I/O voltages for compatibility with all Xilinx FPGAs.
2. The CC44 and PC44 packages are footprint/pin compatible. For information on DSCC qualification contact Xilinx.

Manufacturing Grades
http://www.xilinx.com/products/milaero/rpt003.pdf

Grade	Description	Temperature
V	Device Xilinx V-Grade Flow[1] Military Ceramic	T_C = –55°C to +125°C
H	Device Flip-Chip Radiation Tolerant Ceramic	T_J = –55°C to +125°C
B	SMD Radiation Tolerant and Non-RT SMD Military Ceramic	T_C = –55°C to +125°C
N	Military Plastic	T_J = –55°C to +125°C
M	Military Ceramic or Plastic	T_J = –55°C to +125°C (Plastic), T_C = –55°C to +125°C (Ceramic)
I	Industrial Plastic	T_J = –40°C to +100°C

XMP078 (v1.0)

Notes: 1. Per ADQ0007.

		XA Zynq™-7000 All Programmable SoC			
	Device Name	Z-7010		Z-7020	
	Part Number	XA7Z010		XA7Z020	
Processing System	Processor Core	Dual ARM® Cortex™-A9 MPCore™ with CoreSight™			
	Processor Extensions	NEON™ & Single / Double Precision Floating Point for each processor			
	Maximum Frequency	667 MHz			
	L1 Cache	32 KB Instruction, 32 KB Data per processor			
	L2 Cache	512 KB			
	On-Chip Memory	256 KB			
	External Memory Support[1]	DDR3, DDR2, LPDDR2			
	External Static Memory Support[1]	2x Quad-SPI, NAND, NOR			
	DMA Channels	8 (4 dedicated to Programmable Logic)			
	Peripherals	2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO			
	Peripherals w/ built-in DMA[1]	2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO			
	Security[2]	AES and SHA 256b Decryption and Authentication for Secure Boot			
	Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only)	2x AXI 32b Master, 2x AXI 32b Slave, 4x AXI 64b/32b Memory AXI 64b ACP 16 Interrupts			
Programmable Logic	Xilinx 7 Series Programmable Logic Equivalent	Artix™-7 FPGA		Artix™-7 FPGA	
	Programmable Logic Cells (Approximate ASIC Gates[3])	28K Logic Cells (~430K)		85K Logic Cells (~1.3M)	
	Look-Up Tables (LUTs)	17,600		53,200	
	Flip-Flops	35,200		106,400	
	Extensible Block RAM (# 36 Kb Blocks)	240 KB (60)		560 KB (140)	
	Programmable DSP Slices (18x25 MACCs)	80		220	
	Peak DSP Performance (Symmetric FIR)	74 GMACs		204 GMACs	
	Agile Mixed Signal (AMS) / XADC[1]	2x 12 bit, MSPS ADCs with up to 17 Differential Inputs			
	Security[2]	AES and SHA 256b Decryption and Authentication for Secure Programmable Logic Configuration			
Speed Grades	Industrial (-40C to 100C)	-1			
	Automotive (-40C to 125C)	-1			
Packages	Package Type[4]	**CLG225[1]**	**CLG400**	**CLG400**	**CLG484**
	Size (mm)	13x13	17x17	17x17	19x19
	Pitch (mm)	0.8	0.8	0.8	0.8
	Processing System User I/Os (excludes DDR dedicated I/Os)[5]	32	54	54	54
	Multi-Standards and Multi-Voltage SelectIO™ Interfaces (1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V)	54	100	125	200

XMP088 (v1.0)

Notes:
1. Z-7010 in CLG225 has restrictions on PS peripherals, Memory interfaces, and I/Os. Please refer to the Technical Reference Manual for more details.
2. Security block is shared by the Processing System and the Programmable Logic.
3. Equivalent ASIC gate count is dependent of the function implemented. The assumption is 1 Logic Cell = ~15 ASIC Gates.
4. Devices in the same package are pin-to-pin compatible.
5. Static memory interface combined with the usage of many peripherals could require more than 54 I/Os. In that case, the designer can use the Programmable Logic SelectIO interface.
6. Preliminary product information. Subject to change. Please contact your Xilinx representative for the latest information.

			Spartan®-6 LX FPGAs Optimized for Lowest-Cost Logic, DSP, and Memory (1.2V)							Spartan-6 LXT FPGAs Optimized for Lowest-Cost Logic, DSP, and Memory with High-Speed Serial Connectivity (1.2V)		
		Part Number	XA6SLX4[10,11]	XA6SLX9	XA6SLX16	XA6SLX25[10]	XA6SLX45	XA6SLX75	XA6SLX100	XA6SLX25T[10]	XA6SLX45T	XA6SLX75T
Logic Resources		Slices[1]	600	1,430	2,278	3,758	6,822	11,662	15,822	3,758	6,822	11,662
		Logic Cells[2]	3,840	9,152	14,579	24,051	43,661	74,637	101,261	24,051	43,661	74,637
		CLB Flip-Flops	4,800	11,440	18,224	30,064	54,576	93,296	126,576	30,064	54,576	93,296
Memory Resources		Maximum Distributed RAM (Kb)	75	90	136	229	401	692	976	229	401	692
		Block RAM (18 Kb each)	12	32	32	52	116	172	268	52	116	172
		Total Block RAM (Kb)[3]	216	576	576	936	2,088	3,096	4,824	936	2,088	3,096
Clock Resources		Clock Management Tiles (CMT)[4]	2	2	2	2	4	6	6	2	4	6
I/O Resources		Maximum Single-Ended Pins	132	200	232	266	316	280	326	250	296	268
		Maximum Differential Pairs	66	100	116	133	158	140	163	125	148	134
Embedded Hard IP Resources		DSP48A1 Slices[5]	8	16	32	38	58	132	180	38	58	132
		Endpoint Block for PCI Express®	—	—	—	—	—	—	-	1	1	1
		Memory Controller Blocks	0	2	2	2	2	2	2	2	2	2
		GTP Low-Power Transceivers	—	—	—	—	—	—	-	2	4	4
		Speed Grade	-2, -3	-2, -3	-2, -3	-2, -3	-2, -3	-2, -3	-2	-2, -3	-2, -3	-2, -3
Miscellaneous		Temperature Grade[6]	I, Q	I, Q	I, Q	I, Q	I, Q	I, Q	I, Q	I, Q	I, Q	I, Q
		XA Released	Q3 2011	Q3 2011	Q3 2011	Q3 2011	Yes	Yes	Q3 2011	Q3 2011	Q3 2011	Yes
Configuration		Configuration Memory (Mb)	2.7	2.7	3.7	6.4	11.9	19.6	26.5	6.4	11.9	19.6
	Package	Area										
	Chip Scale Packages (CSG): Pb-free wire-bond, chip-scale, BGA (0.8 mm ball spacing)											
	CSG225[8]	13 x 13 mm	132	160	160							
	CSG324	15 x 15 mm		200	232	226	218			190 (2)	190 (4)	
	BGA Packages (FTG): Pb-free wire-bond, fine-pitch, thin BGA (1.0 mm ball spacing)											
	FTG256	17 x 17 mm		186	186	186						
	BGA Packages (FGG): Pb-free wire-bond, fine-pitch, BGA (1.0 mm ball spacing)											
	FGG484[9]	23 x 23 mm				266	316	280	326	250 (2)	296 (4)	268 (4)

XMP079 (v2.0)

Notes: 1. Each slice contains four LUTs and eight flip-flops.

2. Spartan-6 FPGA logic cell ratings reflect the increased logic capacity offered by the new 6-input LUT structure.

3. Block RAM are fundamentally 18 Kb in size. Each block can also be used as two independent 9 Kb blocks.

4. Each CMT contains two DCMs and one PLL.

5. Each DSP48A1 slice contains an 18x18 multiplier, an adder, and an accumulator.

6. Temperature Range Automotive I (T_j = –40°C to +100°C); Automotive Q (T_j = –40°C to + 125°C).

7. The LX device pinouts are not compatible with the LXT devices.

8. CSG225 has memory controller support in the LX9 and LX16 devices. There is no memory controller in the XA6SLX4 devices.

9. Devices in the FGG484 have support for two memory controllers.

10. BPI configuration mode not available.

11. SelectMAP configuration modes not available.

Preliminary product information, subject to change. Please contact your Xilinx representative for the latest information.

		Spartan®-3 FPGAs					Spartan-3E FPGAs				
	Part Number	XA3S50	XA3S200	XA3S400	XA3S1000	XA3S1500	XA3S100E	XA3S250E	XA3S500E	XA3S1200E	XA3S1600E
Logic Resources	System Gates[1]	50K	200K	400K	1,000K	1,500K	100K	250K	500K	1,200K	1,600K
	Slices[2]	768	1,920	3,584	7,680	13,312	960	2,448	4,656	8,672	14,752
	Logic Cells	1,728	4,320	8,064	17,280	29,952	2,160	5,508	10,476	19,512	33,192
	CLB Flip-Flops	1,536	3,840	7,168	15,360	26,624	1,920	4,896	9,312	17,344	29,504
Memory Resources	Maximum Distributed RAM (Kb)	12	30	56	120	208	15	38	73	136	231
	Block RAM Blocks	4	12	16	24	32	4	12	20	28	36
	Total Block RAM (Kb)	72	216	288	432	576	72	216	360	504	648
Clock Resources	Digital Clock Managers (DCMs)	2	4	4	4	4	2	4	4	8	8
I/O Resources	Maximum Single-Ended I/Os	124	173	264	333	487	108	172	190	304	376
	Maximum Differential I/O Pairs	56	76	116	149	221	40	68	77	124	156
	I/O Standards Supported	LVTTL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVCMOS12, HSTL15 Class I, HSTL15 Class III, HSTL18 Class I, HSTL18 Class II, HSTL18 Class III, PCI 3.3V 32/64-bit 33 MHz, SSTL3 Class I, SSTL3 Class II, SSTL2 Class I, SSTL2 Class II, SSTL18 Class I, SSTL18 Class II, Bus LVDS, LVDS25, LVDS33, LVPECL25, LVPECL33, Mini-LVDS25, Mini-LVDS33, RSDS25, RSDS33, TMDS25, TMDS33, PPDS25, and PPDS33					LVTTL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVCMOS12, HSTL18 Class I, HSTL18 Class III, PCI 3.3V 32/64-bit 33 MHz, SSTL2 Class I, SSTL18 Class I, Bus LVDS, LVDS25, LVPECL25, Mini-LVDS25, and RSDS25				
Embedded Hard IP Resources	DSP48A Slices	—	—	—	—	—	—	—	—	—	—
	Dedicated Multipliers	4	12	16	24	32	4	12	20	28	36
	Device DNA Security	—	—	—	—	—	—	—	—	—	—
Miscellaneous	Temperature Grades[4]	I, Q	I, Q	I, Q	I, Q	I	I, Q	I, Q	I, Q	I, Q	I, Q
	Speed Grade	-4	-4	-4	-4	-4	Yes	-4	-4	-4	-4
	RoHS (Pb-free)	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	XA Released	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Configuration	Configuration Memory (Mb)	0.4	1	1.7	3.2	5.2	0.6	1.4	2.3	3.8	6
Package	Footprint Area	Maximum User I/Os									
VQFP Packages (VQ): Very thin, QFP (0.5 mm lead spacing)											
VQG100	16 x 16 mm	63	63				66	66			
Chip Scale Packages (CP): Wire-bond, chip-scale, BGA (0.5 mm ball spacing)											
CPG132	8 x 8 mm						83	92	92		
TQFP Packages (TQ): Thin QFP (0.5 mm lead spacing)											
TQG144	22 x 22 mm		97				108	108			
PQFP Packages (PQ): Wire-bond, plastic, QFP (0.5 mm lead spacing)											
PQG208	30.6 x 30.6 mm	124	141	141				158	158		
FGA Packages (FT): Wire-bond, fine-pitch, thin BGA (1.0 mm ball spacing)											
FTG256	17 x 17 mm		173	173	173			172	190	190	
FGA Packages (FG): Wire-bond, fine-pitch, BGA (1.0 mm ball spacing)											
FGG400	19 x 19 mm									304	304
FGG456	21 x 21 mm			264	333	333					
FGG484	23 x 23 mm										376
FGG676	27 x 27 mm					487					

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Notes: 1. System gates include 20%–30% of CLBs used as RAMs.
2. Each slice comprises two 4-input logic function generators (LUTs), two storage elements, wide-function multiplexers, and carry logic.
3. Integrated in the DSP48A slices (Advanced Multiply Accumulate element).
4. Temperature Range Automotive I (T_j = -40°C to +100°C); Automotive Q (T_j = -40°C to +125°C).

			Spartan®-3A FPGAs				Spartan-3A DSP FPGAs	
	Part Number		XA3S200A	XA3S400A	XA3S700A	XA3S1400A	XA3SD1800A	XA3SD3400A
Logic Resources	System Gates[1]		200K	400K	700K	1,400K	1,800K	3,400K
	Slices[2]		1,792	3,584	5,888	11,264	16,640	23,872
	Logic Cells		4,032	8,064	12,248	25,344	37,440	53,712
	CLB Flip-Flops		3,584	7,168	11,776	22,528	33,280	47,744
Memory Resources	Maximum Distributed RAM (Kb)		28	56	92	176	260	373
	Block RAM Blocks		16	20	20	32	84	126
	Total Block RAM (Kb)		288	360	360	576	1,512	2,268
Clock Resources	Digital Clock Managers (DCMs)		4	4	8	8	8	8
I/O Resources	Maximum Single-Ended I/Os		195	311	372	375	519	469
	Maximum Differential I/O Pairs		90	142	165	165	227	213
	I/O Standards Supported		LVTTL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVCMOS12, HSTL15 Class I, HSTL15 Class III, HSTL18 Class I, HSTL18 Class II, HSTL18 Class III, PCI 3.3V 32/64-bit 33 MHz, SSTL3 Class I, SSTL3 Class II, SSTL2 Class I, SSTL2 Class II, SSTL18 Class I, SSTL18 Class II, Bus LVDS, LVDS25, LVDS33, LVPECL25, LVPECL33, Mini-LVDS25, Mini-LVDS33, RSDS25, RSDS33, TMDS25, TMDS33, PPDS25, and PPDS33					
Embedded Hard IP Resources	DSP48A Slices		—	—	—	—	84	126
	Dedicated Multipliers		16	20	20	32	84[3]	126[3]
	Device DNA Security		Yes	Yes	Yes	Yes	Yes	Yes
Miscellaneous	Temperature Grades [4]		I, Q	I, Q	I, Q	I, Q	I, Q	I
	Speed Grade		-4	-4	-4	-4	-4	Yes
	RoHS (Pb-free)		Yes	Yes	Yes	Yes	Yes	Yes
	XA Released		Yes	Yes	Yes	Yes	Yes	Yes
Configuration	Configuration Memory (Mb)		1.2	1.9	2.7	4.8	8.2	11.7
	Package	Footprint Area	Maximum User I/Os					
	FGA Packages (FT): Wire-bond, fine-pitch, thin BGA (1.0 mm ball spacing)							
	FTG256	17 x 17 mm	195	195				
	Chip Scale Packages (CS): Wire-bond, chip-scale, BGA (0.8 mm ball spacing)							
	CSG484	19 x 19 mm					309	309
	FGA Packages (FG): Wire-bond, fine-pitch, BGA (1.0 mm ball spacing)							
	FGG400	21 x 21 mm		311	311			
	FGG484	23 x 23 mm			372	375		
	FGG676	27 x 27 mm					519	469

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Notes: 1. System gates include 20%–30% of CLBs used as RAMs.
2. Each slice comprises two 4-input logic function generators (LUTs), two storage elements, wide-function multiplexers, and carry logic.
3. Integrated in the DSP48A slices (Advanced Multiply Accumulate element).
4. Temperature Range Automotive I (T_J = –40°C to +100°C); Automotive Q (T_J = –40°C to +125°C).

			XA9500XL Family			CoolRunner™-II Family				
	Part Number		XA9536XL	XA9572XL	XA95144XL	XA2C32A	XA2C64A	XA2C128	XA2C256	XA2C384
	System Gates		800	1,600	3,200	750	1,500	3,000	6,000	9,000
	Macrocells		36	72	144	32	64	128	256	384
Logic Resources	Product Terms Per Macrocell		90	90	90	56	56	56	56	56
	Global Clocks		3	3	3	3	3	3	3	3
Clock Resources	Product Term Clocks Per Function Block		18	18	18	16	16	16	16	16
	Maximum I/O		34	72	117	33	64	100	118	118
	Input Voltage Compatible (V)		2.5/3.3/5	2.5/3.3/5	2.5/3.3/5	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3
I/O Resources	Output Voltage Compatible (V)		2.5/3.3	2.5/3.3	2.5/3.3	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3	1.5/1.8/2.5/3.3
	Minimum Pin-to-Pin Logic Delay		15.5	15.5	15.5	5.5	6.7	7	7	9.2
	Automotive I Speed Grades		-15	-15	-15	-6	-7	-7	-7	-10
Speed Grades	Automotive Q Speed Grades		-15	-15	-15	-7	-8	-8	-8	-11
	Temperature Grades[1]		I, Q	I, Q	I, Q	I, Q	I, Q	I, Q	I, Q	I, Q
	RoHS (Pb-free)		Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Miscellaneous	XA Released		Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Package	Area[2]	Maximum User I/Os							
	VQFP Packages (VQ): Very thin QFP (VQG44: 0.8 mm lead spacing; VQG64 and VQG100: 0.5 mm lead spacing)									
	VQG44	12 x 12 mm	34	34		33	33			
	VQG64	12 x 12 mm		52						
	VQG100	16 x 16 mm					64	80	80	
	TQFP Packages (TQ): Thin QFP (0.5 mm lead spacing)									
	TQG100	16 x 16 mm		72						
	TQG144	22 x 22 mm							118	118
	Chip Scale Packages (CP): Wire-bond, chip-scale, BGA (0.5 mm ball spacing)									
	CPG132	8 x 8 mm						100		
	Chip Scale Packages (CS): Wire-bond, chip-scale, BGA (0.8 mm ball spacing)									
	CSG144	12 x 12 mm			117					

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Notes: 1. Temperature Grade XA CPLD Automotive I (T_A = –40°C to +85°C); Automotive Q (T_A = –40°C to +105°C with $T_{j\ MAXIMUM}$ = +125°C).
2. Area dimensions for lead-frame products are inclusive of the leads.

Virtex®-6 FPGA Development Boards and Kits

Product Name	Purpose	Part Number	Devices Supported	Features
Virtex-6 FPGA ML605 Evaluation Kit www.xilinx.com/ml605	General-purpose FPGA Evaluation kit	EK-V6-ML605-G	XC6VLX240T-1FFG1156	x8 PCI Express, FMC (HPC & LPC), DDR3 SO-DIMM (512 MB), PlatformFlash & BPI Flash Memory, System ACE™, USB-To-UART, USB 2.0 Host & Device, 10/100/1000 Ethernet, SFP, DVI Out, 16x2 Character Display
Virtex-6 FPGA ML623 Characterization Kit www.xilinx.com/ml623	GTX Characterization Kit	CK-V6-ML623-G	XC6VLX240T-1FFG1156	40 SMA pairs, System ACE controller, SuperClock-2 module, 10 differential SMA connector pairs for GTX transceiver clock inputs, Three FMC HPC connectors (Each with 79 differential user-defined pairs, no GTX transceivers), USB-to-UART bridge
Virtex-6 FPGA Connectivity Kit	Serial Connectivity Kit with Targeted Reference Design	DK-V6-CONN-G	XC6VLX240T-1FFG1156	ML605 (EK-V6-ML605-G) + Serial Connectivity FMC Module (HW-FMC-XM104-G) and Serial Connectivity Reference Design
Virtex-6 FPGA Embedded Kit	Embedded Kit with Targeted Reference Design	DK-V6-EMBD-G	XC6VLX240T-1FFG1156	ML605 (EK-V6-ML605-G) + Embedded Reference Design
Virtex-6 FPGA DSP Kit	DSP Kit with Targeted Reference Design	AES-V6DSP-LX240T-G	XC6VLX240T-1FFG1156	ML605 (EK-V6-ML605-G) + DSP Reference Design
Virtex-6 FPGA Broadcast Connectivity Kit	Broadcast Connectivity Kit with Targeted Reference Design	DK-V6-BCCN-G	XC6VLX240T-1FFG1156	ML605 (EK-V6-ML605-G) + Broadcast FMC Module and Broadcast Reference Design

Virtex-5 FPGA Development Boards and Kits

Product Name	Purpose	Part Number	Devices Supported	Features
Virtex-5 FPGA ML501 www.xilinx.com/ml501	General-purpose FPGA development board	HW-V5-ML501-UNI-G	XC5VLX50FFG676	DDR2 SO-DIMM (256 MB), ZBT SRAM (1 MB), NOR Flash, PlatformFlash PROM and SPI Flash Memory, System ACE™ CompactFlash, JTAG Header or External JTAG Connector, 2x USB, 2x PS/2, 10/100/1000 Ethernet, RS-232, 2x Audio In/Out, DVI/VGA Video, XGI Expansion Port
Virtex-5 FPGA ML505 www.xilinx.com/ml505	General-purpose FPGA and RocketIO™ GTP development board	HW-V5-ML505-UNI-G	XC5VLX50TFF1136	DDR2 SO-DIMM (256 MB), ZBT SRAM (1 MB), Linear, platform, and SPI flash, System ACE CompactFlash, JTAG Header or External JTAG Connector, 2x USB, 2x PS/2, 10/100/1000 Ethernet, RS-232, 2x Audio In/Out, DVI/VGA Video, XGI Expansion Port, MGT support with PCI Express, SFP, SMA, SGMII
Virtex-5 FPGA ML506 www.xilinx.com/ml506	General-purpose FPGA, DSP, and RocketIO GTP transceiver development board	HW-V5-ML506-UNI-G	XC5VSX50TFF1136	DDR2 SO-DIMM (256 MB), ZBT SRAM (1 MB), Linear, platform, and SPI flash, System ACE CompactFlash, JTAG Header or External JTAG Connector, 2x USB, 2x PS/2, 10/100/1000 Ethernet, RS-232, 2x Audio In/Out, DVI/VGA Video, XGI Expansion Port, MGT support with PCI Express, SFP, SMA, SGMII
Virtex-5 FPGA ML507 www.xilinx.com/ml507	General-purpose FPGA , PPC®440 processor, and RocketIO GTX transceiver development platform	HW-V5-ML507-UNI-G	XC5VFX70TFF1136	DDR2 SO-DIMM (256 MB), ZBT SRAM (1 MB), Linear, platform, and SPI flash, System ACE CompactFlash, JTAG Header or External JTAG Connector, 2x USB, 2x PS/2, 10/100/1000 Ethernet, RS-232, 2x Audio In/Out, DVI/VGA Video, XGI Expansion Port, MGT support with PCI Express, SFP, SMA, SGMII
Virtex-5 FPGA ML510 www.xilinx.com/ml510	Advanced hardware/software embedded processing development platform	HW-V5-ML510-G	XC5VFX130T-FFG1738	32-bit component DDR memory and 64-bit DDR2 DIMM, 512 MB CompactFlash card and System ACE CompactFlash controller for configuration, Two onboard 10/100/1000 Ethernet PHYs with RJ-45 connectors, Two PCI Express® interface, VGA graphics interface, ATX Form Factor, 4x PCI 32-bit/33MHz slots, 2x USB ports, 2x SATA ports, 2x RS-232, 2x PS/2, XPM Expansion Port
Virtex-5 FPGA ML523 www.xilinx.com/ml523	RocketIO GTP transceiver characterization development platform	HW-V5-ML523-UNI-G	XC5VLX110T-FF1136	16 RocketIO GTP Transceivers connected to SMA pairs, 8 RocketIO GTP REFCLK inputs connected to SMA pairs, SuperClk module supporting a wide range of clock frequencies, Power indicator LEDs, General-purpose DIP switches, LEDs, and pushbutton switches
Virtex-5 FPGA Gigabit Ethernet Development Kit www.xilinx.com/ gbedevkit	Virtex-5 FPGA Gigabit Ethernet development	HW-V5GBE-DK-UNI-G	XC5VLX50T-1FF1136C	Quick Start Guide and platform USB programming cable, ISE® evaluation software and access to LogiCORE™ IP, Resource CD (reference designs, labs, and demonstrations), Connectors: GbE - SFP and RJ-45 connectors, 10/100 Mb/s, RJ-45 connector
Virtex-5 LXT Development Kit for PCI Express, PCI-X and PCI www.xilinx.com/v5pciekit	Application development board for PCI Express and PCI	HW-V5-ML555-G	Virtex-5 FPGA LXT XC5VLX50T-1FF1136CES	Quick Start Guide and platform USB programming cable, ISE evaluation software and access to LogiCORE IP, Resource CD (reference designs, labs, and demonstrations), Connectors: PCIe - 8-land add-in card connector, PCI/PCI-X; standard edge connector
Virtex-5 FPGA Embedded Kit www.xilinx.com/v5embedded	Advanced embedded processing development kit	DK-V5-EMBD-ML507-G	X5LX50T-1FFG1136C	Powerful Virtex-5 FPGA MC507 development board, Full seat of Platform Studio Embedded tool suite, Full seat of ISE Foundation™ FPGA design software, Reference designs, USB JTAG probe, flash device, cables, and power supply

Virtex-4 FPGA Development Boards and Kits

Product Name	Purpose	Part Number	Devices Supported	Features
Virtex-4 FPGA ML401 www.xilinx.com/ml401	General-purpose FPGA development board	HW-V4-ML401-UNI-G	XC4VLX25-FF668	64 MB DDR SDRAM, ZBT synchronous SRAM, 10/100/1000 tri-speed Ethernet PHY transceiver, USB interface device with host and peripheral ports, RS-232 serial port, XGI Expansion Port
Virtex-4 FPGA ML402 www.xilinx.com/ml402	General-purpose FPGA/DSP development board	HW-V4-ML402-UNI-G	XC4VSX35-FF668	64 MB DDR SDRAM, ZBT synchronous SRAM, 10/100/1000 tri-speed Ethernet PHY transceiver, USB interface device with host and peripheral ports, RS-232 serial port, XGI Expansion Port
Virtex-4 FPGA ML403 www.xilinx.com/ml403	General-purpose FPGA/PPC processor development board	HW-V4-ML403-UNI-G	XC4VFX12-FF668	64 MB DDR SDRAM, ZBT synchronous SRAM, 10/100/1000 tri-speed Ethernet PHY transceiver, USB interface device with host and peripheral ports, RS-232 serial port, XGI Expansion Port
Virtex-4 FPGA ML405 www.xilinx.com/ml405	General-purpose FPGA/PPC/RocketIO transceiver development board	HW-V4-ML405-UNI-G	XC4VFX20-FF672	128 MB SDRAM DDR SDRAM, ZBT synchronous DRAM, MGT: Serial ATA host connectors (x2), MGT: SFP connector (x1), MGT: SMA connector connected to one RocketIO MGT, XGI Expansion Port
Virtex-4 FPGA ML410 www.xilinx.com/ml410	Embedded system development platform	HW-V4-ML410-UNI-G	XC4VFX60-11FFG1152	ATX form factor motherboard, 64 MB DD and 256 MB DDR2 DIMM, 512 MB CompactFlash card and System ACE CompactFlash controller for configuration, 10/100/1000 tri-speed Ethernet PHY transceiver, RJ-45 connectors (x2), XPM Expansion Port
Virtex-4 FPGA ML423 www.xilinx.com/ml423	RocketIO transceiver characterization	HW-V4-ML423-UNI-G	XC4VFX100-11FF1152	20 RocketIO GTP Transceivers connected to SMA pairs, 10 RocketIO GTP REFCLK inputs connected to SMA pairs, SuperClk module supporting a wide range of clock frequencies, Power indicator LEDs, General-purpose DIP switches, LEDs, and pushbutton switches

Spartan®-6 FPGA Development Boards and Kits

Product Name	Purpose	Part Number	Devices Supported	Features
Spartan-6 FPGA SP601 Evaluation Kit www.xilinx.com/sp601	General-purpose FPGA development board	EK-S6-SP601-G EK-S6-SP601-G-J (Japan)	XC6SLX16-CS324	Onboard configuration circuitry, Quad SPI flash 64 MB, 16 MB parallel (BPI) flash, DDR2 component memory 128 MB
Spartan-6 FPGA SP605 Evaluation Kit www.xilinx.com/sp605	General-purpose FPGA evaluation board	EK-S6-SP605-G EK-S6-SP605-G-J (Japan)	XC6SLX45T-FGG484 -3	Onboard JTAG configuration circuitry, 128 MB Platform Flash XL, Quad SPI flash 64 MB, System ACE 2G CompactFlash card
Avnet Spartan-6 LX150T Development Kit http://www.xilinx.com/products/devkits/AES-S6DEV-LX150T-G.htm	General-purpose FPGA evaluation board	AES-S6DEV-LX150T-G	XC6SLX150T-3FGG676	The Xilinx Spartan-6 LX150T Development Kit provides a complete development platform for designing and verifying applications based on the Xilinx Spartan-6 LXT FPGA family.
Avnet Spartan-6 LX16 Evaluation Kit http://www.xilinx.com/products/devkits/AES-S6EV-LX16-G.htm	General-purpose FPGA evaluation board	AES-S6EV-LX16-G	XC6SLX16-CSG324	Utilizing Spartan-6, Avnet introduces the first-ever battery-powered Xilinx FPGA development board, the Xilinx Spartan-6 LX16 Evaluation Kit.
Spartan-6 FPGA Embedded Kit http://www.xilinx.com/products/devkits/DK-S6-EMBD-G.htm	Spartan-6 FPGA Embedded Kit	DK-S6-EMBD-G DK-S6-EMBD-G-J (Japan)	XC6SLX45T-FGG484 -3	Embedded Design Platforms enable rapid software application development as well as easy customization of the processor hardware subsystems.
Spartan-6 FPGA Connectivity Kit http://www.xilinx.com/products/devkits/DK-S6-CONN-G.htm	Spartan-6 FPGA Connectivity Kit	DK-S6-CONN-G DK-S6-CONN-G-J (Japan)	XC6SLX45T-FGG484 -3	The Spartan®-6 FPGA Connectivity kit is a complete, easy-to-use Connectivity Development and Demonstration platform for designing with standards based protocols – PCIe®, Ethernet, implementing low-cost protocol bridging, providing higher efficiency alternative to LVDS communication, etc in multiple market segments.
Spartan-6 FPGA DSP Kit http://www.xilinx.com/products/devkits/AES-S6DSP-LX150T-G.htm	Spartan-6 FPGA DSP Development	AES-S6DSP-LX150T-G	XC6SLX150T-3	Wireless, aerospace and defense, instrumentation and medical imaging applications continue to demand greater performance to support standards, while high-level design flows continue to improve to provide an easier entry point for using FPGAs for DSP.
Spartan-6 FPGA Industrial Ethernet Kit http://www.xilinx.com/products/devkits/AES-S6IEK-LX150T-G.htm	Spartan-6 FPGA Industrial Ethernet Developmet	AES-S6IEK-LX150T-G	XC6SLX150T-3FGG676	The Spartan-6 FPGA Industrial Ethernet Kit is a comprehensive design environment for rapid prototyping and development of leading edge industrial applications in connectivity, motor control, and embedded processing.
Spartan-6 FPGA Industrial Video Processing Kit http://www.xilinx.com/products/devkits/AES-S6IVK-LX150T-G.htm	Spartan-6 FPGA Industrial Video Processing	AES-S6IVK-LX150T-3FGG676	XC6SLX150T-3	The Spartan-6 FPGA Industrial Video Processing Kit is a comprehensive design environment for rapid prototyping and streamlined development of high resolution video conferencing, video surveillance and machine vision systems.
Spartan-6 FPGA Consumer Video Kit http://www.xilinx.com/products/devkits/TB-6S-CVK.htm	Spartan-6 FPGA Consumer Video	TB-6S-CVK	XC6SLX150T-3	Speed up development of video algorithms and incorporate the latest video interface standards right out of the box. The Spartan-6 FPGA Consumer Video Kit is a comprehensive design environment for developing and debugging advanced video algorithms.

Spartan-3 FPGA Development Kits

Product Name	Purpose	Part Number	Devices Supported	Features
Spartan-3A FPGA Starter Kit www.xilinx.com/s3astarter	Low-cost Spartan-3A FPGA board evaluation kit	HW-SPAR3A-SK-UNI-G	XC3S700A-FG484	Evaluation board with Spartan-3A FPGA, onboard 10/100 Ethernet PHY, SPI based ADC and DAC circuitry, 64 MB DDR2, two 16 Mb SPI serial flash. Interfaces include a 2x16 LCD display and various I/O ports, including a PS/2 port, a VGA display port, and two serial ports. Kit includes evaluation board, power supply with universal adaptors, programming cable, quick-start guide, design tools, evaluation software, and collateral.
Spartan-3AN FPGA Starter Kit www.xilinx.com/s3anstarter	Low-cost Spartan-3AN FPGA board evaluation kit	HW-SPAR3AN-SK-UNI-G	XC3S700AN-4FGG484C	Evaluation board with Spartan-3AN FPGA, onboard 10/100 Ethernet PHY, SPI based ADC and DAC circuitry, 64 MB DDR2, and two 16 Mb SPI serial flash. Interfaces include a 2x16 LCD display and various I/O ports, including a PS/2 port, a VGA display port, and two serial ports. Kit includes evaluation board, power supply with universal adaptors, programming cable, quick-start guide, design tools, evaluation software, and collateral.
Spartan-3A DSP FPGA 1800A Edition XtremeDSP™ Solution Starter Board www.xilinx.com/s3adspstarter	Low-cost, entry-level environment for developing signal processing designs	HW-SD1800A-DSP-SB-UNI-G	XC3SD1800A-4FGG676C	Memory: 128 MB (32M x 32) DDR2 SDRAM; 16M x 8 parallel / BPA configuration flash; 64 Mb SPI configuration/storage flash (with 4 extra SPI selects), EXP expansion connector
Spartan-3E FPGA Starter Kit www.xilinx.com/s3estarterkit	Low-cost Spartan-3E FPGA development kit	HW-SPAR3E-SK-UNI-G	XC3S700A-FG484	Evaluation board with Spartan-3E FPGA, CoolRunner™-II CPLD, 128 Mb parallel flash, 16 Mb SPI flash, 64 MB DDR SDRAM, Interfaces include Ethernet 10/100 PHY, two RS-232 serial ports, PS/2 style mouse/keyboard, 2x16 character LCD, Kit includes evaluation board, power supply with universal adaptors, programming cable, quick-start-guide, design tools evaluation software, and collateral.
XtremeDSP Solution Video Kit www.xilinx.com/vsk_s3	Video application development on Spartan-3A FPGAs	DO-SEADSP-VIDEO-SK-UNI-G	XC3SD3400A-4FGG676C	Includes full seats of System Generator and EDK, Example video reference designs, Complete documentation, Platform USB cable, power supply, and video cables, Carrier board: Spartan-3A FPGA DSP DPFA F3400A Development Board, Mezzanine card: FMC-video
Spartan-3A DSP S3D1800A MicroBlaze Processor Edition Embedded Development HW/SW Kit www.xilinx.com/s3adspmb	Flexible embedded processing development kit	DO-SD1800A-EDK-DK-UNI-G	XC3SD1800A-4FGG676C	Full seat of Platform Studio embedded tool suite, ISE WebPACK FPGA design software, Reference designs, USB programming download cable, UART, Ethernet cables and power supply
Spartan-3A DSP FPGA 3400A Edition XtremeDSP Solution Development Platform www.xilinx.com/s3adap_dp	Spartan-3A FPGA DSP application development solution	HW-SD3400A-DSP-DB-UNI-G	XC3SD3400A-4FGG676C	Onboard 256 MB DDR2 SDRAM; 256 Mb flash; 9 Mb ZBT SRAM; 32 Mb Platform flash 16 Mb SPI EEPROM; 256 MB CompactFlash, Two FMC and a LPC expansion connector

CPLD Starter Kits

Product Name	Purpose	Part Number	Devices Supported	Features
CoolRunner-II CPLD Starter Kit Featuring the DataGATE Low-Power Advantage www.xilinx.com/products/devkits/SK-CRII-L-G.htm	General-purpose CPLD evaluation board	SK-CRII-L-G	XC2C256-TQ144	Complete 'out-of-the-box' evaluation platform, CoolRunner-II CPLD utility window, Easy set-up and monitoring, DataGATE evaluation "switch", Free reference designs

FMC Daughter-cards

Product Name	Purpose	Part Number	Devices Supported	Features
FMC Debug Mezzanine Card www.xilinx.com/products/devkits/HW-FMC-DBG-G.htm	FMC XM105 Debug Mezzanine Card	HW-FMC-XM105-G		VITA 57.1 FMC HPC connector, Single-ended signals from the carrier board, clocks, JTAG, and power, 40 single-ended I/O (20 pairs) on the LPC pins, 80 single-ended I/O (40 pairs) on the HPC pins, Mictor connector 38 pins female Mictor connector
FMC XM104 Connectivity Card www.xilinx.com/xm104	FMC Connectivity	HW-FMC-XM104-G		The FMC XM104 Connectivity Card is designed to provide access to eight serial transceivers on the FMC HPC connector found on Xilinx FMC-supported boards including Virtex®-6 ML605. These eight serial transceivers can be accessed through one CX4 (x4 transceivers), two SATA (x2 transceivers), and eight SMA (x2 transceivers) connectors.

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Advanced IP

Quickly and easily search for IP Cores from Xilinx and its 3rd party alliance partners at www.xilinx.com/ipcenter.

Reference Designs

Reference Designs can be found under the 'Topics' tab of the Documentation Center, www.xilinx.com/documentation.

Instructor Led Training Courses
*Recommended Courseware
Elective Courseware

FPGA Curriculum	Learning Level
*ISE® Design Tool Flow *Designing with Verilog* *Designing with VHDL* *FPGA Design for ASIC Users* Designing with the Virtex®-6 and Spartan®-6 Families	1
*Essentials of FPGA Design *Design Techniques for Lower Cost* *Debugging Techniques Using the ChipScope™ Pro Tools*	2
*Designing for Performance *Designing with the PlanAhead™ Analysis and Design Tool* *TMRTool*	3
*Advanced FPGA Implementation *Advanced VHDL*	4
Embedded Hardware Curriculum	**Learning Level**
*Embedded Systems Development	3
*Advanced Embedded Systems Development	4
Embedded Software Curriculum	**Learning Level**
*Embedded Systems Software Development	3
*Embedded Open-Source Linux Development	4
Connectivity Curriculum	**Learning Level**
*Designing a LogiCORE™ PCI Express® System *Designing with Multi-Gigabit Serial I/O *Designing with Ethernet MAC Controllers *Signal Integrity and Board Design for Xilinx FPGAs	3
DSP Curriculum	**Learning Level**
*DSP Design Using System Generator	3

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Xilinx Productivity Advantage (XPA)			www.xilinx.com/xpa
Xilinx Productivity Advantage (XPA) helps you efficiently migrate your FPGA designs to our hardware platforms through a customizable software and services bundle. With the help of a Xilinx sales representative and application engineering team, you can choose the right mix of productivity solutions at the start of your design. Bundle and save today!			
Custom XPA Part Numbers			
1 Year	2 Years	3 Years	Description
DS-XPA-10K			Custom XPA for $0 - $10,000
DS-XPA-50K	DS-XPA2-50K	DS-XPA3-50K	Custom XPA for $10,001 - $50,000
DS-XPA-200K	DS-XPA2-200K	DS-XPA3-200K	Custom XPA for $50,001 - $200,000
DS-XPA-500K	DS-XPA2-500K	DS-XPA3-500K	Custom XPA for $200,001 - $500,000

Note: Multi-year option only available when the 1 year deal list price is greater than $40,000.

XMP083 (v1.0)

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