THE LOW-COST PROGRAMMABLE SILICON FOUNDATION FOR TARGETED DESIGN PLATFORMS

BALANCING COST, SPACE, POWER AND PERFORMANCE

The Programmable Imperative

- System designers in today's price-sensitive markets face a confluence of economic, financial, and market pressures
- Market windows are narrowing, design complexity is increasing, and product lifetimes are shrinking
- Developers need to do more with less and still push the limits of innovation to remain competitive

Targeted Design Platforms

- Targeted Design Platforms from Xilinx and its network of third parties provide system designers with simpler and smarter methodologies for creating FPGA-based system-on-chip solutions
- Targeted Design Platforms enable software and hardware designers to leverage open standards, common design methodologies, development tools, and run-time platforms
- Designers can spend less time developing the infrastructure of an application and more time building differentiating features into their products

Where Low Cost, Low Power Converge with High Performance

When design requirements call for low cost and low power, the new Spartan®-6 family is the answer. This silicon foundation of the Xilinx Targeted Design Platform merges industry-leading process and programmable logic technology with transceiver capabilities and controllers for advanced memory support to deliver a high-performance FPGA for cost-sensitive applications. Innovation in advanced power management technology and the ability to operate at a lower power 1.0V core option enable the new Spartan-6 FPGA family to achieve 65% lower power than previous Spartan families.

At the Heart of Innovation

The sixth generation in the Spartan FPGA Series enables system developers to meet demands for new features, while at the same time reducing system costs by up to half for lower-power, "greener" products. Supporting applications such as automotive infotainment, flat-panel displays, multi-function printers, set-top boxes, home networking, and video surveillance, Spartan-6 FPGAs offer an optimal balance of low risk, low cost, low power, and high performance.

A Proven, Industry-Leading Architecture

The Spartan-6 FPGA family's efficient, dual-register six-input LUT logic structure leverages the industry's leading Virtex® architecture to enable cross-platform compatibility and to increase system performance. The addition of Virtex-series system-level blocks including DSP slices, high-speed transceivers, and PCI Express® endpoint block make for greater system-level integration than ever before.

XILINX®

Spartan-6 FPGA Families

The Spartan®-6 FPGA family comprises of two domain-optimized sub-families with a mix of features matched to stringent market requirements for price-sensitive, high-volume applications:

Spartan-6 LX FPGAs are optimized for applications that require the absolute lowest cost. They support up to 147K logic cell density, 4.8Mb memory, integrated memory controllers, DSP slices, ease-of-use, and high-performance Hard IP with an innovative open standards-based configuration.

Spartan-6 LXT FPGAs extend the LX family to deliver up to eight 3.2Gbps GTP transceivers and an integrated PCI Express Block, both derived from proven Virtex® FPGA family technology, to provide the industry's lowest-risk and lowest-cost solution for serial connectivity.

Discover how this new family delivers even higher performance, lower power, and lower system cost than previous-generation Spartan FPGAs.

Key Capability Overview

Greater Ease-of-Use

- Faster design using integrated wizards for built-in blocks, an efficient logic architecture derived from the Virtex series as well as development kits complete with IP and reference designs
- Easier configuration with broad, low-cost third-party flash support, and simplified two-pin auto-detect configuration

New Levels of Performance

- Abundant logic resources with increased logic capacity of up to 147K logic cells enables driving high performance in systems
- Build high-performance digital signal processing systems for video, wireless, and many other applications with efficient, second-generation DSP48A1
- Simplify high-bandwidth interfaces with multi-voltage, multi-standard high-performance SelectIO™ banks with 3.3V capability, an integrated memory controller block, and DisplayPort-enabled 3.2Gb/s GTP transceivers
- Integrated memory controller blocks enable streamlined access to video and data storage in external DDR3 memory, while double the block RAM provides a wider range of granularity (1x18Kb or 2x9Kb)
- Speedy embedded processing with enhanced MicroBlaze™ soft processor

Faster, More Comprehensive Connectivity

- Connect to more with support for major single and double differential I/O standards
- Connect faster with 1Gbps differential I/O, multiple 3.2Gbps integrated serial transceivers, and 12.8Gbps memory bandwidth access
- Connect at lower cost with integrated SDRAM memory controller and PCI Express® interfaces

Twice the Capability, Half the Power

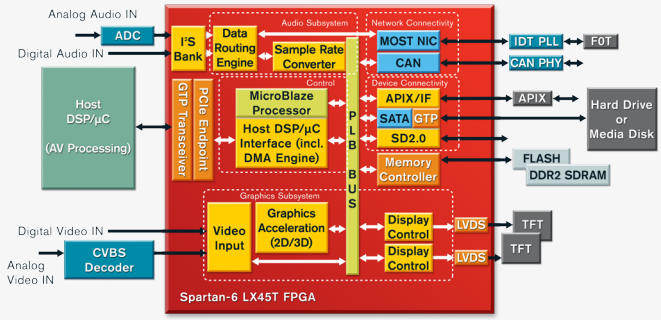
- Process more, faster with increased block RAM, 2X logic capability, 50% more DSP48A1 slices, six-input LUT with dual flip-flops, low noise, and flexible clocking
- Reduce power consumption with ~50% lower dynamic power and ~40% lower static power compared to previous generation, and by using system-level power management features
- 45nm process technology optimized for low-cost, cost-optimized wire-bond packaging and new hard IP blocks reduce size to help you drive down system costs

FEATURES OVERVIEW

45nm Low Power Process Technology Optimized for cost, power and performance, most efficient utilization of low-power copper process technology	▪ Efficient six-input LUTs improve performance and minimize power ▪ LUT designed with dual flip-flops for pipelined applications ▪ Flexible LUTs are configurable as logic, distributed RAM, or shift registers ▪ From 3,800 to 147,000 logic cells for system-level integration
Low Cost by Design Cost-optimized Virtex®-series based architecture	▪ Multiple efficient integrated blocks ▪ Optimized selection of I/O standards ▪ Staggered I/O pads ▪ High-volume plastic wire-bonded packages ▪ Low-cost third-party configuration
1050MHz Clocking Technology Clock Management Tile (CMT) for enhanced performance	▪ Low noise, flexible clocking ▪ Digital Clock Managers (DCMs) eliminate clock skew and duty cycle distortion ▪ Phase-Locked Loops (PLLs) for low-jitter clocking ▪ Frequency synthesis with simultaneous multiplication, division, and phase shifting ▪ Sixteen low-skew global clock networks
Increased Memory Block Capacity to 4.8Mbits Block RAM with a wide range of granularity	▪ Efficient block RAM ▪ Fast block RAM with byte write enable ▪ 18Kb blocks can be split into two independent 9Kb block RAMs
Integrated Memory Controllers Only low-cost FPGA with integrated memory controller blocks	▪ DDR, DDR2, DDR3, and LPDDR support ▪ Data rates up to 800Mbps (12.8Gbps peak bandwidth) ▪ Multi-port bus structure with independent FIFO to reduce design timing issues ▪ Simplifies memory interface and board layout ▪ Predictable timing for memory interface designs ▪ Software wizard to guide through the entire process
SelectIO™ Interface Technology Multi-voltage, multi-standard SelectIO banks	▪ Up to 1,050Mbps data transfer rate per differential I/O ▪ Selectable output drive, up to 24mA per pin ▪ 3.3V to 1.2V I/O standards and protocols ▪ Low-cost HSTL and SSTL memory interfaces ▪ Hot-swap compliance ▪ Adjustable I/O slew rates to improve signal integrity
Up to 180 Efficient DSP48A1 Slices Drive high-performance arithmetic and signal processing	▪ Each slice contains a fast 18 x 18 multiplier and a 48-bit accumulator capable of operating at 250MHz ▪ Pipelining and cascading capability ▪ Pre-adder to assist in symmetric filter applications
Enhanced Configuration and Bitstream Protection Reduce system cost, increase reliability, and safeguard your design	▪ Simplified configuration, supports low-cost standards ▪ Broad third-party SPI (up to x4) and NOR Flash support ▪ Feature-rich Xilinx Platform Flash with JTAG ▪ MultiBoot support for remote upgrade with multiple bitstreams, using watchdog protection ▪ Unique Device DNA identifier for design authentication ▪ AES bitstream encryption in the larger devices
GTP Transceivers in Spartan-6 LXT: 100Mbps to 3.2Gbps Implement serial protocols at lowest power	▪ Up to 3.2Gbps performance ▪ High-speed interfaces: Serial ATA, Aurora, 1G Ethernet, PCI Express®, OBSAI, CPRI, EPON, GPON, DisplayPort, and XAUI ▪ Low power consumption: < 150 mW (typical) at 3.2Gbps
PCI Express Block in Spartan-6 LXT FPGA Integrated block for PCI Express designs	▪ Works with GTP transceivers to deliver PCIe endpoint funtionality ▪ Built-in hard IP frees user logic resources and reduces power ▪ PCI SIG-verified Gen1 compliance (on integrators list)
Optimized Power Saving Modes Hibernate power-down mode for zero power	▪ Suspend mode maintains state and configuration with multi-pin wake-up, control enhancement ▪ Software power optimization option
Embedded Processing Faster embedded processing with enhanced, low-cost, MicroBlaze™ soft processor	▪ New MicroBlaze 7.0 adds MMU and FPU for greater functionality ▪ Six-input LUT architecture improves performance and efficiency for comparator and multiplexer ▪ 2X flip-flops for embedded registers ▪ Hard DRAM memory controller with 12.8Gbps memory bandwidth

How Targeted Design Platforms accelerate innovation

Automotive Infotainment



In-Car Infotainment System

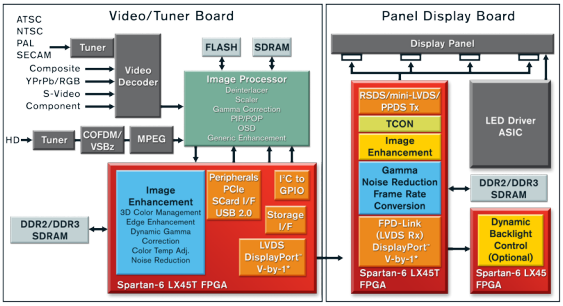
Serving as a companion to the host processor, a single Spartan-6 LX45T FPGA supports audio/video acceleration, graphics subsystem, and vehicle networking functions.

Enhance the user experience

Spartan®-6 FPGAs provide the flexibility to respond rapidly to changing consumer requirements.

- Improve video performance with customized graphics accelerators and flexible parallel and serial interface capabilities
- Simplify interfacing to host processors and reduce component count with integrated PCI Express® technology
- Accelerate design with IP offerings for graphics processing, video conversion, high-speed interfacing, and vehicle networks

Flat-Panel Displays



High-Resolution Video Flat-Panel Display with Dynamic Backlight Control

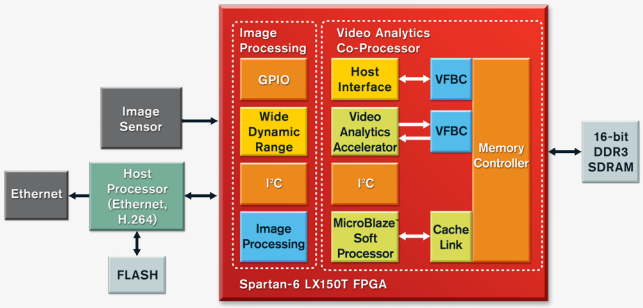
Achieve higher image quality while reducing power and cost using Spartan-6 FPGAs with integrated serial I/O capabilities.

Increase picture quality

Spartan-6 FPGAs offer a cost-efficient alternative to ASICs and enable DTV manufacturers to rapidly develop and deliver displays offering a superior viewing experience within ever-shrinking product lifecycles.

- Achieve tough performance and EMI targets easily with low-jitter spread-spectrum clocking
- Reduce power consumption, simplify thermal management, increase reliability, and reduce cost with high-capacity, low-power FPGAs
- Increase image quality with a rich library of image enhancement IP such as dynamic gamma correction, motion adaptive temporal noise reduction, and dynamic range compression
- Simplify high-bandwidth interfaces with flexible SelectIO technology, an integrated memory controller block, and DisplayPort-enabled 3.2Gbps GTP transceivers

Video Surveillance



Surveillance Image Capture and Analytics Engine

Integrate sensor interfacing, video analytics, image enhancement and network interfacing in a single Spartan-6 LX150T FPGA.

Increase security through real-time image interpretation

Spartan-6 FPGAs offer the ideal combination of performance and flexibility to address requirements for high resolution, video analytics, and increased channels in video surveillance systems.

- Build flexible front-end image processing to support higher video resolutions
- Process native-resolution image data at full frame rate using highly parallel implementations based on DSP48A1 slices
- Implement edge-based video analytics with cost-effective customized co-processors

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