

JTAG HS1

Programming Cable for Xilinx FPGAs

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Overview

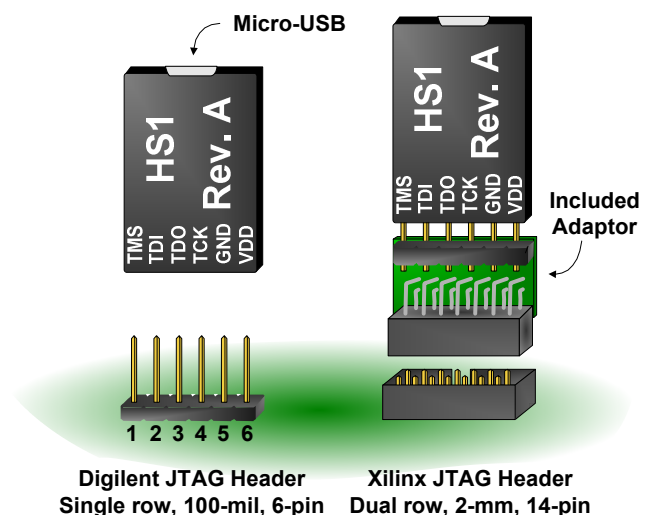
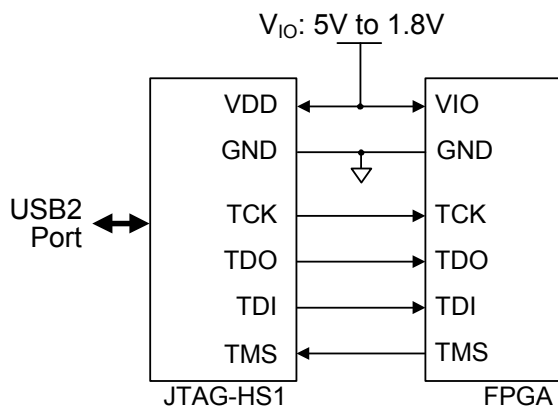
The JTAG-HS1 programming cable is a high-speed programming solution for Xilinx FPGAs. It is fully compatible with all Xilinx tools, and can be seamlessly driven from iMPACT, Chipscope, and EDK. The HS-1 attaches to target boards using Digilent's 6-pin, 100-mil spaced programming header, or Xilinx's 2x7, 2mm connector (using the included adaptor).

The JTAG-HS1 is powered from a PC's USB port, and will be recognized as a Digilent programming cable when connected to a PC, whether or not it is attached to the target board. A separate Vdd pin is provided on the HS1 to supply JTAG signal buffers. The high speed, 24mA, three-state buffers allow target boards to drive the HS1 with signal voltages from 1.8V to 5V, with bus speeds of up to 30Mbit/sec. The HS1's Vdd pin must be tied to the same voltage supply that drives the JTAG port on the FPGA.

JTAG signals are held in high-impedance except when actively driven during programming, so the JTAG bus can be shared with other devices. The HS1 uses a standard Type-A to Micro-USB cable (included with the HS1) that attaches to the end of the module opposite the system board connector. The HS1 is small and light, allowing it to be held firmly in place by the system board connector.



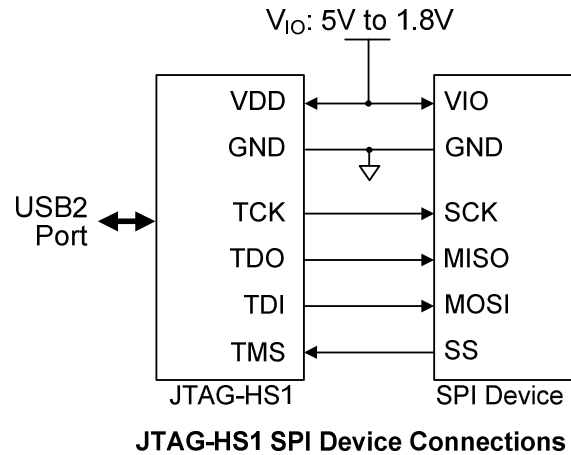
- Small, complete, all-in-one JTAG programming solution for Xilinx FPGAs
- Separate Vref drives JTAG/SPI signal voltages; Vref can be any voltage between 1.8V and 5V.
- High-Speed USB2 port that can drive JTAG/SPI bus at up to 30Mbit/sec
- JTAG/SPI frequency settable by user
- Compatible with all Xilinx tools
- Uses micro-AB USB2 connector
- SPI programming solution (modes 0 and 2 supported)
- Fully supported by the Adept SDK, allowing custom JTAG/SPI applications to be created



Software Support

In addition to working seamlessly with all Xilinx tools, the HS1 is supported by Digilent’s Adept software and the Adept SDK (the SDK can be freely downloaded from Digilent’s website). Adept includes a full-featured programming environment, and a set of public APIs that allow user applications to directly drive the JTAG chain.

Using the Adept SDK, custom applications can be created to drive JTAG ports on virtually any device. The HS1 also supports SPI modes 0 and 2. By using the API’s provided by the SDK applications can drive any SPI device supporting those modes. Please see the Adept SDK reference manual for more information.



The HS1 is also supported by Digilent’s AVR programmer that can target any AVR device.

Absolute Maximum Ratings

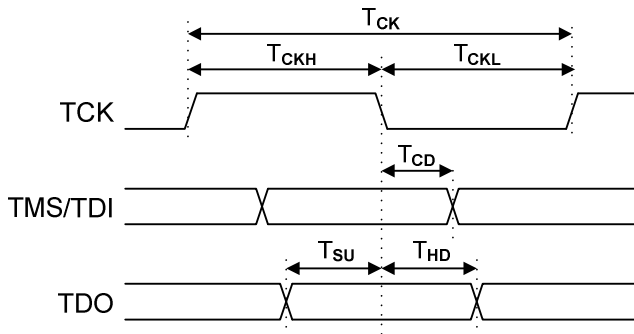
Symbol	Parameter	Condition	Min	Max	Unit
Vdd	Operating supply voltage		-0.3	4.0	V
Vref	I/O reference/supply voltage		-0.3	6	V
VIO	Signal Voltage		-0.3	6	V
I _{IK} , I _{OK}	TMS, TCK, TDI, TDO DC Input/Output Diode Current	VIO < -0.3V		-50	mA
		VIO > 6V		+20	
I _{OUT}	DC Output Current			±50	mA
T _{STG}	Storage Temperature		-20	+120	°C
ESD	Human Body Model JESD22-A114			2000	V
	Charge Device Model JESD22-C101			500	V

DC Operating Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
Vdd	Operating supply voltage	2.97	3.3	3.63	Volts
Vref	I/O reference/supply voltage	1.65	2.5/3.3	5.5	Volts
TDO	Input High Voltage (V_{IH})	$0.75 \times V_{ref}$		5.5	Volts
	Input Low Voltage (V_{IL})	0		$0.25 \times V_{ref}$	Volts
TMS, TCK, TDI	Output High (V_{OH})	$0.85 \times V_{dd}$	$0.95 \times V_{dd}$	Vdd	Volts
	Output Low (V_{OL})	0	$0.05 \times V_{dd}$	$0.15 \times V_{dd}$	Volts

AC Operating Characteristics

HS1 JTAG/SPI signals are driven according to the timing diagram below. [TCK frequencies](#) from 30MHz to 8 KHz are supported, at integer [divisions of 30MHz from 1 to 3750](#). Common frequencies include 30MHz, 15MHz, 10MHz, 7.5MHz, and 6MHz.



Symbol	Parameter	Min	Max
T_{CK}	T_{CK} period	33ns	2.185ms
T_{CKH}, T_{CKL}	T_{CLK} pulse width	20ns	1.1ms
T_{CD}	T_{CLK} to TMS, TDI	0	15ns
T_{SU}	TDO Setup time	19ns	
T_{HD}	TDO Hold time	0	

Design Notes

The HS1 is designed to drive JTAG/SPI signals on target boards that have less than 100ohms of series resistance. Higher resistance may result in degraded operation.