

APPLICATION NOTE

SIMPLIFY BOARD LAYOUT USING LVDS TERMINATORS

INTRODUCTION

The Xilinx® Virtex-E™ family of Field Programmable Gate Arrays (FPGA) offers a wide range of flexible Input/Output interfaces including Low Voltage Differential Signaling (LVDS). The Virtex-E device is comprised of eight banks of definable I/O arranged around the perimeter of the device. See Figure 1 below.

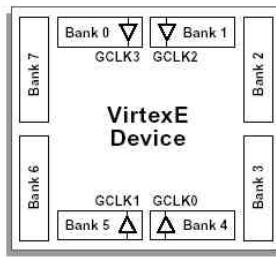


Figure 1.

LVDS is a differential I/O standard that requires a pair of signal lines for each channel. The differential transmission scheme is less susceptible to common-mode noise than single-ended transmission methods. LVDS standards require termination resistors to reduce signal reflection. The standard voltage swing for the differential pair is approximately 350mV, and the typical V_{CC0} is 2.5V.

The ClearONE Series RT1710B6/B7, RT1722B7, and RT1723B6/B7 have been designed to help the PCB Layout and Design Engineer simplify the termination for the LVDS I/O Standards, while at the same time conserving valuable PCB real estate.

The circuits for terminating LVDS transmitters and receivers are different. The following sections explain each.

LVDS TRANSMITTER TERMINATION

In general, the LVDS transmitter termination consists of a series-shunt resistor combination for each differential pair. The shunt resistor value is

140 ohms, whereas the series pair consists of 165 ohms each. See figure 2 below. *Note: these values assume a 50-Ohm characteristic impedance on the transmission line.*

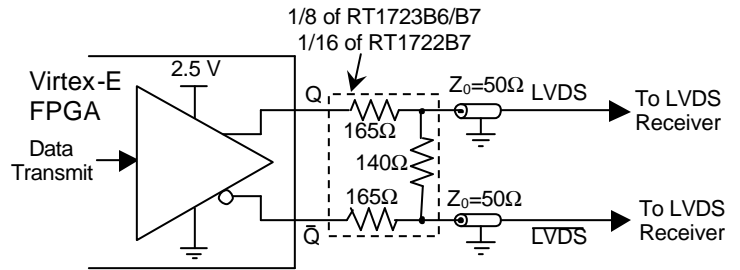


Figure 2.

LVDS RECEIVER TERMINATION

The LVDS receiver termination consists of a shunt resistor between each differential pair. The shunt resistor value is 100 Ohms. See figure 3 below. *Note: this value assumes a 50-Ohm characteristic impedance on the transmission line.*

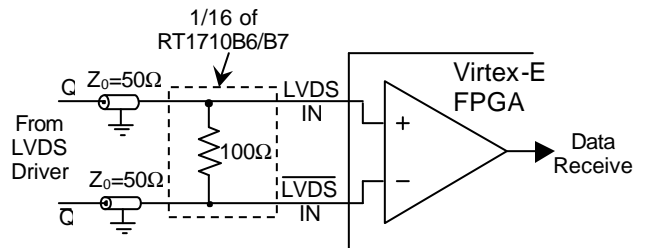


Figure 3.

CLEARONE BGA RESISTOR LAYOUT

A typical application is illustrated by terminating 64 LVDS lines on a Xilinx XCV300E device (BG432 package). As few as two ClearONE terminator packages can be used for transmitter terminations, and another two for the receiver, as opposed to up to sixteen total termination packs with other resistor termination solutions.

The 32 LVDS pairs can be routed from the 432-pin BGA package through the ClearONE CBGA terminators, and then over to twin 34-pin headers with 100-mil contact spacing. Refer to the diagrams in Figure 4, which, though not to scale, accurately show the comparisons of terminating LVDS receivers with ClearONE terminators versus terminating with standard resistor arrays. The center pin pairs of each header are best connected to the ground plane, which provides a return path for any common-mode currents that may be introduced by external noise or mismatches in layout or loads.

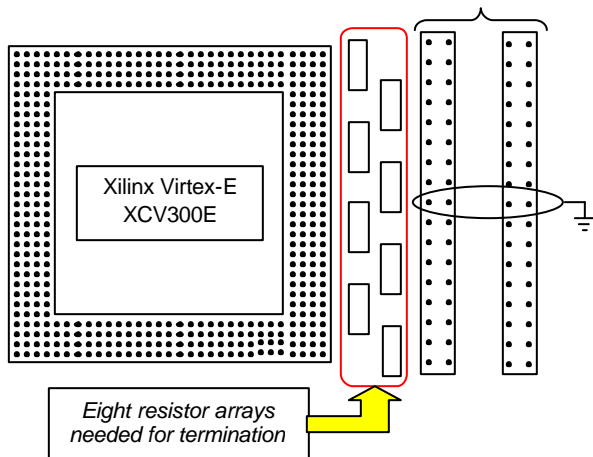
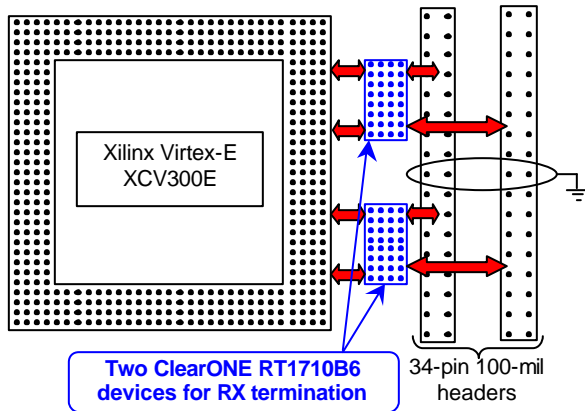


Figure 4.

Table 1 illustrates the CTS ClearONE part numbers that can be used for the transmitter/receiver LVDS resistor terminations with the Xilinx Virtex-E series FPGA's. The B6 suffix denotes a 1.27mm (50-mil) BGA pitch, and the B7 suffix denotes a 1mm (39-mil) BGA pitch.

CLEARONE PART NUMBER GUIDE

| Part Number | I/O Standard Termination for: | # of Pairs | Pins |
|-------------|-------------------------------|------------|------|
| RT1722B7 | LVDS Transmitter | 16 | 64 |
| RT1723B6/B7 | LVDS Transmitter | 8 | 32 |
| RT1710B6/B7 | LVDS Receiver | 16 | 32 |

Table 1.

Refer to Figure 5 and Table 2 for details of where the ClearONE terminators are used, the part numbers available, the resistance values for each part, and the ball grid pitch.

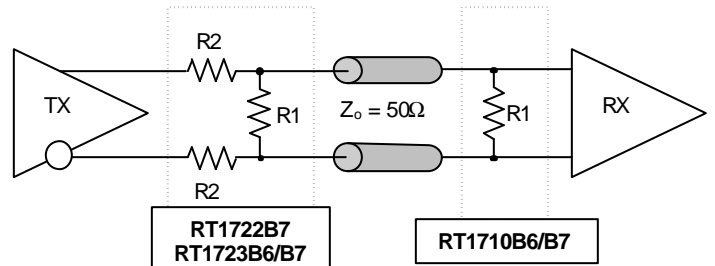


Figure 5.

Detailed Information

| Part Number | R1 W | R2 W | Array Size | Pitch (mm) |
|-------------|------|------|------------|------------|
| RT1710B6 | 100 | N/A | 4 x 8 | 1.27 |
| RT1710B7 | 100 | N/A | 4 x 8 | 1.00 |
| RT1722B7 | 140 | 165 | 4 x 16 | 1.00 |
| RT1723B6 | 140 | 165 | 4 x 8 | 1.27 |
| RT1723B7 | 140 | 165 | 4 x 8 | 1.00 |

Table 2.

SUMMARY

The CTS ClearONE BGA terminators offer the simplest solution for board layout on LVDS transmitter/receiver connections using the Xilinx Virtex-E series FPGA's. In addition, these terminators offer the lowest parasitic I/O capacitance and inductance in the industry. Our full line of BGA terminators have been modeled up to 1.2 GHz and the SPICE models and equivalent circuits can be found on our Web site at www.ctsclearone.com.

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