High Frequency Termination and the SCSI Bus

Termination networks, either passive or active, are widely used to provide for impedance normalization in bus topologies and play an important role in maintaining computer data bus transfer signal integrity, which reduce data errors. With the steady increase of microprocessor speeds, the design of data buses and termination devices is requiring a more exacting component selection and physical design methodology or practice. Present microprocessor speeds are reaching beyond the 1GHz range, while busses like SCSI (Small System Computer Interface) Ultra320 appears with a data transfer rate of 320Mbyte and data clock rates of 160MHz. The edge rates of active bus devices used in digital circuits are now approaching speeds greater than 1V/ns. The residual skew error may be as low as $\pm$0.15ns. With the steady increase of bus speed and the reduction of skew budgets, design margins are becoming tighter and tighter. Under such bus speeds all components contribute parasitic impedance to the bus, which results in the reduction of signal integrity. Termination networks can significantly contribute to the bus parasitic impedance. Parasitic impedance effects of termination devices caused by physical circuit mismatches can no longer be considered negligible. The problem is that a termination device is usually characterized at low frequencies and no information is provided about its parasitic parameters. For the reasons mentioned above, it is critical to evaluate those parasitic parameters to know its effects on digital circuit quantitatively as well as a means to validate and improve termination device performance.

Because the parasitic parameters in a termination network are generally low value series inductance and coupling capacitance, measuring those parasitics can become a significant challenge. Traditionally a digital device or circuit is characterized using TDR (Time Domain Reflectometry) techniques in the time domain. But there are two barriers to overcome when using TDR techniques that will remain unsolved. One is the dynamic range of TDR measurement system. The other is the technique to de-embedding the transition from test probe to device under test (DUT). The former will results in limitations in detecting small inductance and capacitance values, while the latter may cause hard-to-interpret measurements, especially in fast-rise-time measurement environments. Unfortunately, no concrete approached has been found that can be resolved these two problems using TDR techniques [1].

In the frequency domain, the above mentioned obstacles can easily be removed by using a network analyzer and TRL (Through Reflection Line) calibration techniques. The network analyzer receiver used for this needs at least a 100 dB dynamic range, leading to a TRL technique that is ideal for the de-embedding measurement. The setback of the frequency domain measurement, s-parameters, in this specific case is obvious; that is, the measurement results are not explicit in term of edge rate or skew rate, which are the terms used by digital circuit designer. However this setback can be resolved by extraction of a spice model, which will be shown later in this paper [2].

The TRL measurement scheme includes the following steps: design and fabrication of test PCB/test fixture, design and fabrication of TRL calibration standards, measurement and data processing. To ensure the measurement accuracy, special attention should be placed on the calibration standard fabrication accuracy and test fixture accuracy, as they are key steps. Ideally the test printed circuit board (PCB) and TRL calibration standards material properties should be well known. Since the PCB material FR4 has a wide range of dielectric constant variation, it is not an ideal material for accurate measurements. But the shortcomings of FR4 materials can be overcome by fabricating calibration standards on the same test PCB and characterizing the properties of the test PCB material. In the measurements presented in this paper, the test PCB trace width was carefully selected to ensure the difference from the calibration standards trace line width to the test PCB trace line width was less than 0.5 mil. Another consideration was that the calibration standards design should be de-embedded from the trace and impedance discontinuity effects in the test fixture. This consideration has the following two effects: i) the calibration standards are designed to de-embedding the test PCB trace. ii) The Microstrip line impedance was chosen as close as possible to the impedance value of termination network to be measured to minimize the measurement error. Figure 1 shows the measurement setup and BGA terminator installed on a test PCB/fixture. An Agilent 8753E network analyzer with TRL calibration capability was used for the s-parameter extraction.

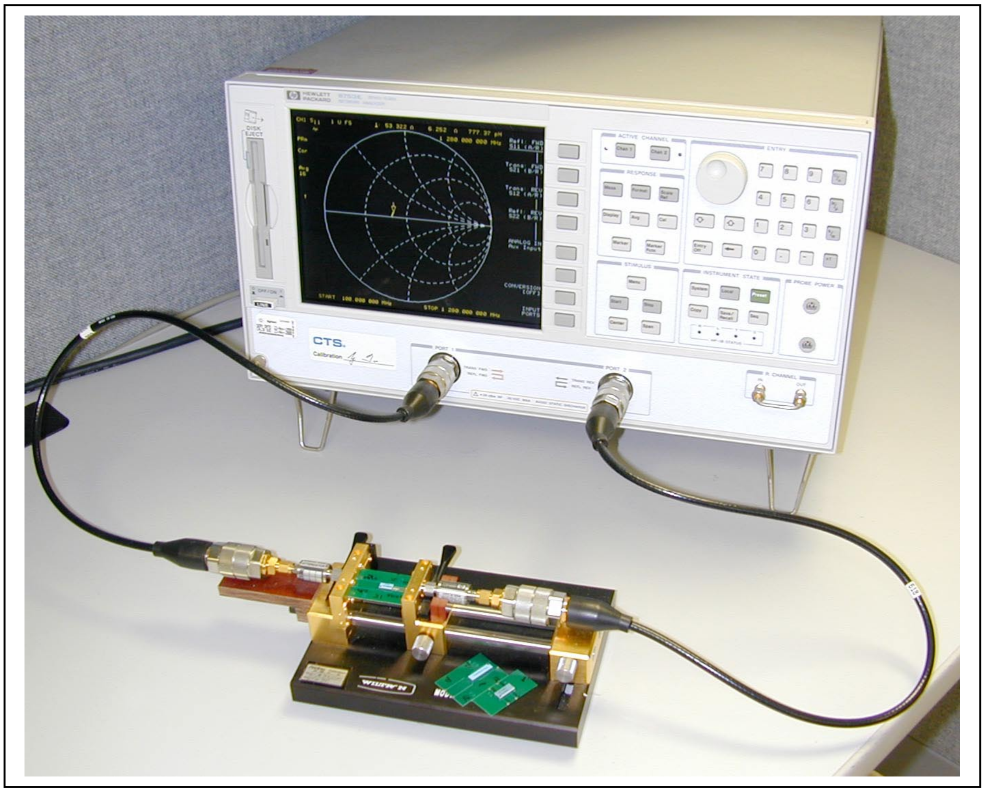


Figure1. Resistor network measurement setup

Generally speaking, the s-parameters should be measured as an n-port network and the termination network, then should be modeled as an n-port network for its equivalent circuit [1]. A Y or Z matrix then can be derived from the knowledge of n-port s-parameters [3]. However, based on the fact that the coupling between two adjacent ones is dominant (S21 is below –40 to -50 dB at the low frequency end and –22dB to –42 dB at the high frequency end), the coupling between two termination channels further apart can then be neglected. Therefore a π network can be used to model the two adjacent termination channels. Under this assumption, measurement work can be greatly reduced.

The termination networks under test are installed on a test PCB in pairs to form π type circuits with a common ground. Two port measurements are carried out with the average factor set to 16, and the IF bandwidth equal to 3700Hz. The network analyzer frequency span is set from 100MHz to 1280MHz. The s-parameters are converted into equivalent circuits by means of conventional S-Y parameter conversion.

Another significant step in frequency domain measurements is to derive the equivalent circuits in a wide frequency span. Therefore, time domain and frequency domains can be bridged with network spice model developed. This transformation can be carried out as follows:

i) Extract equivalent circuits from s parameters at discrete frequency points.
ii) Extract equivalent circuits at certain frequency span, for example 100MHz to 1280MHz for the resistor network characterization.
iii) Use an ADS linear simulator for fine tuning and verification of the equivalent circuit.

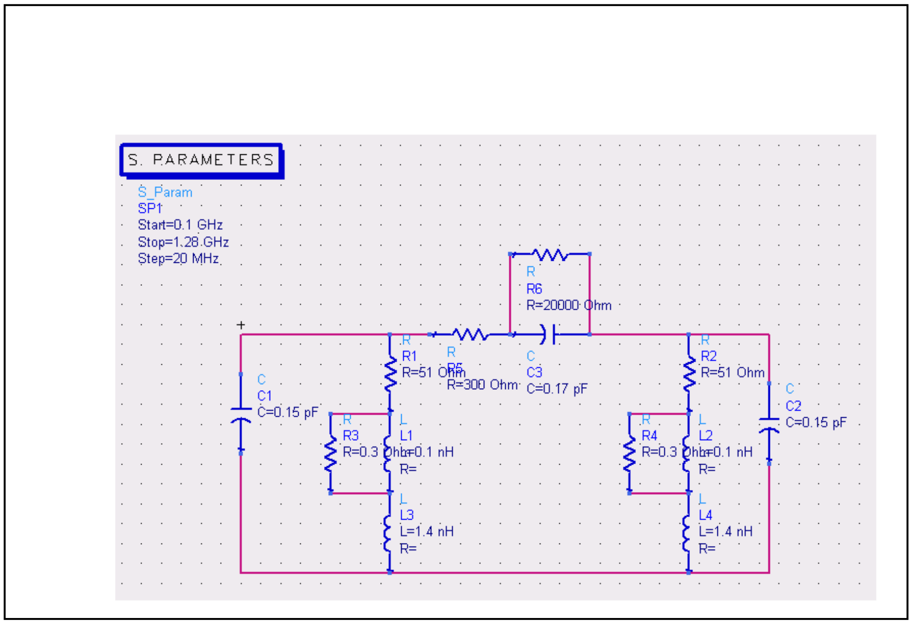


Figure 2. 51 Ω BGA (CTS 73510J022) termination network equivalent circuit

A sample of 5 different CTS terminator part numbers were measured. Each resistance value had 10 samples and was measured on the set up as shown in Figure 1. The measured data were processed to derive the equivalent circuit. Figure2 and Figure3 show the equivalent circuit of a 51Ω BGA termination network and a LVD SCSI termination network.

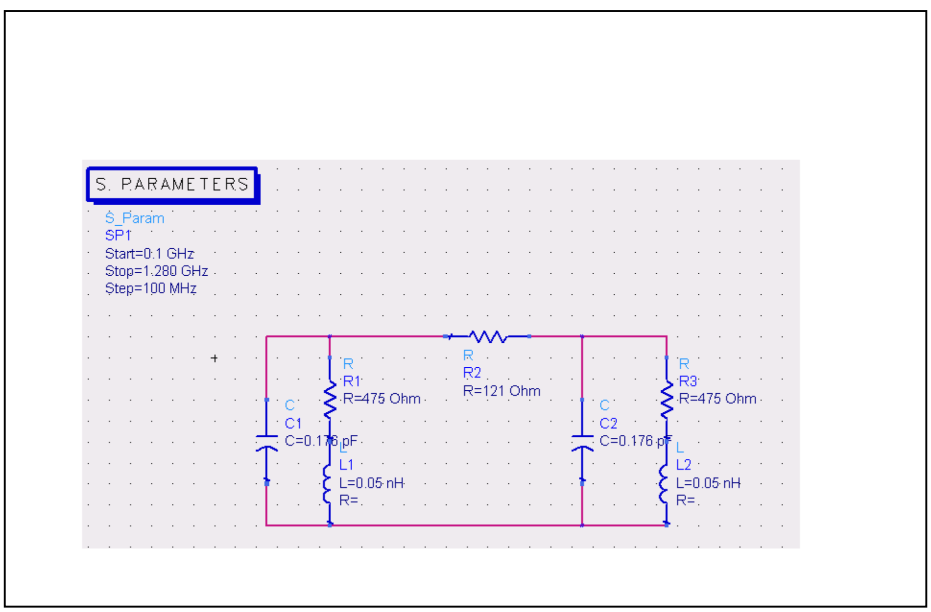


Figure 3. LVD SCSI BGA (CTS RT1300EV, T1) termination network equivalent circuit

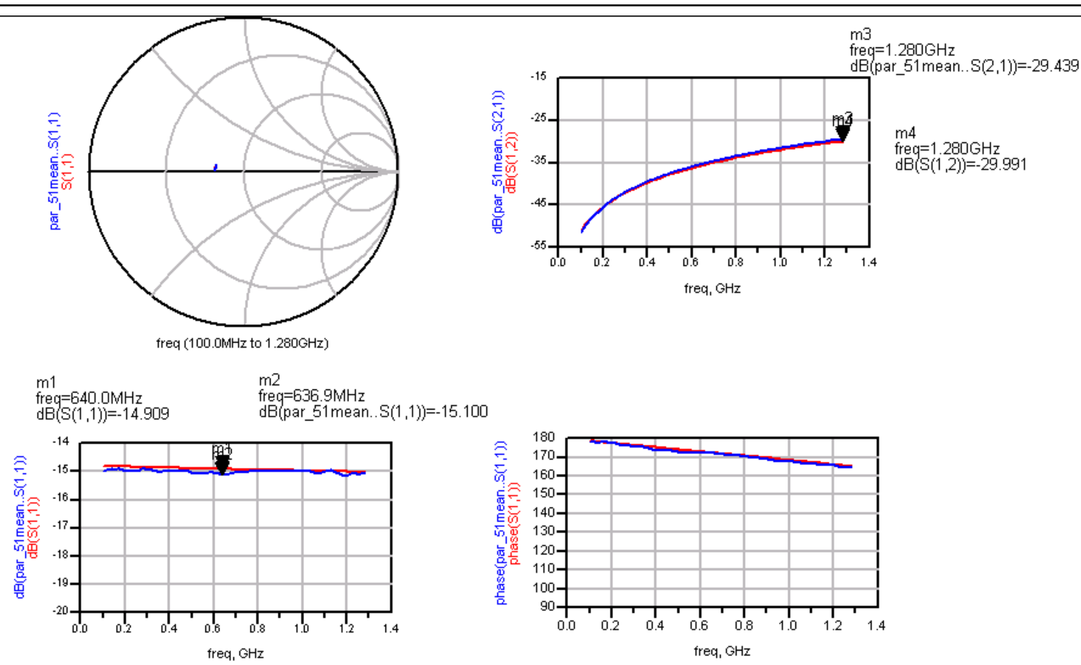
Figure 4 and Figure 5 show the comparison of equivalent circuit simulations and measured s parameter results of the 51 Ω BGA network and LVS SCSI BGA termination network respectively. It can be observed that satisfactory agreements between the s-parameter and equivalent circuit simulation have been obtained.

In digital data transmission the parasitic parameters are of great interests because they may cause undesired skew, cross talk or jitter. The major BGA resistor network design goal is to reduce these parasitics. With the s-parameters measurements and equivalent circuit derivation those parasitic parameters can be well characterized. The major parasitic parameters of various CTS BGA termination networks are listed in Table1.

Table 1.

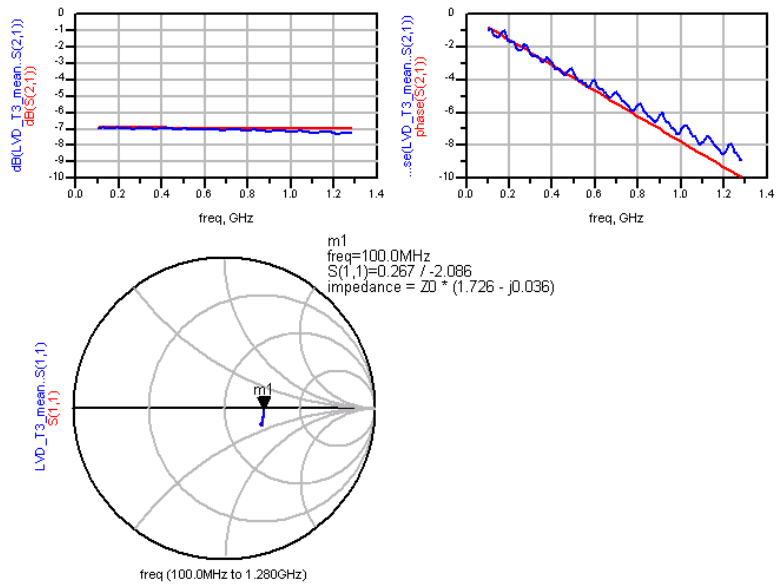
	I/O Inductance (nH)	I/O capacitance (pF)	Coupling Capacitance Of two adjacent resistors (pF)
CTS 73220J022	1.5	0.2	0.6
CTS 71220G010	1.5 –1.7	0.2	1.5
CTS 73380J018	1.5	0.2	0.25
CTS 73510J018	1.5	0.15	0.17
CTS RT1300EV	0.05	0.22	0.12

The equivalent circuits are simulated with ADS to compare s parameters with measurement results. Good correlation has been reached between measurements and simulations. Figure 4 and Figure 5 are the examples of these comparisons.



51 Ohm isolated measurement results and equivalent circuit simulation comparison

Figure 4. 51Ω BGA termination network (CTS73510J022) simulation and measurement comparison



LVD T3 measurement results and equivalent simulation comparison

Figure 5. LVD SCSI BGA termination network (CTS RT1300EV) simulation and measurement comparison.

The results presented in this paper show good agreement between the measurement and simulation methods of model extraction. Which suggests that high-speed digital prototype circuits and production digital/analog circuits may be verified in the frequency domain by extraction of a spice model. It follows from these results that reliable results can be generated in the frequency domain using spice model extraction with recent software package developments and programs used in high frequency simulation, simulation of transmission lines, and interconnections. With the aid of these simulation tools and proper modeling of the circuits, digital circuit hardware development cycles should be shortened.

The next question to answer is how does this next generation low inductance and capacitance BGA SCSI terminator fit into the next generation of SCSI technology? Where we will soon be seeing SPI-4 (Ultra320) LVD SCSI with a data rate of 320 MB/sec (Mega-byte/sec), double data clocking, bus training with different pre and post compensation voltages and current driver schemes along with smart active adaptive filtering schemes and technologies. Ultra640 SCSI (SPI-5) is between 2 and 4 years away. What will be the effects of parasitics and the inherent packaging characteristics on the Ultra640 generation of SCSI?

The following figures begin to give some indication of the importance of being able to extract equivalent circuit parameters at different frequencies for modeling purposes as SCSI speeds continue to climb. Using models generated by these techniques we should be able to address these questions to arrive at answers that will be needed as the technology continues to move forward.

Fig. 6: Output waveforms (ch1, ch2) at beginning and end of 25m cable with precomp disabled, at nominal drive strength and slew rate settings (12mA assertion, 8mA negation, 1.9ns).

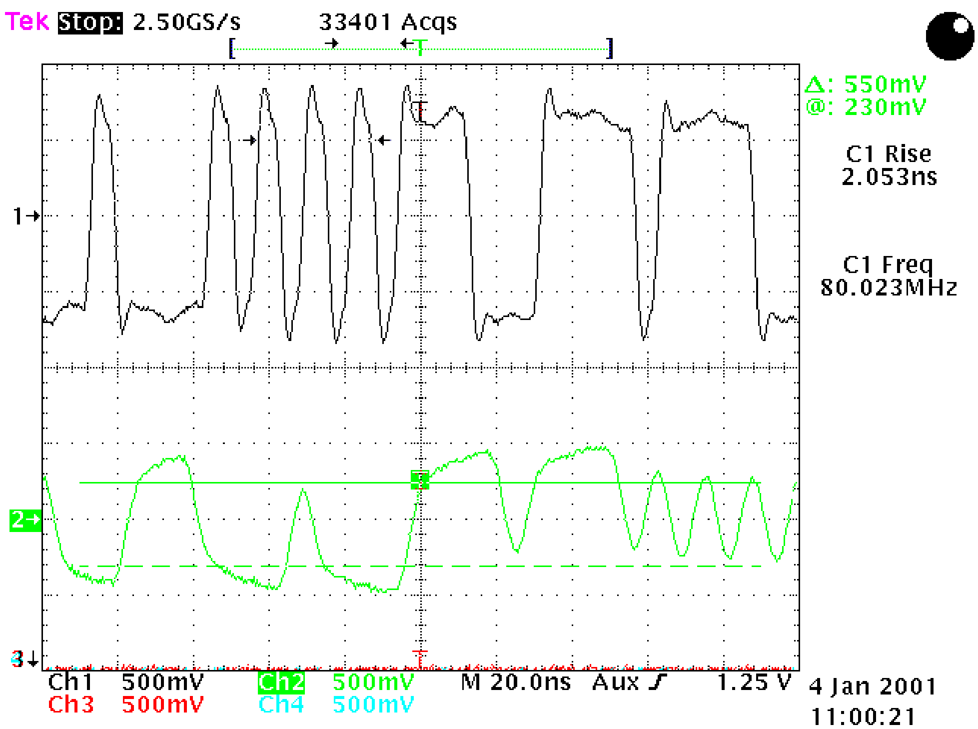
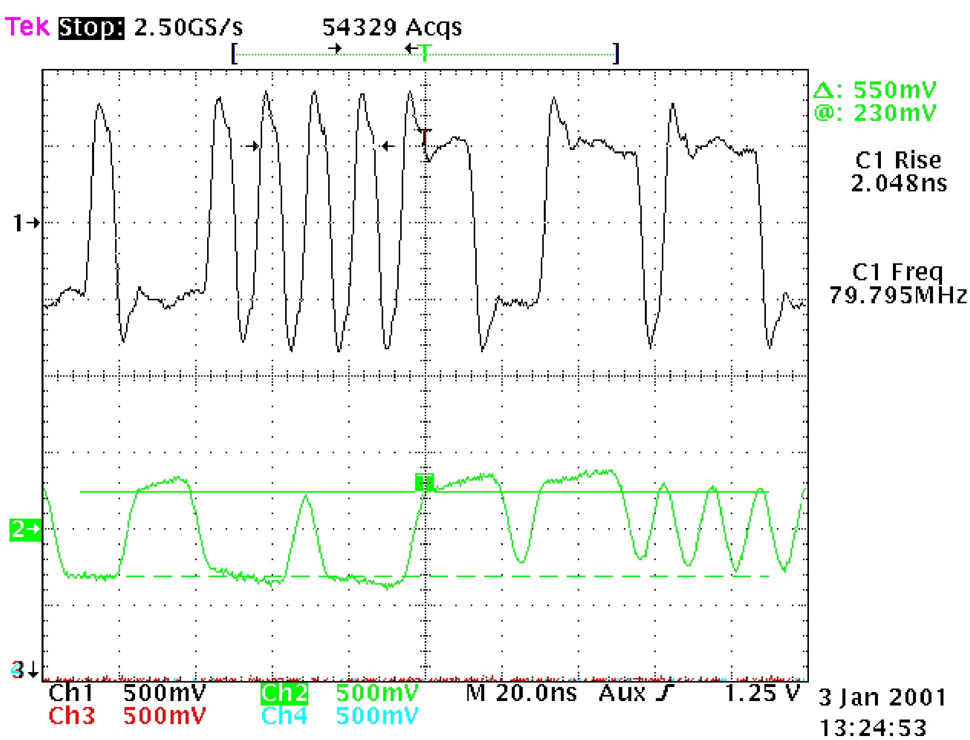


Fig 7: Output waveforms (ch1, ch2) at beginning and end of 25m cable with precomp enabled, with LVD signaling set up for nominal drive strength and slew rate (10mA assertion, 6mA negation, 1.9ns). Note the improvement in the leveling out of the far end signal (ch. 2).



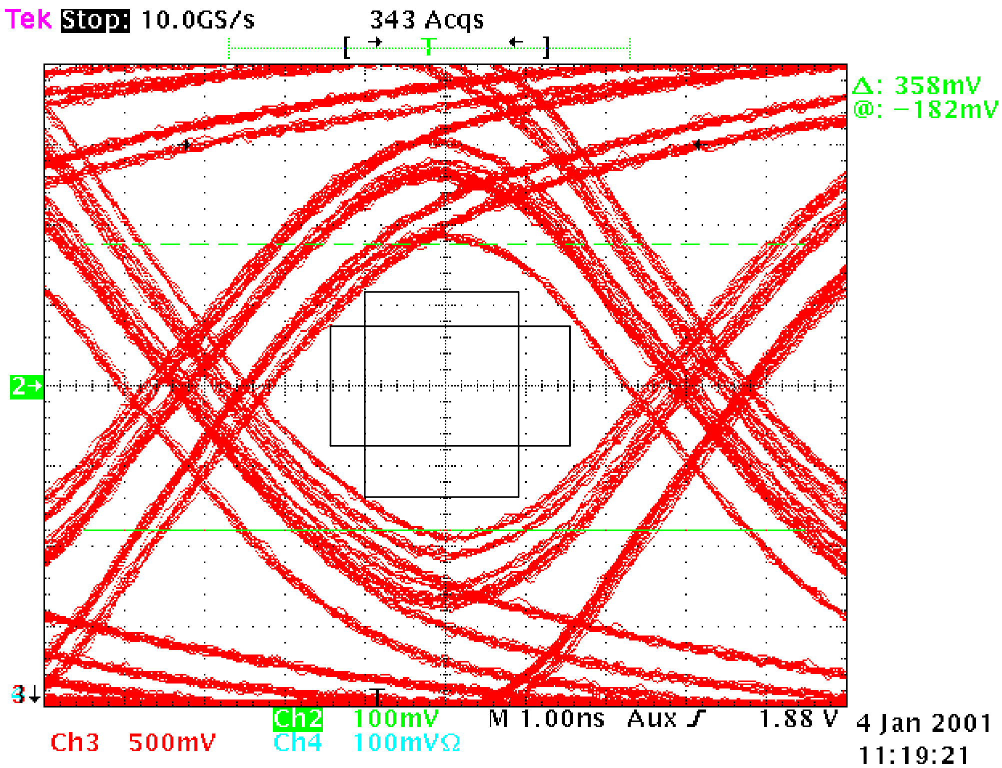


Fig 8: Eye diagram of DB9 (DataBit9) at far end of 25m cable with pre-emphasis disabled and nominal settings.

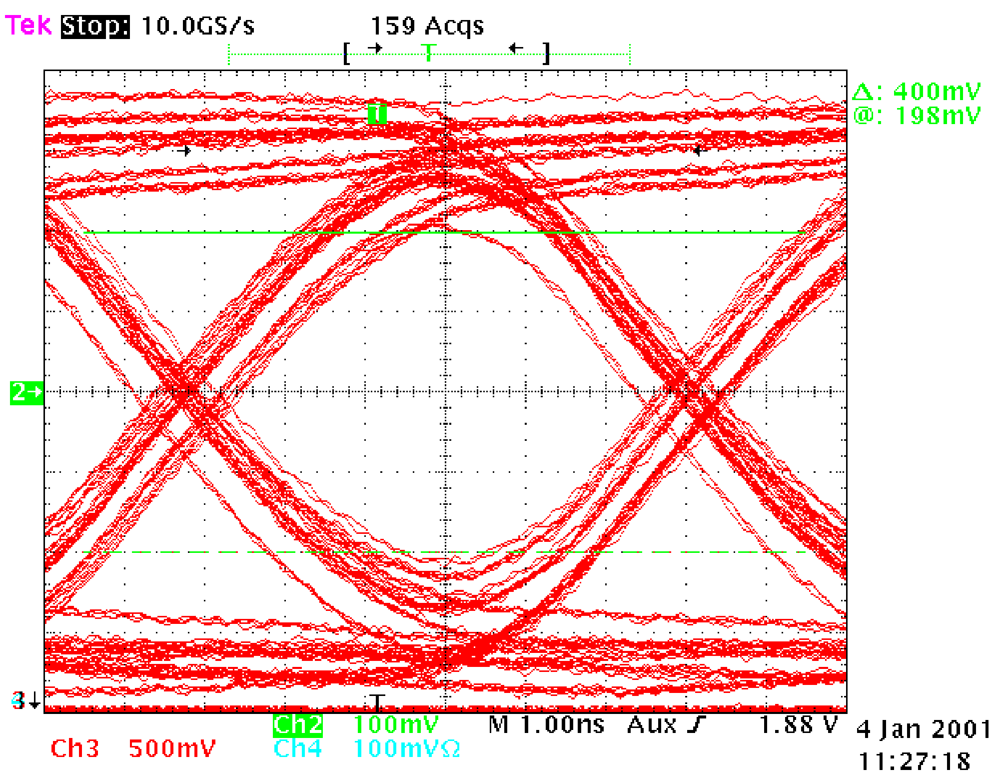
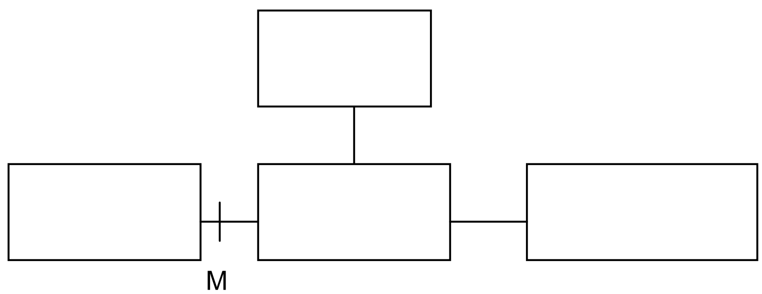


Fig 9: Eye diagram of DB9 at far end of 25m cable with pre-emphasis enabled and nominal settings.

Generally in digital circuit design which the current and future SCSI technologies fall under, empirical formulas describing the circuit characteristics are frequently used. Those formulas are generally frequency independent and lack accuracy. As digital system speeds and particularly SCSI bus speeds steadily climb higher good agreement between the measured and simulation results are needed. Results presented in this paper suggest that the high-speed prototype circuits may be verified in the frequency domain by extraction of it spice models. With recent developments of software packages used in high frequency simulation, simulation of a transmission lines and interconnections can generate reliable results in the frequency domain using spice model extraction. With the aid of those simulation tools and proper modeling of the circuits, digital circuit hardware development cycles should be shortened.

As an example of what could be done about the termination device, we suggest that a preferable termination, i.e. a preferable reflection, can be obtained with a certain match circuit if a target refection coefficient looking into the data bus at M is known,



The remaining issue is to know what are the s parameters at the network connection for a certain match circuit and termination device. The network S parameters can be derived as

$$S_{ep} = S_{pp} + S_{pc}(\mathrm{I} - S_{cc})^{-1} S_{cp}$$

Where S_{ep} is the S parameter matrix of external and internal ports of overall system. S_{pp} S_{cp}, S_{pc} and S_{cc} are the s parameter matrix from circuit blocks. I is the internal ports connection matrix.

$$I = \begin{bmatrix} 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 \end{bmatrix}$$

With recent developments of software packages used in high frequency simulation, simulation of a transmission lines and interconnections can generate reliable s parameters in the frequency domain. S_{pp} S_{cp}, S_{pc} and S_{cc} can be obtained from simulation results of the design. After S_{ep} is calculated, the spice model can be derived and time domain results can be obtained. Because the circuit can be simulated before real prototype devices are fabricated, a more accurate design is expected. This approach should greatly shorten the cut and try process of the digital circuit hardware development cycles. This is one of the author's experiences that by means of electromagnetic simulation a termination device high frequency performance can be predicted at a prototype design phase with good accuracy. It is also believed that this frequency domain to time domain approach can be applicable to termination/data bus design with many aspects of superiority over time domain approach.

References

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