Application Report
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Use of the CMOS Unbuffered Inverter in Oscillator Circuits

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ABSTRACT

CMOS devices have a high input impedance, high gain, and high bandwidth. These characteristics are similar to ideal amplifier characteristics and, hence, a CMOS buffer or inverter can be used in an oscillator circuit in conjunction with other passive components. Now, CMOS oscillator circuits are widely used in high-speed applications because they are economical, easy to use, and take significantly less space than a conventional oscillator. Among the CMOS devices, the unbuffered inverter (’U04) is widely used in oscillator applications. This application report discusses the performance of some TI ’U04 devices in a typical crystal-oscillator circuit.

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1 Introduction

Resistors, inductors, capacitors, and an amplifier with high gain are the basic components of an oscillator. In designing oscillators, instead of using discrete passive components (resistors, inductors, and capacitors), crystal oscillators are a better choice because of their excellent frequency stability and wide frequency range. A crystal basically is an RLC network that has a natural frequency of resonance.

2 Theory of Oscillators

In principle, an oscillator can be composed of an amplifier, A, with voltage gain, a, and phase shift, α, and a feedback network, F, with transfer function, f, and phase shift, β (see Figure 1).

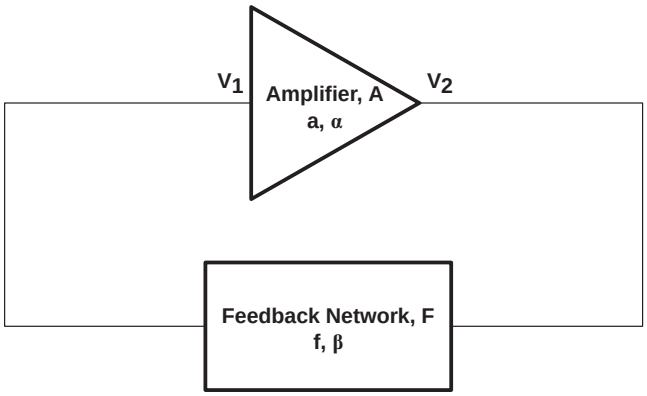

Figure 1. Oscillator

For $|f| \times |\alpha| \geq 1$ the oscillating condition is fulfilled, and the system works as an oscillator.

f and a are complex quantities; consequently, it is possible to derive from equation 1

$$|f| \times |\alpha| \times \exp\left[j(\alpha + \beta) \geq 1\right] \quad (1)$$

the amplitude

$$|f| \times |\alpha| \geq 1 \quad (2)$$

and the phase

$$(\alpha + \beta) = 2 \times \pi \quad (3)$$

To oscillate, these conditions of amplitude and phase must be met. These conditions are known as the Barkhausen criterion. The closed-loop gain should be ≥1, and the total phase shift of 360 degrees is to be provided.

2.1 Characteristics of Crystals

Figure 2 is an electrical-equivalent circuit of a quartz crystal.

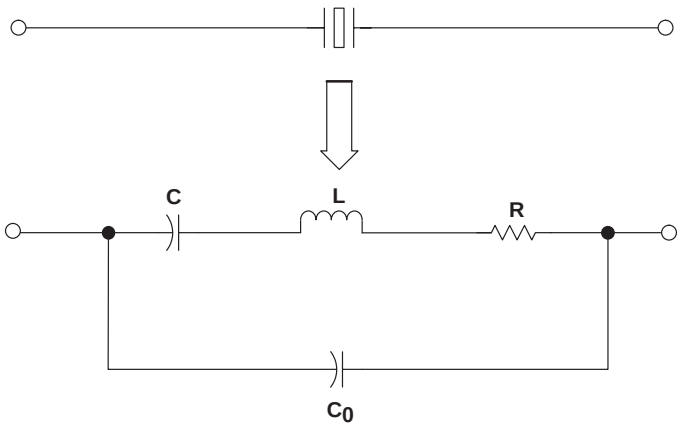

Figure 2. Electrical-Equivalent Circuit of a Crystal

The quantities C and L are determined by the mechanical characteristics of the crystal; R is the resistance of the resonant circuit at the series resonance, and C_0 represents the capacitance of the leads and electrodes. C_0 is much larger than C and is affected by the stray capacitances of the final circuit. Because R is negligible, the impedance of this circuit is given by equation 4.

$$Z = \frac{j}{\omega} \times \frac{\omega^2 LC - 1}{(C_o + C) - (\omega^2 LCC_o)} \tag{4}$$

A series-resonance frequency is attained when the impedance, Z, approaches 0, $Z \rightarrow 0$

$$f_{ser} = \frac{1}{2\pi\sqrt{LC}} \tag{5}$$

A parallel-resonance frequency is attained when the impedance, Z, approaches ∞, $Z \rightarrow \infty$

$$f_{par} = f_{ser}\sqrt{1 + \frac{C}{C_o}} \tag{6}$$

An oscillator circuit using the parallel resonance mode of the crystal is less stable than the equivalent circuit using the series resonance, because of the dependence on the external circuit parameter. For series resonance, the crystal appears as a series-resonant resistance, R. For parallel resonance, the crystal appears as an inductive load.

In the oscillator circuit, the crystal acts as the feedback network. For proper operation, the input impedance of the amplifier should be well matched to the low series-resonant resistance of the crystal. For HCMOS devices, because of the high input impedance, a crystal operated in series resonance would be completely mismatched. The solution is to operate the crystal in parallel-resonance mode. But, parallel resonance has a poor frequency response compared to series resonance because of the dependence on C_0 (stray capacitance or circuit capacitance). Connecting a capacitance in parallel (C_P) with the crystal can reduce the influence of C_0 on the parallel-resonance frequency. From the equation of the parallel-resonance frequency

$$f_{par} = \frac{1}{2\pi\sqrt{LC}}\sqrt{1 + \frac{C}{C_p + C_o}} \tag{7}$$

By choosing $C_P > C_0$ (C_0 is approximately 3 pF to 5 pF, and C_P typically is 30 pF).

$C_P >> C$ (C is in the range of femtofarads)

$$f_{par} \approx \frac{1}{2\pi\sqrt{LC}} \tag{8}$$

Now, the parallel-resonance frequency is approximately equal to the series-resonance frequency.

A popular application of the parallel-resonance circuit is the Pierce oscillator circuit (see Figure 3) in which the parallel combination of C_1 and C_2 constitutes C_P.

$$C_P = \frac{C_1 C_2}{C_1 + C_2} \tag{9}$$

C_1 and C_2 form a capacitor voltage divider that determines the degree of feedback. The feedback factor is given by

$$f = \frac{C_1}{C_2} \tag{10}$$

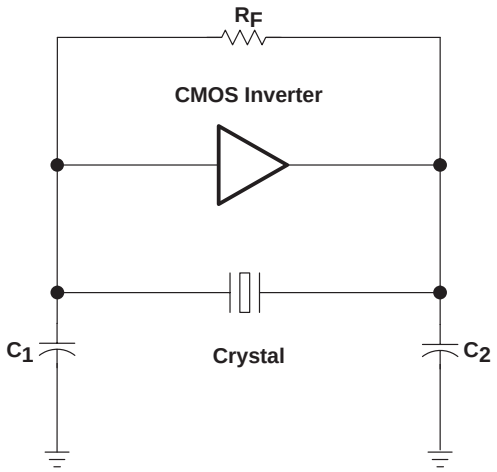

Figure 3. Pierce Oscillator Using CMOS Inverter

The optimal value for C_p determines the quality and frequency stability of the crystal oscillator. Usually, the crystal manufacturer's data sheet specifies the recommended load for the crystal (C_L). C_p represents the load for the crystal, and this should be equal to C_L, as specified in the crystal manufacturer's data sheet.

In an oscillator circuit, the CMOS inverter operates in the linear mode and works as an amplifier. The phase shift provided by the inverter is 180 degrees. To meet the oscillating condition, the crystal oscillator must provide an additional 180 degrees of phase shift. If $C_1 = C_2$, current through them is identical and 180 degrees out of phase from each other. Hence, for $C_1 = C_2$, the crystal provides a phase shift of 180 degrees.

The feedback resistor modifies the input impedance of the CMOS inverter. For an inverter with an open-loop gain much higher than 1, the input impedance becomes

$$Z_i = \frac{R_F}{\alpha} \tag{11}$$

The parallel-resonance resistance of the crystal is modified by the load capacitor, C_p.

$$R_p = \frac{1}{R\omega^2 (C_o + C_p)^2} \tag{12}$$

R_p should match the input impedance of the CMOS inverter. For example, if a crystal oscillator has the following parameters:

$C_p = C_L = 30$ pF

$C_o = 7$ pF

R = 80 Ω at 5 MHz

$$R_p = \frac{1}{\left[80 \times \left(2 \times \pi \times 5 \times 10^6\right)^2 \times \left(30 \times 10^{-12} + 7 \times 10^{-12}\right)^2\right]} \tag{13}$$

From the calculation

$R_p \approx 10\ k\Omega$

R_p should be equal to Z_i, i.e.,

$Z_i = R_p = 10\ k\Omega$

$Z_i = \frac{R_F}{\alpha} = 10\ k\Omega$

$Z_i = \frac{R_F}{a}$ = 10 kΩ

$R_F = 10\ k\Omega \times \alpha$

For a CMOS inverter with an open-loop gain, a = 100, the value of the feedback resistor is calculated as:

$$R_F = 10000 \times 100 = 1 \times 10^6 = 1\ M\Omega \tag{14}$$

By using a feedback resistor of 1 MΩ, successful oscillation can be accomplished. In practical applications, the value of the feedback resistor usually will be greater than 1 MΩ in order to attain higher input impedance, so the crystal can easily drive the inverter.

3 Buffered and Unbuffered CMOS Inverters in Oscillator Circuits

Unbuffered inverters have a single inverting stage, and the gain of this type of inverter is in the range of hundreds. Buffered inverters have more than one stage, and the gain is in the range of several thousand. In the buffered inverter, power consumption usually is less than in the unbuffered inverter, because the first and the second inverter stages consume significantly less power-supply current than the output stage. Because the first stage remains in linear mode during oscillation, a buffered inverter consumes less power than an unbuffered inverter. Both buffered and unbuffered inverters can be used for oscillator applications, with only slight design changes. Because the gain of buffered inverters is very high, they are sensitive to parameter changes in the oscillator circuit and are less stable than unbuffered inverters.

4 Characteristics of a CMOS Unbuffered Inverter

The choice of a CMOS inverter for oscillator applications depends on various factors, for example open-loop gain, power consumption, duty-cycle variation with temperature, etc. In the following paragraphs, some of these characteristics of TI CMOS inverters that are critical in selecting an inverter for oscillator application are described.

4.1 Open-Loop Gain

A CMOS inverter is used as a linear amplifier in oscillator applications and, similar to a conventional amplifier, their open-loop gain is a critical characteristic. The bandwidth of an inverter decreases as the operating voltage decreases. The open-loop gain of the LVC1GU04, AHC1GU04, and AUC1GU04 is shown in Figures 4, 5, and 6.

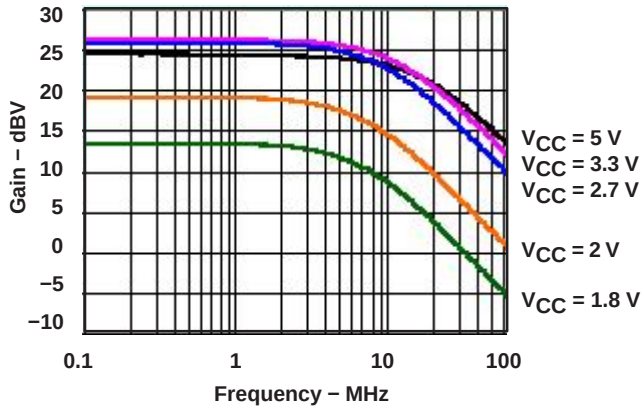

Figure 4. Open-Loop Gain Characteristics of LVC1GU04

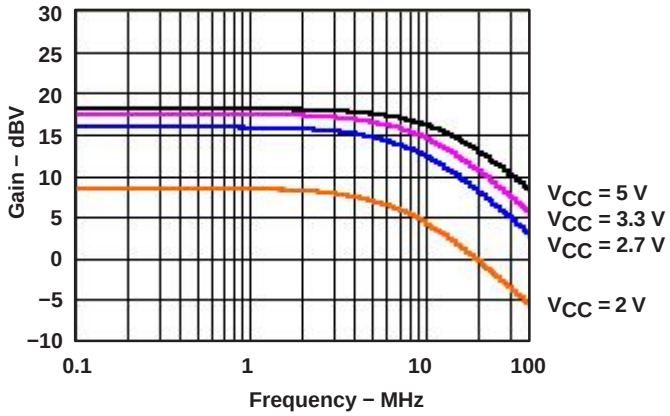

Figure 5. Open-Loop Gain Characteristics of AHC1GU04

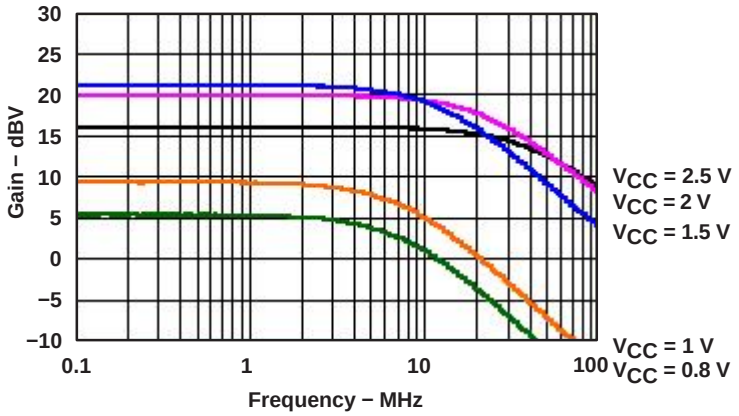

Figure 6. Open-Loop Gain Characteristics of AUC1GU04

4.2 V_O vs V_I

V_O vs V_I characteristics can be used to determine the bias point of the inverter. In the oscillator application, the inverter operates in the linear mode or in the transition region. The transition region is defined as the region where the slope of the curve is maximum. For example, for the LVC1GU04, the region is between 2 V and 2.5 V for V_{CC} = 5 V. A device with a higher open-loop gain will have a narrower transition region compared to the transition region of a device with lower open-loop gain. V_O vs V_I characteristics of the LVC1GU04, AHC1GU04, and AUC1GU04 are shown in Figures 7, 8, and 9.

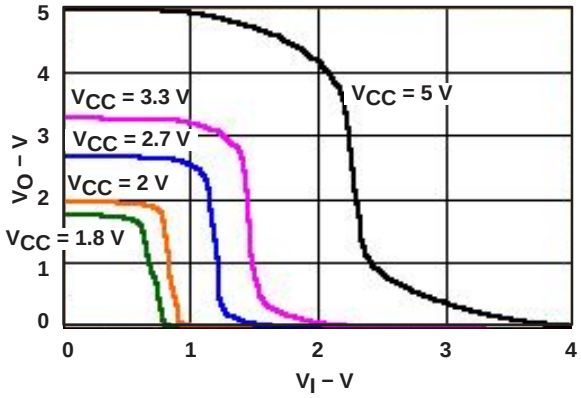

Figure 7. V_O vs V_I Characteristics of LVC1GU04

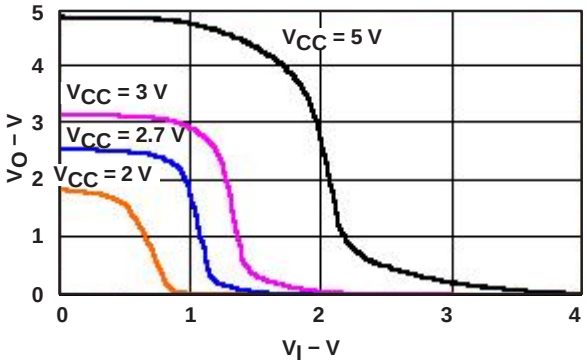

Figure 8. V_O vs V_I Characteristics of AHC1GU04

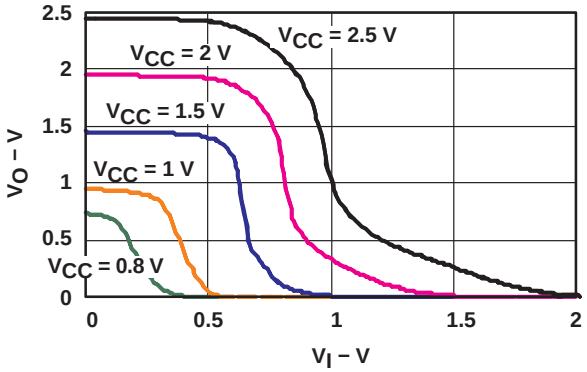

Figure 9. V_O vs V_I Characteristics of AUC1GU04

4.3 I_{CC} vs V_I

I_{CC} vs V_I characteristics of the LVC1GU04, AHC1GU04, and AUC1GU04 are shown in Figures 10, 11, and 12. This characteristic determines the dynamic power consumption of the inverter in the oscillator circuit. The setup is shown in Appendix A. Due to the 1-kΩ load, I_{CC} is high when V_I is 0.

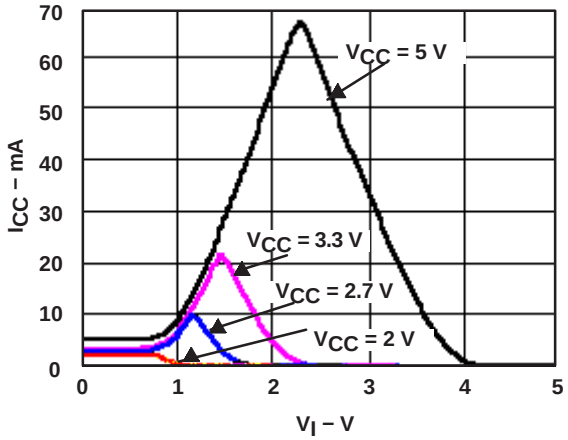

Figure 10. I_{CC} vs V_I Characteristics of LVC1GU04

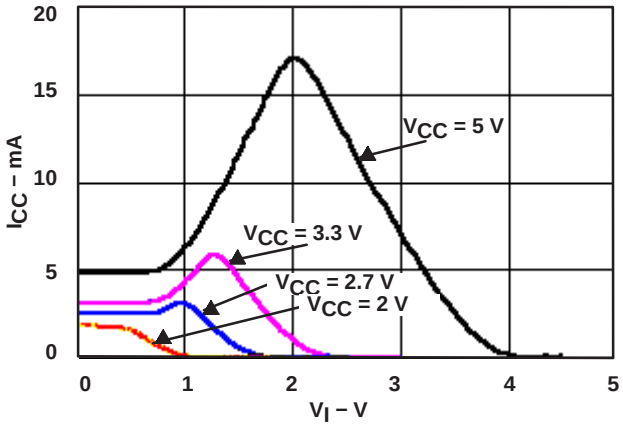

Figure 11. I_{CC} vs V_I Characteristics of AHC1GU04

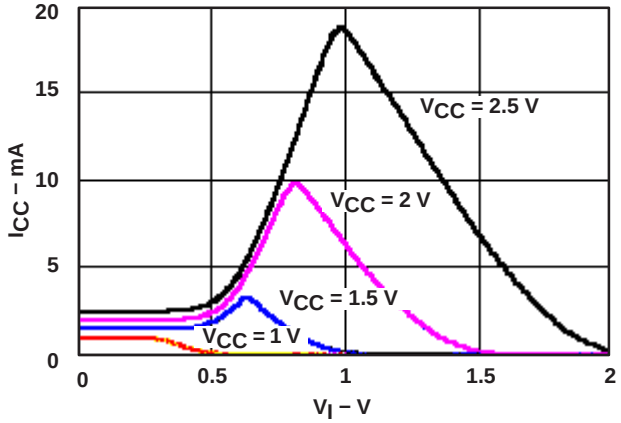

Figure 12. I_{CC} vs V_I Characteristics of AUC1GU04

4.4 Variation of Duty Cycle With Temperature

One of the primary concerns in the oscillator application is the variation of duty cycle with temperature. For example, in the clock-pulse generator circuits, too much variation of the duty cycle with the temperature is not permitted. Figures 13, 14, and 15 show the variation of duty cycle with temperature for the LVC1GU04, AHC1GU04, and AUC1GU04.

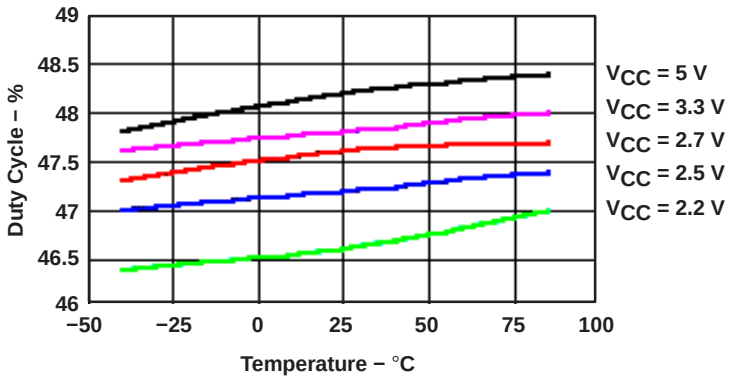

Figure 13. Duty-Cycle Variation in LVC1GU04

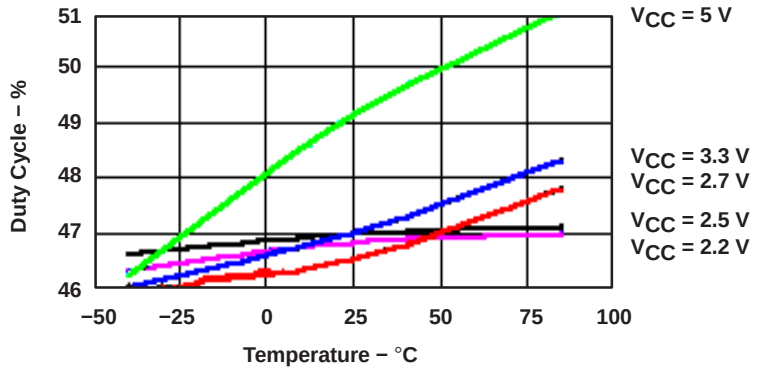

Figure 14. Duty-Cycle Variation in AHC1GU04

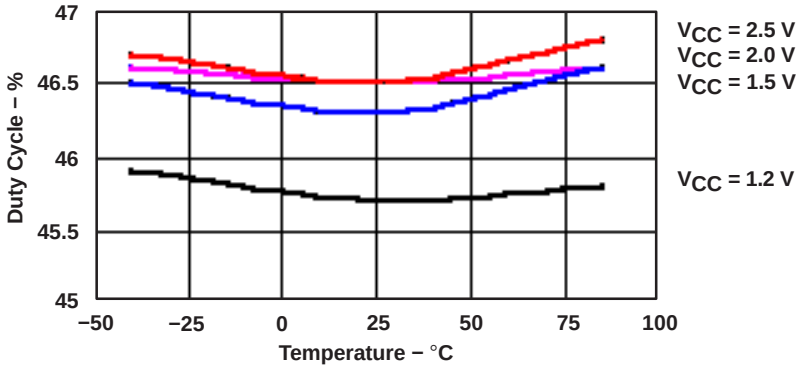

Figure 15. Duty-Cycle Variation in AUC1GU04

5 Characteristics of LVC1404

The TI LVC1404 is a dual inverter gate that is very suitable for oscillator applications. This device has a wide V_{CC} range and can be used for a wide range of frequencies. The device has both unbuffered and buffered outputs. Figure 16 shows the pinout diagram and Figure 17 shows the logic diagram for LVC1404.

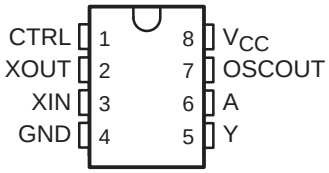

Figure 16. Pinout Diagram for LVC1404

As shown in Figure 17, XIN is connected to an unbuffered inverter, and the output of this inverter (XOUT) is connected to the input of another inverter to get a clean rail-to-rail signal and to provide sufficient drive capability. The crystal is connected between the XIN and XOUT.

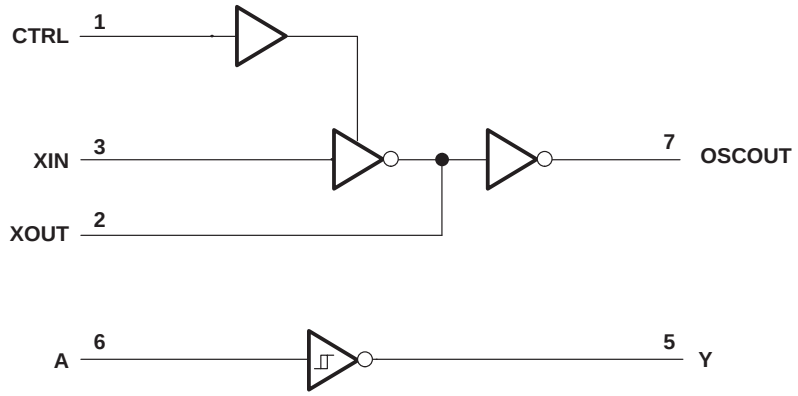

Figure 17. Logic Diagram of LVC1404

Figure 18 shows the open-loop-gain characteristics of the unbuffered inverter of the LVC1404 (i.e., between XIN and XOUT). The device provides a high gain over a wide range of frequencies.

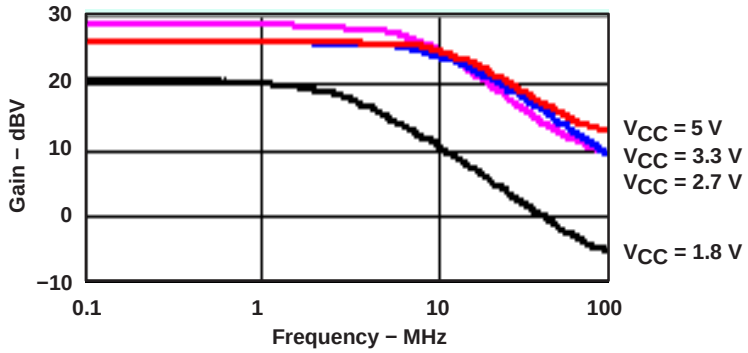

Figure 18. Open-Loop-Gain Characteristics of LVC1404

6 Practical Oscillator Circuits

Figure 19 shows an example of an oscillator circuit that uses a 16-pF, 25-MHz crystal and an unbuffered inverter, LVC1GU04. In actual applications, the passive components may require adjustment to get the desired oscillation. For example, C_1 and C_2 can be adjusted to take into consideration the input and output capacitance of the LVC1GU04 and the desired duty cycle of oscillation.

Appendixes B and C show the performance of TI's LVC1GU04 and LVC1404 devices in this Pierce crystal-oscillator circuit.

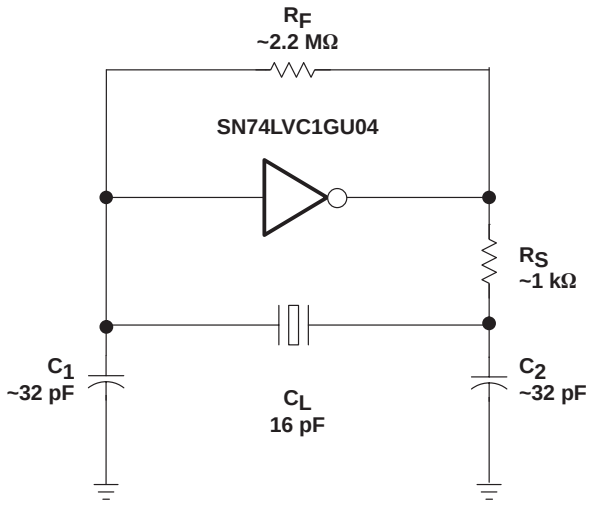

Figure 19. Pierce Oscillator Circuit Using Unbuffered CMOS Inverter

6.1 Selection of Resistors and Capacitors

Selection of resistors and capacitors depends on various factors, such as inverter gain, frequency stability, power consumption, crystal characteristics, startup time, etc. Several trial-and-error methods may be needed to find optimum values for these resistors and capacitors. The effects of these components are discussed in the following paragraphs.

6.1.1 R_F

R_F is the feedback resistor of the CMOS inverter and it biases the inverter in its linear region. The chosen value of R_F is sufficiently large so that the input impedance of the inverter and the crystal can be matched. Usually, the value chosen is between 1 MΩ and 10 MΩ.

6.1.2 R_S

R_S isolates the output of the inverter from the crystal and prevents spurious high-frequency oscillation, so that a clean waveform can be obtained. The optimum value of R_S depends on the frequency of operation and the required stability.

The minimum value of R_S depends on the recommended power consumption of the crystal. Crystal manufacturers usually specify a recommended value of R_S in the crystal data sheet. Using a value lower than that in the crystal data sheet may cause overdriving of the crystal and result in damage to the crystal or shorten the crystal life.

Acceptable results can be accomplished by choosing the value to be approximately equal to the capacitive reactance, i.e., $R_S \approx X_{C_2}$, provided X_{C_2} is greater than or equal to the manufacturer's recommended value. Making $R_S \approx X_{C_2}$ will cause a 50% voltage drop due to voltage-divider action. This requires that the gain of the inverter be equal to, or greater than, 2. Because the gain of a CMOS inverter is much higher than 2, the closed-loop gain is still higher than unity. The gain of a buffered inverter is considerably higher than an unbuffered inverter. If a buffered inverter is used, R_S can be increased so that the closed-loop gain of the system is decreased and stability is improved.

The effect of R_S is shown in Figures 20 and 21. Decreasing R_S results in a faster edge rate and increased closed-loop gain.

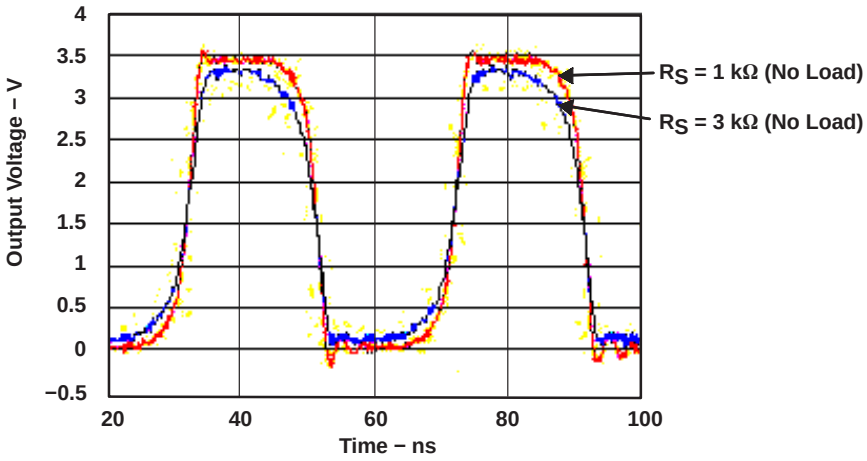

Figure 20. Effect of R_S on Oscillator Waveform (No Load)

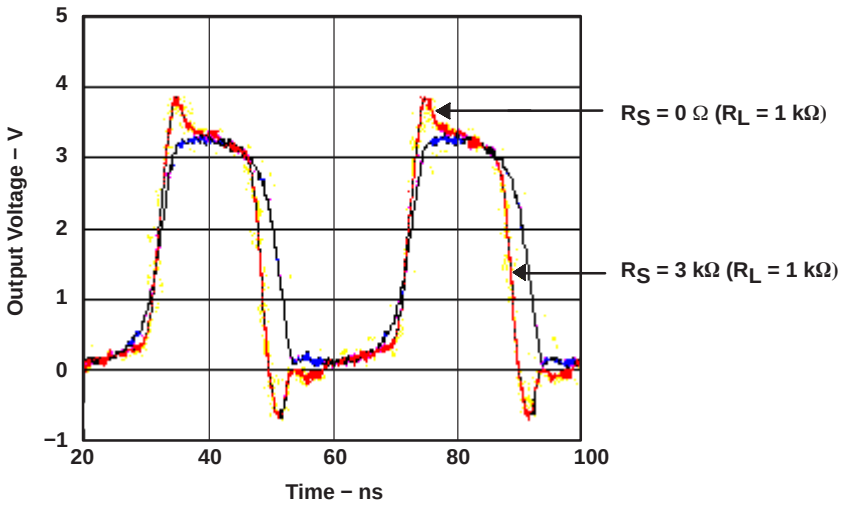

Figure 21. Effect of R_S on Oscillator Waveform (R_L = 1 kΩ)

Figures 22 and 23 show the relative effect of the R_S on the gain and the phase response of the feedback network of the oscillator circuit described in Figure 19. R_S not only reduces the gain, but also shifts the resonance frequency and introduces additional phase delay.

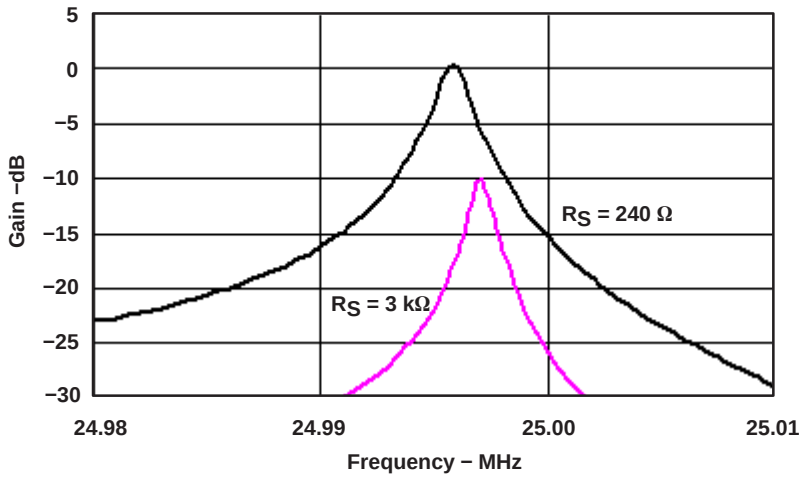

Figure 22. Effect of R_S on the Frequency Response of Feedback Network

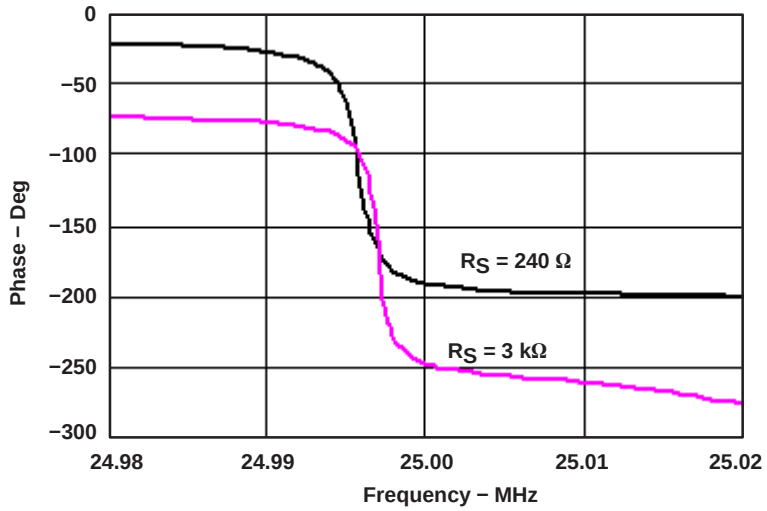

Figure 23. Effect of R_S on the Phase Response of Feedback Network

R_S also affects the duty cycle and power consumption (I_{CC}) of the oscillator circuit. Appendix B shows the effect of R_S on duty cycle and the power consumption (I_{CC}) in an oscillator circuit using an LVC1GU04 as the amplifier.

At low frequency, phase shift due to the CMOS inverter is small and can be neglected. Phase shift is given by equation 15.

Phase shift = Frequency of oscillation × Propagation delay × 360 degrees (15)

If the propagation delay of a CMOS inverter is 5 ns, then, at 25 MHz, the phase shift introduced by the inverter is 45 degrees. For high frequency, using a series feedback resistor (R_S) is not feasible because it adds additional phase shift. R_S can be replaced by a capacitor whose value is approximately equal to the input impedance of the crystal, i.e., $C_S \approx C_2$.

6.1.3 C_1 and C_2

The values of C_1 and C_2 are chosen such that the parallel combination of C_1 and C_2 equals the recommended capacitive load (C_L) specified in the crystal data sheet, i.e.:

$$C_L = \frac{C_1 C_2}{C_1 + C_2}$$

R_S and C_2 form a low-pass filter and reduce spurious oscillation. The value can be adjusted, based on the desired cutoff frequency. Another factor in choosing C_2 is the start-up time. For a low-gain amplifier, sometimes C_2 is increased over C_1 to increase the phase-shift and help in start-up, but C_1 should be within a limit such that the load capacitance introduced to the crystal does not exceed the manufacturer's recommended value of C_L. Otherwise, the resonance frequency will change.

7 Practical Design Tips

The performance of an oscillator circuit using a CMOS inverter is sensitive to the circuit components, layout etc. In designing an oscillator circuit, careful attention should be given to eliminate external effects:

- The oscillator circuit feedback factor should not be too large; otherwise, there will be instability, and oscillation will not be determined by the crystal alone.
- A CMOS inverter with a Schmitt-trigger input is not suitable for use in the oscillator circuit described previously. A Schmitt-trigger input device has two different thresholds, and it may not be possible to bias them properly in the linear region using the circuit described previously.
- At higher frequencies, the ground lead to the central point of connection always should be as large in area and as short in length as possible. This provides low resistance and low inductance and, thereby, the effect on oscillation is less. Use of a multilayer board, with one layer for V_{CC} and one for ground, is preferable.
- An unbuffered inverter itself may not have enough drive for a high-capacitive load. As a result, the output voltage swing may not be rail to rail. This also will slow down the edge rate of the output signal. To solve these problems, a buffer or inverter with a Schmitt-trigger input can be used at the output of the oscillator. Examples of Schmitt-trigger input buffers and inverters are the LVC1G17 and LVC1G14. Figure 24 shows an example circuit.

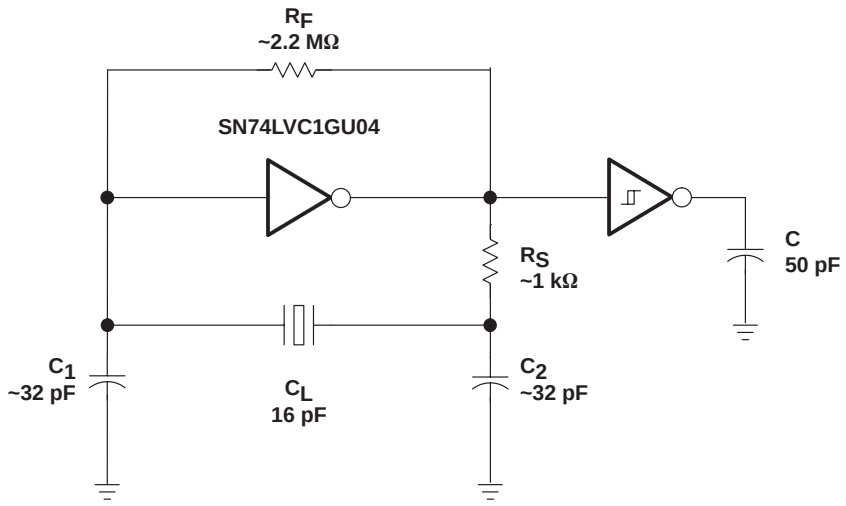

Figure 24. Oscillator Circuit Using a Schmitt-Trigger Input Inverter

- Good power-supply decoupling is necessary to suppress noise spikes on the supply line. Low-resonance ceramic capacitors should be used as close to the circuit as possible. The reference value is 100 nF.
- Connections in the layout should be as short as possible to keep the resistance and inductance low.
- To reduce crosstalk, standard PCB design techniques should be used. For example, if the signal is routed together with other signals, crosstalk can be reduced by a factor of 3 if there is a ground line between adjacent signal lines.
- Without a crystal, the oscillator should not oscillate. To check this, the crystal in a CMOS oscillator can be replaced by its equivalent parallel-resonant resistance.

Appendix A. Laboratory Setup

A.1 Laboratory Setup to Measure Open-Loop Gain Characteristics

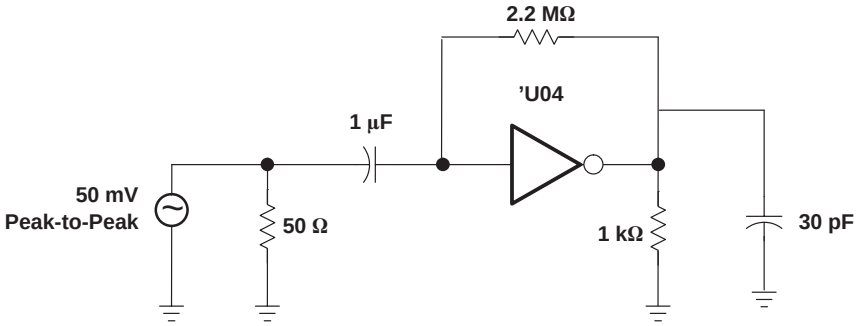

Figure A−1. Open-Loop-Gain Measurement Setup

A.2 Laboratory Setup to Measure I_{CC} vs V_I Characteristics

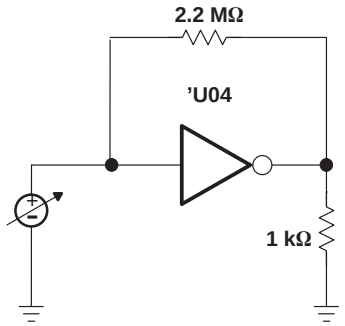

Figure A−2. I_{CC} vs V_I Measurement Setup

Appendix B. LVC1GU04 in Crystal-Oscillator Applications

B.1 LVC1GU04 in 25-MHz Crystal-Oscillator Circuit

$C_1 \approx C_2 = 30\ pF$

$X_{C_2} = 200\ \Omega$ *(capacitive reactance at resonance frequency, i.e., 25 MHz)*

$V_{CC} = 3.3$ V

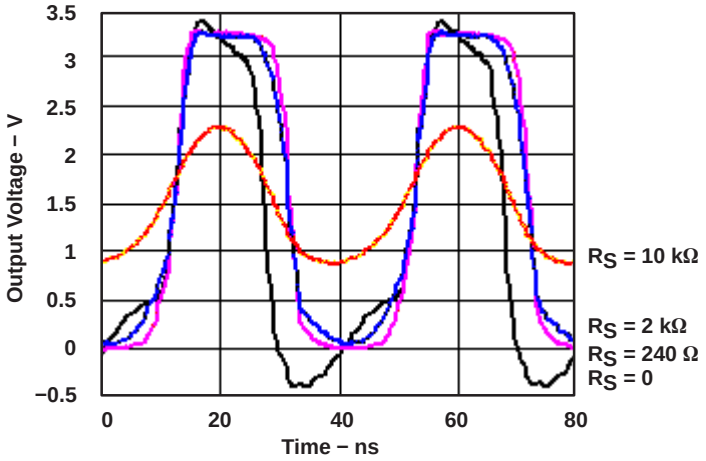

Figure B−1. Effect of R_S on Oscillator Waveform (Frequency = 25 MHz)

Table B−1. Effect of R_S on Duty Cycle and I_{CC} (Frequency = 25 MHz)

R_S (Ω)	I_{CC} (mA)	Positive Duty Cycle (%)
0	22.2	43
240	11.1	45.9
2 k	7.3	47.3
10 k	8.6	46.7

B.2 LVC1GU04 in 10-MHz Crystal-Oscillator Circuit

$C_1 \approx C_2 = 30pF$

X_{C_2} = 480 Ω (capacitive reactance at resonance frequency, i.e., 10 MHz)

V_{CC} = 3.3 V

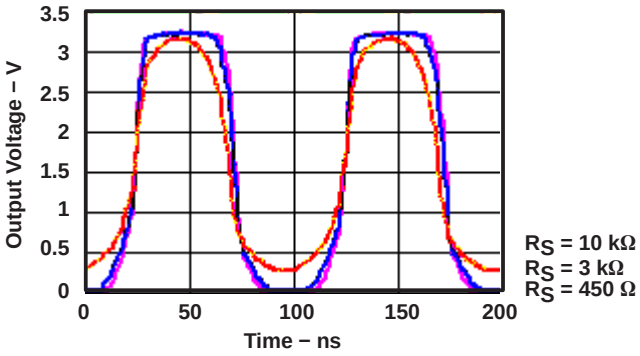

Figure B−2. Effect of R_S on Oscillator Waveform (Frequency = 10 MHz)

Table B−2. Effect of R_S on Duty Cycle and I_{CC} (Frequency = 10 MHz)

R_S (Ω)	I_{CC} (mA)	Positive Duty Cycle (%)
450	6.9	40
3 k	8.4	47.6
10 k	15.1	43.9

B.3 LVC1GU04 in 2-MHz Crystal-Oscillator Circuit

$C_1 \approx C_2 = 30pF$

X_{C_2} = 2.4 kΩ (capacitive reactance at resonance frequency, i.e., 2 MHz)

V_{CC} = 3.3 V

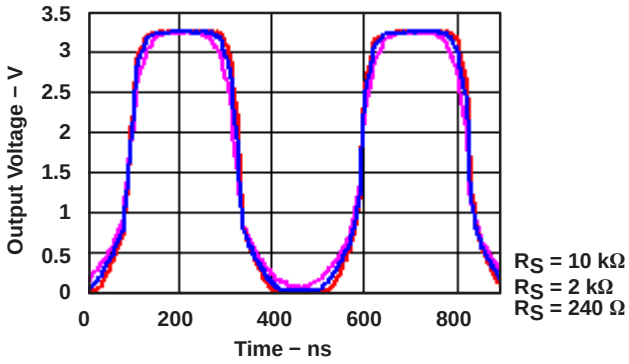

Figure B−3. Effect of R_S on Oscillator Waveform (Frequency = 2 MHz)

Table B−3. Effect of R_S on Duty Cycle and I_{CC} (Frequency = 2 MHz)

R_S (Ω)	I_{CC} (mA)	Positive Duty Cycle (%)
240	11.1	45.9
2 k	7.3	47.3
10 k	8.6	46.7

B.4 LVC1GU04 in 100-kHz Crystal-Oscillator Circuit

$C_1 \approx C_2 = 30pF$

X_{C_2} = 48 kΩ (capacitive reactance at resonance frequency, i.e., 100 kHz)

V_{CC} = 3.3 V

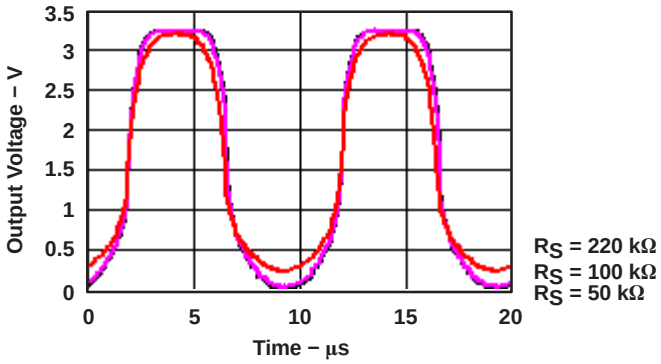

Figure B−4. Effect of R_S on Oscillator Waveform (Frequency = 100 kHz)

Table B−4. Effect of R_S on Duty Cycle and I_{CC} (Frequency = 100 kHz)

R_S (Ω)	I_{CC} (mA)	Positive Duty Cycle (%)
50 k	9	46.4
100 k	9.5	46.1
220 k	13.7	44.3

Appendix C. LVC1404 in Crystal-Oscillator Applications

C.1 LVC1404 in 25-MHz Crystal-Oscillator Circuit

$C_1 \approx C_2 = 30pF$

$R_S = X_{C_2}$ = 200 Ω (capacitive reactance at resonance frequency, i.e., 25 MHz)

V_{CC} = 3.3 V

I_{CC} = 8.6 mA

Duty cycle = 48.1%

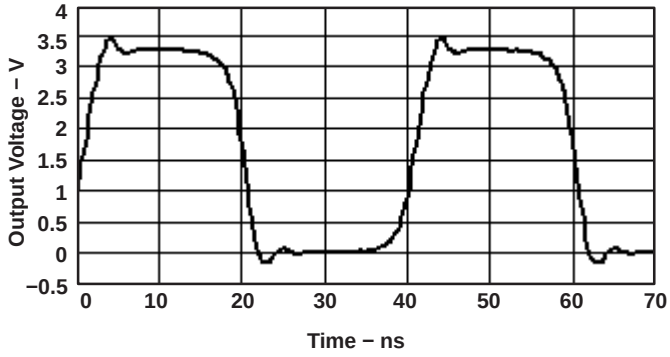

Figure C−1. Output Waveform of Oscillator Circuit Using LVC1404 (Frequency = 25 MHz)

C.2 LVC1404 in 100-kHz Crystal-Oscillator Circuit

$C_1 \approx C_2 = 30pF$

$R_S = X_{C_2}$ = 48 kΩ (capacitive reactance at resonance frequency, i.e., 100 kHz)

V_{CC} = 3.3 V

I_{CC} = 5.7 mA

Duty cycle = 47.4%

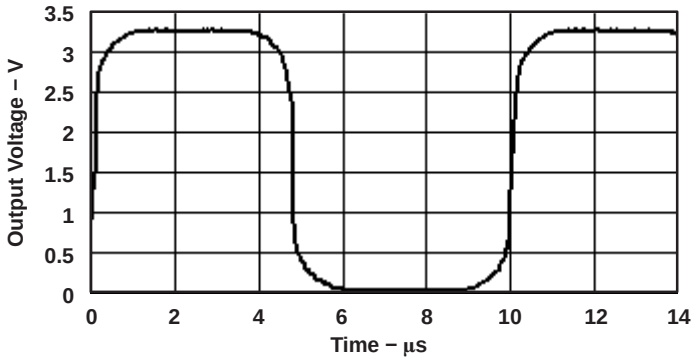

Figure C−2. Output Waveform of Oscillator Circuit Using LVC1404 (Frequency = 100 kHz)

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