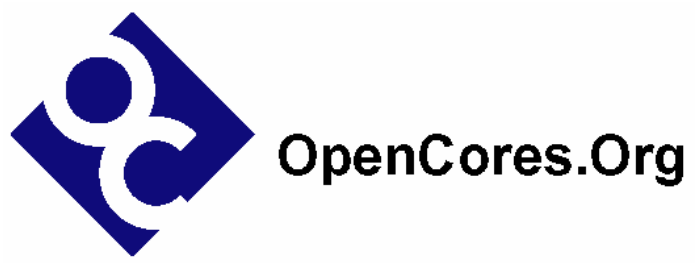

PLBv46 to Wishbone Bridge

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Rev. 0.1

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Revision History

Rev.	Date	Author	Description
0.1	7/30/08	Mark Sasten	First Draft

Contents

1 Introduction

This document provides specifications for the PLBv46™ to Wishbone™ bridge that has been made to work inside Xilinx EDK projects. Many embedded projects require simple interfaces to different bus standards. One very popular bus interface is the Wishbone bus used by many OpenCores.org peripherals. This bridge allows Microblaze and PowerPC applications to utilize many of these open source cores.

Features:

- PLBv46 Slave Attachment (non-bursting)
  - Native 32-bit slave interface to PLBv46 bus.
  - 32-bit master interface to Wishbone bus.
- Directly integrated into EDK tools as a custom pcore.
  - Comes as synthesizable VHDL
  - Microprocessor Peripheral Definition (MPD) file provided.
  - Compiles with PLBv46 subset of IBM CoreConnect™ Bus Standard.
- Supports
  - Handling of retries.
    - User can set the retry wait time.
    - User can set number of times to retry transaction.
    - Result of unsuccessful retry is a PLBv46 bus error ack.
  - Handling of Bus Errors
    - User can set how long to wait for a bus-timeout resulting from no-acknowledgement from a Wishbone transaction.
    - Results in an immediate PLBv46 Bus Error.
    - Will translate Wishbone Bus Errors to PLBv46 bus.

2

Architecture

This section describes the architecture of the block. A block diagram should be included describing the top level of the design.

3

Operation

This section describes the operation of the core. Specific sequences, such as startup sequences, as well as the modes and states of the block should be described.

4

Registers

This section specifies all internal registers. It should completely cover the interface between the core and the host as seen from the software view.

List of Registers

Name	Address	Width	Access	Description

Table 1: List of registers

Register 1 – Description

(You shall choose the style of register you prefer. Do not use both options in one and the same document.)

Bit #	Access	Description

Reset Value:

Reg_Name: 0000h

31	30	29	28	...	8	7	6	5	4	3	2	1	0

Table 2: Description of registers

Reset Value:

Reg_Name: 0000h

5 Clocks

This section specifies all the clocks. All clocks, clock domain passes and the clock relations should be described.

Name	Source	Rates (MHz)			Remarks	Description
		Max	Min	Resolution		
clk_pad_i	Input Pad	10	4	0.1	Duty cycle 70/30.	For external interface.
wb_clk_I	PLL	200	-	-	Must be synchronized to sm_clk_i	System clock.
sm_clk_i	Input port	55	40	1	There are multi-clocks paths.	Clock 55MHz for State machine.

Table 3: List of clocks

6

IO Ports

This section specifies the core IO ports.

Port	Width	Direction	Description
wb_clk_i	1	Input	Block's WISHBONE Clock Input
wb_rst_i	1	Input	Block's WISHBONE Reset Input
wb_sel_i	4	Input	Block's WISHBONE Select Inputs
foo_pad_o	1	Output	Block's foo output to output pad
…			

Table 4: List of IO ports

Appendix A

Name

This section may be added to outline different specifications.

Appendix B

Name

This section may be added to outline different specifications.

Index

This section contains an alphabetical list of helpful document entries with their corresponding page numbers.