Product Code Iterative Decoder

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Contents

List of Figures

1

Introduction

1.1. Product Code

Product code is also known as turbo code, this error correction methods is known to approach the Shannon Limit. This design uses iterative methods on decoding the product codes, see Figure 1-3, this design is based on Mr. Wada-san homepage[1].

This is two dimesional product code iterative decoder, there are four bits information followed by two row parity bits and two column parity bits. Each signal informations is represented in two's complement eight bit data, thus it indicate an integer value of -128 to 127 for each of information bit.

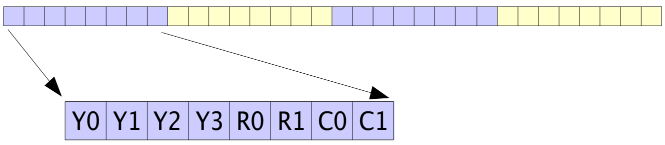
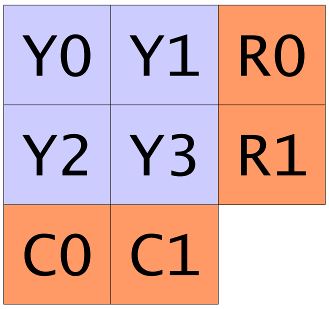


Figure 1-1: Sequence of Product Codes



```
R0 = Y0 xor Y1

R1 = Y2 xor Y3

C0 = Y0 xor Y2
C1 = Y1 xor Y3
```

Figure 1-2: Product Code generations

1.2. Decoding Algorithm

$$posteriori\ value = channel\ value\ (Lch) + priori\ value + external\ value\ (Le) \tag{1-1}$$

$$\left\{ \begin{array}{ll} posteriori = Lch\ +\ priori\ +\ Le\,(row\ parity) & (0) \\ posteriori = Lch\ +\ priori\ +\ Le\,(column\ parity) & (1) \\ .... & \\ .... & \\ posteriori = Lch\ +\ priori\ +\ Le\,(row\ parity) & (n-1) \\ posteriori = Lch\ +\ priori\ +\ Le\,(column\ parity) & (n) \end{array} \right\} \tag{1-2}$$

$$Lch = Y0,\ Y1,\ Y2,\ Y3 \tag{1-3}$$

$$priori = posteriori\ (n-1) \tag{1-4}$$

$$Le = sgn(a\ *\ b)\ *\ min\{abs(a), abs(b)\} \tag{1-5}$$

sgn(a * b) means the sign result of multiplication between operand a and b, and abs(x) means absolute value of operand x. The last value of posteriori is the decoded informations, i.e the posteriori value at nth iterations. The decoded informations can be obtained from the sign of the last posteriori value, positive value is zero and negative value is one, i.e this is the most significant bit of the posteriori value.

1.3. Circuit Schematic

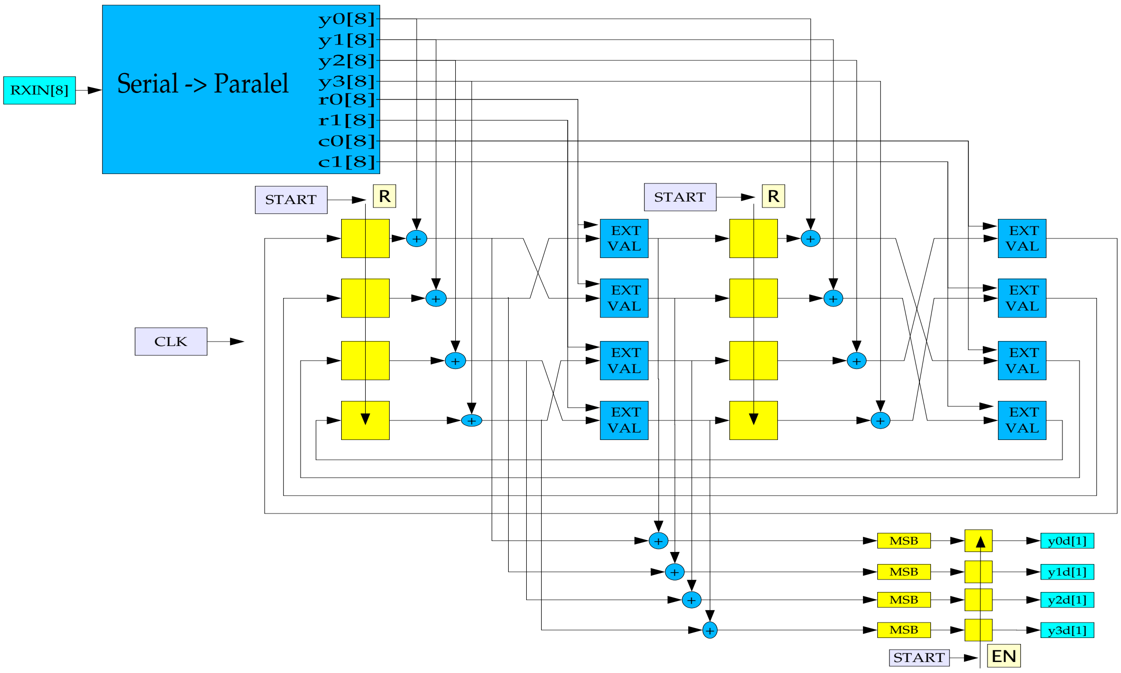


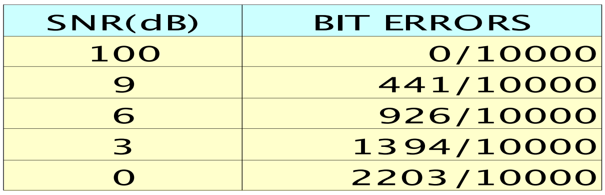
Figure 1-3: Schematic of Product Code Decoder

2

Implementation

2.1. Simulation

This design has been simulated using ModelSim 6.0 SE, here is the summary of bit errors on different signal to noise ratio (SNR) of input signal:



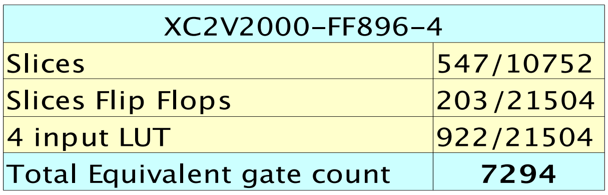
SNR(dB)	BIT ERRORS
100	0/10000
9	441/10000
6	926/10000
3	1394/10000
0	2203/10000

Table 2-1: Bit errors on different SNR

signal with SNR 0 dB is signal with very big noise.

2.2. Synthesize

This design has been synthesized using ISE Xilinx 6.3i, here is the summary of the area utilization in FPGA Xilinx:



XC2V2000–FF896–4	
Slices	547/10752
Slices Flip Flops	203/21504
4 input LUT	922/21504
Total Equivalent gate count	**7294**

Table 2-2: Area utilizations summary

The maximum clock frequency is 64.070 MHz (Minimum period 15.608ns)

Bibliography

[1] Tom Wada, **2-D Product Code Iterative Decoder**,
http://www.ie.u-ryukyu.ac.jp/˜ wada/design06/spec_e.html
October 1st, 2005

A

Informations

A.1. Warranty

NO WARRANTY

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A.2. Tools

- ALLIANCE CAD SYSTEM developed by ASIM team at ©LIP6/Université Pierre et Marie Curie, **http://asim.lip6.fr/recherche/alliance**
  The primary VHDL Analyser for Synthesize
- **ModelSim 6.0** The Simulator
- **Xilinx 6.3i** The Synthesizer

- **VIM** (Vi IMproved) The Editor
- **LaTeX** The Typesetter

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