C16 WISHBONE DATA SHEET

According to RULE 2.15 of WISHBONE SoC Architecture Specification Rev. B.3

Applicable to VHDL module "**cpu_engine.vhd**".

(1) The module **cpu_engine.vhd** was designed against WISHBONE specification **B.3**.

(2) The type of interface is **MASTER**.

(3) The interface supports the following signals:

- **CLK_I**
- **DAT_I()**
- **DAT_O()**
- **RST_I**
- **ACK_I**
- **ADR_O()**
- **CYC_O**
- **STB_O**
- **TGA_O(0)**
- **WE_O**

(4) The optional **ERR_I** signal is not supported.

(5) The optional **RTY_I** signal is not supported.

(6) The tag signal **TGA_O(0)** is used to distinguish 16 bit memory addresses from 8 bit I/O addresses. If **TGA_O(0)** is **'0'** then **ADR_O(15:0)** is valid and the address refers to memory. Otherwise (**TGA_O(0)** is **'1'**) only **ADR_O(7:0)** is valid, and the address refers to an I/O address (the **IN** and **OUT** instructions of the CPU).

(7) The port size is **8 bit**.

(8) The port granularity is **8 bit**.

(9) The maximim operand size is **8 bit**.

(10) The data transfer ordering is **BIG/LITTLE ENDIAN**.

(11) The sequence of data transfer is **UNKNOWN** (what does "sequence of data transfer" mean, anyway?)

(12) There are no known constraints on the clock signal.