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Reed Solomon Decoder

- Reed Solomon Decoder (204,188), with T=8.
- Input codeword length is 204 bytes and output length is 188 bytes.
- Corrects up to 8 byte errors per input codeword.
- Code generator polynomial: (x + λ) (x + λ^2) (x + λ^3) … (x + λ^16).
- Field generator polynomial: x^8+ x^4+ x^3+ x^2+1.

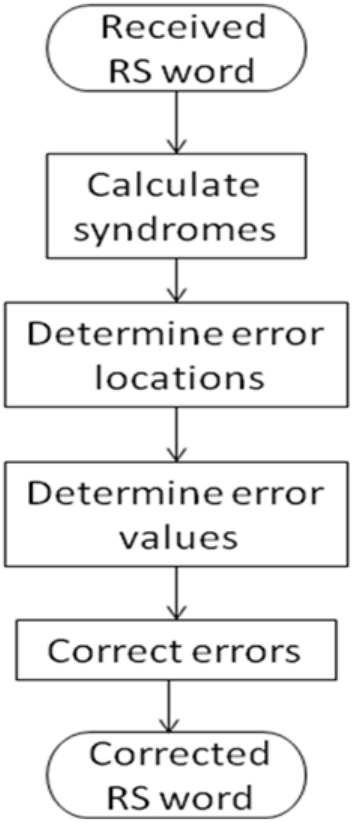

Figure 1 (Functional flow chart)

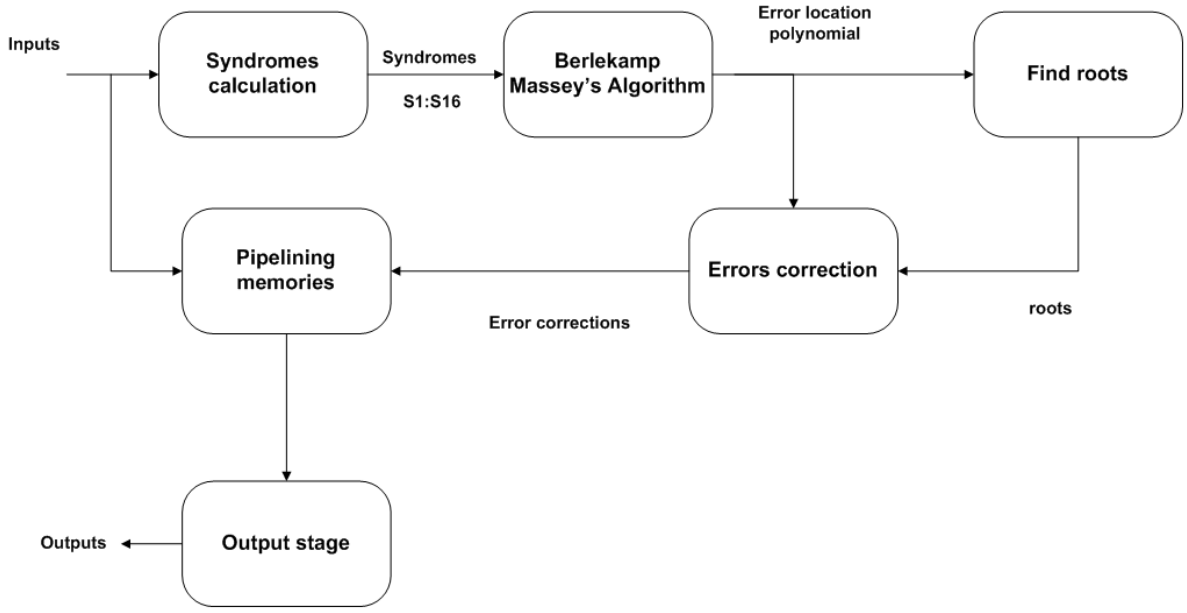

Figure 2 (Block diagram)

- Design estimated Gate count is 52,400 gates and total memory bits are 12,432 bits.
- Synthesis Results on Xilinx Spartan 3A DSP:
  - Number of occupied slices: 3,397/23,872 (14%).
  - Best achievable clock is 12.084 ns.
  - Total block RAMs RAMB16BWERs: 11/126 (8%).
- Synthesis Results on Altera Stratix III L150F1152C2:
  - Logic utilization 5 %.
  - Combinational ALUTs 3,372 / 113,600 (3 %).
  - Memory ALUTs 256 / 56,800 (< 1 %).
  - Dedicated logic registers: 2,935 / 113,600 (3 %).
  - Total block memory bits 12,432 / 5,630,976 (< 1 %).
  - Best achievable clock is 3.977 ns.

- The core is pipelined, and minimum latency between every input byte and the next input byte is 8 clock cycles (see figure 3).

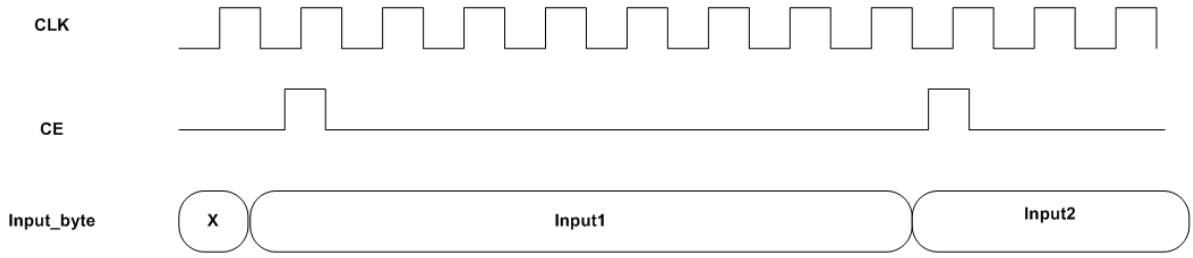

Figure 3 (Input timing diagram)

- Figure 4 is illustrating the output bytes timing, one output byte every 8 clocks.

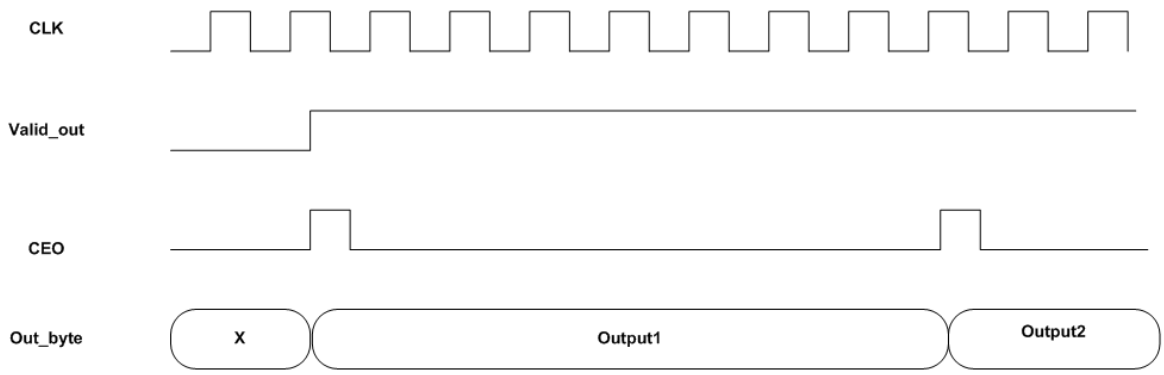

Figure 4 (Output timing diagram)

- This version of the Reed Solomon core is distributed under the GPL license. An optimized and considerably more advanced version, which may be customized on request for different code generator polynomials, is available under a commercial license.
- Deliverables:
    - Verilog RTL files.
    - Simulation test bench.
    - MATLAB script to generate test vectors.