Real-Time Clock IP Core Specification

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Revision History

Rev.	Date	Author	Description
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Introduction

The real-time clock (RTC) IP core implements real-time clock facility together with an alarm function.

Features

The following lists the main features of RTC IP core:

- Programmable divider for 50Hz, 60Hz, 32.768KHz or custom clock
- 24 hour time mode with highest precision of tenth of a second
- Calendar function with correction for leap year
- Programmable alarm with interrupt generation
- Registers contain BCD data
- WISHBONE SoC Interconnection Rev. B compliant interface

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Architecture

Figure 1 below shows general architecture of RTC IP core. It consists of four main building blocks:

- WISHBONE host interface
- RTC registers/circuitry
- Alarm registers/circuitry
- Clock divider and rtcclk input

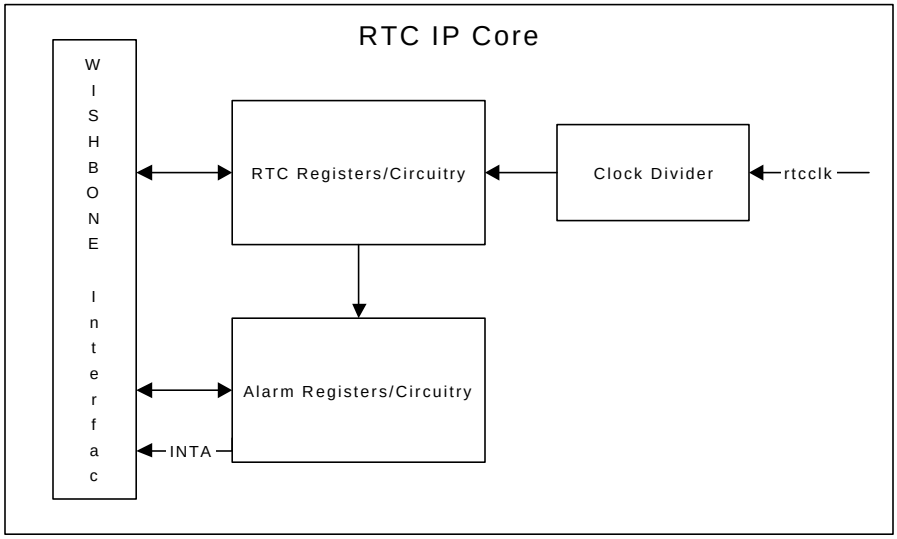

Figure 1. Core's Architecture

Clocks

The RTC core has two clock domains. WISHBONE clock is a reference for synchronous reads and writes to all RTC registers. Input signal rtc_clk is an external real-time clock source.

WISHBONE Interface

WISHBONE slave interface connects RTC core to the host system. It is WISHBONE SoC Interconnection specification Rev. B compliant. The implementation implements a 32-bit bus width and does not support other bus widths.

RTC Registers/Circuitry

The RTC IP Core has several software accessible registers. Some of these registers reflect values of BCD time and date counters. Control register controls the operation of the RTC counters and the divider.

Alarm Registers/Circuitry

The RTC IP Core has several software accessible registers. Some of these registers contain alarm values that set a bit and optionally trigger an alarm interrupt if RTC time or date match the alarm values.
Triggering of an alarm interrupt as well as which alarm values trigger an alarm are programmable in the control register.

Divider and RTC Clock Input

Divider divides real-time clock source frequency down to ten clock periods per second. Real-time clock source can be either rtc_clk input or WISHBONE clock input.

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Operation

This section describes the operation of the RTC core. Almost every aspect of RTC operation is controlled by configuration of the control bits.

Hardware Reset

Reset input asynchronously resets all registers and counters in RTC core. Interrupt request signal is masked and RTC normal operation halted.

Initializing/Changing Time and Date

User has one tenth of a second to initialize/change all the time/date counters after the first write to any of the time/date counters while the RTC is enabled. This guarantees that the tenth of a second counter roll over does not occur and thus potentially roll over other counters.

Reading RTC Registers

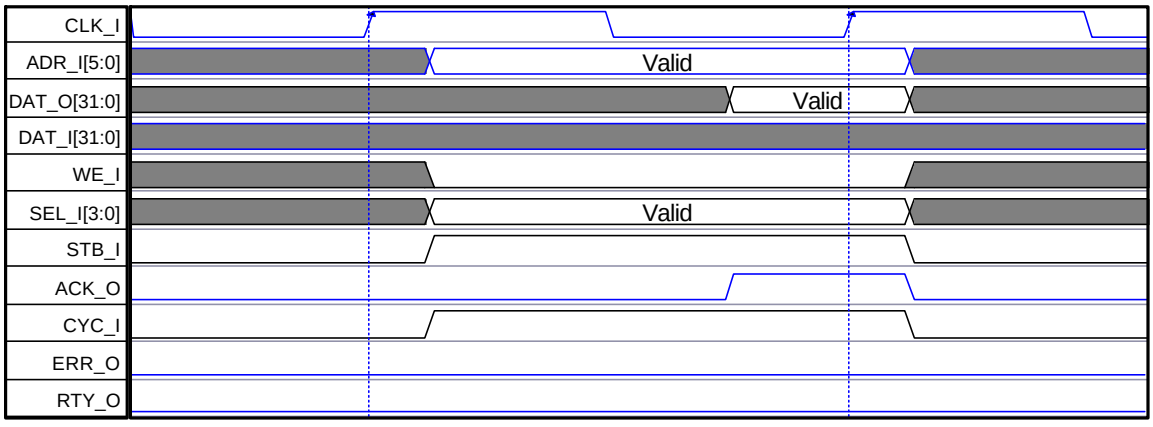

Figure 2. WISHBONE Read Cycle

Figure 2 shows how a WISHBONE read single transfer cycle reads the RTC registers.

Writing RTC Registers

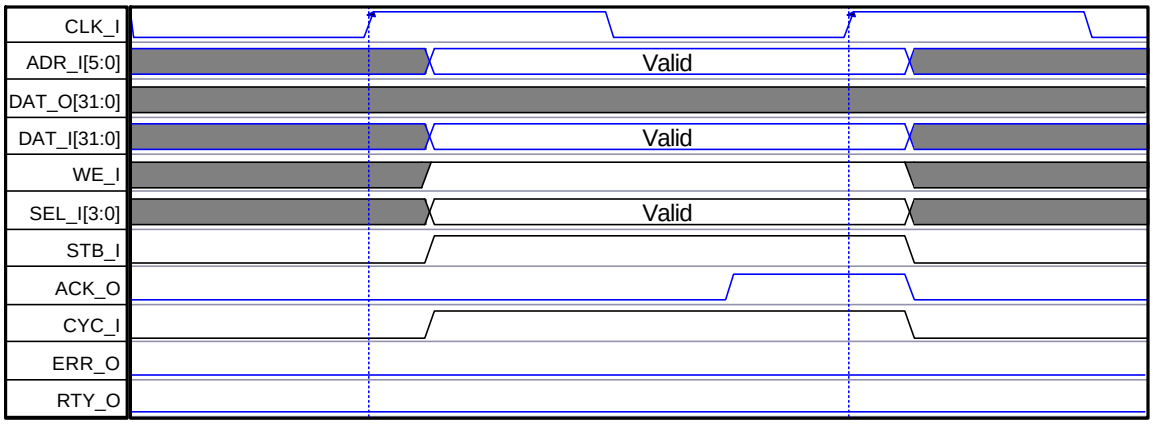

Figure 3. WISHBONE Write Cycle

Figure 3 shows how a WISHBONE write single transfer cycle writes the RTC registers.

Time and Date Counters Operation

Time and date counters count time and date in BCD format. Time counters use 24 hour format and date counters support leap year calculation.

For normal operation time and date counters must be enabled by setting bit RRTC_CTRL[EN]. They operate with a precision of tenth of a second if RRTC_CTRL[BTOS] bit is cleared.
If RRTC_CTRL[BTOS] bit is set, RRTC_TIME[TOS] tenth of a second counter is bypassed and real-time clock clocks the seconds counter.

Real-time clock source can be either rtc_clk input or WISHBONE clock input. When RRTC_CTRL[ECLK] is set, rtc_clk is used as clock source.
Real-time clock is divided by a division factor RRTC_CTRL[DIV]+1. When this value is zero, real-time clock frequency is not divided.

Alarms

An Alarm can be set with any combination of century, year, month, day, day of week, hour, minute, second or tenth of a second. To set an alarm, write the desired values into appropriate alarm registers and enable comparison of desired groups of bits in alarm registers.

When the time and date counters match all enabled alarm groups of bits, RRTC_CTRL[ALRM] bit is set. The software must later clear this bit in order to allow detection of future alarms.

Alarm Interrupt

If RRTC_CTRL[INTE] bit is set, an alarm interrupt is generated once alarm is triggered. Software should clear the RRTC_CTRL[ALRM] bit in order to clear the pending alarm interrupt.

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Registers

This section describes all control and status register inside the RTC core. The *Address* field indicates address in hexadecimal. *Width* specifies the number of bits in the register, and *Access* specifies the valid access types for that register. R/W stands for read and write access and R stands for read only access.

Registers list

Name	Address	Width	Access	Description
RRTC_TIME	Base + 0x0	27	R/W	RTC time register
RRTC_DATE	Base + 0x4	27	R/W	RTC date register
RRTC_TALRM	Base + 0x8	32	R/W	RTC time alarm register
RRTC_DALRM	Base + 0xC	31	R/W	RTC date alarm register
RRTC_CTRL	Base + 0x10	32	R/W	RTC control register

Table 1. List of All Software Accessible Registers

Register RRTC_TIME description

RRTC_TIME register is composed of several BCD counters that measure time. BCD counters represent tenth of a second, seconds, minutes, hours and day of week. Setting any group of bits outside its defined range will result in undefined operations.

Bit #	Access	Reset	Description
3:0	R/W	0x0	TOS Tenth of a second, with valid values from 0 to 9.
7:4	R/W	0x0	S Seconds, with valid values from 0 to 9.
10:8	R/W	0x0	TS Ten seconds, with valid values from 0 to 5.
14:11	R/W	0x0	M Minutes, with valid values from 0 to 9.
17:15	R/W	0x0	TM Ten minutes, with valid values from 0 to 5.
21:18	R/W	0x0	H Hours, with valid values from 0 to 9 except when ten hours is 2.
23:22	R/W	0x0	TH

			Ten hours, with valid values from 0 to 2 when operating in 24 hour mode and 0 to 1 when operating in 12 hour mode.
26:24	R/W	0x0	DOW Day of week, with valid values from 1 (Sunday) to 7 (Saturday).

Table 2. RRTC_TIME Register

Register RRTC_DATE description

RRTC_DATE register is composed of several BCD counters that measure time. BCD counters represent days, months, years and centuries. Setting any group of bits outside its defined range will result in undefined operations.

Bit #	Access	Reset	Description
3:0	R/W	0x0	D Days, with valid values from 0 to 9 except when ten days is 2 or 3.
5:4	R/W	0x0	TD Ten days, with valid values from 0 to 3 except for February.
9:6	R/W	0x0	M Months, with valid values from 0 to 9 except when ten months is 1.
10	R/W	0x0	TM Ten months, with valid values from 0 to 1.
14:11	R/W	0x0	Y Years, with valid values from 0 to 9.
18:15	R/W	0x0	TY Ten years, with valid values from 0 to 9.
22:19	R/W	0x0	C Centuries, with valid values from 0 to 9.
26:23	R/W	0x0	TC Ten centuries, with valid values from 0 to 9.

Table 3. RRTC_DATE Register

Register RRTC_TALRM description

RRTC_TALRM register contains several reference values that are compared to RRTC_TIME register and an alarm can be triggered.

Bit #	Access	Reset	Description
3:0	R/W	0x0	TOS Tenth of a second, with valid values from 0 to 9.
7:4	R/W	0x0	S Seconds, with valid values from 0 to 9.
10:8	R/W	0x0	TS Ten seconds, with valid values from 0 to 5.

14:11	R/W	0x0	M Minutes, with valid values from 0 to 9.
17:15			TM Ten minutes, with valid values from 0 to 5.
21:18	R/W	0x0	H Hours, with valid values from 0 to 9 except when ten hours is 2.
23:22	R/W	0x0	TH Ten hours, with valid values from 0 to 2 when operating in 24 hour mode and 0 to 1 when operating in 12 hour mode.
26:24	R/W	0x0	DOW Day of week, with valid values from 1 (Sunday) to 7 (Saturday).
27	R/W	0	CTOS When set, RRTC_TIME[TOS] is compared to RRTC_TALRM[TOS].
28	R/W	0	CS When set, second is compared to second alarm value.
29	R/W	0	CM When set, minute is compared to minute alarm value.
30	R/W	0	CH When set, hour is compared to hour alarm value.
31	R/W	0	CDOW When set, day of week is compared to day of week alarm value.

Table 4. RRTC_TIME Register

Register RRTC_DALRM description

RRTC_DALRM register contains several reference values that are compared to RRTC_DATE register and an alarm can be triggered.

Bit #	Access	Reset	Description
3:0	R/W	0x0	D Days, with valid values from 0 to 9 except when ten days is 2 or 3.
5:4	R/W	0x0	TD Ten days, with valid values from 0 to 3 except for February.
9:6	R/W	0x0	M Months, with valid values from 0 to 9 except when ten months is 1.
10	R/W	0x0	TM Ten months, with valid values from 0 to 1.
14:11	R/W	0x0	Y Years, with valid values from 0 to 9.
18:15	R/W	0x0	TY Ten years, with valid values from 0 to 9.
22:19	R/W	0x0	C Centuries, with valid values from 0 to 9.

26:23	R/W	0x0	TC Ten centuries, with valid values from 0 to 9.
27	R/W	0	CD When set, day is compared to day alarm value.
28	R/W	0	CM When set, month is compared to month alarm value.
29	R/W	0	CY When set, year is compared to year alarm value.
30	R/W	0	CC When set, century is compared to century alarm value.

Table 5. RRTC_DALRM Register

Register RRTC_CTRL description

Control bits in RRTC_CTRL register control operation of the RTC core.

Bit #	Access	Reset	Description
26:0	R/W	0x0	DIV Divide factor for dividing real-time clock source down to a rate of ten clock periods per second.
27	R/W	0	BTOS When set, tenth of a second counter is bypassed and divided real-time clock should be equal to a rate of a one second.
28	R/W	0	ECLK When set, rtc_clk signal is used as real-time clock source. When cleared, WISHBONE clock is used instead.
29	R/W	0	INTE If this bit is set then the RTC will generate an interrupt when RRTC_CTRL[ALRM] bit is set.
30	R/W	0	ALRM This bit represents alarm status. When it is set, an alarm is pending. The software must write zero to this bit in order to clear it.
31	R/W	0	EN When set, RTC is operating normally. When cleared, RTC operation is halted.

Table 6. RTC Control Register

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IO ports

RTC IP core has two interfaces. Figure 4 below shows both interfaces:

- WISHBONE host interface
- Real-time clock input

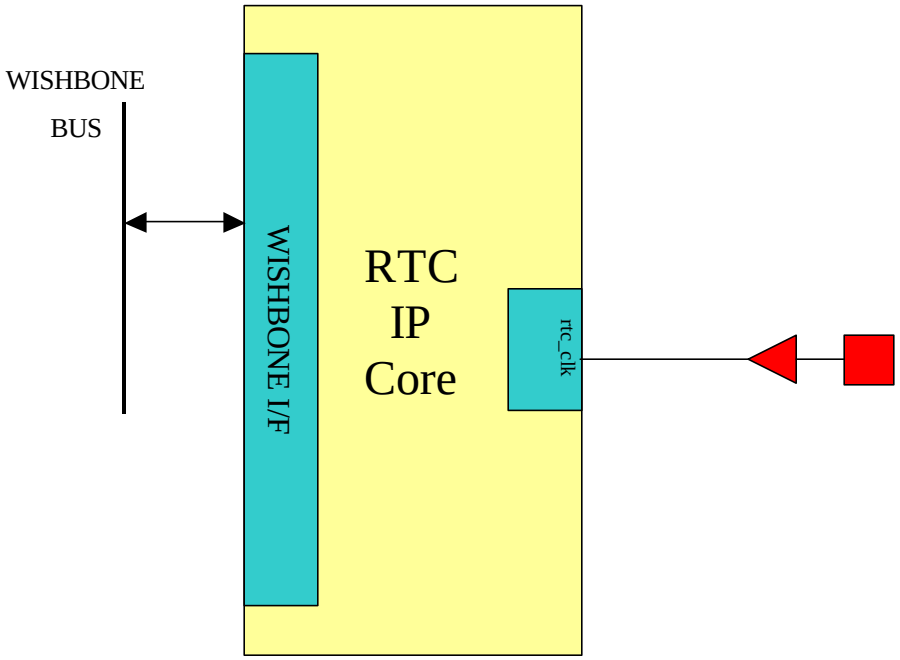

Figure 4. Core's Interfaces

WISHBONE host interface

The host interface is a WISHBONE Rev B compliant interface. RTC IP core works as a slave device only. When it needs the intervention of the local microcontroller, it will assert INTA_O.

Port	Width	Direction	Description
CLK_I	1	Input	Clock input
RST_I	1	Input	Reset input
CYC_I	1	Inputs	Indicates valid bus cycle (core select)
ADR_I	6	Inputs	Address inputs

DAT_I	32	Inputs	Data inputs
DAT_O	32	Outputs	Data outputs
SEL_I	4	Inputs	Indicates valid bytes on data bus (during valid cycle it must be 0xf)
ACK_O	1	Output	Acknowledgment output (indicates normal transaction termination)
ERR_O	1	Output	Not used
RTY_O	1	Output	Not used
WE_I	1	Input	Write transaction when asserted high
STB_I	1	Input	Indicates valid data transfer cycle
INTA_O	1	Output	Interrupt output

Table 7. WISHBONE Interface' Signals

Real-Time Clock Input

Real-time clock input can be connected to an external I/O ring cell and pad. This way the RTC core can be clocked by a clock source completely independent of an internal chip clock.

Port	Width	Direction	Description
rtc_clk	1	Input	Real-time clock input

Table 8. Real-time clock input

A

Core HW Configuration

This section describes parameters that are set by the user of the core and define configuration of the core. Parameters must be set by the user before actual use of the core in simulation or synthesis.

The RTC IP core has no user configurable parameters.