WISHBONE Compatibility Datasheet

The rtfBitmapController5 core may be directly interfaced to a WISHBONE compatible bus.

WISHBONE Datasheet WISHBONE SoC Architecture Specification, Revision B.3		
Description:	Specifications:	
General Description:	Frame Buffer Display / Bitmap controller	
Supported Cycles:	SLAVE, READ / WRITE SLAVE, BLOCK READ / WRITE SLAVE, RMW	
Data port, size: Data port, granularity: Data port, maximum operand size: Data transfer ordering: Data transfer sequencing	64 bit (128/64 or 32 for master) 64 bit (some registers will respect greater granularity) 64 bit Little Endian any (undefined)	
Clock frequency constraints:		
Supported signal list and cross reference to equivalent WISHBONE signals (Slave)	Signal Name: rst_i S_ack_o S_adr_i(11:0) S_clk_i S_dat_i(63:0) S_dat_o(63:0) S_cyc_i	WISHBONE Equiv. RST_I ACK_O ADR_I() CLK_I DAT_I() DAT_O() CYC_I

	S_stb_i S_we_i S_sel_i(7:0)	STB_I WE_I SEL_I
Data port, size: Data port, granularity: Data port, maximum operand size: Data transfer ordering: Data transfer sequencing	Configurable (128/64 or 32 for master) 128/64/ or 32 bit 128/64 or 32 bit Little Endian any (undefined)	
MASTER	Signal Name: rst_i m_ack_i m_adr_o(31:0) m_clk_i m_dat_i(63:0) m_dat_o(63:0) m_cyc_o m_stb_o m_we_o m_sel_o(7:0)	WISHBONE Equiv. RST_I ACK_I ADR_O CLK_I DAT_I DAT_O CYC_O STB_O WE_O SEL_O
Special Requirements:		