rfTextController

Description

This is a text or tile mode video display controller that supports color intended for use with a 64 or 32-bit bus. The controller uses several internal dual ported r/w memories to store text, text attributes and character bitmaps. The display memory is sixty-four bits wide. Up to 8192 different simultaneous characters may be displayed along with 21-bit background and foreground colors (RGB777 format). The use of internal dual ported memories means that the text controller does not consume any memory bandwidth from the processor. The text controller may also be used as a tile graphics controller via the programmable character set.

The controller is programmable using only seven registers. Default values are established that should provide a reasonable display for 800x600 VGA mode.

The core respects byte lane selects, and partial updates of registers are possible. This makes it possible for the core to have an optional 32-bit bus slave interface.

The core has a 256-byte config space. The config space is used to indicate device presence and configure the I/O address the controller responds to.

Address	Description
\$00000 to \$3FFFF	text screen and attribute memory area, currently the controller supports a 256kB memory max, enough for eight 80x50 screens
\$40000 to \$7FEFF	character bitmap memory, only byte addressable (LDB, STB) number of chars depends on char size
\$80000 to \$800FF	Text controller register area

Text and Attribute Memory Layout

63 60	59 58	57 37	36 16	15 13	12 0
Plane$_4$	~	Fore Color$_{21}$	Back Color$_{21}$	~	Char code$_{13}$

Clocks

The text video display controller uses two clocks, a bus timing clock (clk_i) and a video timing clock (dot_clk_i), which can be completely independent.

The core synchronizes the display relative to externally supplied horizontal and vertical synchronization signals.

Register Description

Config Space

A 256-byte config space is supported. Most of the config space is unused. The only configuration is for the I/O address of the register set.

Regno	Width	R/W	Moniker	Description		
000	32	RO	REG_ID	Vendor and device ID		
004	32	R/W				
008	32	RO				
00C	32	R/W				
010	32	R/W	REG_BAR0	Base Address Register		
014	32	R/W	REG_BAR1	Base Address Register		
018	32	R/W	REG_BAR2	Base Address Register		
01C	32	R/W	REG_BAR3	Base Address Register		
020	32	R/W	REG_BAR4	Base Address Register		
024	32	R/W	REG_BAR5	Base Address Register		
028	32	R/W				
02C	32	RO		Subsystem ID		
030	32	R/W		Expansion ROM address		
034	32	RO				
038	32	R/W		Reserved		
03C	32	R/W		Interrupt		
040 to 0FF	32	R/W		Capabilities area		

REG_BAR0 defaults to $EC000001 which is used to specify the address of the controller’s text video ram in the I/O address space. A 256kB region is reserved.
REG_BAR1 defaults to $EC040001 which is used to specify the address of the controller’s character bitmap memory in the I/O address space. A 256kB region is reserved.
REG_BAR2 defaults to $EC080001 which is used to specify the address of the controller’s registers in the I/O address space. A 256B region is reserved.

The controller will respond with a memory size request of 0MB (0xFFFFFFFF) when BAR0, BAR1, or BAR2 is written with all ones. The controller contains its own dedicated memory and does not require memory allocated from the system.

Parameters

CFG_BUS	defaults to zero
CFG_DEVICE	defaults to one
CFG_FUNC	defaults to zero

Config parameters must be set correctly. CFG device and vendors default to zero.

Control Register Description

Reg No.	Bit	R/W		Default Value	
00	7 – 0	RW	Number of character columns	64	
	15 - 8	RW	Number of character row	32	
	19 - 16	RW	Character output delay	7	
	31 – 20	-	These bits are reserved		
	43 – 32	RW	Window left	3956	
	47-44	-	These bits are reserved		
	59-48	RW	Window top	4058	
	63 – 60	-	These bits are reserved		
08	4 – 0	RW	Character height in pixels -1 Height < 33	17	
	7 - 5	-	Reserved	-	
	11 – 8	RW	Pixel size width -1 (dot clocks)	0	
	15 – 12	RW	Pixel size height -1 (scan lines)	0	
	20-16	RW	Character width in pixels -1 Width must be even < 33 and > 5 for proper operation.	11	
	23 – 21	-	Reserved	-	
	24	RW	Reset state (auto resets to zero)	0	
	32	RW	Controller enable	1	
	40	RW	Multi-color mode enable	0	
	52 – 48	RW	Y scroll	0	
	60 – 56	RW	X scroll	0	
	Other	-	reserved	-	
10	30 – 0	RW	Color for transparent color ZRGB 4-9-9-9	511	
	62 – 32	RW	Border color ZRGB 4-9-9-9	FFBF2020h	
18	30 – 0	RW	Tile color 1 (multi-color mode)	0	
	62 - 32	RW	Tile color 2 (multi-color mode)	0	
20	4 – 0	RW	Cursor end	31	
	7 – 5	RW	Blink Control 00 | No blink 01 | No display 10 | 1/16 field rate 11 | 1/32 field rate	7	
	12 - 8	RW	Cursor start	0	
	15 - 14	RW	Cursor image type	0	
	47 - 32	RW	Cursor location in memory	3	
	Other	-	reserved		
28	15 – 0	RW	start address – index into display memory	0	
	Other	-	reserved		
30	15 – 0	RW	Font address in char bitmap memory	0	
	63 -32	RW	“LOCK” or “UNLK” font locking	“LOCK”	
	Other	-	reserved		

Graphics

The core may be used as a low-resolution graphics controller via the programmable character set. The characters can be programmed for block graphics. For instance, each character could be a two-by-two grid of pixels. Sixteen different characters would be required to represent all the different combinations. It is also possible to program characters to a three-by-three grid of pixels using 512 programmable characters to represent every possible combination of on/off pixels. The default resolution is 64x32 or (768x576 pixels).

Graphics and text may be intermixed by allocating part of the programmable character set for a graphic array. For instance, using 256 programmable characters a 128x128 bitmapped display can be created.

Fonts

Multiple fonts can be loaded into the character bitmap memory. The controller supports a 64kB font memory. Which font is selected is determined by the contents of the font address register. The font memory may be locked so that it is not inadvertently changed by an errant program. The number of character glyphs that may be stored depends on the size of characters. An 8x8 glyph will use eight bytes of memory, meaning 8192 different characters can be supported. The default pre-loaded font is 12x18 requiring 36 bytes of memory for each character, therefore only 1820 characters of this size can be supported. Fonts with character glyphs up to 64x64 pixels can be used. Horizontally, glyphs are blocked into a size of 8,16,32,or 64 bits. Vertically, glyphs are a multiple of the horizontal size. A 47x56 glyph must be mapped into a 64x56 array of bytes.
The character width of a font must be an even number between six and thirty-two.

Multi-color Mode

If multi-color mode is enabled, pixels are combined into pairs to select one of four colors, the foreground color, background color, tile color 1 or tile color2. Each character or tile may then display pixels in one of the four colors.

Output Planes

A four-bit output plane number may be supplied as part of the character attributes. The plane number controls the display priority when multiple video display devices are present in the video pipeline. Higher numbered planes will appear in front of lower numbered ones.

Smooth Scrolling

Scrolling the screen in a smooth fashion is supported with the x and y scroll registers which allow the screen to be scrolled pixel by pixel.

Power On Screen Randomizer

The controller features an automatic screen randomizer that causes random characters to be displayed when the controller is reset. Video display memory is loaded with random values. This is a visual aid that the controller is working properly.

Display Input / Output Bus

The controller inputs 40-bit ZRGB data and outputs 40-bit ZRGB video data. ZRGB is RGB data with plane number indicator bits tacked on. Four bits are reserved for the plane number and 12 bits are reserved for each RGB color component.

Core Parameters

The amount of memory used for the controller depends on the number of text cells supported. The default is 8192 cells or 64kB of memory. A maximum of 32768 cells or 256kB of memory is supported. An 80x50 text screen would use 4,000 cells.

Name	Default Value	Description
COLS	64	default number of columns of text
ROWS	32	default number of rows of text
BUSWID	64	Slave bus width may be 64 or 32
TEXT_CELL_COUNT	8192	Number of supported text cells. Power of 2
CFG_BUS	8	config bus number (default 0)
CFG_DEVICE	5	config device number (default 1)
CFG_FUNC	3	config function number (default 0)
CFG_VENDORID	16	Default 0
CFG_DEVICEID	16	Default 0

Module Interface Description

rfTextController

module rfTextController(rst_i, clk_i, cs_i, cyc_i, stb_i, ack_o, wr_i, sel_i, adr_i, dat_i, dat_o, dot_clk_i, hsync_i, vsync_i, blank_i, border_i, zrgb_i, zrgb_o, xonoff_i);

System	Description
rst_i	This signal is normally connected to the system reset signal. It resets the text controller interface forcing it to the reset state.
clk_i	This is usually connected to the system clock and is used as a base timing clock for I/O operations.
Slave Port	
cs_confg_i	circuit select input – active for the PCI config space (256MB)
cs_io_i	circuit select input – active for the IO address space (256MB)
cyc_i	indicates that a valid bus cycle is taking place. The core will not respond to the bus unless this signal is active.
stb_i	This strobe signal also indicates that a valid bus cycle is taking place
ack_o	This signal indicates that the core has processed the bus transaction (it is the logical and of cyc_i and stb_i).

wr_i	This signal is used to signify a write operation to the text controller.
sel_i	These are byte lane selects Either 8 for 64 bit interface or 4 for 32-bit interface.
adr_i	This thirty-two bit address bus is used to address one of text controllers's registers or internal memory. (Registers are described above). Registers respond to the address range $FFD1DFxx
dat_i	This is the 64 or 32 bit data input bus to the text controller.
dat_o	This is the 64 or 32 bit data output bus from the text controller.
Video Ports	
dot_clk_i	This input is the video clock input. Pixel timing is derived from it.
hsync_i	Horizontal sync. This input signal signals the start/end of a video scanline (end-of-line)
vsync_i	Vertical sync. This input signal indicates the end of the video frame.
blank_i	This input signal indicates that the display should be blanked. It is active during the video blanking period.
border_i	This input signal indicates that a border area is active.
zrgb_i	This 40-bit input bus can be connected to an external RGB input. (The text controller may display on top of the external input).
zrgb_o	This output signal bus contains the 40-bit RGB display data.

WISHBONE Compatibility Datasheet

The text controller core may be directly interfaced to a WISHBONE compatible bus.

WISHBONE Datasheet WISHBONE SoC Architecture Specification, Revision B.3		
Description:	Specifications:	
General Description:	rfTextController - Text mode video display controller	
Supported Cycles:	SLAVE, READ / WRITE SLAVE, BLOCK READ / WRITE SLAVE, RMW	
Data port, size: Data port, granularity: Data port, maximum operand size: Data transfer ordering: Data transfer sequencing	64 or 32 bit (configurable) 8 bit byte lane selects 64 or 32 bit Little Endian any (undefined)	
Clock frequency constraints:	None, uses separate independent slave bus and video clocks.	
Supported signal list and cross reference to equivalent WISHBONE signals	Signal Name:	WISHBONE Equiv.
	ack_o	ACK_O
	sel_i(7:0)	SEL_I()
	adr_i(16:0)	ADR_I()
	clk_i	CLK_I
	dat_i(63:0)	DAT_I()
	dat_o(63:0)	DAT_O()
	cyc_i	CYC_I
	stb_i	STB_I
	wr_i	WE_I
	rst_i	RST_I
Special Requirements:	external sync generator	