Process Properties - HDL Options

Category

- Synthesis Options
- HDL Options
- Xilinx Specific Options

Properties are not editable while a process is running

| Switch Name | Property Name | Value |
|---|---|---|
| -fsm_extract, -fsm_encoding | FSM Encoding Algorithm | Auto |
| -safe_implementation | Safe Implementation | No |
| -vldcase | Case Implementation Style | None |
| -fsm_style | FSM Style | LUT |
| -ram_extract | RAM Extraction | ☑ |
| -ram_style | RAM Style | Auto |
| -rom_extract | ROM Extraction | ☑ |
| -rom_style | ROM Style | Auto |
| -auto_bram_packing | Automatic BRAM Packing | ☑ |
| -shreg_extract | Shift Register Extraction | ☑ |
| -shreg_min_size | Shift Register Minimum Size | 2 |
| -resource_sharing | Resource Sharing | ☑ |
| -use_dsp48 | Use DSP Block | Auto |
| -async_to_sync | Asynchronous To Synchronous | ☐ |

Property display level: Advanced ☑ Display switch names Default

OK Cancel Apply Help