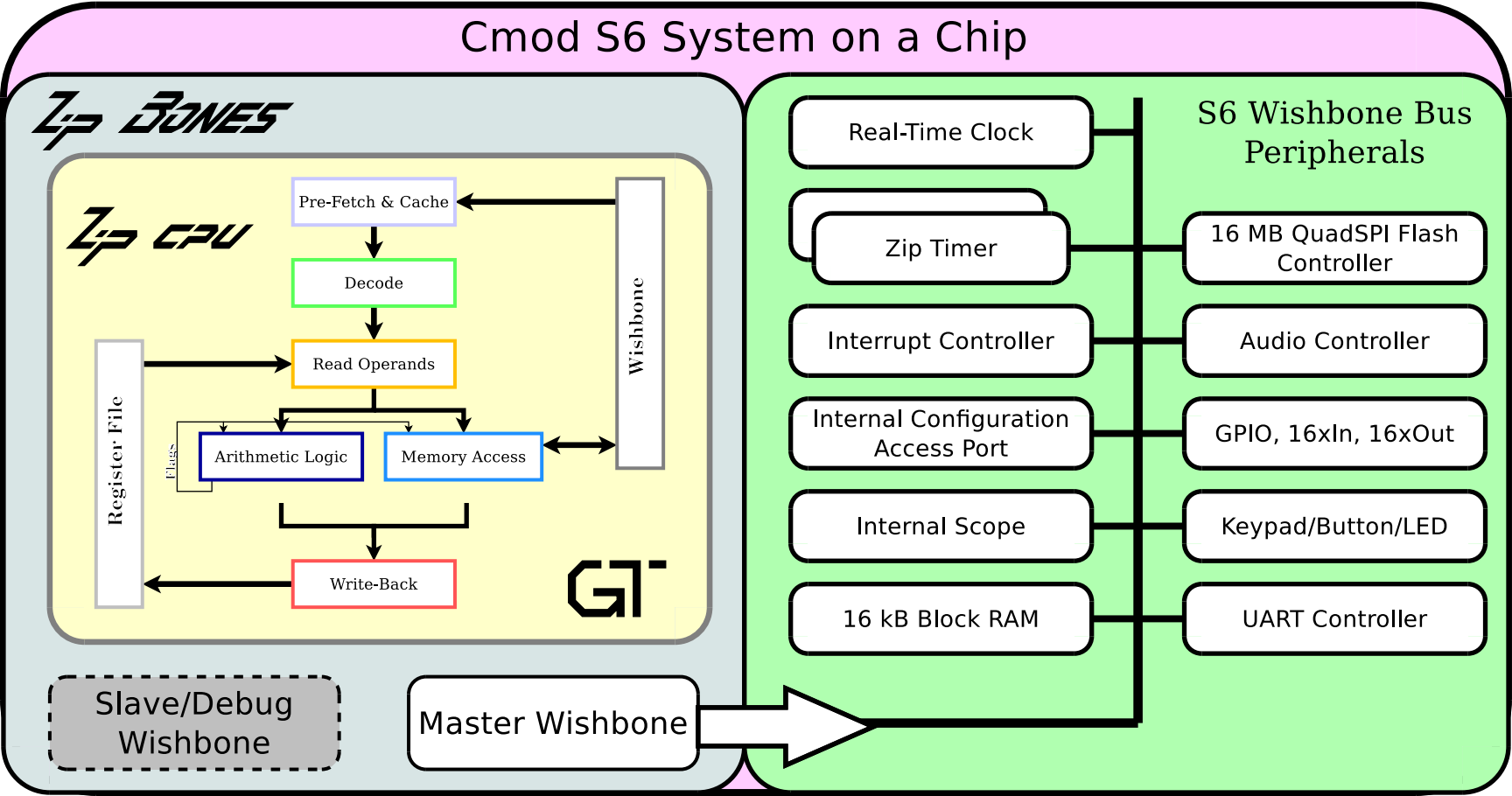
Cmod S6 System on a Chip
Zip Bones
Zip CPU
Pre-Fetch & Cache
Decode
Read Operands
Arithmetic Logic
Memory Access
Write-Back
Register File
Flags
Wishbone
GT
Slave/Debug Wishbone
Master Wishbone
S6 Wishbone Bus Peripherals
Real-Time Clock
Zip Timer
Interrupt Controller
Internal Configuration Access Port
Internal Scope
16 kB Block RAM
16 MB QuadSPI Flash Controller
Audio Controller
GPIO, 16xIn, 16xOut
Keypad/Button/LED
UART Controller