Process Properties - Xilinx Specific Options

Category

- Synthesis Options
- HDL Options
- Xilinx Specific Options

| Switch Name | Property Name | Value |
|---|---|---|
| -iobuf | Add I/O Buffers | ☑ |
| -max_fanout | Max Fanout | 100000 |
| -bufg | Number of Clock Buffers | 16 |
| -register_duplication | Register Duplication | ☑ |
| -equivalent_register_removal | Equivalent Register Removal | ☑ |
| -register_balancing | Register Balancing | No |
| -move_first_stage | Move First Flip-Flop Stage | ☑ |
| -move_last_stage | Move Last Flip-Flop Stage | ☑ |
| -iob | Pack I/O Registers into IOBs | Yes |
| -lc | LUT Combining | Area |
| -reduce_control_sets | Reduce Control Sets | Auto |
| -use_clock_enable | Use Clock Enable | Auto |
| -use_sync_set | Use Synchronous Set | Auto |
| -use_sync_reset | Use Synchronous Reset | Auto |
| -optimize_primitives | Optimize Instantiated Primitives | ☐ |

Property display level: Advanced ☑ Display switch names Default

OK Cancel Apply Help