Process Properties - Synthesis Options

Category

- Synthesis Options
- HDL Options
- Xilinx Specific Options

Switch Name	Property Name	Value
-opt_mode	Optimization Goal	Area
-opt_level	Optimization Effort	Normal
-power	Power Reduction	☐
-iuc	Use Synthesis Constraints File	☐
-uc	Synthesis Constraints File	
-keep_hierarchy	Keep Hierarchy	No
-netlist_hierarchy	Netlist Hierarchy	As Optimized
-glob_opt	Global Optimization Goal	AllClockNets
-rtlview	Generate RTL Schematic	Yes
-read_cores	Read Cores	☑
-sd	Cores Search Directories	+
-write_timing_constraints	Write Timing Constraints	☐
-cross_clock_analysis	Cross Clock Analysis	☐
-hierarchy_separator	Hierarchy Separator	/
-bus_delimiter	Bus Delimiter	<>
-slice_utilization_ratio	LUT-FF Pairs Utilization Ratio	100
-bram_utilization_ratio	BRAM Utilization Ratio	100
-dsp_utilization_ratio	DSP Utilization Ratio	100
-case	Case	Maintain
	Work Directory	[redacted]
set -xsthdpini	HDL INI File	
	Library for Verilog Sources	
-lso	Library Search Order	
-vlgincdir	Verilog Include Directories	+

Property display level: Advanced ☑ Display switch names Default

OK Cancel Apply Help