SATA PHY Design Manual

BeanDigital

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Revision History

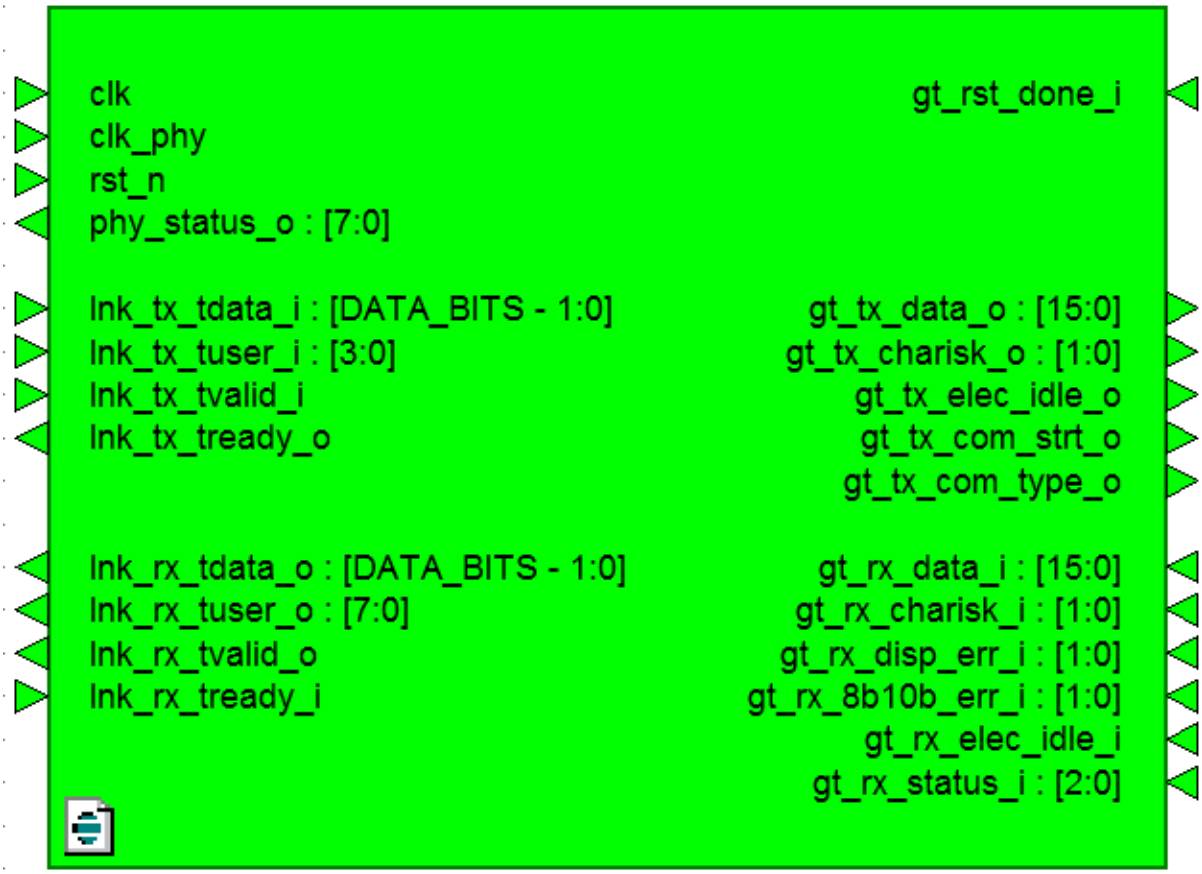
Date	Version	Revision
11/07/12	1.0	Initial release

1 Contents

2 Introduction

This design implements the PHY layer of the SATA standard, which can be implemented as a host or device. The PHY must be connected to an external transceiver which performs the necessary serialisation/deserialization and encoding/decoding of the data. The transmit and receive interfaces are implemented using the AXI-Stream protocol. These should be connected to a compliant SATA link layer which will perform the necessary functions outlined in the standard.

3 Block Diagram



4 Interface

Name	Direction	Description
clk	Input	Clock: SATA clock.
clk_phy	Input	Clock PHY: PHY clock.
rst_n	Input	Reset: Active low reset.
phy_status_o[7:0]	Output	PHY Status: Indicates the status of the PHY. [0] = Link up. [7:1] = Unused
lnk_tx_tdata_i[31:0]	Input	Link Layer Transmit Data: Transmit data received from the link layer.
lnk_tx_tuser_i[3:0]	Input	Link Layer Transmit User Data: Used to indicate if a primitive is being transmitted. [3:0] = 0001 - Primitive [3:0] = 0000 – Data
lnk_tx_tvalid_i	Input	Link Layer Transmit Source Ready: Indicates that valid data is available on the data input.
lnk_tx_tready_o	Output	Link Layer Transmit Destination Ready: Indicates that the PHY layer is ready to accept data from the link layer.
lnk_rx_tdata_o[31:0]	Output	Link Layer Receive Data: Received data sent to the link layer.
lnk_rx_tuser_o[3:0]	Output	Link Layer Receive User Data: Used to indicate if a primitive is being received. [3:0] = 0001 - Primitive [3:0] = 0000 - Data
lnk_rx_tvalid_o	Output	Link Layer Receive Source Ready: Indicates that valid data is available on the data output.
lnk_rx_tready_i	Input	Link Layer Receive Destination Ready: Indicates that the link layer is ready to accept data from the PHY layer.
gt_rst_done_i	Input	GT Reset Done: The reset sequence has completed.
gt_tx_data_o[15:0]	Output	GT Transmit Data: Data to transmit.
gt_tx_charisk_o[1:0]	Output	GT Transmit K/D: Indicates if the data byte is to be transmitted as a K character.
gt_tx_elec_idle_o	Output	GT Transmit Electrical Idle: Used to put the transmitter into an idle state.
gt_tx_com_strt_o	Output	GT Transmit COM Start: Starts a COM sequence.
gt_tx_com_type_o	Output	GT Transmit COM Type: Sets the type of COM to transmit. [0] = COMRESET/COMINIT [1] = COMWAKE

gt_rx_data_i[15:0]	Input	GT Receive Data: Data received.
gt_rx_charisk_i[1:0]	Input	GT Receive K/D: Indicates if the received data byte is a K character.
gt_rx_disp_err_i[1:0]	Input	GT Receive Disparity Error. Indicates that the data byte has a disparity error.
gt_rx_8b10b_err_i[1:0]	Input	GT Receive 8b10b Error: Indicates that the data byte has a 8b10b decode error.
gt_rx_elec_idle_i	Input	GT Receive Electrical Idle: Indicates the receiver is in an idle state.
gt_rx_status_i[2:0]	Input	GT Receive Status: [0] = Transmission of COM complete. [1] = COMWAKE received. [2] = COMRESET/COMINIT received.

5 Parameters

Name	Description
DATA_BITS	32
IS_HOST	0 = PHY behaves as a device. 1 = PHY behaves as a host.
SATA_REV	1 = SATA Rev 1 2 = SATA Rev 2 3 = SATA Rev 3

6 Clocking

6.1 SATA Revision 1

clk	37.5 MHz
clk_phy	75 MHz

6.2 SATA Revision 2

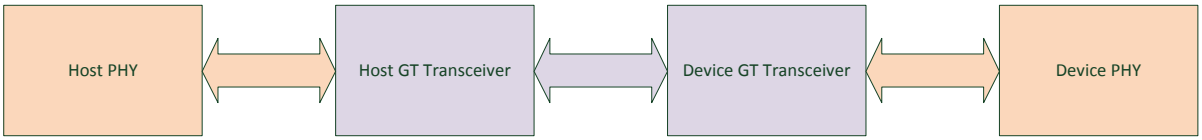
clk	75 MHz
clk_phy	150 MHz

6.3 SATA Revision 3

clk	150 MHz
clk_phy	300 MHz

7 Test Bench

The test bench instantiates a host and device PHY along with a transceiver for each and connects them together. When running a simulation the PHY status signal can be monitored for the host and device PHY. Once the link has been established the link up signal will be asserted and the SYNC primitive will be continuously transmitted.



8 Contact

Any problems I can be contacted at the email address below.

Jon Bean (jbean@beandigital.co.uk)

I have also implemented a SATA host controller with AXI bus. A reference design is available which interfaces the controller to a Xilinx Microblaze processor and AXI DMA.