SGMII Core

SGMII

This document describes interfaces and design of SGMII Core

[Pick the date]

1. Overview

This core implements Physical Coding Sublayer of 1000BaseX transmission (IEEE 802.3 Clause36 and 37). This core can also be used for SGMII interface as this interface leverages 1000BaseX PCS. The differences between the 2 protocols are Link-timer and the control information exchanged during Auto-negotiation process .

2. Interface

Tranceiver Interface		
input i_SerRx, output o_SerTx, input i_CalClk, input i_RefClk125M, input i_ARstHardware_L,		This interface requires 125MHz reference clock and 50MHz Calibration Clock to feed to Transceiver. o_SerTx and i_SerRx are Transmit and Receive line of the transceiver. i_ArstHardware_L is to be connected to hardware reset line.
Local BUS interface Wishbonebus, single transaction mode (non-pipeline slave)		
input i_Cyc, input i_Stb, input i_WEn, input [31:00] i32_WrData, input [07:00] iv_Addr, output [31:00] o32_RdData, output o_Ack,		This wishbone interface is to configures registers such as mode, link-timer or speed …
input i_Mdc, inout io_Mdio,		Mdio clause 22 interface, not supported yet
Link Status		
output o_Linkup, output o_ANDone, output [1:0] o2_SGMIISpeed, output o_SGMIIDuplex,		Link-up is asserted after the synchronization is acquired. AN_Done is asserted after auto-negotiation process is done. SGMIISpeed encodes speed of SGMII mode: 10b: 1000Mbps 01b: 100Mbps 00b: 10Mbps (not supported) SGMIIDuplex, this core only support full duplex mode.
GMII Interface		
input [07:00] i8_TxD, input i_TxEN, input i_TxER, output [07:00] o8_RxD, output o_RxDV, output o_RxER, output o_GMIIClk, output o_MIIClk, output o_Col, output o_Crs		Standard GMII interface GMIIClk output 125MHz clock output by the tranceiver. MIIClk output 25MHz clock used in 100Mbps mode.

2.1. Registers

The registers in the cores are accessed through 32-bit bus. Therefore registers are mapped into Double-word address although each register is only 16-bit. The 16 most significant bits are always zeros.

Bit	Name	Offset	Default	Description
	Control Registers	0x00		
5:0	Reserved	R/W	5'b0	Not used
6	MSB Speed Selection	R/W	0	From Table 22-7 (IEEE 802.3-2008-Section2) 0.6 0.13 1 1 = Reserved 1 0 = 1000 Mb/s 0 1 = 100 Mb/s 0 0 = 10 Mb/s This bit is used only inSGMII mode. The speed of SGMII mode can be configured to use these 2 bits or use link partner advertised speed and duplex.
7	Collision Test	R/W	1'b0	Not support
8	Duplex Mode	R/W		Only full duplex mode is supported, this bit has no effect
9	Auto-nego Restart	R/W SC	1'b0	Restart autonegotiation process. This bit is self cleared.
10	Isolate	R/W	1'b0	Not supported
11	PowerDown	R/W	1'b0	To power down the tranceiver, this bit goes directly to powerdown pin of transceiver. Use with care. This feature has not been tested yet.
12	ANEnable	R/W	1'b0	Enable auto negotiation
13	LSB Speed Selection	R/W	1'b0	LSB of bit selection
14	Loopback	R/W	1'b0	Enable/Disable Loopback mode (not tested)
15	Reset	R/W/SC	1'b0	Write '1' to Soft-Reset the whole module
31:16	Reserved	RO		Zeros

Bit	Name	Offset	Default	Description
	Status Register	0x04		
1:0		RO	2'b00	
2	Sync Status	RO	1'b0	Status of Synchronization process 1: Synchronization has been done. 0: Rx can't sync to the incoming bit stream
4:3		RO	2'b00	2'b01
5	AN complete	RO	1'b0	Autonegotiation is done
31:6		RO	26'h0	Zeros

<table>
<tr><th>Bit</th><th>Name</th><th>Offset</th><th>Default</th><th>Description</th></tr>
<tr><td></td><td>Local Advertised Ability</td><td>0x10</td><td></td><td>This register sets the advertised capability of local link. Some bits are used in 1000BaseX, some are used in SGMII Mode, some are used in both.</td></tr>
<tr><td></td><td></td><td></td><td></td><td>1000BaseX mode</td></tr>
<tr><td>4:0</td><td></td><td></td><td></td><td></td></tr>
<tr><td>6:5</td><td></td><td></td><td></td><td>Only supports Full Duplex mode</td></tr>
<tr><td>7</td><td></td><td></td><td></td><td>Pause</td></tr>
<tr><td>8</td><td></td><td></td><td></td><td>Asymetric dir
Table 37–2—Pause encoding
<table><tr><th>PAUSE (D7)</th><th>ASM_DIR(D8)</th><th>Capability</th></tr><tr><td>0</td><td>0</td><td>No PAUSE</td></tr><tr><td>0</td><td>1</td><td>Asymmetric PAUSE toward link partner</td></tr><tr><td>1</td><td>0</td><td>Symmetric PAUSE</td></tr><tr><td>1</td><td>1</td><td>Both Symmetric PAUSE and Asymmetric PAUSE toward local device</td></tr></table></td></tr>
<tr><td>11:10</td><td>SGMII Speed</td><td></td><td></td><td>Speed select in SGMII mode
Encoding:
10: 1000Mbps
01: 100Mbps
00: 10Mbps</td></tr>
<tr><td>12</td><td>SGMII Duplex/ Remote Fault 1</td><td></td><td></td><td>1000BaseX mode: Remote fault bit 1
SGMII Mode: Duplex mode</td></tr>
<tr><td>13</td><td>Remote Fault 2</td><td></td><td></td><td>Table 37–3—Remote Fault encoding
<table><tr><th>RF1</th><th>RF2</th><th>Description</th></tr><tr><td>0</td><td>0</td><td>No error, link OK (default)</td></tr><tr><td>0</td><td>1</td><td>Offline</td></tr><tr><td>1</td><td>0</td><td>Link_Failure</td></tr><tr><td>1</td><td>1</td><td>Auto-Negotiation_Error</td></tr></table>
Table 37-3 and 37-2 from IEEE 802.3-2008 Section 3.</td></tr>
<tr><td>14</td><td>Ack bit</td><td></td><td></td><td></td></tr>
<tr><td>15</td><td>1’b0</td><td></td><td></td><td></td></tr>
</table>

Link Partner capability					
0x14		Link Partner capability		Capability advertised by Link Partner. The values change with mode of operations	
				1000BaseX mode	SGMII mode
	0	reserved		1'b0	1'b1
	1	reserved		1'b0	1'b0
	2	reserved		1'b0	1'b0
	3	reserved		1'b0	1'b0
	4	reserved		1'b0	1'b0
	5	FD		Full Duplex	1'b0
	6	HD		Half Duplex	1'b0
	7	PS1		Pause	1'b0
	8	PS2		ASM_DIR	1'b0
	9				1'b0
	10	Speed0			Speed Bit 0
	11	Speed1			Speed Bit 1. Encoding: 10: 1000Mbps 01: 100Mbps 00: 10Mbps
	12	RF1		Remote fault 1	1: Full Duplex 0: Half Duplex
	13	RF2		Remote fault 2	
	14	Ack Bit			SGMII Mode, sent from PHY to Mac 1: Link Up 0: Link Down
	15	Link State			
	31:16	Reserved			
0x20	16	Link Timer 1		Least Significant 16-bit of Link Timer	
0x24	16	Link Timer 2		Most Significant 5 bit of Link Timer Together these 2 registers from 21 bit timer which is run by 8-ns clock. Change the value of this register to smaller value during simulation to speed up simulation process.	
0x28	16	Scratch		Scratch register to test	
0x7C	16	Mode			
	0	SGMII		1: SGMII mode 0: 1000BaseX mode The 2 modes differ in autonegotiation process and capability resolution	
	1	Phy		1: Use as in SGMII Phy Side, i.e. transmit the control information. 0: Use as in SGMII Mac Side, i.e receive the control information and send ack bit	
	2	Use Local Config		For SGMII Mode – Mac Side, the speed and duplex by default are set by Link-partner's "advertised" information. If set to "1", the Speed and Duplex are set by control bits 6,13 and 8.	

Architectures

3. Revision History

Date	Author	Core's Revision	Description
	Jeff	1.0	Core is in verification state