IP Core Specification

Universal Pipeline Stage

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Rev. [0.1]

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Revision History

Rev.	Date	Author	Description
0.1	2010/dec/10	Gerhard Hoffmann	Initial version

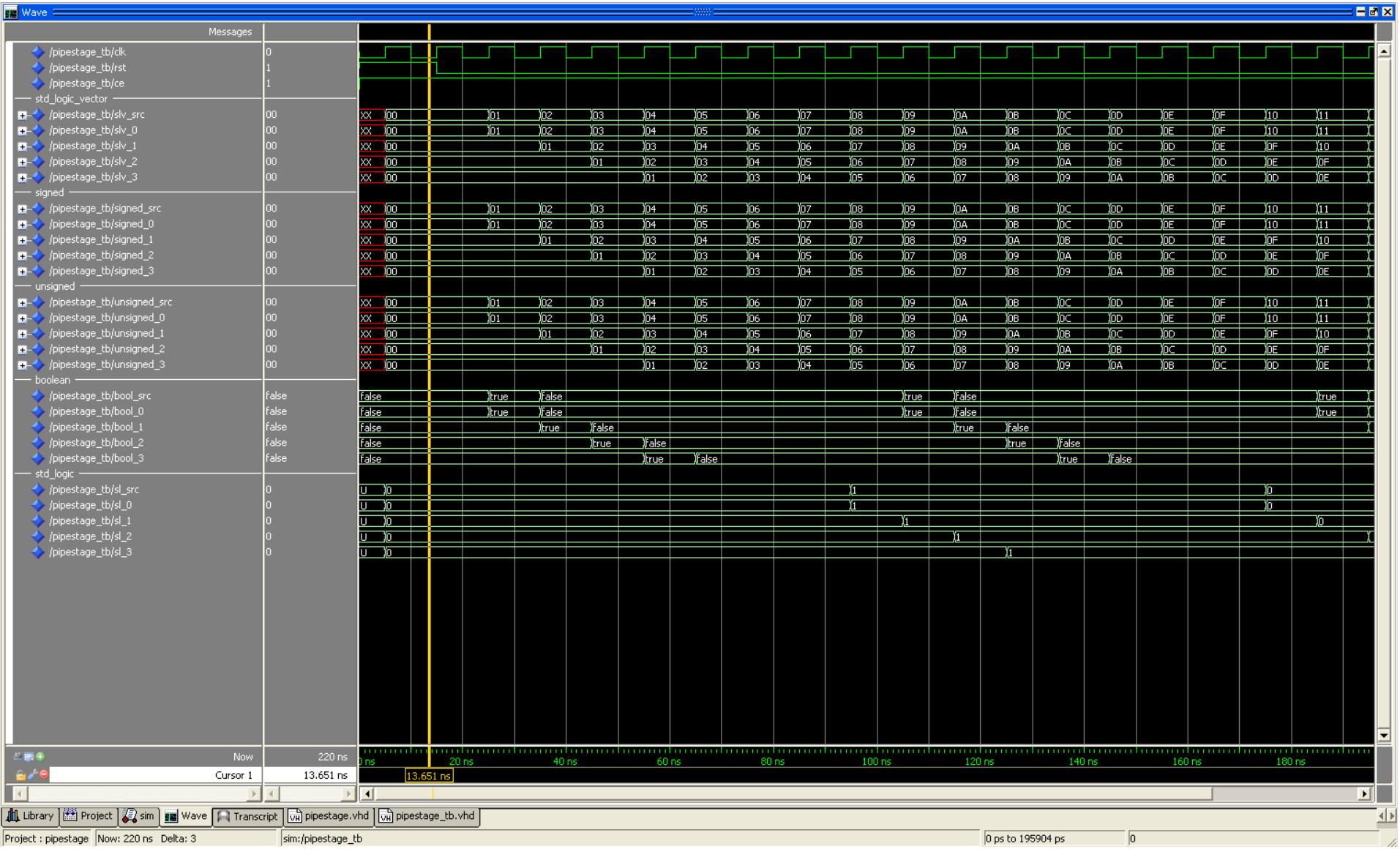
Contents

1. Introduction

This block is a pipeline register with adjustable depth and width. There are flavors for the following types:

For std_logic_vector, signed and unsigned, the width is taken from the buses that are connected during instantiation. Input and output width must be the same.

real	
integer	
boolean	
std_logic	
std_logic_vector	
signed	
unsigned	


Wave
Messages
/pipestage_tb/clk
/pipestage_tb/rst
/pipestage_tb/ce
std_logic_vector
/pipestage_tb/slv_src
/pipestage_tb/slv_0
/pipestage_tb/slv_1
/pipestage_tb/slv_2
/pipestage_tb/slv_3
signed
/pipestage_tb/signed_src
/pipestage_tb/signed_0
/pipestage_tb/signed_1
/pipestage_tb/signed_2
/pipestage_tb/signed_3
unsigned
/pipestage_tb/unsigned_src
/pipestage_tb/unsigned_0
/pipestage_tb/unsigned_1
/pipestage_tb/unsigned_2
/pipestage_tb/unsigned_3
boolean
/pipestage_tb/bool_src
/pipestage_tb/bool_0
/pipestage_tb/bool_1
/pipestage_tb/bool_2
/pipestage_tb/bool_3
std_logic
/pipestage_tb/sl_src
/pipestage_tb/sl_0
/pipestage_tb/sl_1
/pipestage_tb/sl_2
/pipestage_tb/sl_3
Now
220 ns
Cursor 1
13.651 ns
0 ns
20 ns
40 ns
60 ns
80 ns
100 ns
120 ns
140 ns
160 ns
180 ns
Library
Project
sim
Wave
Transcript
pipestage.vhd
pipestage_tb.vhd
Project : pipestage
Now: 220 ns Delta: 3
sim:/pipestage_tb
0 ps to 195904 ps

2.

Registers

3.

IO Ports And Generics

Port	Width	Direction	Description
clk	1	Input	clock input that controls all activities. Rising edge is active.
ce	1	Input	Must be high to qualify a clock edge as active.
rst	4	Input	Synchronous reset. Defaults to '0'. Overrides CE. Forces the internal memories to a known state. This state is: 0.0 for float 0 for integer false for boolean '0' for std_logic / vectors, signed or unsigned If you want this to synthesize to Xilinx SRL16 shift registers, rst cannot be used. In most cases this is not much of a loss because after a few clocks, the output reflects the input history only.
i	variable	Input	Signal to be delayed. If this is a vector, the length is taken from the connected signal.
o	variable	Output	Delayed version of the signal. If this is a vector, the length is taken from the connected signal and its size must be the same as that of the input.
n_stages	0...2G	generic	Amount of delay in clock cycles For 0 clocks delay, the pipeline stage is transparent. Clk, ce and rst are don't cares in this case.

Table 1: List of IO ports

1.

Name

[This section may be added to outline different specifications.]

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