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# Single Clock non-restoring unsigned division algorithm

Methodology and Implementation results

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# Single-clock division algorithm.

Now two division algorithms are wide spread in computing: restoring and non-restoring algorithms. They consider that both algorithms may be used in sequential calculation scheme, when one digit of the result is achieved during one clock. However there are no principle objections against getting all digits of the quotient and the remainder during one clock. So the author tried to develop such kind of algorithm.

Restoring algorithm is seemed to be sequential in nature because during remainder restoring there is positive feedback (A=A – B + B at the same cycle). To avoid the feedback it is necessary to insert register for intermediate result storing.

Thus, non-restoring algorithm was chosen as basic for one-clock division algorithm.

Typical scheme of non-restoring unsigned division algorithm is as follows (see Fig. 1).

For implementation recursive approach was chosen due to it provides compact and transparent description. It is easy to see that synthesis result of the description is sequence of adders.

**Synthesis results.**

Synthesis was done for the following parameters: dividend – 32 bits, divisor – 16 bits, library 0.35u and typical operating conditions. Maximum frequency of the one-clock divider for these parameters is about 14 MHz, hardware resources are about 4,600 gates equivalent, combinational area is 4,200 gates.

**Conclusion**

The frequency is not so high due to algorithm follows traditional idea of sequential calculation of quotient. But it may be enough for some applications. Based on this algorithm signed division algorithms may be developed. The author is about to finish the debugging of this algorithm and will publish it when ready.

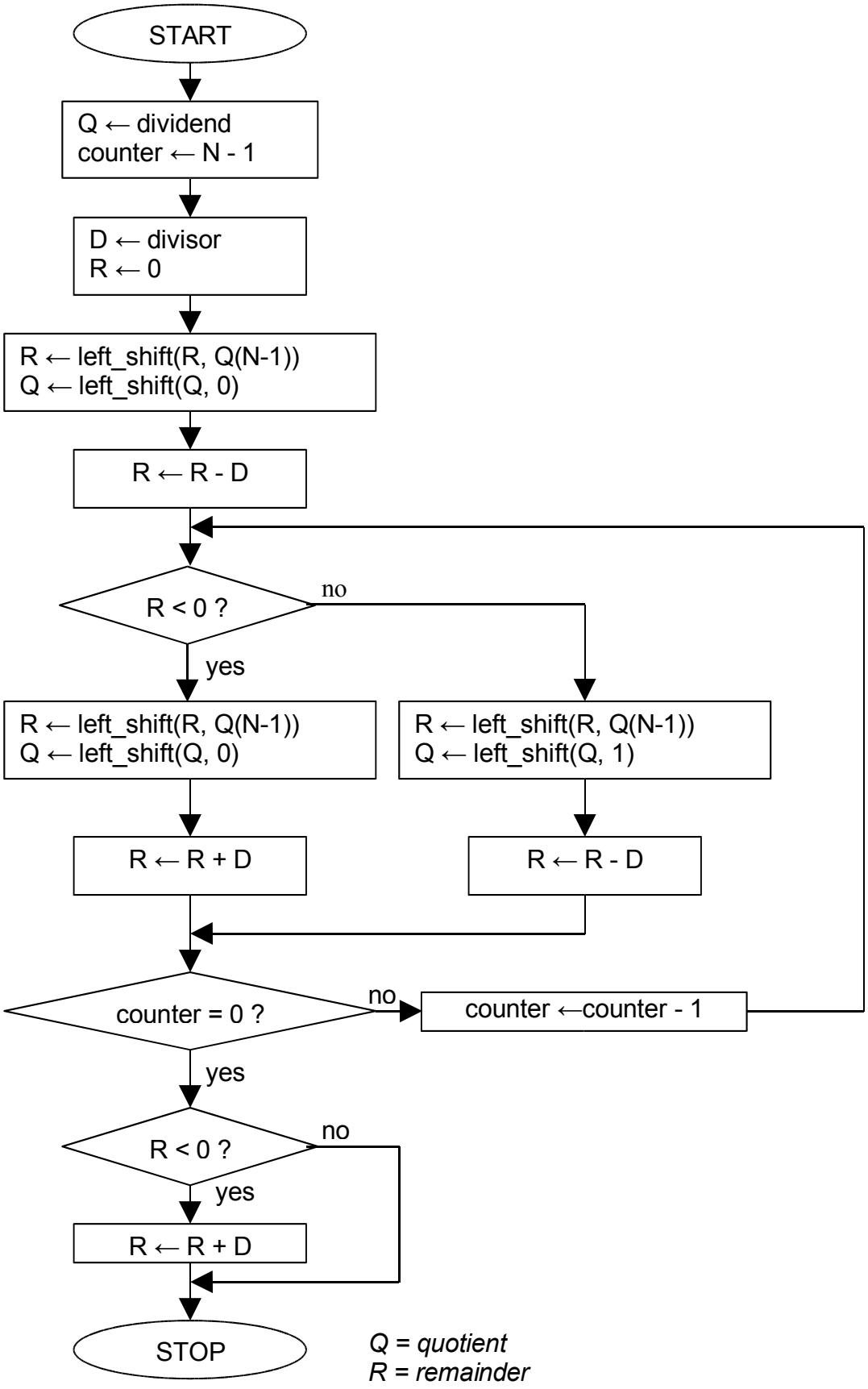


**Fig. 1.** Non-restoring unsigned division algorithm