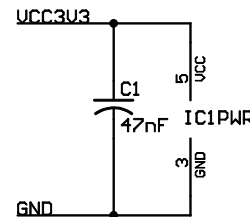
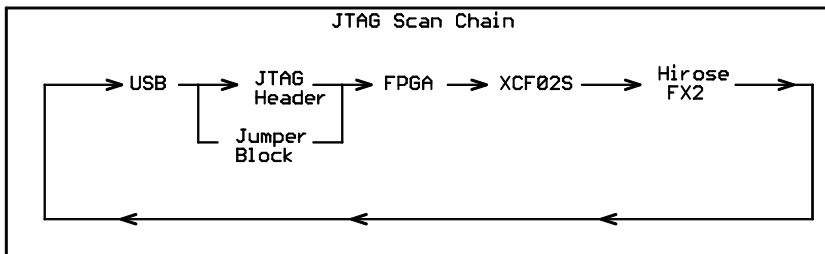
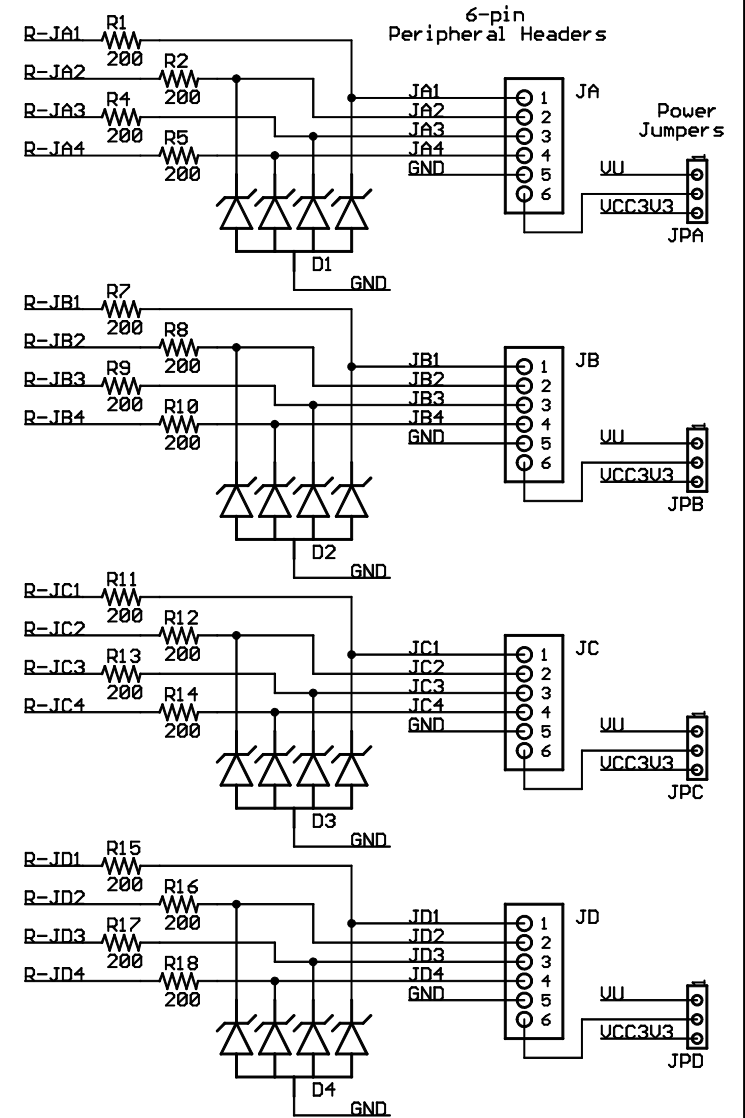
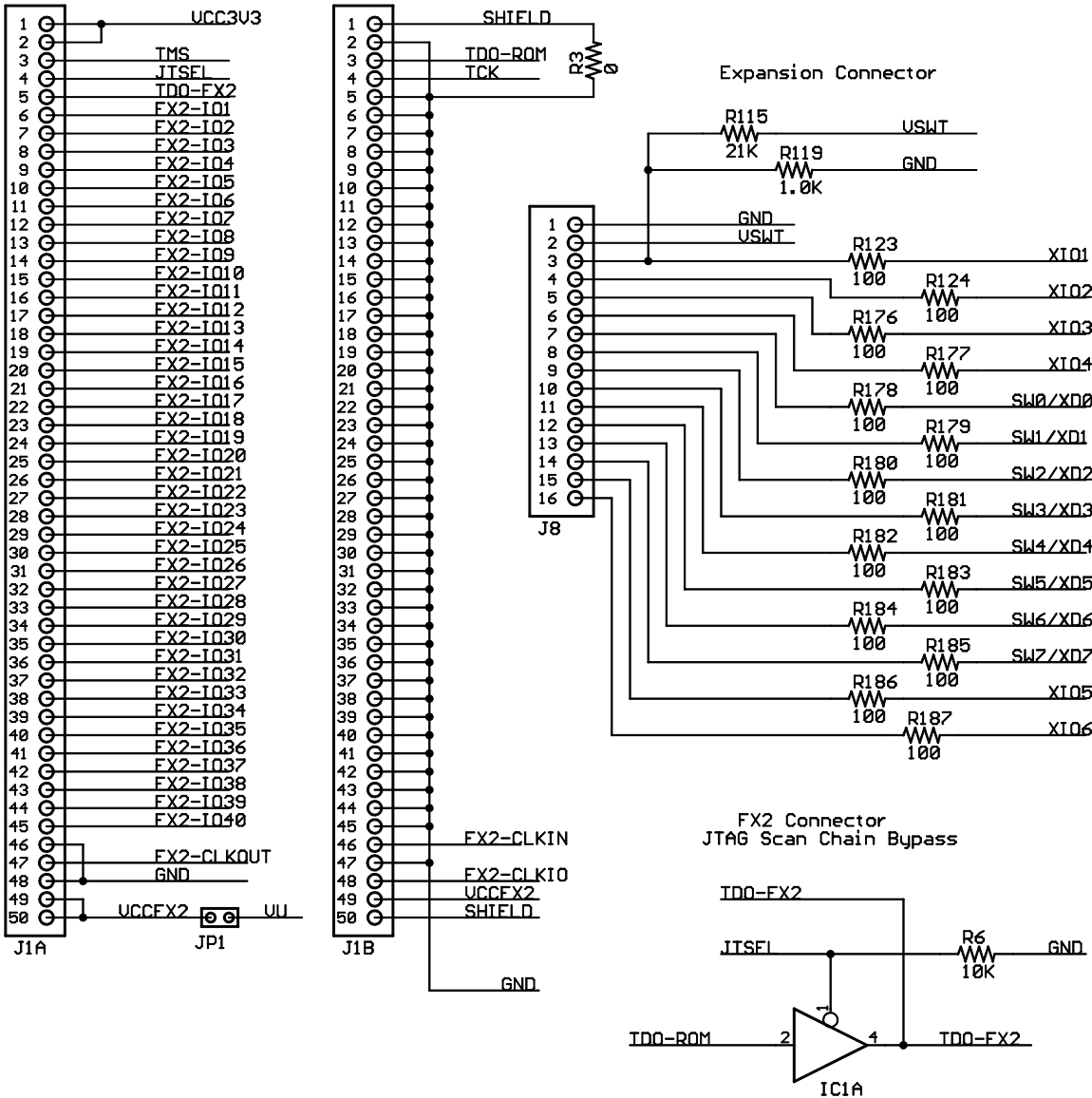
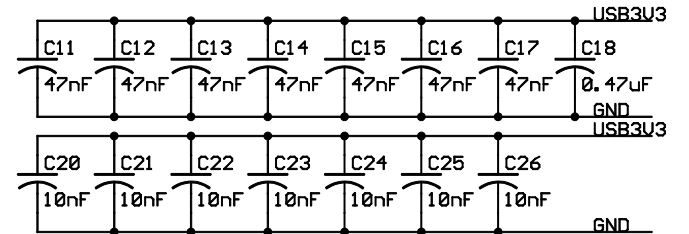
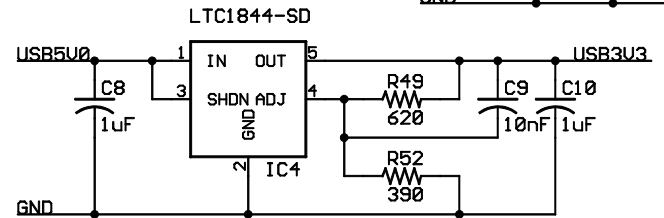
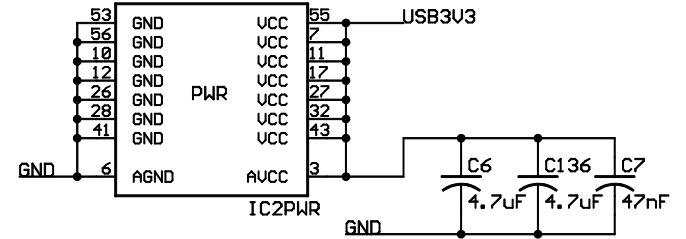
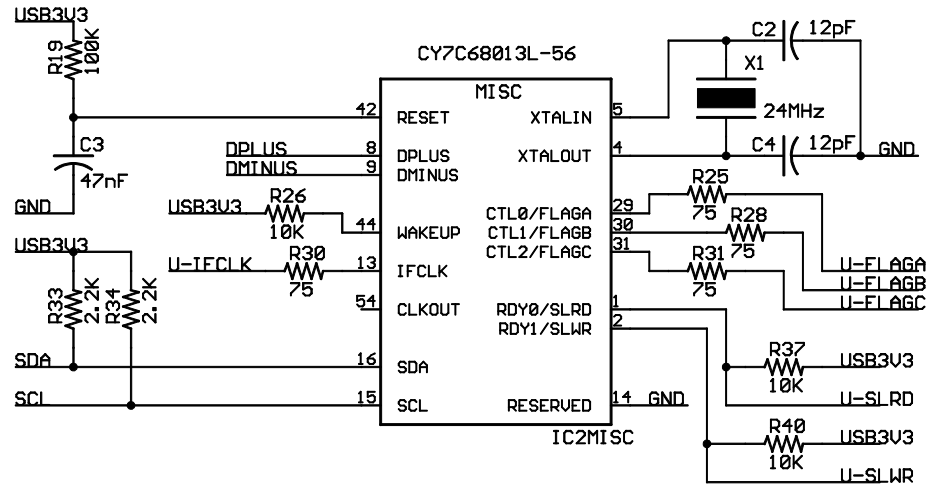
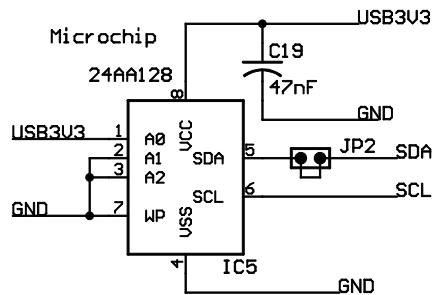
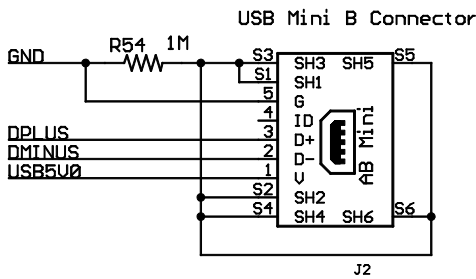
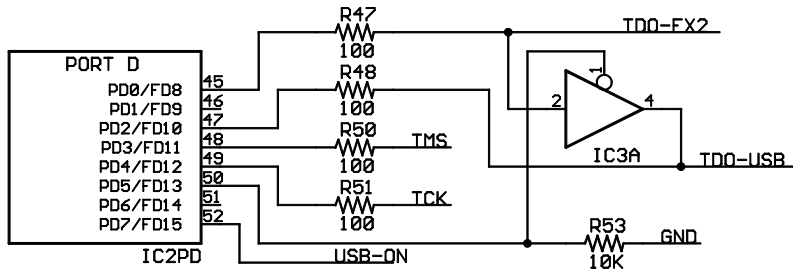
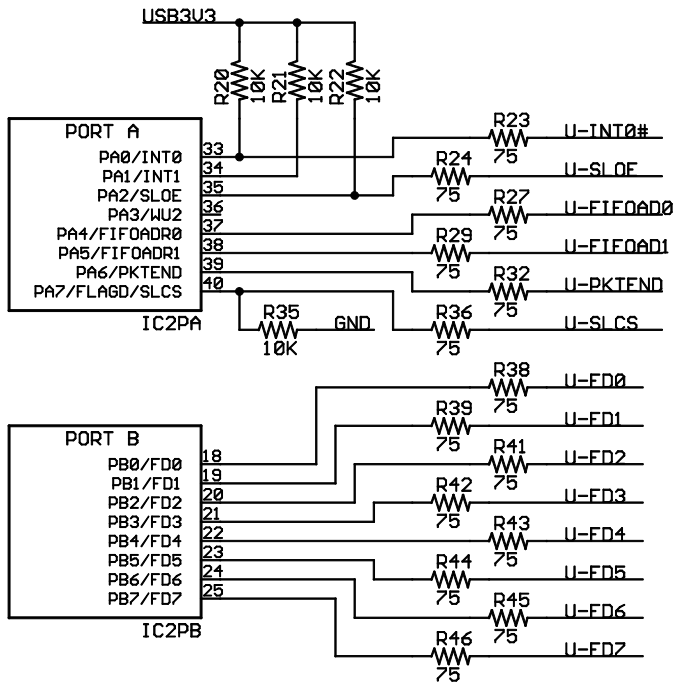


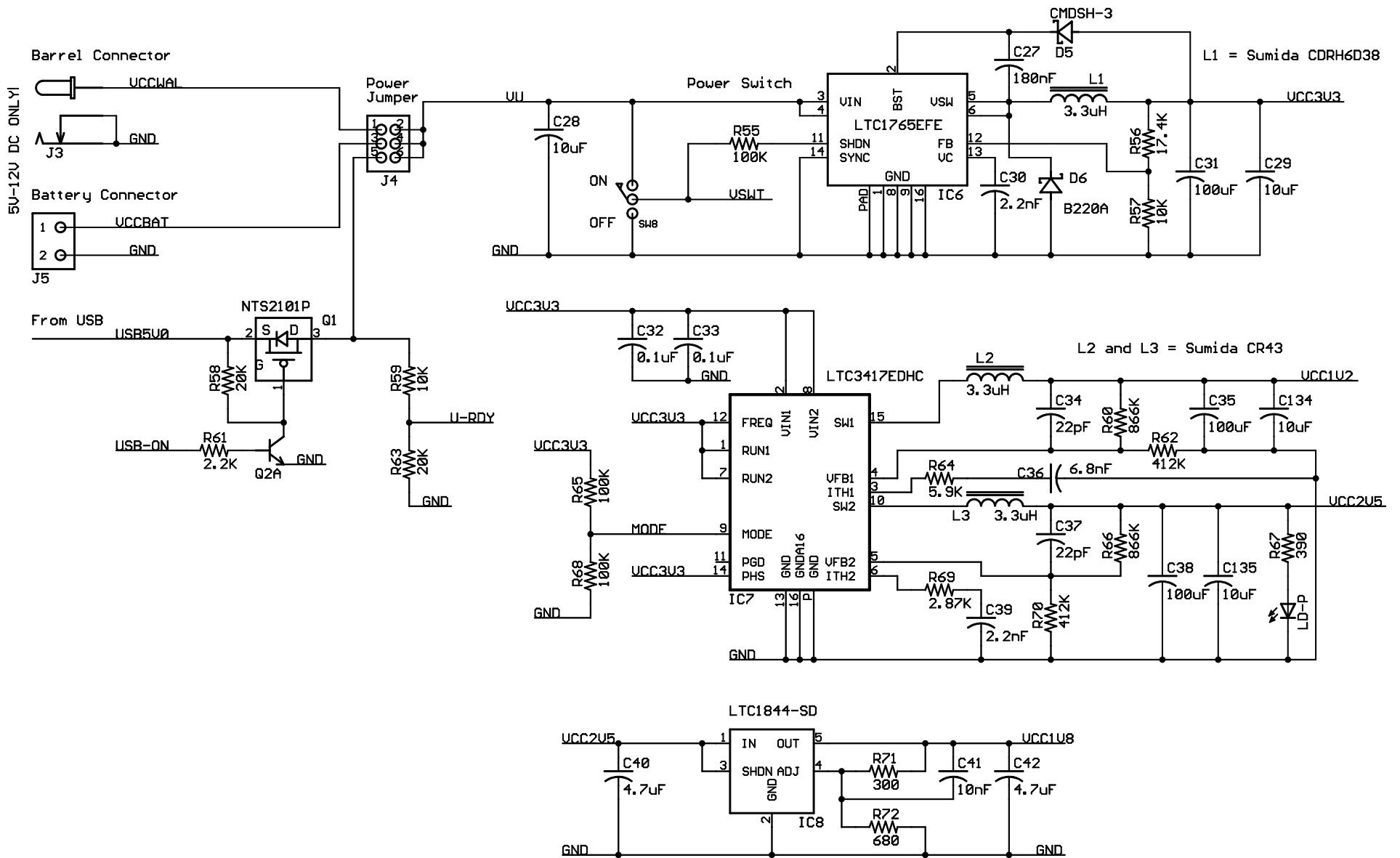
Hirose FX2 Connector



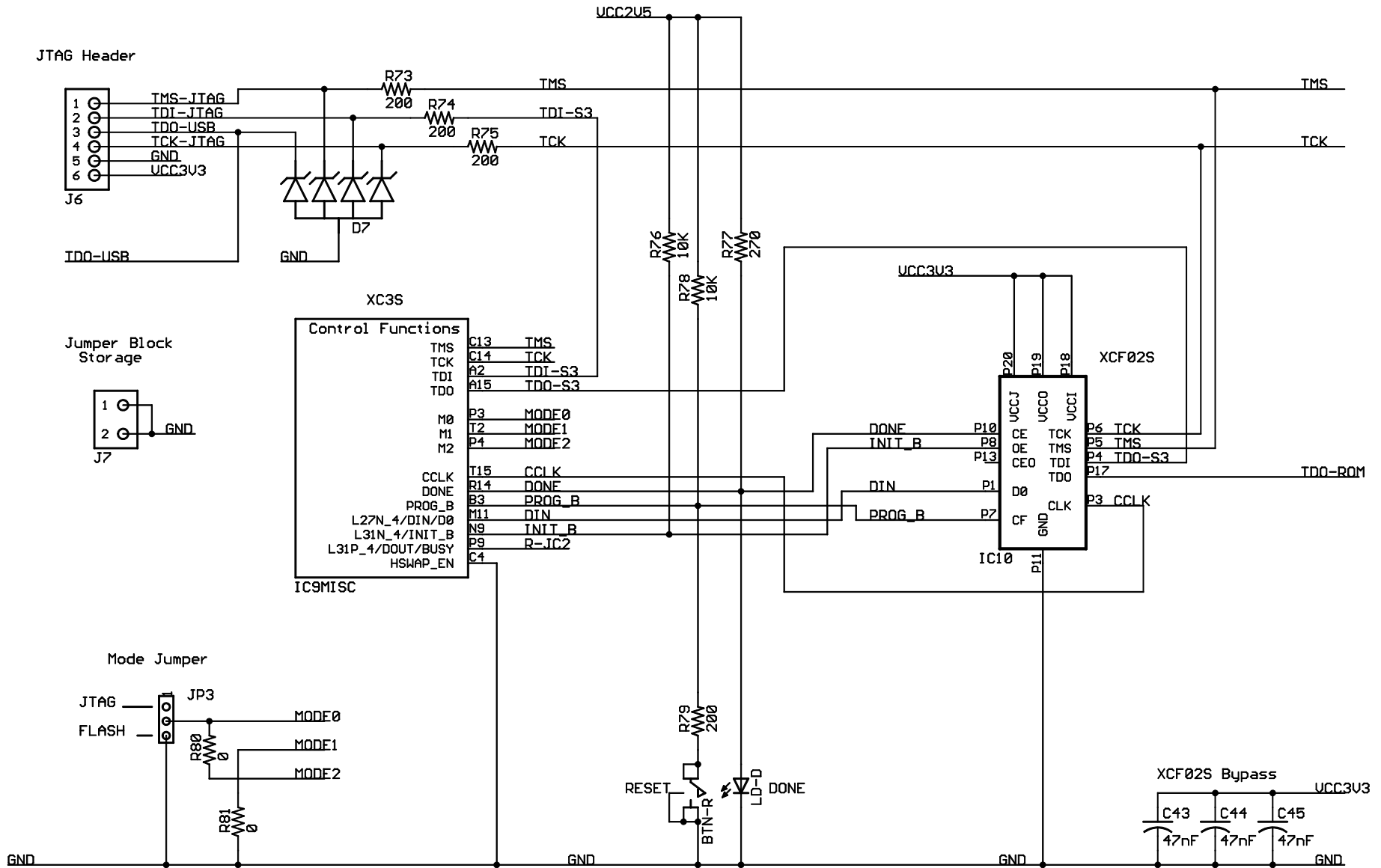
Designed and Manufactured by Digilent Inc.		Intel Strataflysh	Xilinx Micron WECC
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SHEET: I/O Connectors		Author: GMA	
TITLE: Nexys		Rev: G	
Nexys	Doc#: 500-100	Date: 10/12/2006	Sheet: 1/9



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SHEET: USB Interface		Rev: G
TITLE: Nexys		Doc#: 500-100
Date: 10/12/2006		Sheet: 2/9



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SHEET: Main Power Supplies		Rev: G
TITLE: Nexys		Doc#: 500-100
Date: 10/12/2006		Sheet: 3/9



Digilent Nexys Board		Engineer: NEA
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SHEET: FPGA Programming and JTAG		Rev: G
TITLE: Nexys		Date: 10/12/2006
Doc#: 500-100	Date: 10/12/2006	Sheet: 4/9

4/16<2>

I/O Bank 0		
I01	A5	R-JC3
I02	A7	R-JC4
I03/UREF_0	A3	ADR22
I04/UREF_0	D5	R-IC1
L01N_0	B4	R-I01
L01P_0	A4	R-I02
L25N_0	C5	R-I03
L25P_0	B5	R-I04
L27N_0	E6	R-I05
L27P_0	D6	R-I06
L28N_0	C6	R-I07
L28P_0	B6	R-I08
L29N_0	E7	R-I09
L29P_0	D7	R-I010
L30N_0	C7	R-I011
L30P_0	B7	R-I012
L31N_0	D8	R-I013
L31P_0/UREF_0	C8	R-I014
L32P_0/GCLK6	A8	GCLK
L32N_0/GCLK7	B8	R-CLKIO

IC9B0

4/16<2>

I/O Bank 1		
I01	A9	R-JD1
I02	A12	R-JD2
I03	C10	R-JD3
I04/UREF_1	D12	R-ID4
L01N_1	A14	R-I027
L01P_1	B14	R-I028
L10N_1/UREF_1	A13	R-I025
L10P_1	B13	R-I026
L127N_1	B12	R-I023
L127P_1	C12	R-I024
L20N_1	D11	R-I021
L20P_1	E11	R-I022
L29N_1	B11	R-I019
L29P_1	C11	R-I020
L30N_1	D10	R-I017
L30P_1	E10	R-I018
L31N_1/UREF_1	A10	R-I015
L31P_1	B10	R-I016
L32N_1/GCLK5	C9	FX2-CLKIN
L32P_1/GCLK4	D9	FX2-CLKOUT

IC9B1

1/22

I/O Bank 2		
I01	G16	R-CG
L01N_2	B16	R-I029
L01P_2	C16	R-I030
L16N_2	C15	R-I031
L16P_2	D14	R-I032
L17N_2	D15	R-I033
L17P_2/UREF_2	D16	R-I034
L19N_2	E13	R-CB
L19P_2	E14	R-CF
L20N_2	E15	R-I035
L20P_2	E16	R-I036
L21N_2	F12	R-AN3
L21P_2	F13	R-CA
L22N_2	F14	R-I037
L22P_2	F15	R-I038
L23N_2/UREF_2	G12	R-AN1
L23P_2	G13	R-AN2
L24N_2	G14	R-AN0
L24P_2	G15	R-CC
L39N_2	H13	R-CD
L39P_2	H14	R-CDP
L40N_2	H15	R-I040
L40P_2/UREF_2	H16	R-I039

IC9B2

1/22

I/O Bank 3		
I01	K15	SW3/XD3
L01N_3	P16	XT01
L01P_3	R16	ID7
L16N_3	P15	XT02
L16P_3	P14	ID6
L17N_3	N16	SW2/XD7
L17P_3/UREF_3	N15	SW0/XD0
L19N_3	M14	ID2
L19P_3	N14	ID4
L20N_3	M16	SW5/XD5
L20P_3	M15	SW6/XD6
L21N_3	L13	ID1
L21P_3	M13	ID5
L22N_3	L15	SW4/XD4
L22P_3	L14	ID0
L23N_3	K12	BTN3
L23P_3/UREF_3	L12	ID3
L24N_3	K14	BTN1
L24P_3	K13	BTN2
L39N_3	J14	R-CF
L39P_3	J13	BTN0
L40N_3/UREF_3	J16	SW1/XD1
L40P_3	K16	SW2/XD2

IC9B3

5/13<5>

I/O Bank 4		
I01	T12	R-IB1
I02	T14	R-IA1
I03/UREF_4	N12	U-ED0
I04/UREF_4	P13	U-RDY
I05/UREF_4	T10	R-IB4
L01N_4	R13	R-IA2
L01P_4	T13	R-IA3
L25N_4	P12	U-ED1
L25P_4	R12	R-IA4
L27N_4/D1	N11	U-ED2
L27P_4	P11	U-ED3
L29N_4	R11	R-IB2
L29P_4	M10	U-ED6
L29N_4	N10	U-ED4
L29P_4	P10	U-ED5
L30N_4/D2	R10	U-ED7
L30P_4/D3		
L32N_4/GCLK1	R9	GCLK1
L32P_4/GCLK0	T9	U-IFCLK

IC9B4

4/16<8>

I/O Bank 5		
I01	N5	U-SLRD
I02	P7	U-FLAGB
I03	T5	U-SLWR
I04/UREF_5	T8	U-SLCS
L01N_5/RDWR_B	T3	WF
L01P_5/CS_B	R3	DBZ
L10N_5	T4	RP#
L10P_5	R4	ST-ST5
L27N_5/UREF_5	R5	XT04
L27P_5	P5	U-EIFOAD0
L29N_5/D6	N6	U-SLOE
L29P_5/D7	M6	U-EKTEAD
L29N_5	R6	XT05
L29P_5/UREF_5	P6	U-TNT0#
L30N_5	N7	U-ELAGC
L30P_5	M7	U-EIFOAD1
L31N_5/D4	T7	XT03
L31P_5/D5	R7	XT06
L32N_5/GCLK3		
L32P_5/GCLK2		

IC9B5

1/22

I/O Bank 6		
I01	K1	MT-CE
L01N_6	R1	DB6
L01P_6	P1	DB5
L16N_6	P2	DB4
L16P_6	N3	ADR12
L17N_6	N2	DB2
L17P_6/UREF_6	M1	DB3
L19N_6	M4	ADR21
L19P_6	M3	ADR14
L20N_6	M2	DB0
L20P_6	M1	DB1
L21N_6	L5	ADR13
L21P_6	L4	ADR16
L22N_6	L3	ADR3
L22P_6	L2	MT-CRE
L23N_6	K5	ADR2
L23P_6	K4	ADR7
L24N_6/UREF_6	K3	ADR5
L24P_6	K2	OF
L39N_6	J4	ADR4
L39P_6	J3	ADR1
L40N_6	J2	MT-UB
L40P_6/UREF_6	J1	MT-LB

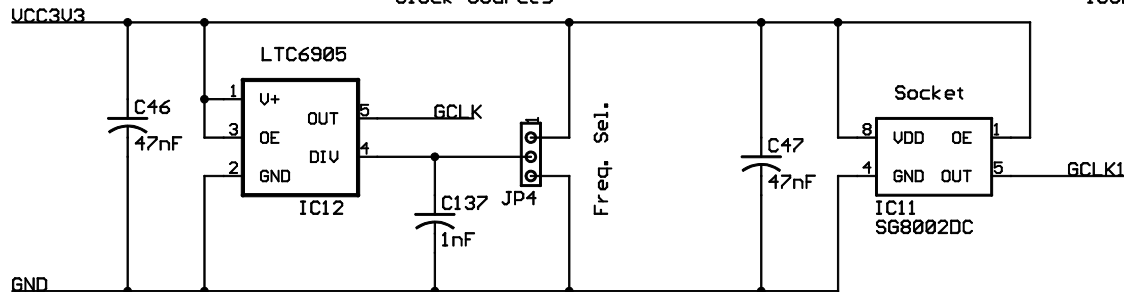
IC9B6

1/22

I/O Bank 7		
I01	G2	DB10
L01N_7	C1	MT-WAIT
L01P_7	B1	MT-ADV
L16N_7	C2	MT-CLK
L16P_7/UREF_7	C3	ADR23
L17N_7	D1	DB13
L17P_7	D2	DB15
L19N_7/UREF_7	E3	ADR9
L19P_7	D3	ADR20
L20N_7	E1	DB12
L20P_7	E2	DB14
L21N_7	F4	ADR10
L21P_7	E4	ST-CE
L22N_7	F2	DB11
L22P_7	F3	ADR15
L23N_7	G5	ADR19
L23P_7	F5	ADR11
L24N_7	G3	ADR8
L24P_7	G4	ADR17
L39N_7	H3	ADR18
L39P_7	H4	ADR6
L40N_7/UREF_7	H1	DB8
L40P_7	G1	DB9

IC9B7

Clock Sources



Digilent Nexys Board

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Engineer: NEA

SHEET: Spartan 3 and Oscillator

Author: GMA

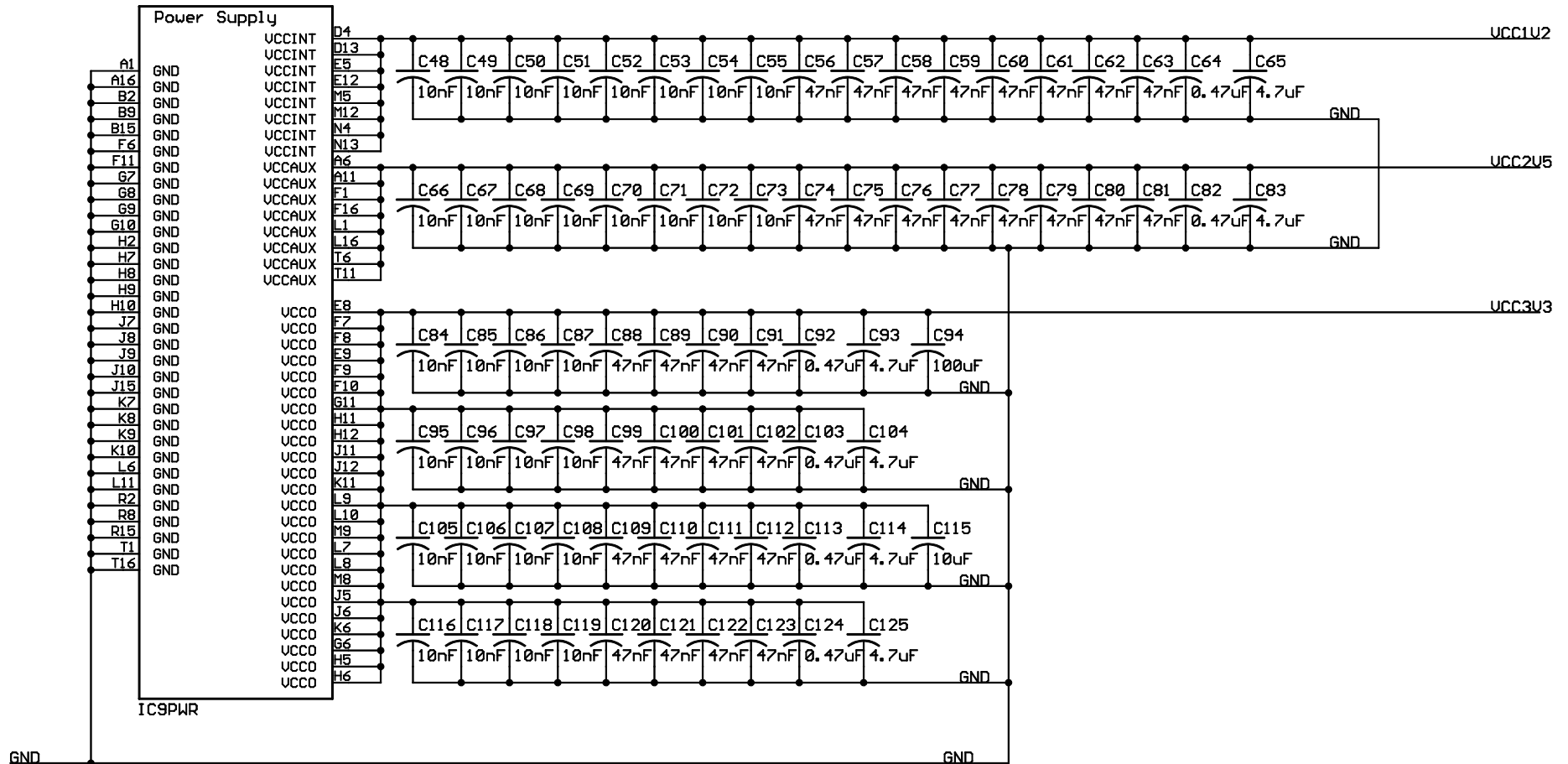
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Rev: G

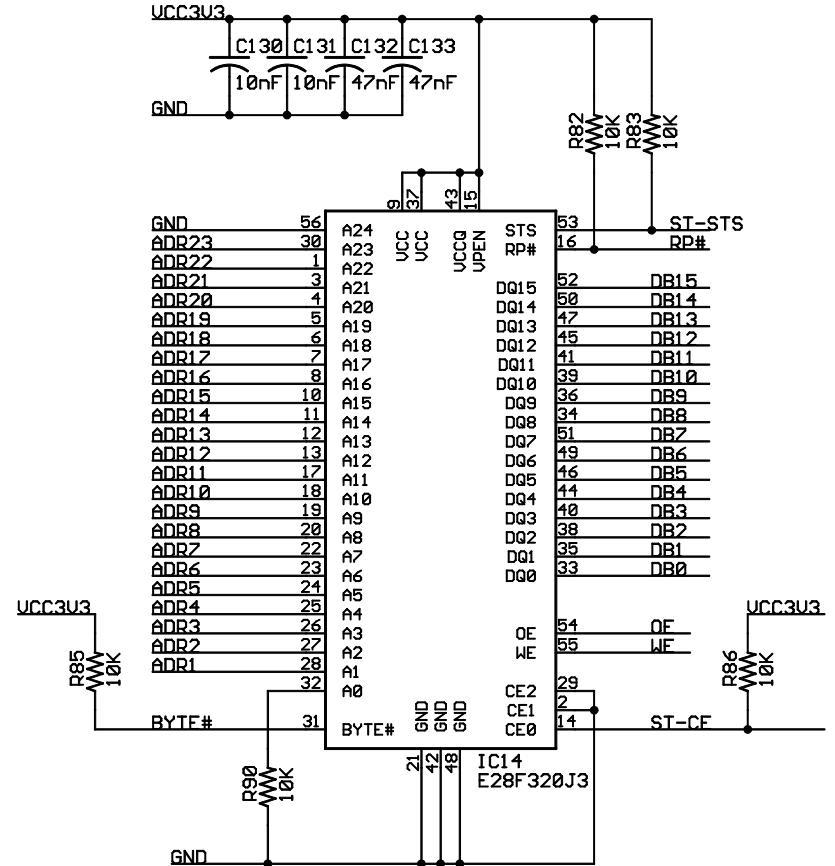
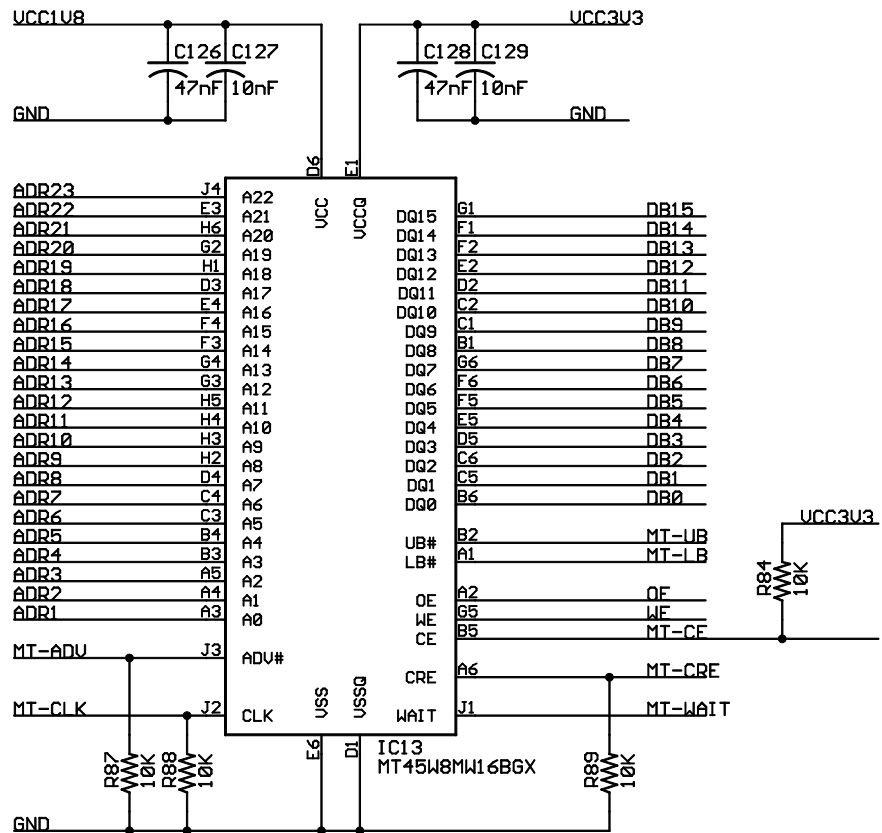
Doc#: 500-100

Date: 10/12/2006

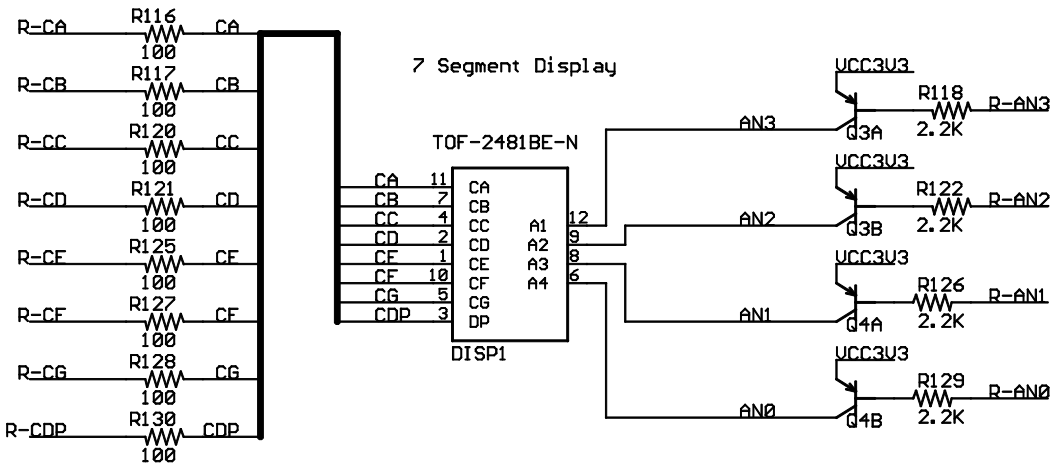
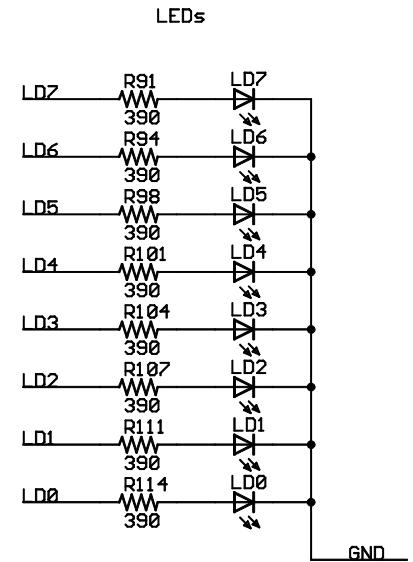
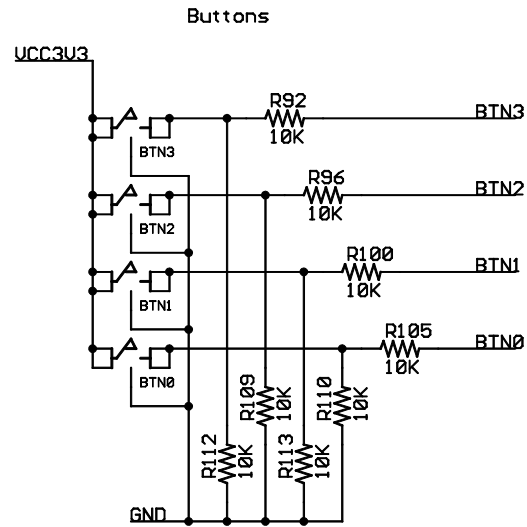
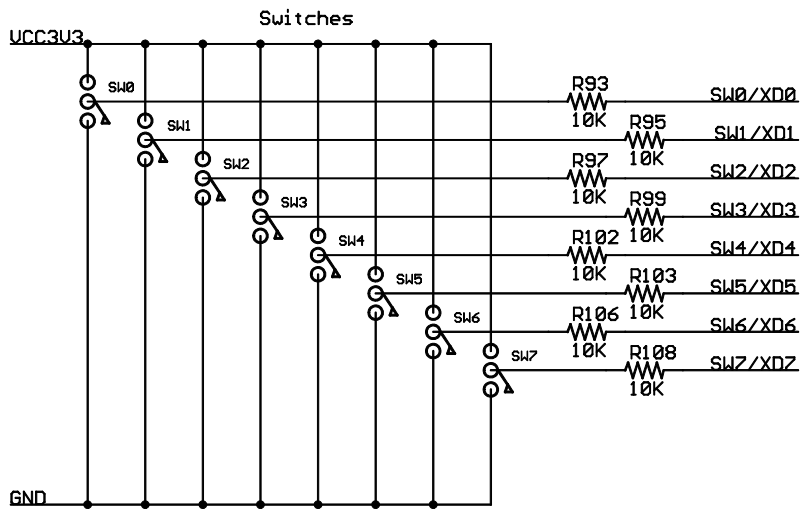
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SHEET: Spartan 3 Decoupling Capacitors		Rev: G
TITLE: Nexys		Date: 10/12/2006
Doc#: 500-100	Date: 10/12/2006	Sheet: 6/9

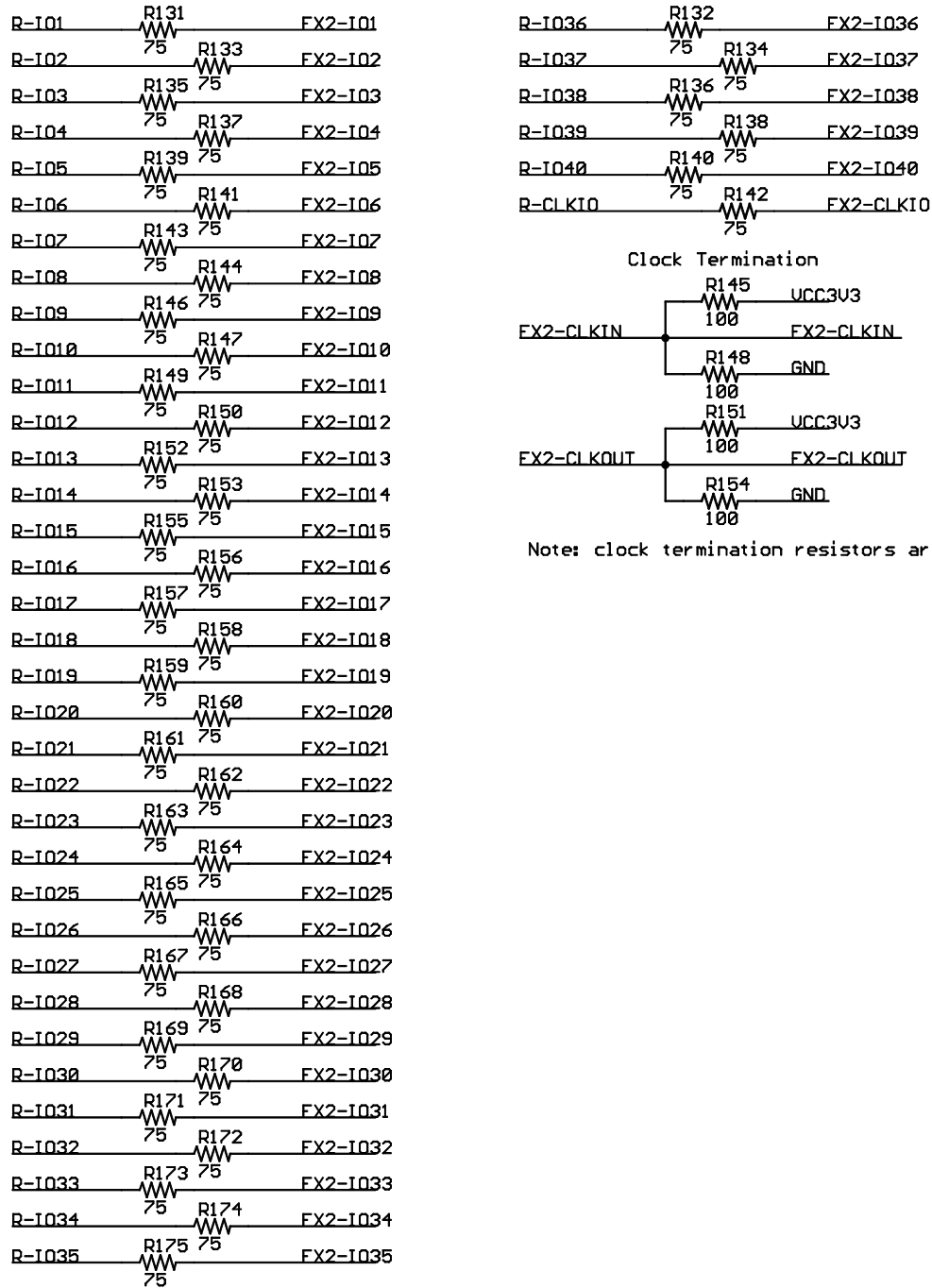


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SHEET: Cellular RAM and StrataFlash		Rev: G
TITLE: Nexys		Doc#: 500-100
Date: 10/12/2006		Sheet: 7/9



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SHEET: I/O and Displays		Rev: G
TITLE: Nexys		Rev: G
Doc#: 500-100	Date: 10/12/2006	Sheet: 8/9

Hirose FX2 Series Resistors



Note: clock termination resistors are not loaded by default

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SHEET: Hirose Series Resistors		Rev: G
TITLE: Nexys		Date: 10/12/2006
Doc#: 500-100	Date: 10/12/2006	Sheet: 9/9