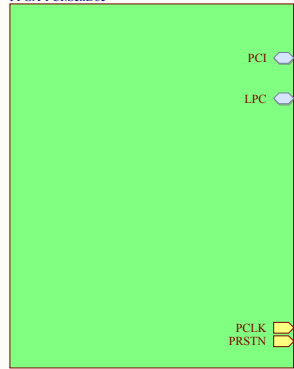
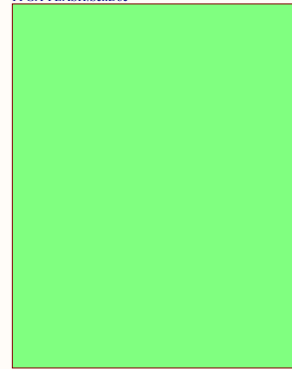


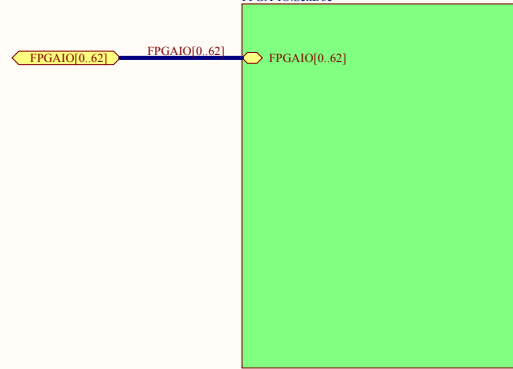
FPGA-PCI
FPGA-PCI.SchDoc



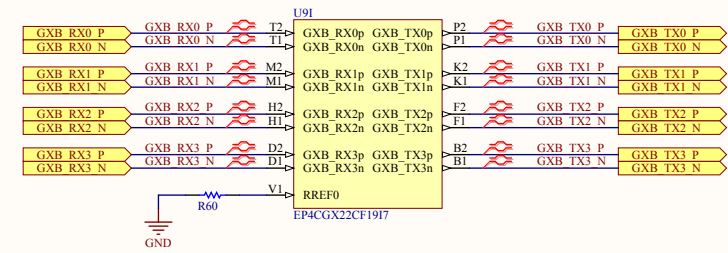
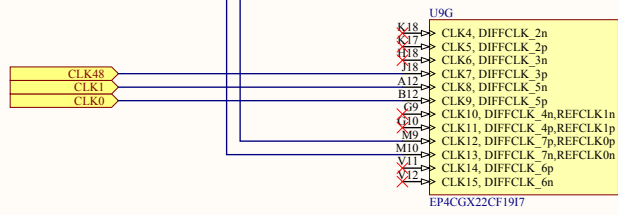
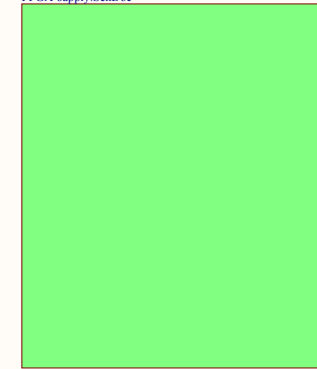
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FPGA-FLASH.SchDoc



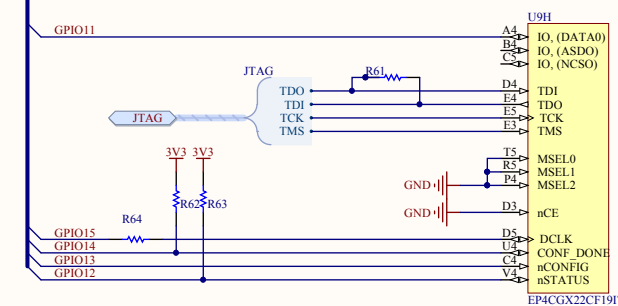
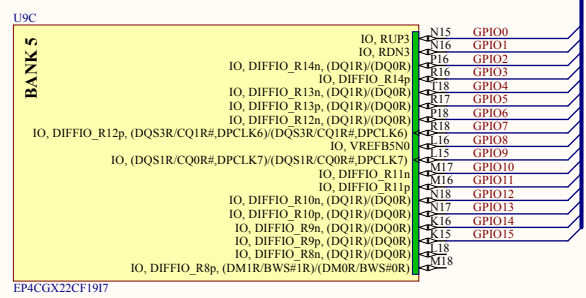
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FPGA-IO.SchDoc



FPGA-SUPPLY
FPGA-supply.SchDoc

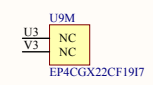


GPIO[15..0] GPIO[15..0]

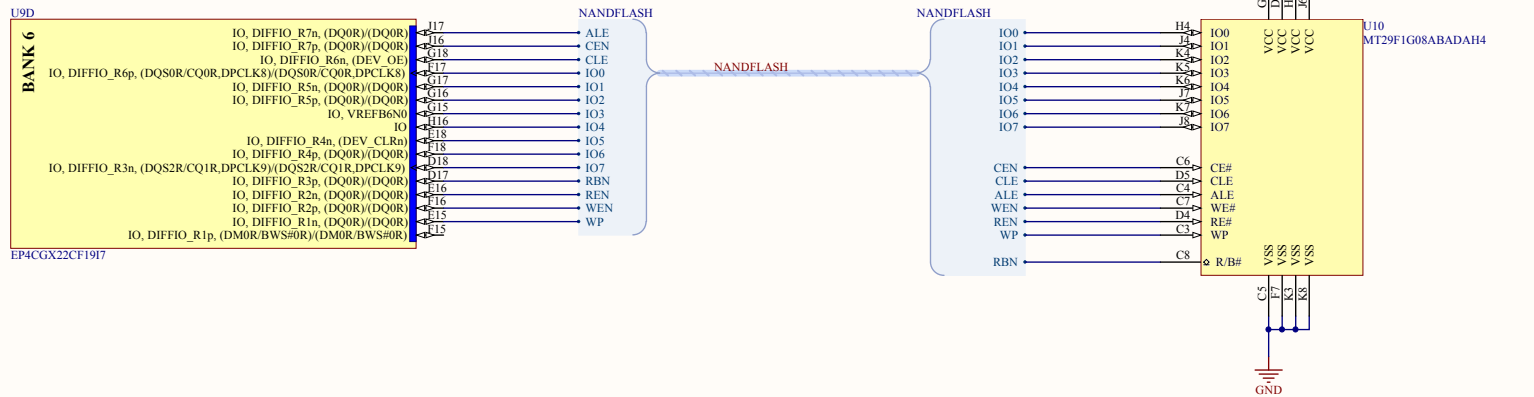


CONFIGURATIONS BITS:
7,600,040

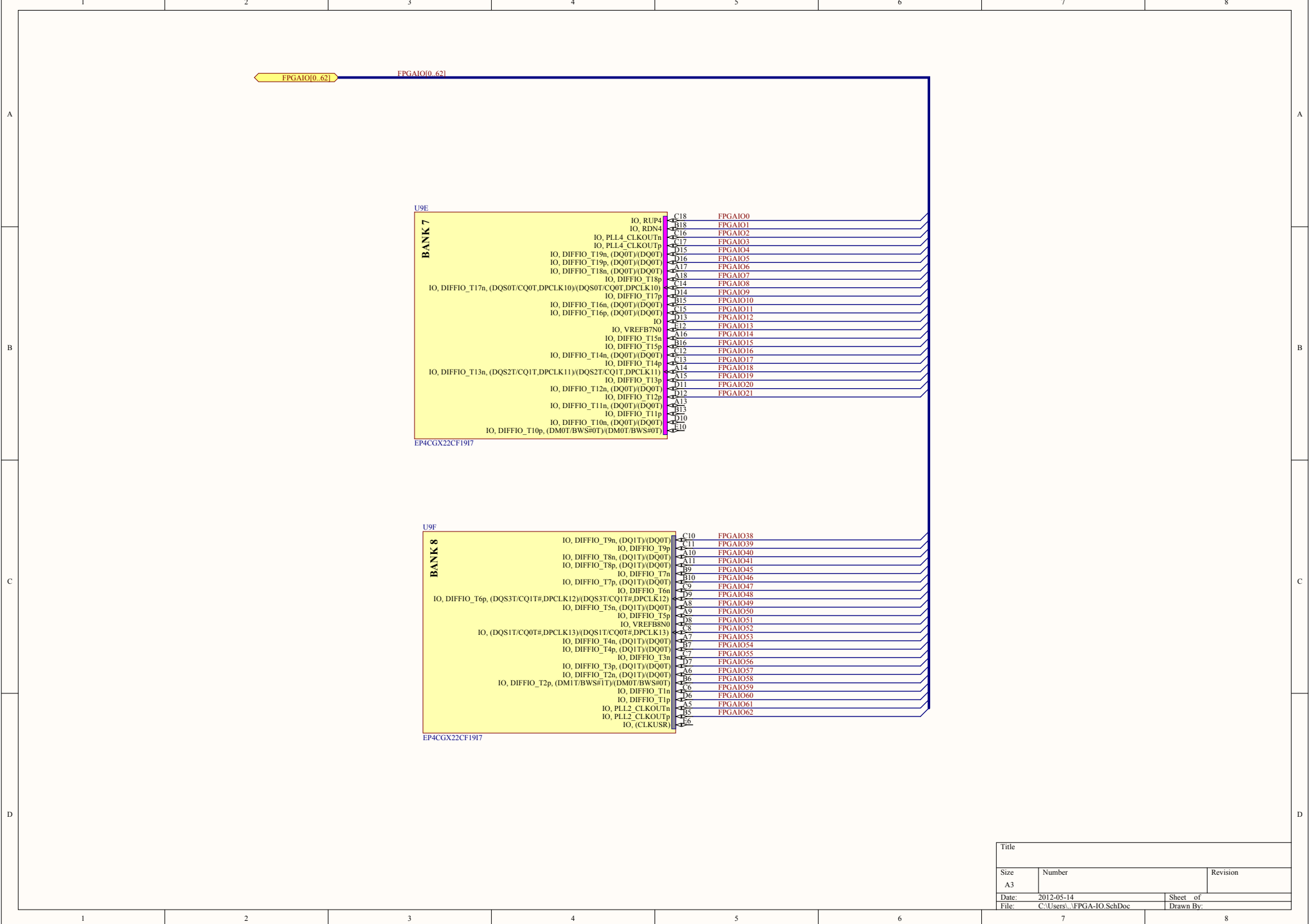
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MSEL2 0



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FPGAIO[0..62]

U9E

BANK 7

IO, RUP4	C18	FPGAIO0
IO, RDN4	B18	FPGAIO1
IO, PLL4_CLKOUTn	A16	FPGAIO2
IO, PLL4_CLKOUTp	C17	FPGAIO3
IO, DIFFIO_T19n, (DQ0T)/(DQ0T)	B15	FPGAIO4
IO, DIFFIO_T19p, (DQ0T)/(DQ0T)	D16	FPGAIO5
IO, DIFFIO_T18n, (DQ0T)/(DQ0T)	A17	FPGAIO6
IO, DIFFIO_T18p, (DQ0T)/(DQ0T)	C18	FPGAIO7
IO, DIFFIO_T17n, (DQS0T/CQ0T, DPCLK10)/(DQS0T/CQ0T, DPCLK10)	B14	FPGAIO8
IO, DIFFIO_T17p, (DQS0T/CQ0T, DPCLK10)/(DQS0T/CQ0T, DPCLK10)	D14	FPGAIO9
IO, DIFFIO_T16n, (DQ0T)/(DQ0T)	B15	FPGAIO10
IO, DIFFIO_T16p, (DQ0T)/(DQ0T)	C15	FPGAIO11
IO, VREFB7N0	D13	FPGAIO12
IO, DIFFIO_T15n, (DQ0T)/(DQ0T)	A16	FPGAIO13
IO, DIFFIO_T15p, (DQ0T)/(DQ0T)	B16	FPGAIO14
IO, DIFFIO_T14n, (DQ0T)/(DQ0T)	C12	FPGAIO15
IO, DIFFIO_T14p, (DQ0T)/(DQ0T)	D13	FPGAIO16
IO, DIFFIO_T13n, (DQS2T/CQ1T, DPCLK11)/(DQS2T/CQ1T, DPCLK11)	A14	FPGAIO17
IO, DIFFIO_T13p, (DQS2T/CQ1T, DPCLK11)/(DQS2T/CQ1T, DPCLK11)	A15	FPGAIO18
IO, DIFFIO_T12n, (DQ0T)/(DQ0T)	B11	FPGAIO19
IO, DIFFIO_T12p, (DQ0T)/(DQ0T)	C12	FPGAIO20
IO, DIFFIO_T11n, (DQ0T)/(DQ0T)	A13	FPGAIO21
IO, DIFFIO_T11p, (DQ0T)/(DQ0T)	B13	FPGAIO22
IO, DIFFIO_T10n, (DM0T/BWS#0T)/(DM0T/BWS#0T)	D10	FPGAIO23
IO, DIFFIO_T10p, (DM0T/BWS#0T)/(DM0T/BWS#0T)	A10	FPGAIO24

EP4CGX22CF1917

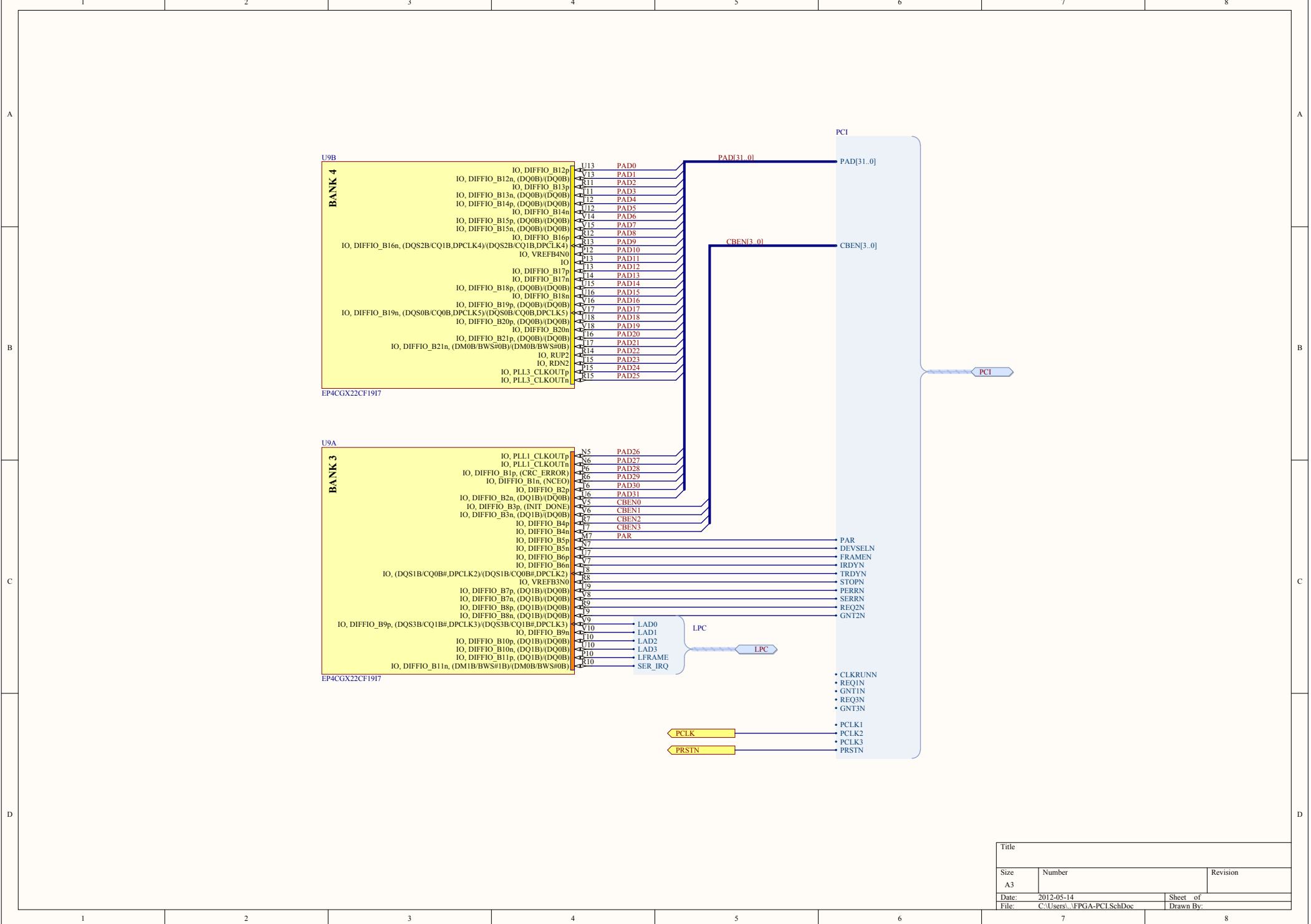
U9F

BANK 8

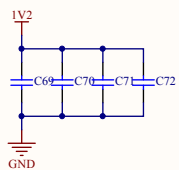
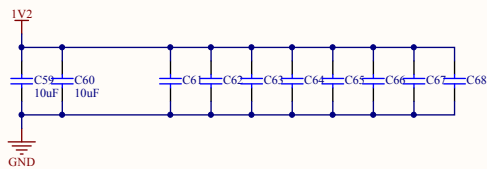
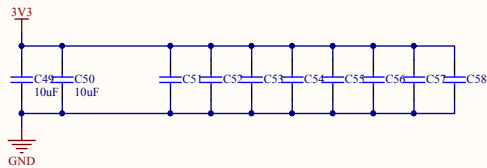
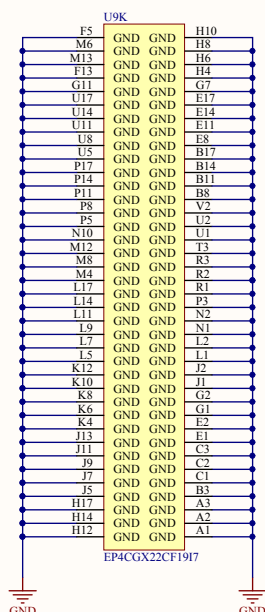
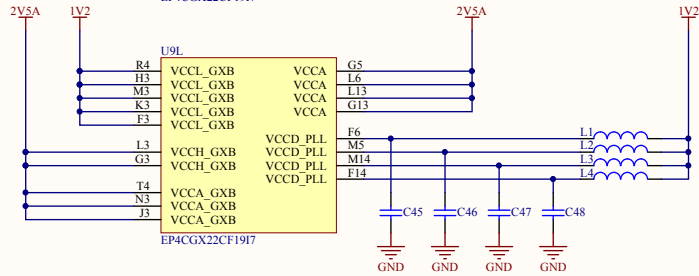
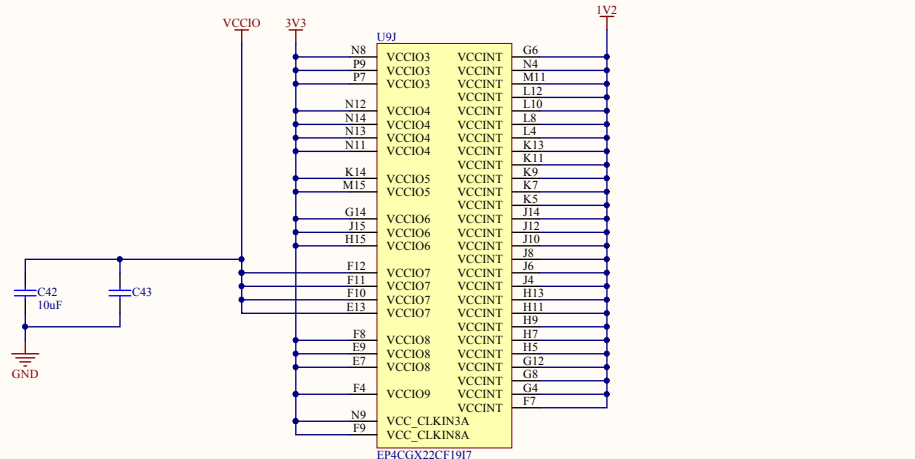
IO, DIFFIO_T9n, (DQ1T)/(DQ0T)	C10	FPGAIO38
IO, DIFFIO_T9p, (DQ1T)/(DQ0T)	C11	FPGAIO39
IO, DIFFIO_T8n, (DQ1T)/(DQ0T)	A10	FPGAIO40
IO, DIFFIO_T8p, (DQ1T)/(DQ0T)	A11	FPGAIO41
IO, DIFFIO_T7n, (DQ1T)/(DQ0T)	B9	FPGAIO42
IO, DIFFIO_T7p, (DQ1T)/(DQ0T)	D10	FPGAIO43
IO, DIFFIO_T6n, (DQS3T/CQ1T#, DPCLK12)/(DQS3T/CQ1T#, DPCLK12)	C9	FPGAIO44
IO, DIFFIO_T6p, (DQS3T/CQ1T#, DPCLK12)/(DQS3T/CQ1T#, DPCLK12)	D9	FPGAIO45
IO, DIFFIO_T5n, (DQ1T)/(DQ0T)	A8	FPGAIO46
IO, DIFFIO_T5p, (DQ1T)/(DQ0T)	A9	FPGAIO47
IO, VREFB8N0	B8	FPGAIO48
IO, (DQS1T/CQ0T#, DPCLK13)/(DQS1T/CQ0T#, DPCLK13)	C8	FPGAIO49
IO, DIFFIO_T4n, (DQ1T)/(DQ0T)	A7	FPGAIO50
IO, DIFFIO_T4p, (DQ1T)/(DQ0T)	B7	FPGAIO51
IO, DIFFIO_T3n, (DQ1T)/(DQ0T)	C7	FPGAIO52
IO, DIFFIO_T3p, (DQ1T)/(DQ0T)	D7	FPGAIO53
IO, DIFFIO_T2n, (DQ1T)/(DQ0T)	A6	FPGAIO54
IO, DIFFIO_T2p, (DQ1T)/(DQ0T)	B6	FPGAIO55
IO, DIFFIO_T1n, (DM1T/BWS#1T)/(DM1T/BWS#1T)	C6	FPGAIO56
IO, DIFFIO_T1p, (DM1T/BWS#1T)/(DM1T/BWS#1T)	D6	FPGAIO57
IO, PLL2_CLKOUTn	A5	FPGAIO58
IO, PLL2_CLKOUTp	B5	FPGAIO59
IO, (CLKUSR)	C6	FPGAIO60
	D6	FPGAIO61
	A6	FPGAIO62

EP4CGX22CF1917

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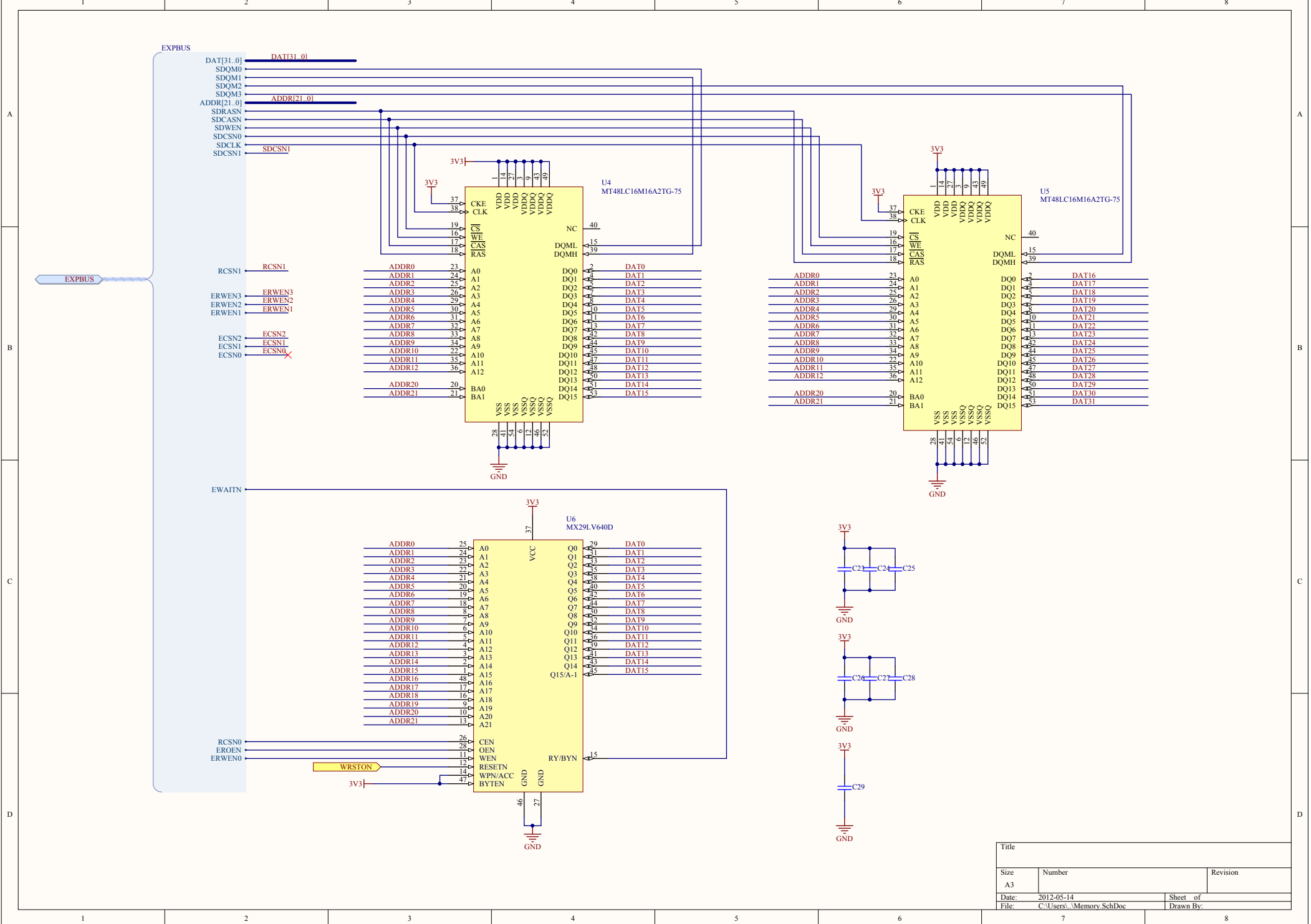
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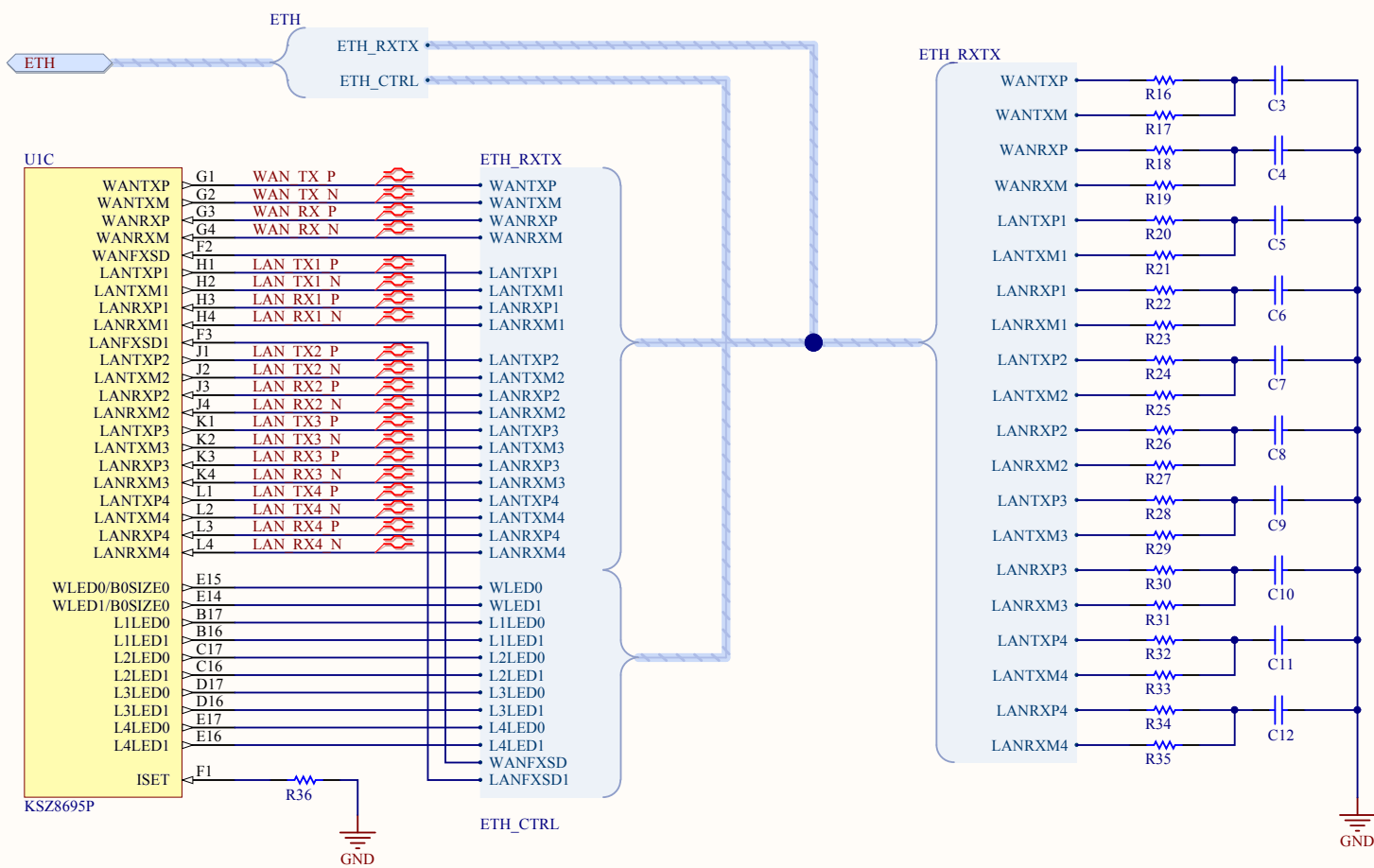
Power supply description for Cyclone IV GX		
VCCINT	1.2	Core voltage, PCI Express (PCIe) hard IP block, and transceiver physical coding sublayer (PCS) power supply
VCCA (1)	2.5	PLL analog power supply
VCCD_PLL	1.2	PLL digital power supply
VCCIO (2)	1.2, 1.5, 1.8, 2.5, 3.0, 3.3	I/O banks power supply
VCC_CLKIN (3)(4)	1.2, 1.5, 1.8, 2.5, 3.0, 3.3	Differential clock input pins power supply
VCCCH_GXB	2.5	Transceiver output (TX) buffer power supply
VCCL_GXB	1.2	Transceiver PMA and auxiliary power supply
VCCA_GXB	2.5	Transceiver physical medium attachment (PMA) and auxiliary power supply

- (1) You must power up VCCA even if the phase-locked loop (PLL) is not used.
- (2) I/O banks 3, 8, and 9 contain configuration pins. You can only power up the VCCIO level of I/O banks 3 and 9 to 1.5 V, 1.8 V, 2.5 V, 3.0 V, or 3.3 V. For Fast Passive Parallel (FPP) configuration mode, you must power up the VCCIO level of I/O bank 8 to 1.5 V, 1.8 V, 2.5 V, 3.0 V, or 3.3 V.
- (3) All device packages of EP4CGX15, EP4CGX22, and device package F169 and F324 of EP4CGX30 devices have two VCC_CLKIN dedicated clock input I/O located at Banks 3A and 8A. Device package F484 of EP4CGX30, all device packages of EP4CGX50, EP4CGX75, EP4CGX110, and EP4CGX150 devices have four VCC_CLKIN dedicated clock input I/O bank located at banks 3A, 3B, 8A, and 8B.
- (4) You must set VCC_CLKIN to 2.5 V if the CLKIN is used as high-speed serial interface (HSSI) refclk. VCC_CLKIN located at I/O banks 3B and 8B only support a nominal voltage level of 2.5 V for LVDS input function because they are dedicated for HSSI refclk. For EP4CGX50, EP4CGX75, EP4CGX110, and EP4CGX150 devices, the single-ended input CLK support is available for dedicated input CLK pins at I/O banks 3B and 8B.

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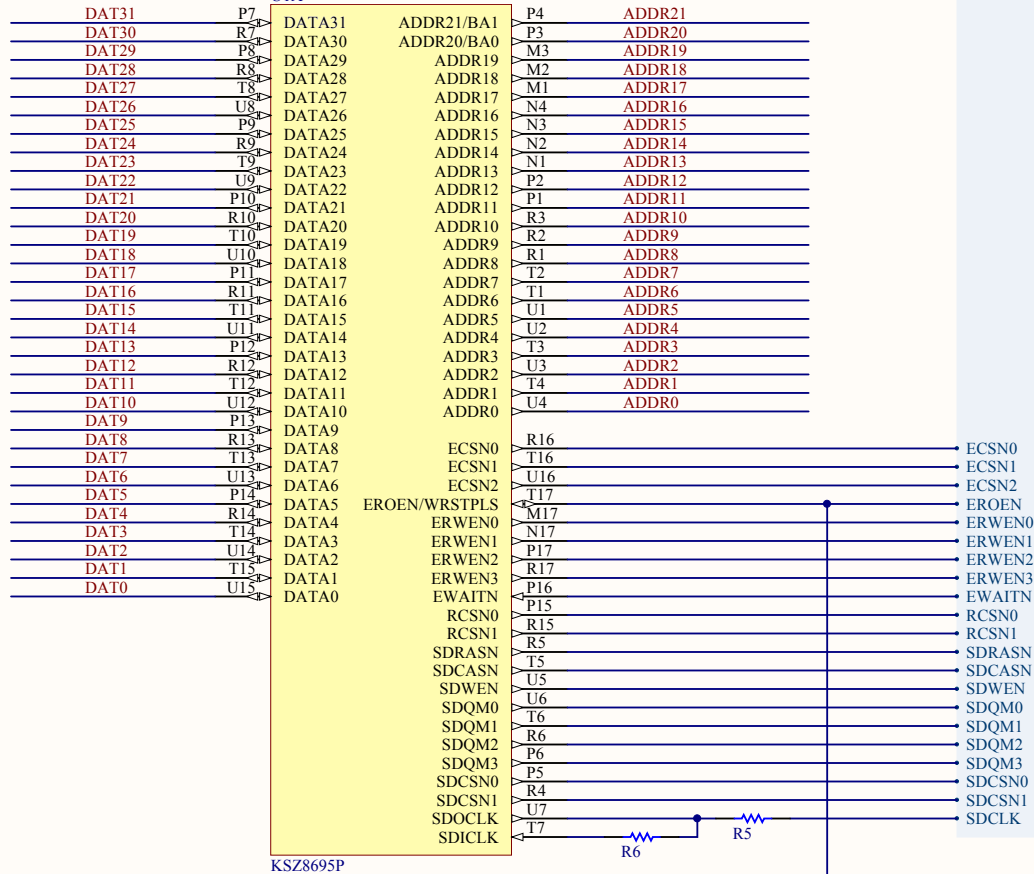
EXPBUS

EXPBUS

DAT[31..0] DAT[31..0]

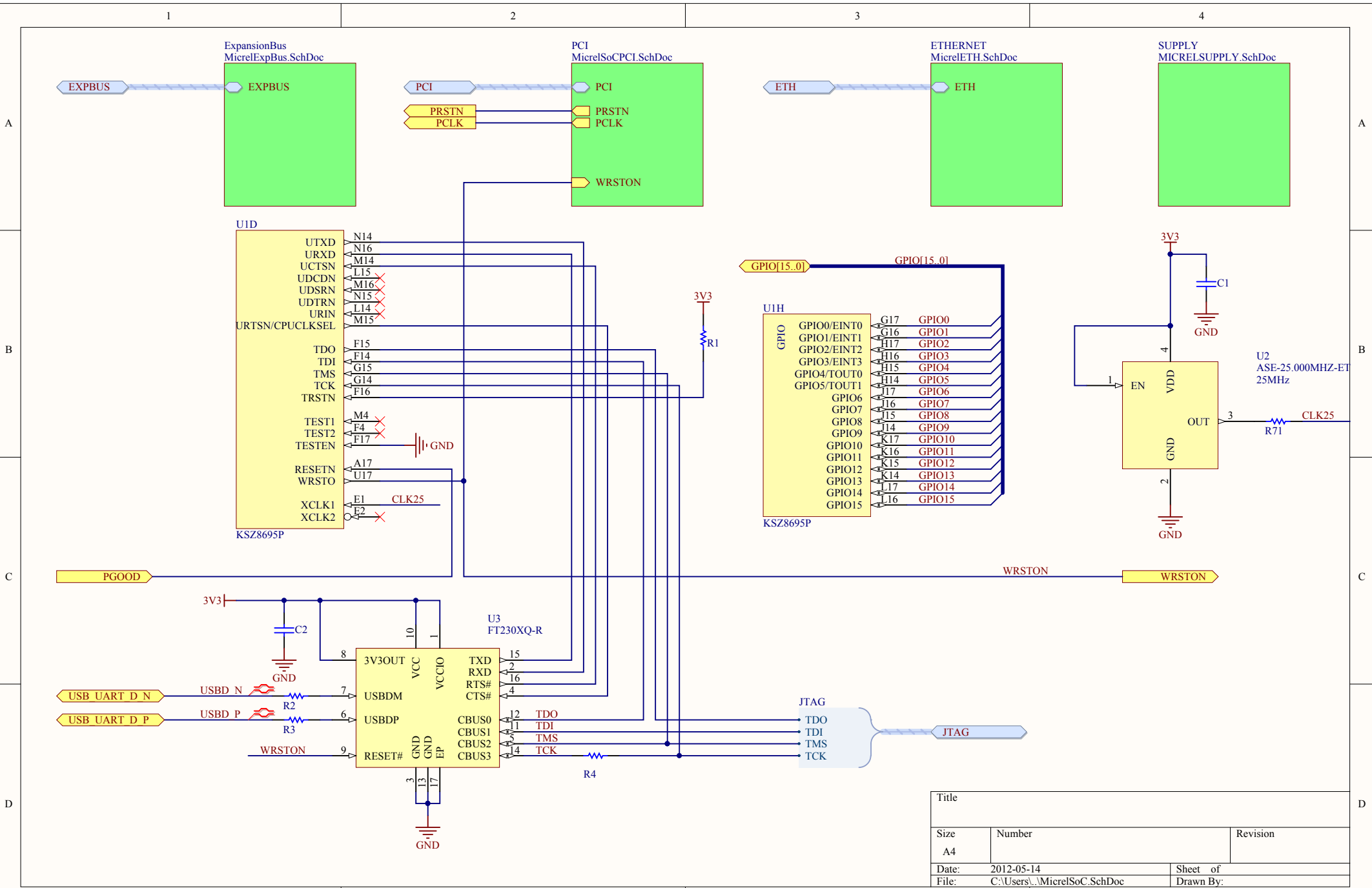
ADDR[21..0] ADDR[21..0]

UIA



KSZ8695P

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PCI

UIB

PCI

A

A

B

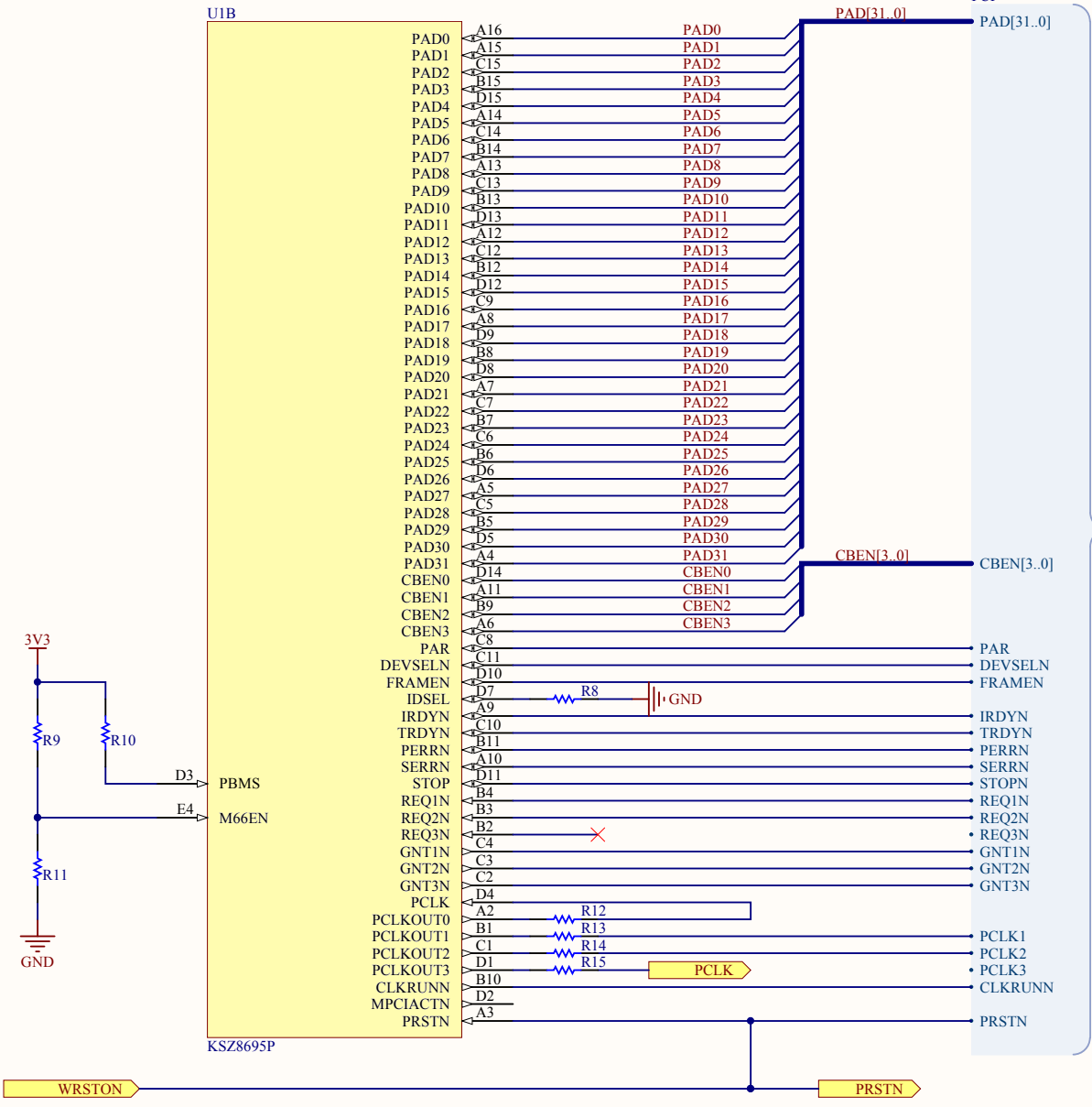
B

C

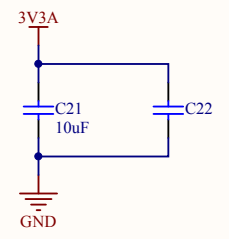
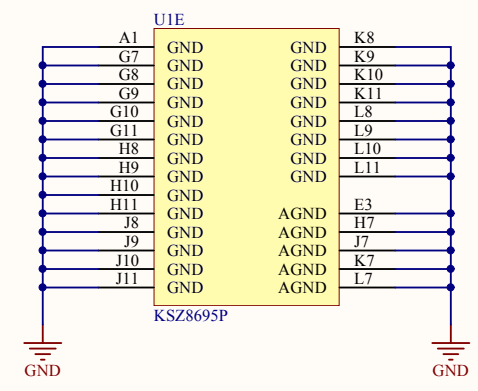
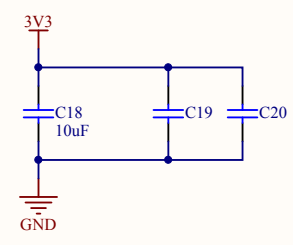
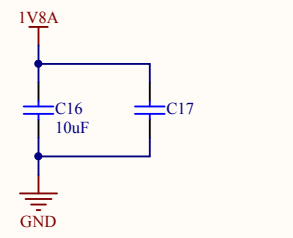
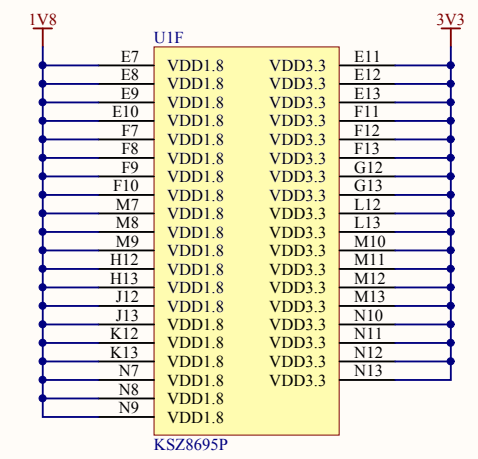
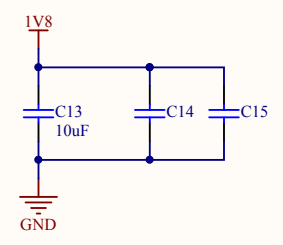
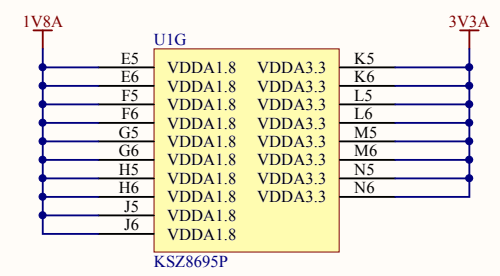
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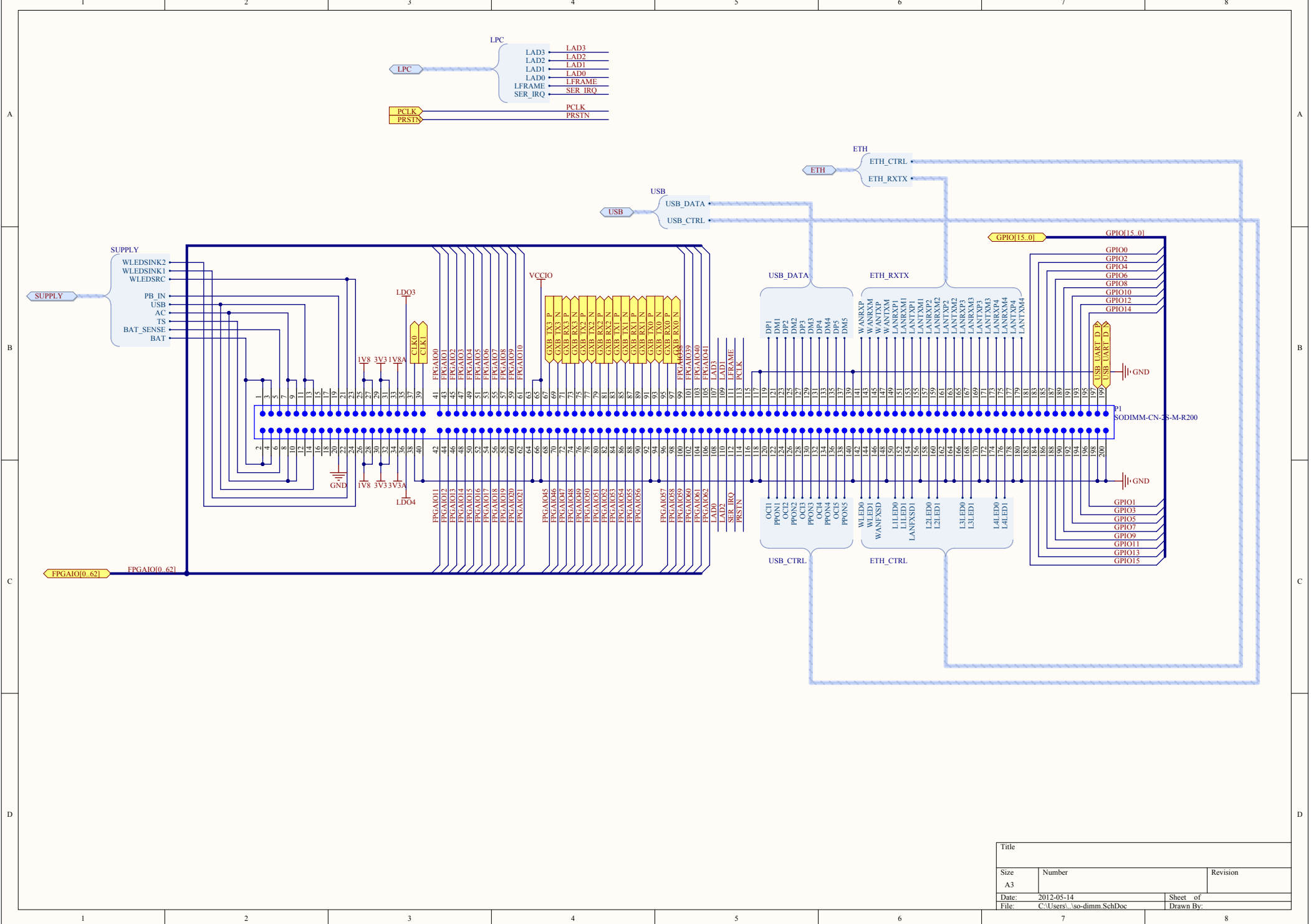
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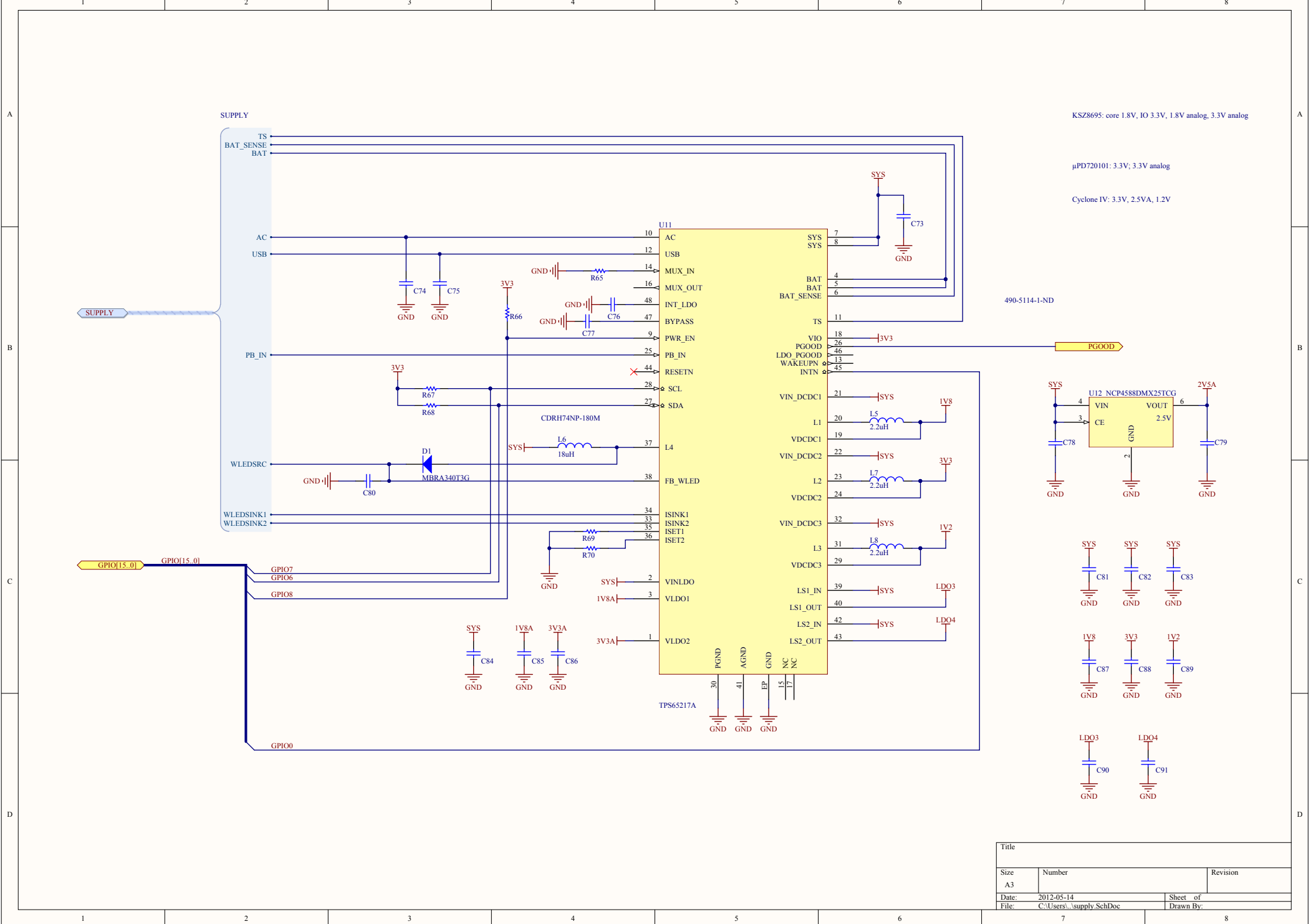
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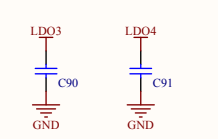
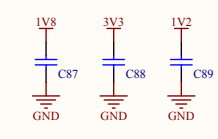
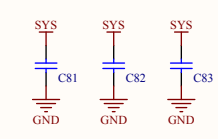
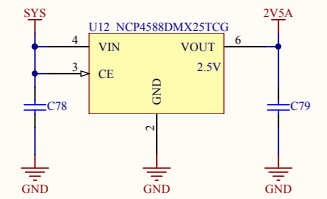


KSZ8695: core 1.8V, IO 3.3V, 1.8V analog, 3.3V analog

µPD720101: 3.3V; 3.3V analog

Cyclone IV: 3.3V, 2.5VA, 1.2V

490-5114-1-ND



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