SPI Master Core Specification

Author: Simon Srot
simons@opencores.org

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Revision History

Rev.	Date	Author	Description
0.1	June 13, 2002	Simon Srot	First Draft

Contents

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Introduction

Synchronous serial interfaces are widely used to provide economical board-level interface between different devices such as microcontrollers, DACs, ADCs and other. Although there is no single standard for synchronous serial bus, there are industry accepted guidelines based on two most popular implementations:

- SPI (a trademark of Motorola Semiconductor)
- Microwire/Plus (a trademark of National Semiconductor)

Many IC manufacturers produce components that are compatible with SPI and Microwire/Plus.

This core is compatible with both upper mentioned protocols as master with some additional functionality. At the hosts side the core acts like WISHBONE compliant slave device.

Features:

- **Full duplex synchronous serial data transfer**
- **Variable length of transfer word up to 32 bits**
- **MSB or LSB first data transfer**
- **Rx and Tx on both rising or falling edge of serial clock independently**
- **8 slave select lines**
- **Fully static synchronous design with one clock domain**
- **Technology independent Verilog**
- **Fully synthesizable**

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IO ports

2.1 WISHBONE interface signals

Port	Width	Direction	Description
wb_clk_i	1	Input	Master clock
wb_rst_i	1	Input	Synchronous reset, active high
wb_adr_i	5	Input	Lower address bits
wb_dat_i	32	Input	Data towards the core
wb_dat_o	32	Output	Data from the core
wb_sel_i	4	Input	Byte select signals
wb_we_i	1	Input	Write enable input
wb_stb_i	1	Input	Strobe signal/Core select input
wb_cyc_i	1	Input	Valid bus cycle input
wb_ack_o	1	Output	Bus cycle acknowledge output
wb_err_o	1	Output	Bus cycle error output
wb_int_o	1	Output	Interrupt signal output

All output WISHBONE signals are registered and driven on rising edge of wb_clk_i.
All input WISHBONE signals are latched on rising edge of wb_clk_i.

2.2 SPI external connections

Port	Width	Direction	Description
/ss_pad_o	8	Output	Slave select output signals
sclk_pad_o	1	Output	Serial clock output
mosi_pad_o	1	Output	Master out slave in data signal output
miso_pad_i	1	Input	Master in slave out data signal input

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Registers

3.1 Core Registers list

Name	Address	Width	Access	Description
Rx	0x00	32	R	Data receive register
Tx	0x00	32	R/W	Data transmit register
CTRL	0x04	32	R/W	Control and status register
DIVIDER	0x08	32	R/W	Clock divider register
SS	0x0c	32	R/W	Slave select register

All registers are 32-bit wide accessible only with 32-bit access (all wb_sel_i signals must be active).

3.2 Data receive register [Rx]

Bit #	31:0
Access	R
Name	Rx

Reset Value: 0x00000000

Rx

Data receive register holds the value of received data of the last executed transfer. Valid bits depend on character length field in CTRL register (i.e. if CTRL[7:3] is set to 0x08, bits Rx[7:0] holds received data).

NOTE:
Data received register is read only register. Write to this register will actually modify transmit register as this two registers shares the same FFs.

3.3 Data transmit register [Tx]

Bit #	31:0
Access	R/W
Name	Tx

Reset Value: 0x00000000

Tx

Data receive register holds the data to be transmitted in next transfer. Valid bits depend on character length field in CTRL register (i.e. if CTRL[7:3] is set to 0x08, the Rx[7:0] holds the received data).

3.4 Control and status register [CTRL]

Bit #	31:10	9	8	7:3	2	1	0
Access	R	R/W	R/W	R/W	R/W	R/W	R/W
Name	Reserved	IE	LSB	CHAR_LEN	Tx_NEG	Rx_NEG	GO_BSY

Reset Value: 0x00000000

IE
If this bit is set, interrupt output is set active after transfer is finished. Interrupt signal is deasserted after read or write to any register.

LSB
If this bit is set LSB is send first on the line (bit Tx[0]) and first bit received from the line will be put in LSB position in Rx register (bit Rx[0]). If this bit is cleared, MSB is transmitted/ received first (which bit in Tx/Rx register is that, depends on CHAR_LEN field in CTRL register).

CHAR_LEN
This field specifies how many bits are transmitted in one transfer. Up to 32 bits can be transmitted.
CHAR_LEN = 0x01 … 1 bit
CHAR_LEN = 0x02 … 2 bits
…
CHAR_LEN = 0x1f … 31 bits
CHAR_LEN = 0x00 … 32 bits

Tx_NEG
If this bit is set, mosi_pad_o signal is changed on falling edge of sclk_pad_o clock signal, otherwise mosi_pad_o signal is changed on rising edge of sclk_pad_o.

Rx_NEG
If this bit is set, miso_pad_i signal is latched on falling edge of sclk_pad_o clock signal, otherwise miso_pad_i signal is latched on rising edge of sclk_pad_o.

GO_BSY
Writing 1 to this bit starts the transfer. This bit remains set during the transfer and is automatically cleared after transfer is finished. Writing 0 to this bit has no effect.

NOTE:
All registers including CTRL register should be set before writing 1 to GO_BSY bit in CTRL register. When changing configuration in CTRL register, this has to be done with GO_BSY bit cleared (this means that two writes to CTRL register has to be executed when changing the configuration and performing the next transfer, first with GO_BSY bit cleared and second with GO_BSY bit set to start the transfer).
When transfer is in progress writing to any register of SPI core has no effect.

3.5 Divider register [DIVIDER]

Bit #	31:16	15:0
Access	R	R/W
Name	Reserved	DIVIDER

Reset Value: 0x0000ffff

DIVIDER

The value in this field is divider of frequency of system clock wb_clk_i to generate serial clock on output sclk_pad_o. The desired frequency is obtained according to following equation:

$$f_{sclk} = \frac{f_{wb\_clk}}{(DIVIDER+1)*2}$$

3.6 Slave select register [SS]

Bit #	31:8	7:0
Access	R	R/W
Name	Reserved	SS

Reset Value: 0x00000000

SS

Writing 1 to any bit location of this field sets the proper ss_pad_o line to active state.

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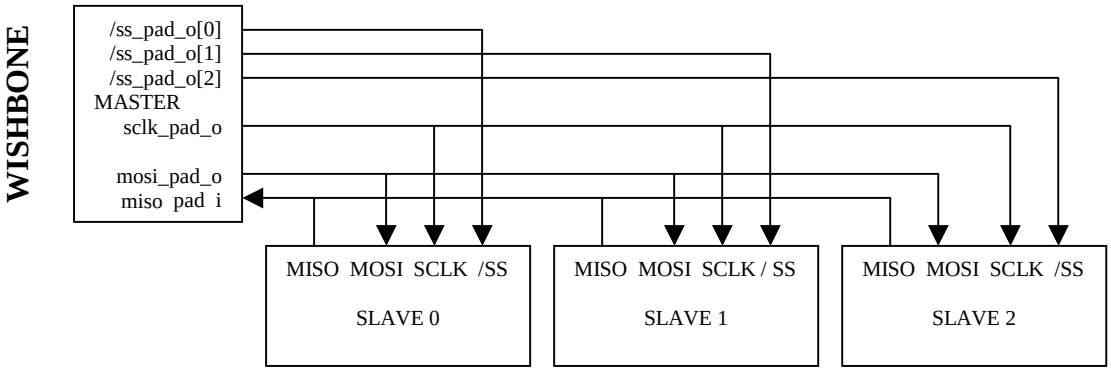
Operation

This core is SPI (Serial Peripheral Interface) and Microwire/Plus compliant synchronous serial controller. At the host side it is controlled via registers accessible trough WISHBONE rev B1 interface.



4.1 WISHBONE interface

SPI Core has four 32-bit registers trough WISHBONE rev B1 compatible interface. All accesses to SPI registers have to be 32-bit (wb_sel[3:0] = 0xf). Please refer to WISHBONE specification at:

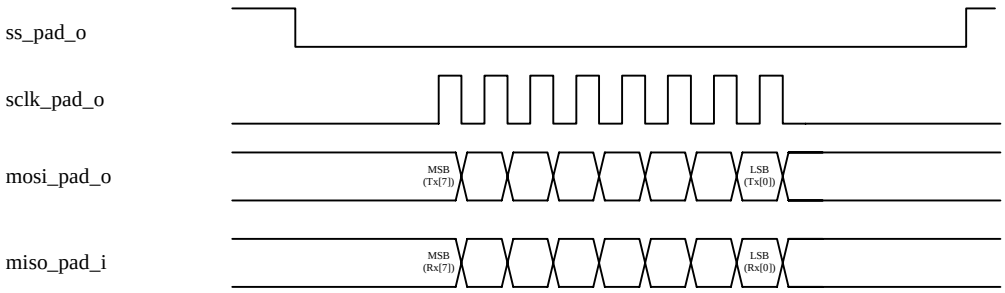
http://www.opencores.org/wishbone/specs/wbspec_b1.pdf

4.2 Serial interface

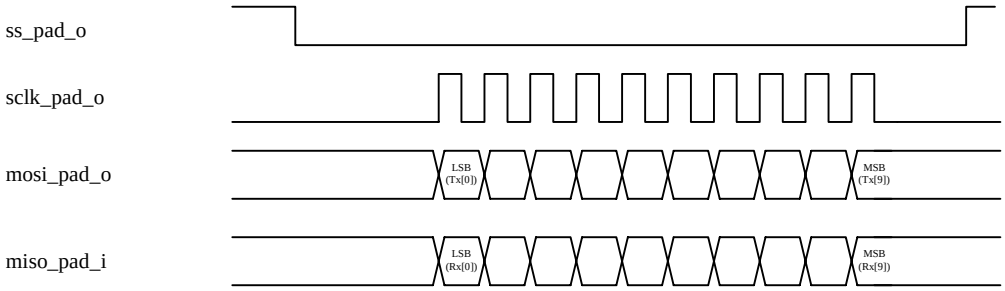
Serial interface consists of slave select lines, serial clock line and input and output data lines. All transfers are full duplex transfers of programmable number of bits per transfer (up to 32 bits).

This core has some additional functionality comparing to SPI/Microwire protocol. It can drive data to the output data line in respect to falling (SPI/Microwire compliant) or rising edge of the serial clock and it can latch data on input data line on rising (SPI/Microwire compliant) or falling edge of serial clock line. It also can transmit (receive) MSB first (SPI/Microwire compliant) or LSB bit first.

It is important to know, that Rx and Tx registers shares the same flip-flops, which means that what is received from the input data line in one transfer will be transmitted on the output data line in the next transfer, if there will be no write access executed to Tx register between the transfers.



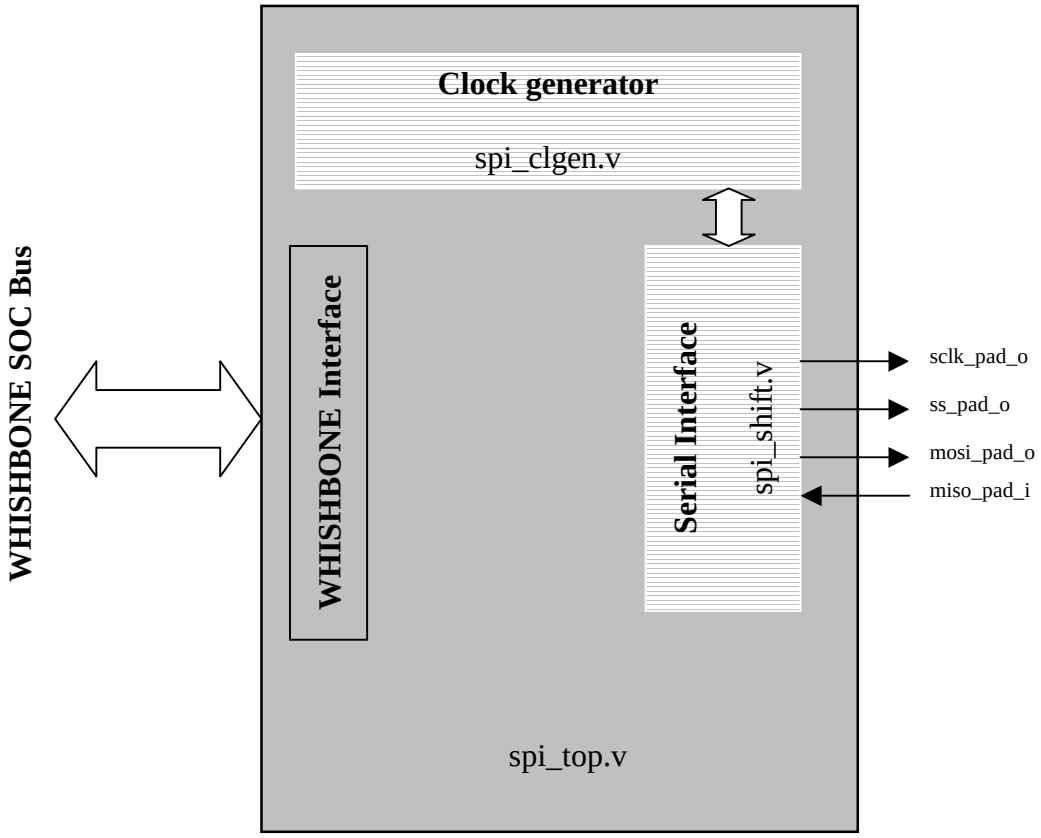
CTRL[LSB] = 0, CTRL[CHAR_LEN] = 0x08, CTRL[TX_NEG] = 1, CTRL[RX_NEG] = 0



CTRL[LSB] = 1, CTRL[CHAR_LEN] = 0x0a, CTRL[TX_NEG] = 0, CTRL[RX_NEG] = 1

5 Architecture

SPI Master Core consists of three parts shown on fallowing figure:



Appendix A

Core configuration

SPI Core can be configured to meet some system requirements and size constraints on behalf of core functionality. Core can be configured with setting appropriate define directives in spi_defines.v source file described here:

SPI_DIVIDER_BIT_NB
This parameter defines the maximum number of bits needed to for divider. Set this parameter accordingly to maximum system frequency and lowest serial clock frequency:

$$\text{SPI\_DIVIDER\_BIT\_NB} = \log_2\left[\frac{f_{sys\,\max}}{f_{sclk\,\min} * 2} - 1\right]$$

Default value is 16.

SPI_MAX_CHAR
This parameter defines the maximum number of bits that can be received/received in one transfer.
Default value is 32.

SPI_SS_NB
This parameter defines the number of slave select lines.
Default value is 8.