



- Pinout SV1
- 1 Start
 - 2 Mode
 - 3 Cfg Clock
 - 4 Cfg Data
 - 5 Done
 - 6 GND

- Pinout SV2
- 1 Cfg Data
 - 2 Done
 - 3 Cfg Clock
 - 4 Config#
 - 6 Init#
 - 7 GND
 - 8 VCC

- Pinout SV3
- 1 CS#
 - 2 DataIn
 - 3 RSV (DAT2)
 - 4 VDD
 - 5 CLK
 - 6 VSS
 - 7 DataOut
 - 8 RSV (DAT1)
 - 9 Present#
 - 10 WProt

Note: CT controls reset delay td
td = 2.1 x 10⁴ x CT

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http://www.opencores.org/projects.cgi/web/spi_boot/overview

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