TIME SLOT INTERCHANGE

DIGITAL SWITCH

256 x 256

TIME SLOT INTERCHANGE DIGITAL SWITCH IP Core   ***For XILINX SPARTAN-II/IIE series FPGA***

FEATURES:

- 256 x 256 channel non-blocking switching at 2.048 Mb/s
- Accept 8 serial data streams of 2.048 Mb/s
- Per-stream frame delay offset programming
- Connection memory block programming
- Microprocessor Interface

DESCRIPTION:

The TDM Switch core is a non-blocking digital switch that has a capacity of 256 x 256 channels at 2.048 Mb/s. Some of the main features are: Processor Mode and input offset delay.

This IP core is synthesized for XILINX SPARTAN-II series FPGA, fit at xc2s50-6tq144 device and the post place & route simulation model simulate with Cadence NC-SIM simulator. In Table 2 we can find information about project files.

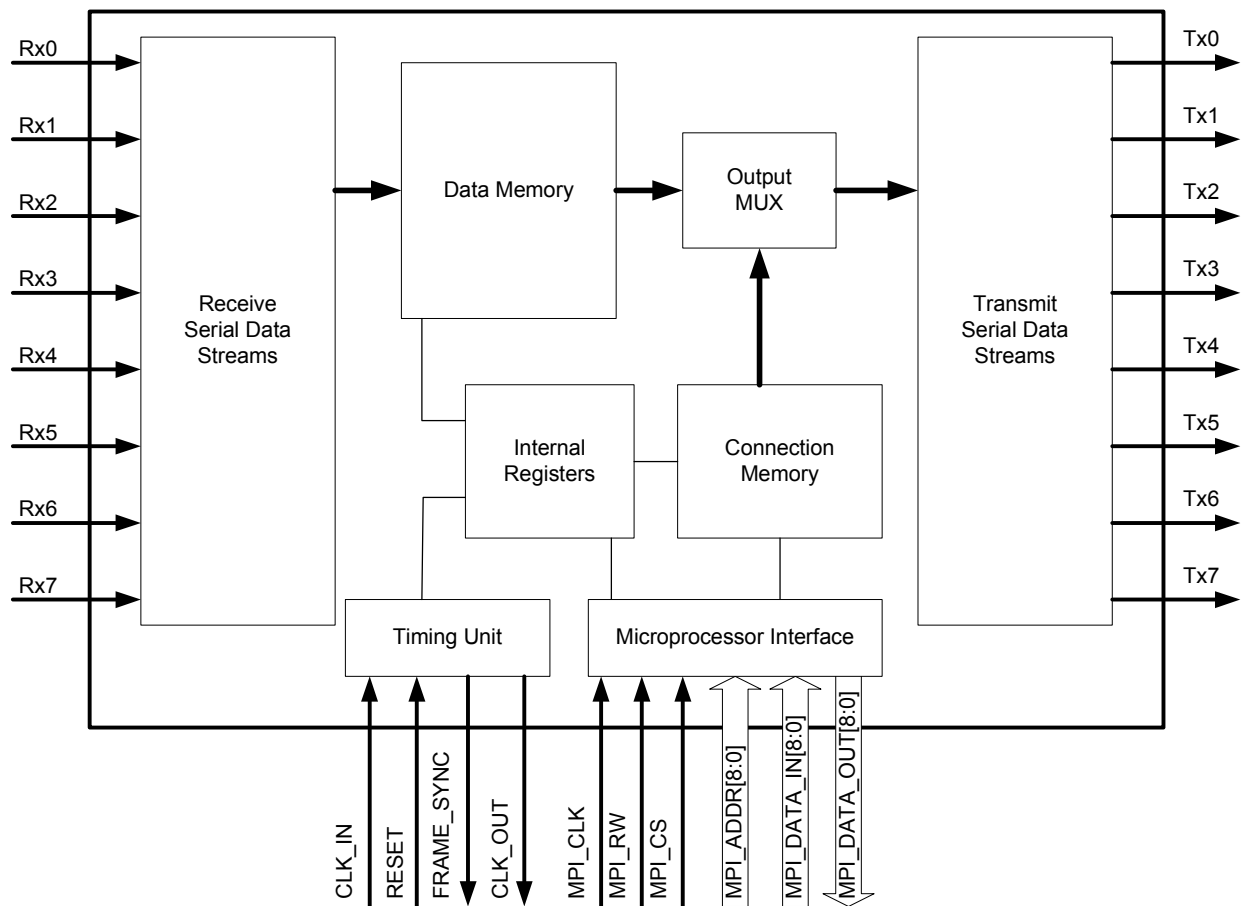The Figure 1 describe the block diagram of Time Slot Interchange Digital Switch IP core.

Figure 1. Block Diagram

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PIN DESCRIPTION

The following table is define the IP core pinout.

Table 1

SYMBOL	NAME	I/O	DESCRIPTION
Tx0-Tx7	*TX Output 0 to7*	**O**	Serial data output stream. These streams have a data rate of 2.048 Mb/s.
Rx0-Rx7	*RX Input 0 to7*	**I**	Serial data input stream. These streams have a data rate of 2.048 Mb/s.
CLK_IN	*Input Clock*	**I**	Serial clock for generation internal sync pulses. This input accepts a 4.096 MHz clock.
CLK_OUT	*Output Clock*	**O**	Serial clock for shifting data in/out on the serial streams (RX/TX 0-7). This output generate 2.048 MHz clock.
FRAME_SYNC	*Frame Sync. Signal*	**O**	Frame sync output. This output generate 8 kHz (125 us) frame pulses.
RESET	*Device Reset*	**I**	This input (active LOW) puts the device in its reset state that clears the device internal counters, registers. The time constant for a power up reset circuit must be a minimum of five times the rise time of the power supply. In normal operation, the RESET pin must be held LOW for a minimum of 100ns to reset the device.
MPI_CLK	*Memory clock*	**I**	Microprocessor interface input clock. To internal connection memory and control registers accessed with positive edge of MPI_CLK
MPI_RW	*Read/Write*	**I**	Microprocessor interface Read/Write input. The logic "1" is Read, "0" is Write.
MPI_CS	*Enable*	**I**	Microprocessor interface Chip Select input. The logic "1" define access to this chip.
MPI_ADDR	*Address [8-0]*	**I**	These lines provide the A8-A0 address lines to the internal memories.
MPI_DATA_IN	*Data Input [8:0]*	**I**	These lines provide the D8-D0 data input lines to the internal memories.
MPI_DATA_OUT	*Data Output [8:0]*	**O**	These lines provide the D8-D0 data output lines to the internal memories.

MEMORY MAP

The IP core consist of two memory **DATA** and **CONNECTION**. The data memory consist two banks of memories. In first frame the data from input streams are stored in the data memory **Bank 1**. At this time the data from data memory **Bank 2** are transmitted to output streams. In second frame the data memory banks are swap around.
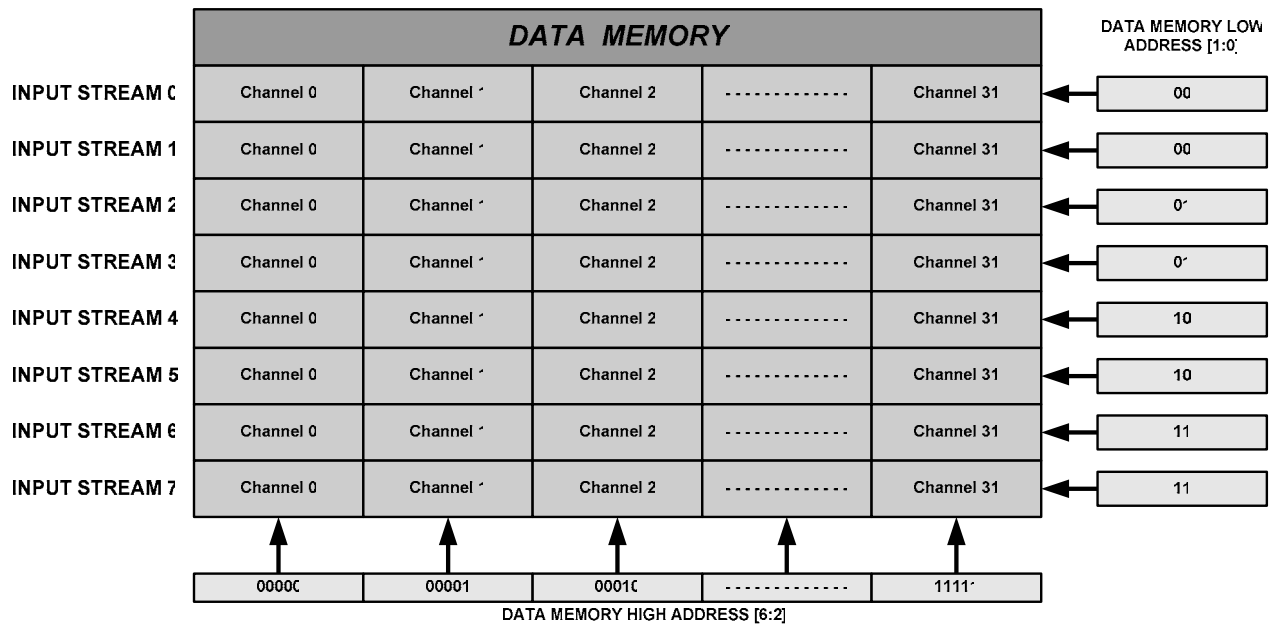
Figure 2. Data Memory Bank Map

The **CONNECTION** memory loaded from microprocessor interface (**MPI**) and consist information about connection between data memory and output streams.
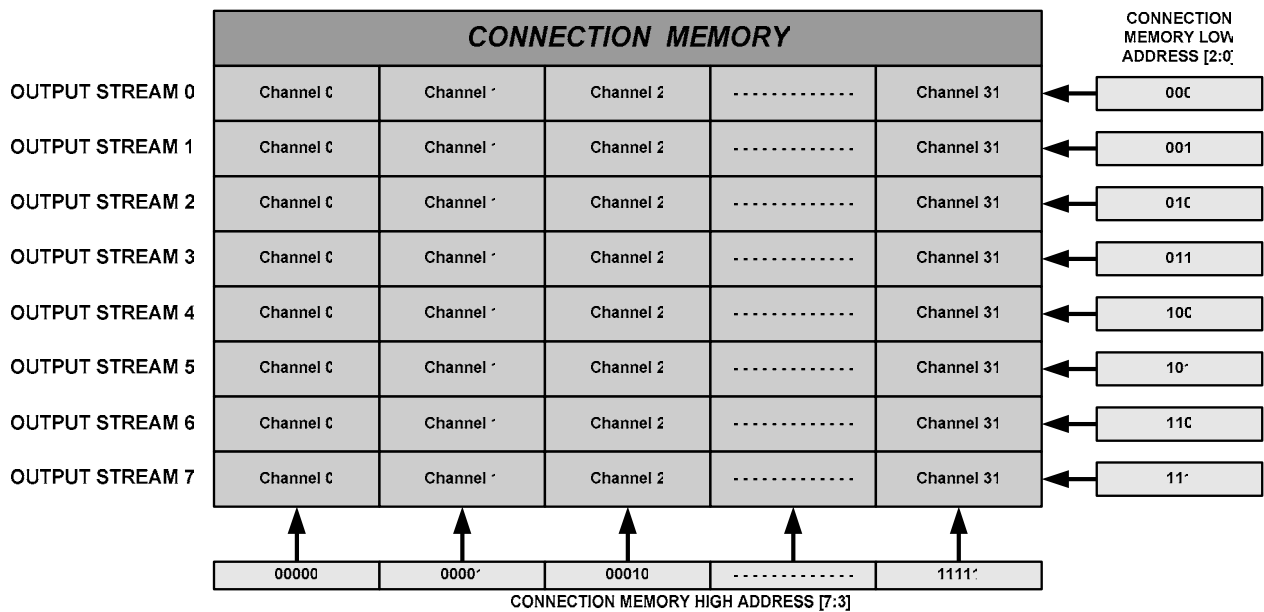
Figure 3. Connection Memory Map

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FRAME DELAY REGISTERS also loaded from MPI. This registers are responsible to frame delay for each input stream correspondingly.

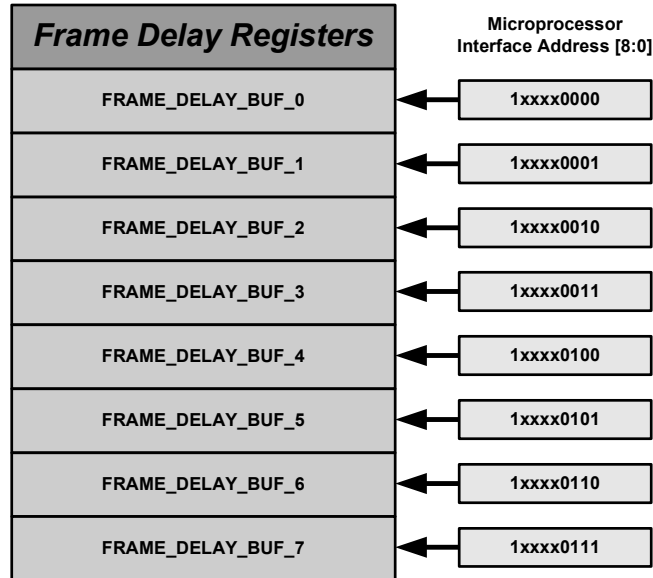| Frame Delay Registers	Microprocessor Interface Address [8:0]
FRAME_DELAY_BUF_0	1xxxx0000
FRAME_DELAY_BUF_1	1xxxx0001
FRAME_DELAY_BUF_2	1xxxx0010
FRAME_DELAY_BUF_3	1xxxx0011
FRAME_DELAY_BUF_4	1xxxx0100
FRAME_DELAY_BUF_5	1xxxx0101
FRAME_DELAY_BUF_6	1xxxx0110
FRAME_DELAY_BUF_7	1xxxx0111

Figure 4. Frame Delay Registers Map

The Time Slot Interchange Digital Switch IP core files

Table 2

NAME	DESCRIPTION
TDM_Switch_DS.pdf	Data Sheet file
tdm_switch_top.v	Top module of Time Slot Interchange Digital Switch
tdm_switch_b.v	Top module of TDM Switch for behavioral simulation
tdm_switch_top_timesim.v	Post Place and Route Verilog netlist file created by Xilinx ISE 5.2i for Concept NC-Verilog simulator
tdm_switch_top_timesim.sdf	SDF annotation file for "tdm_switch_top_timesim.v" netlist
testbench_top.v	Testbench for top module
map.dat	Data file for connection memory (line 1-256) and frame delay registers (line 257-264)
stream_0.dat	Data for input stream 0
stream_1.dat	Data for input stream 1
stream_2.dat	Data for input stream 2
stream_3.dat	Data for input stream 3
stream_4.dat	Data for input stream 4
stream_5.dat	Data for input stream 5
stream_6.dat	Data for input stream 6
stream_7.dat	Data for input stream 7
sim_result.dat	Simulation result file created by testbench "testbench_top.v"