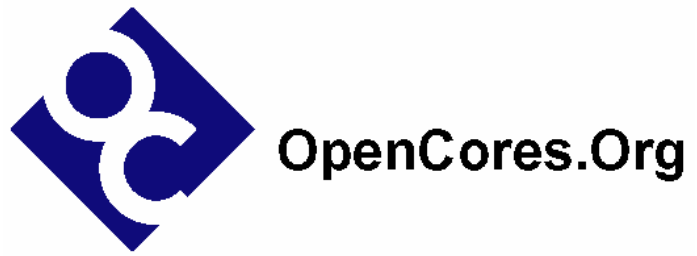

Ultimate CRC Specification

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Revision History

Rev.	Date	Author	Description
1.0	08/05/05	Geir Drange	Specification, first version

Contents

1

Introduction

Ultimate CRC is a fully customable Cyclic Redundancy Check (CRC) generator/checker. CRC's are widely used for data communication error checking.

2

Architecture

The Ultimate CRC uses a XOR logic tree to compute the CRC from a data input word. The XOR logic is generated during synthesis from generics that specify the properties of the CRC.

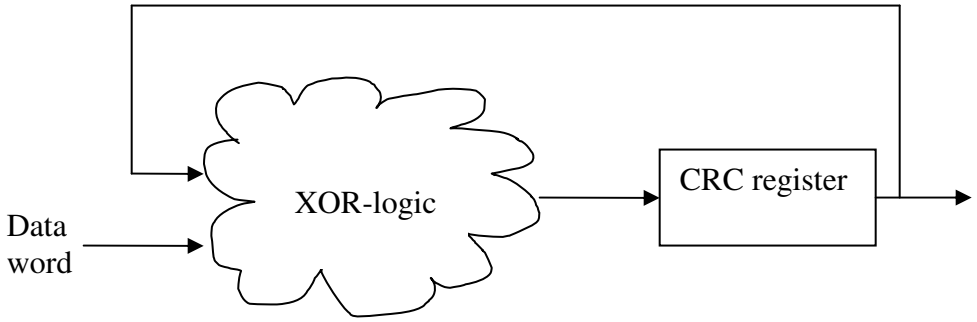

Figure 1: Ultimate CRC architecture

The core uses one clock cycle per data word. The core has two implementations, one for serial data and one for parallel data, but functionally they are identical. CRC generation and checking are basically identical operations. If the CRC is clocked into the core after the data, the CRC register will be all zeros when no errors exist.

The serial implementation has a flush control signal that allows the calculated CRC to be shifted out bit by bit, MSB first.

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3

Operation

This chapter contains timing diagrams for the operation of the core.

3.1 Serial implementation

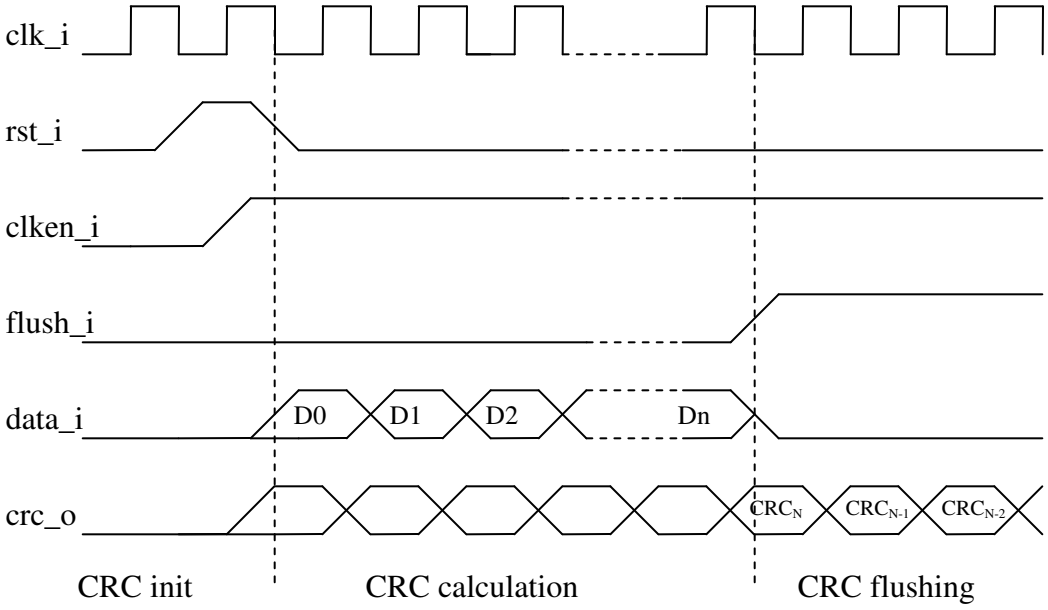

Figure 2: Serial implementation timing diagram

3.2 Parallel implementation

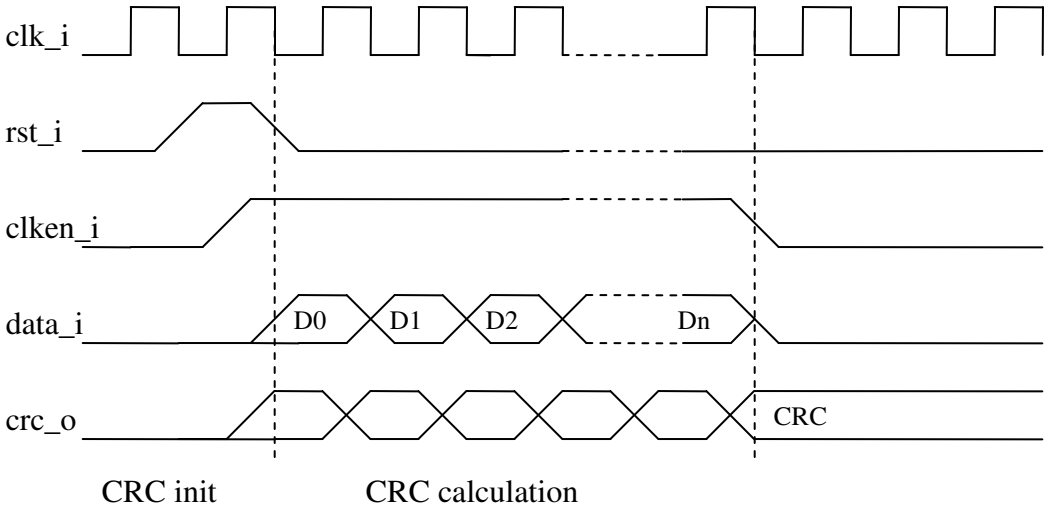

Figure 2: Parallel implementation timing diagram

4

Generics

The Ultimate CRC uses generics to define operation of the CRC..

4.1 Generics

Name	Type	Range	Description
POLYNOMIAL	slv	4-32bits	CRC polynomial. See description below.
INIT_VALUE	slv	4-32bits	Initialization value for the CRC register
DATA_WIDTH	Integer	2-256	Parallel implementation only: Defines the width of the data input vector.
SYNC_RESET	Integer	0-1	0: Use asynchronous reset 1: Use synchronous reset

Table 1: Generics for transmitter and receiver

CRC polynomials are classified by their highest non-zero digit (or place) which is termed the degree of the polynomial. For example, CRC-16 is of degree 16, which means that bits 16 through 0 are significant in their description; a degree 16 polynomial thus has 17 bits. In our case we are concerned only with the remainder of the CRC operation, which has one bit less than the polynomial itself.

CRC-16 is defined as: $x^{16}+ x^{15} + x^2 +1$

POLYNOMIAL for CRC-16 is then set to: “1000000000000101”

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Clocks

The Ultimate CRC uses a single clock.

Name	Source	Rates (MHz)			Remarks	Description
		Max	Min	Resolution		
clk_i	-	-		-		CRC register clock

Table 2: List of clocks

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IO Ports

6.1 Serial implementation

File is ucrc_ser.vhd.

Port	Width	Direction	Description
rst_i	1	Input	CRC register reset.
clken_i	1	Input	Clock enable for data_i and flush_i
data_i	1	Input	Data input
flush_i	1	Input	Flush CRC register
match_o	1	Output	High when contents of CRC register is zero
crc_o	4-32	Output	CRC register output

Table 3: Signals for serial implementation

6.2 Parallel implementation

File is ucrc_par.vhd.

Port	Width	Direction	Description
rst_i	1	Input	CRC register reset.
clken_i	1	Input	Clock enable for data_i
data_i	2-256	Input	Data input
match_o	1	Output	High when contents of CRC register is zero
crc_o	4-32	Output	CRC register output

Table 4: Signals for parallel implementation