

# Active-HDL PDF Export

**version 7.2**

**Active-HDL™**  
Complete FPGA Verification Environment

**ALDEC**  
*The Design Verification Company*

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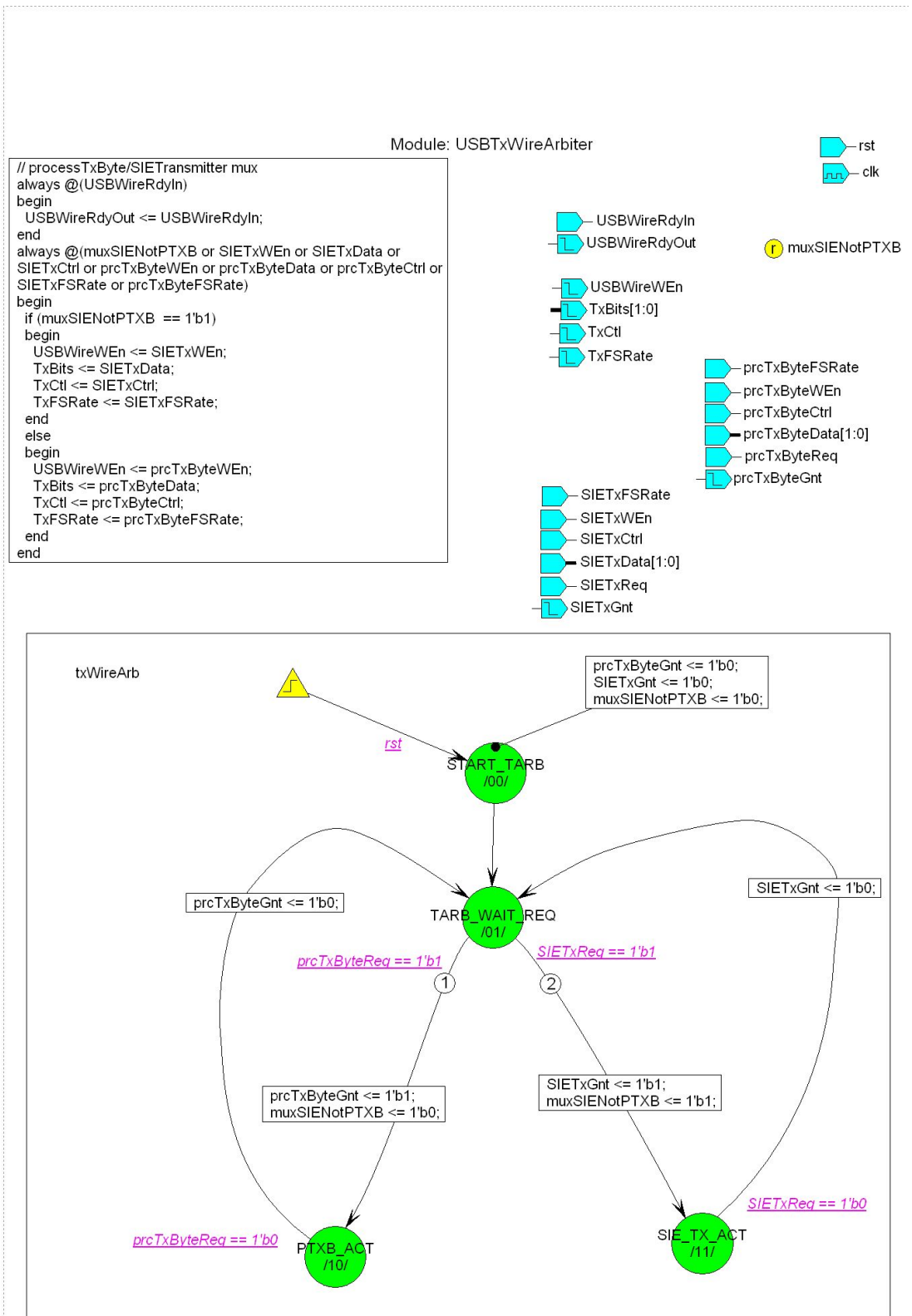
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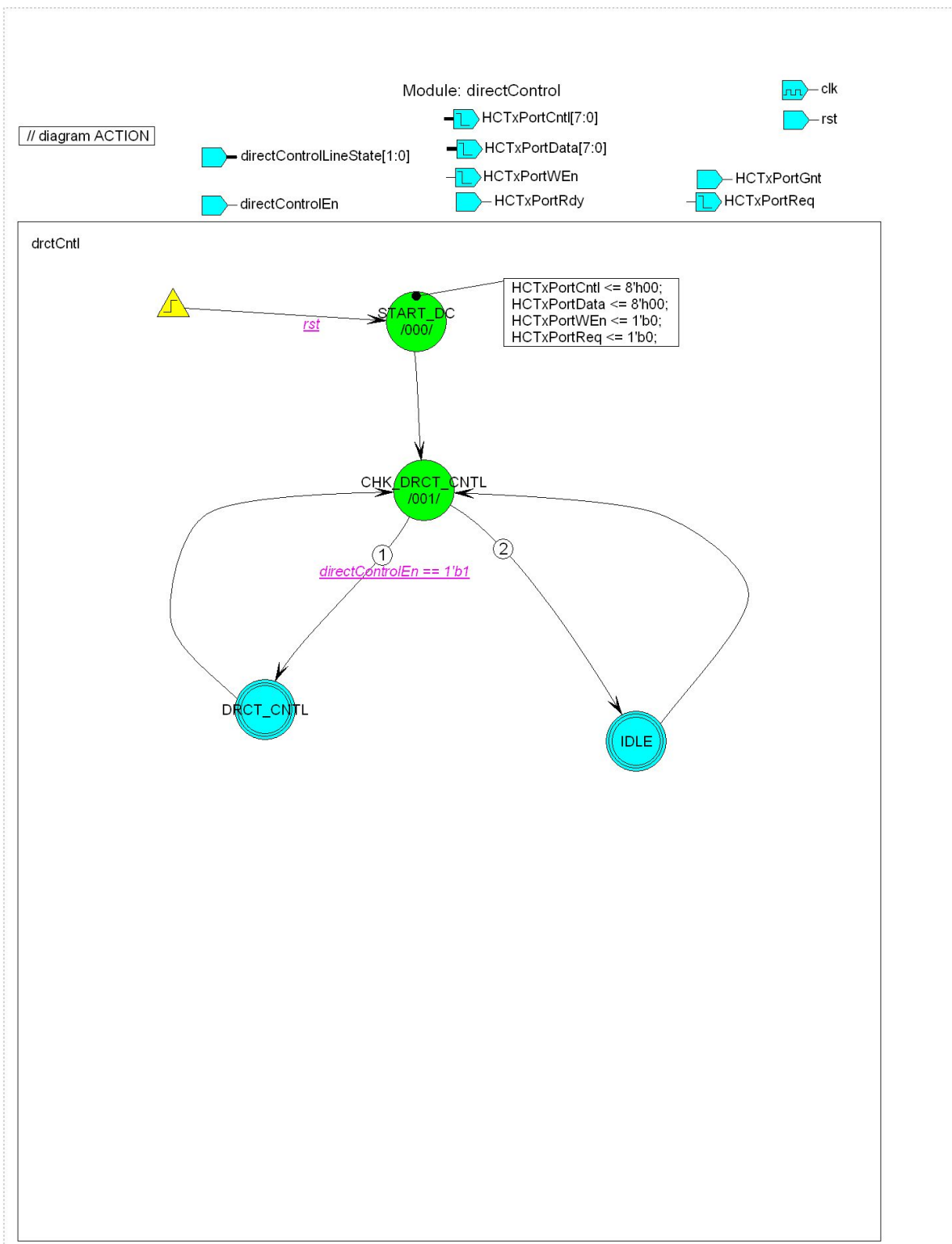
## 2 usbhostslave

### 2.1 usbTxWireArbiter.asf

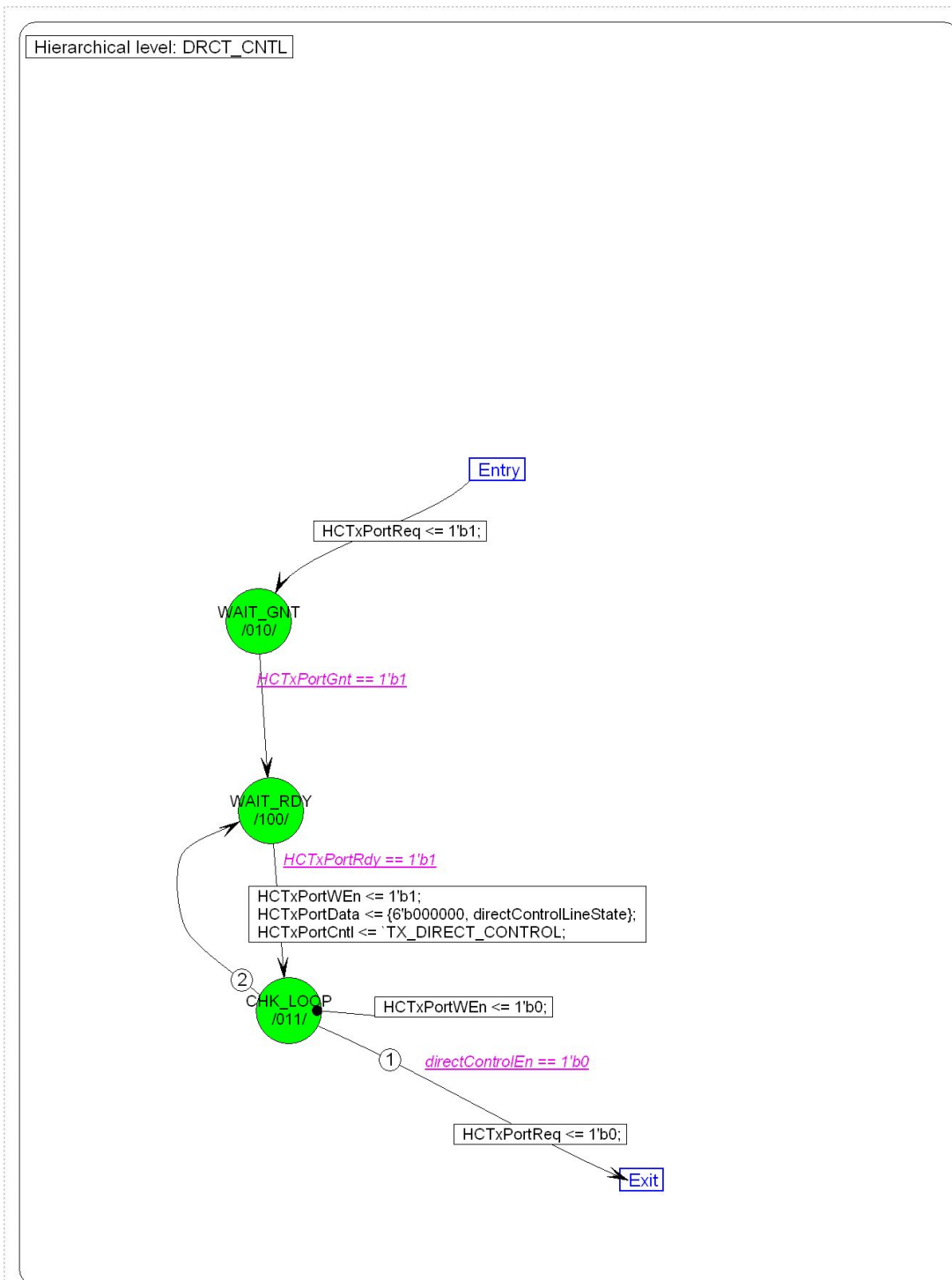




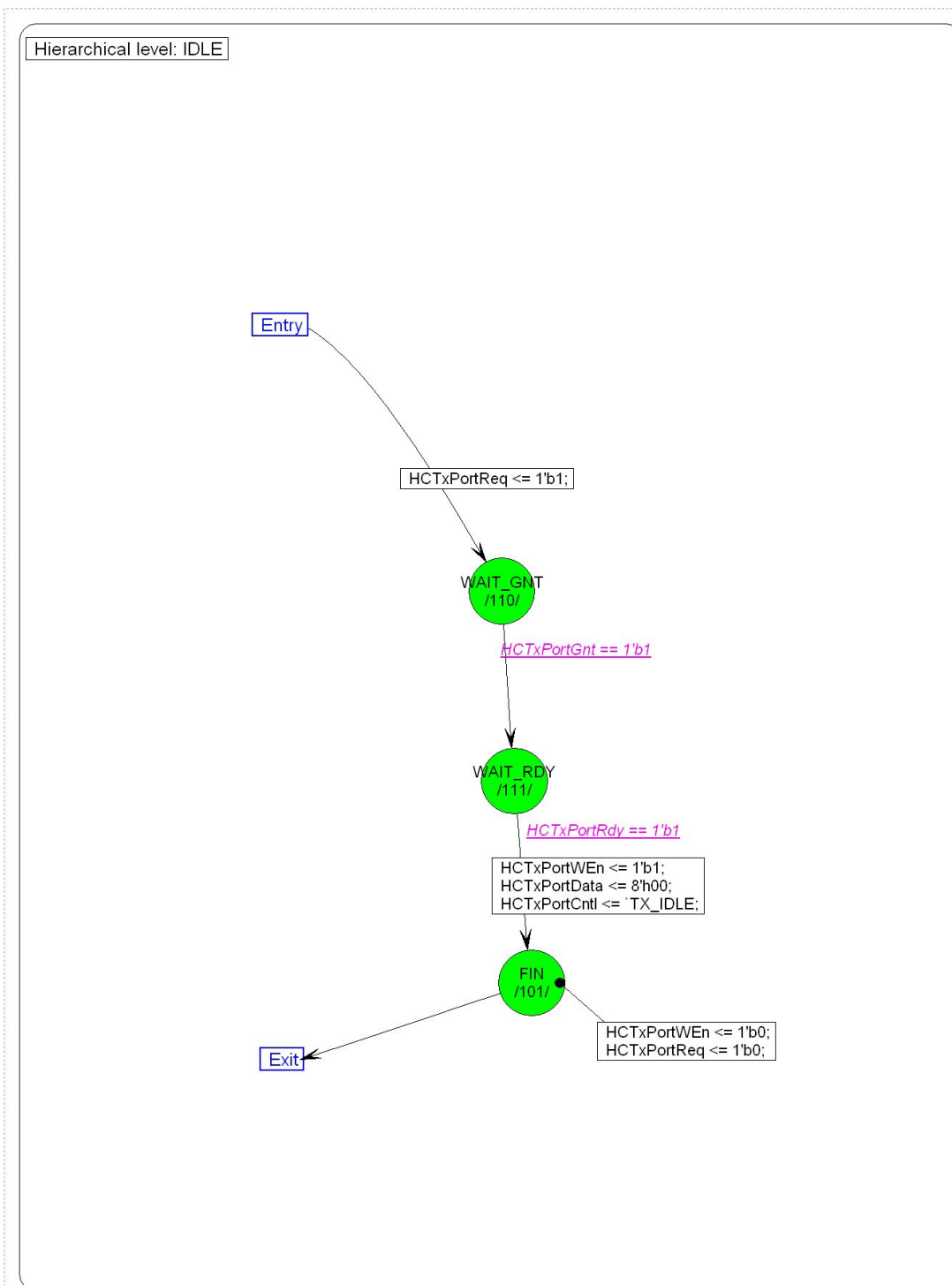
## 2.2 directcontrol.asf



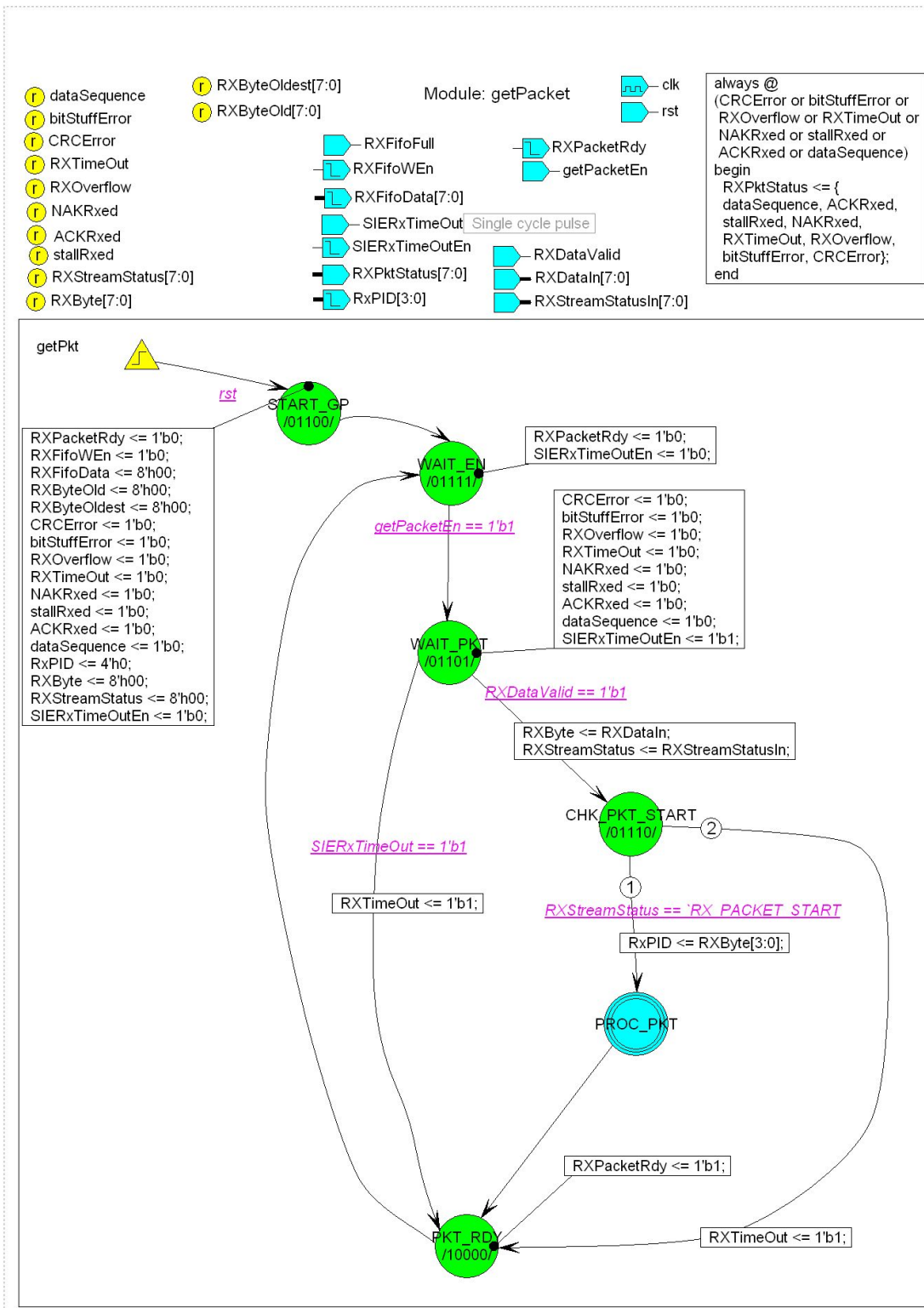
## 2.2.1 DRCT\_CNTL



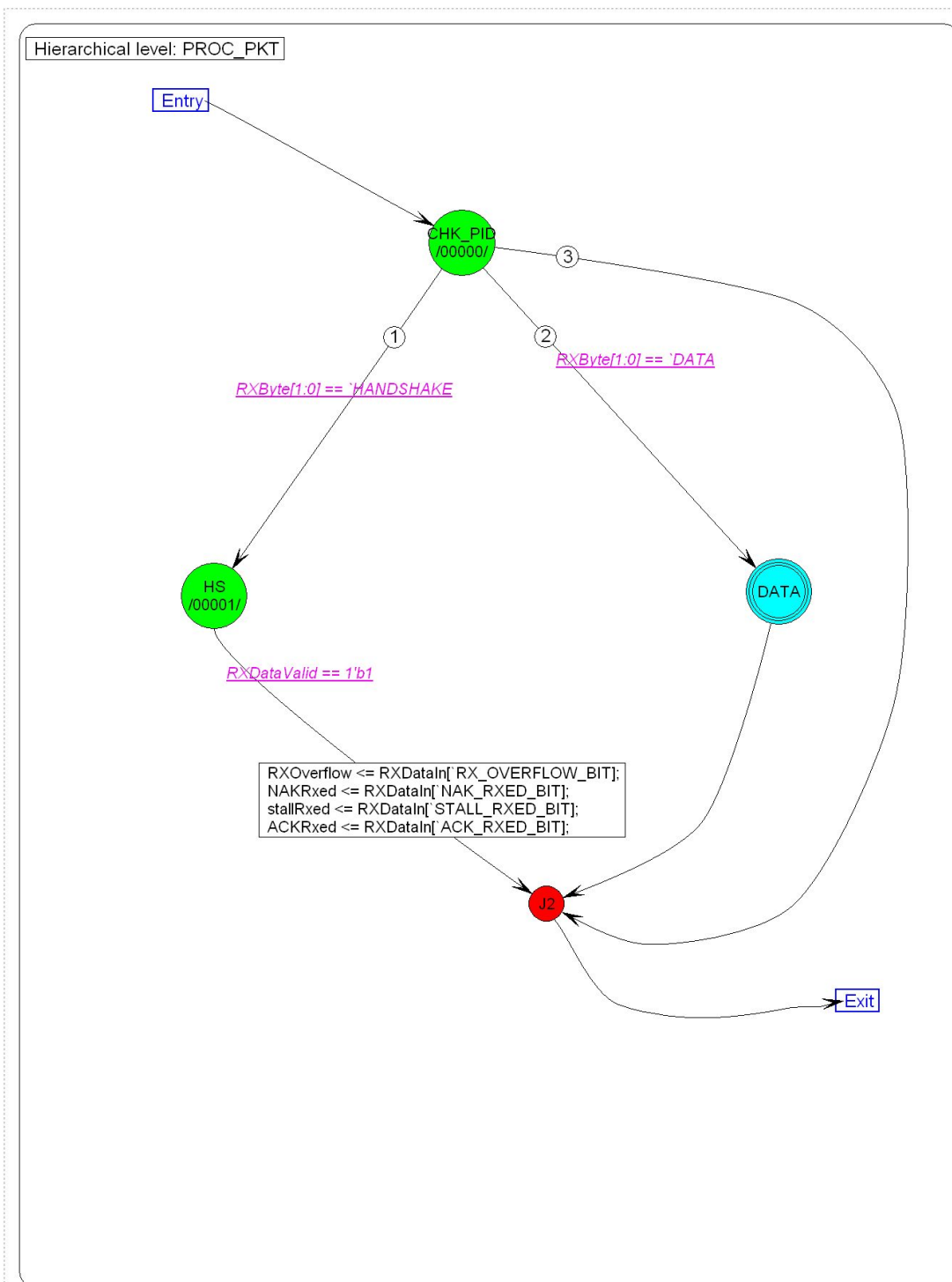
## 2.2.2 IDLE



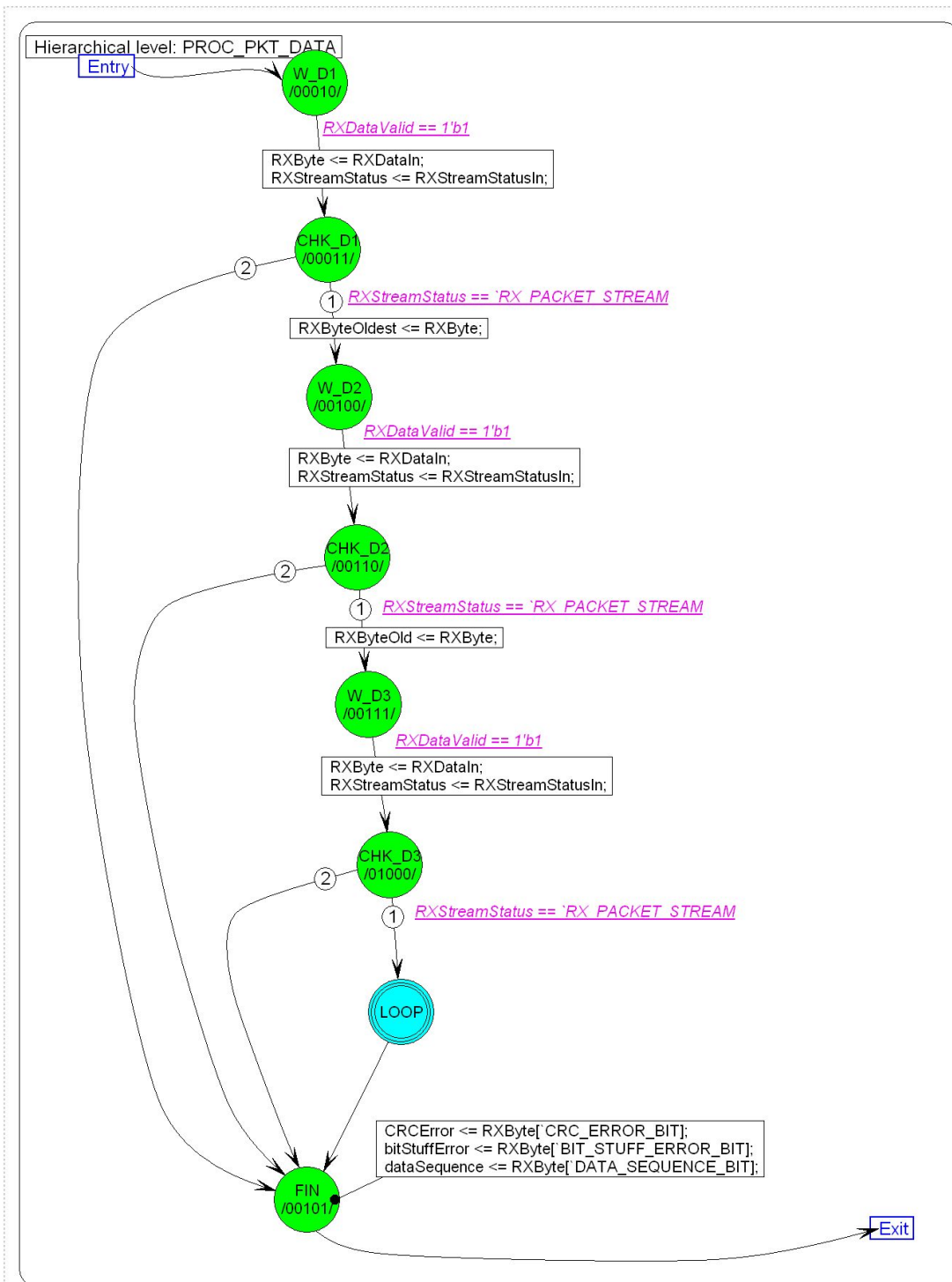
## 2.3 getpacket.asf



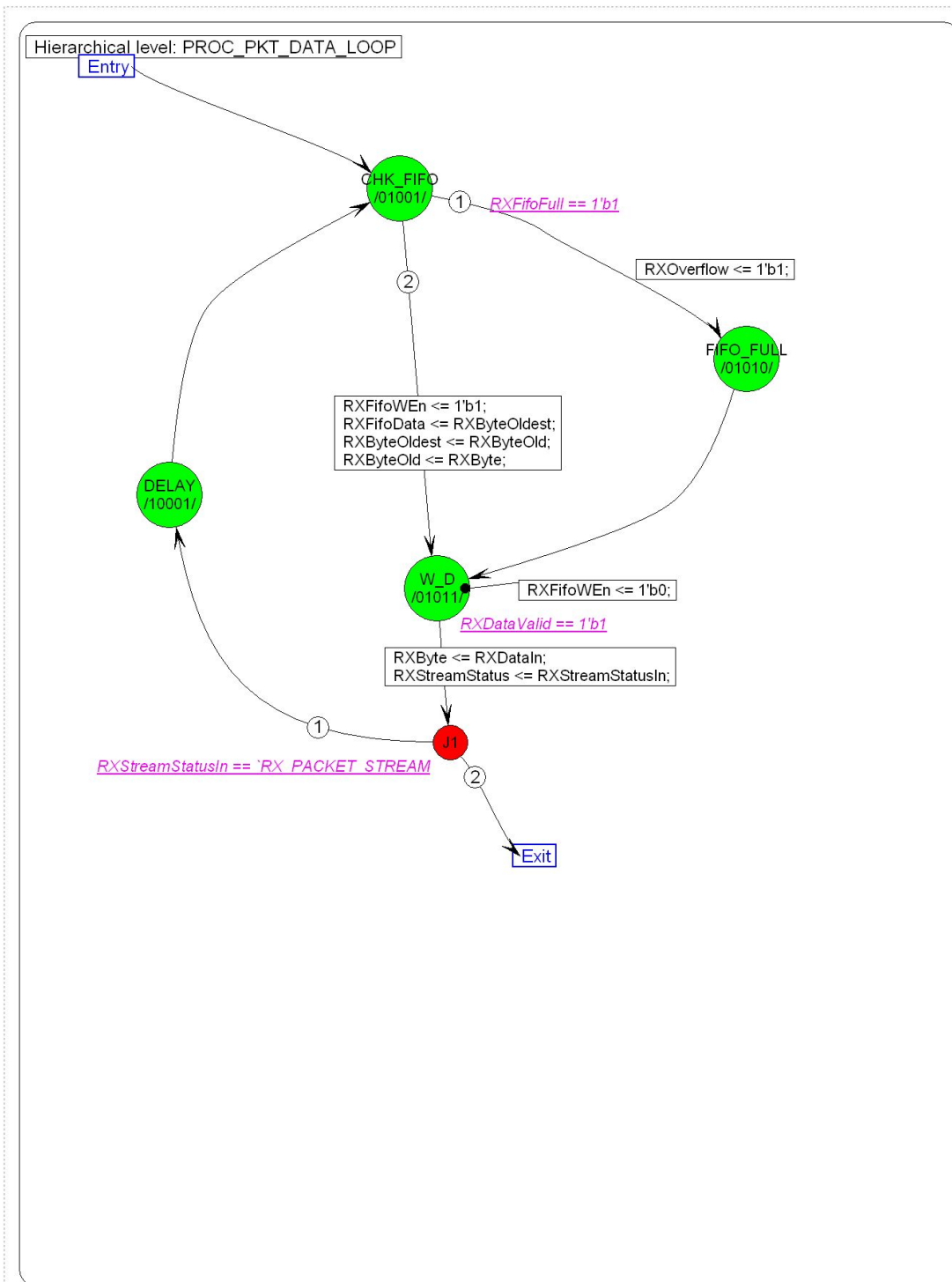
### 2.3.1 PROC\_PKT



### 2.3.1.1 DATA



### 2.3.1.1.1 LOOP



## 2.4 hctxportarbiter.asf

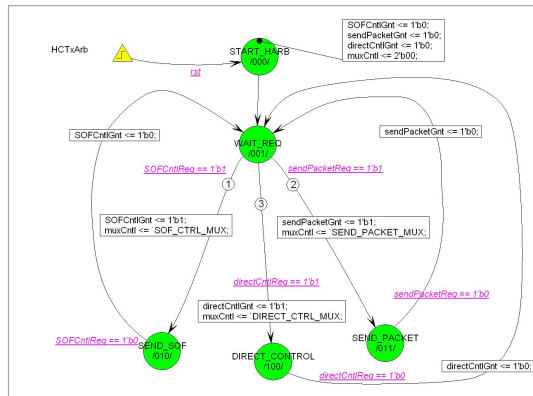
Module: HCTXPortArbiter

- SEND\_PACKET\_MUX=2b00
- SOF\_CTRL\_MUX=2b01
- DIRECT\_CTRL\_MUX=2b10
- muxCtrl[1:0]

Legend for signals:

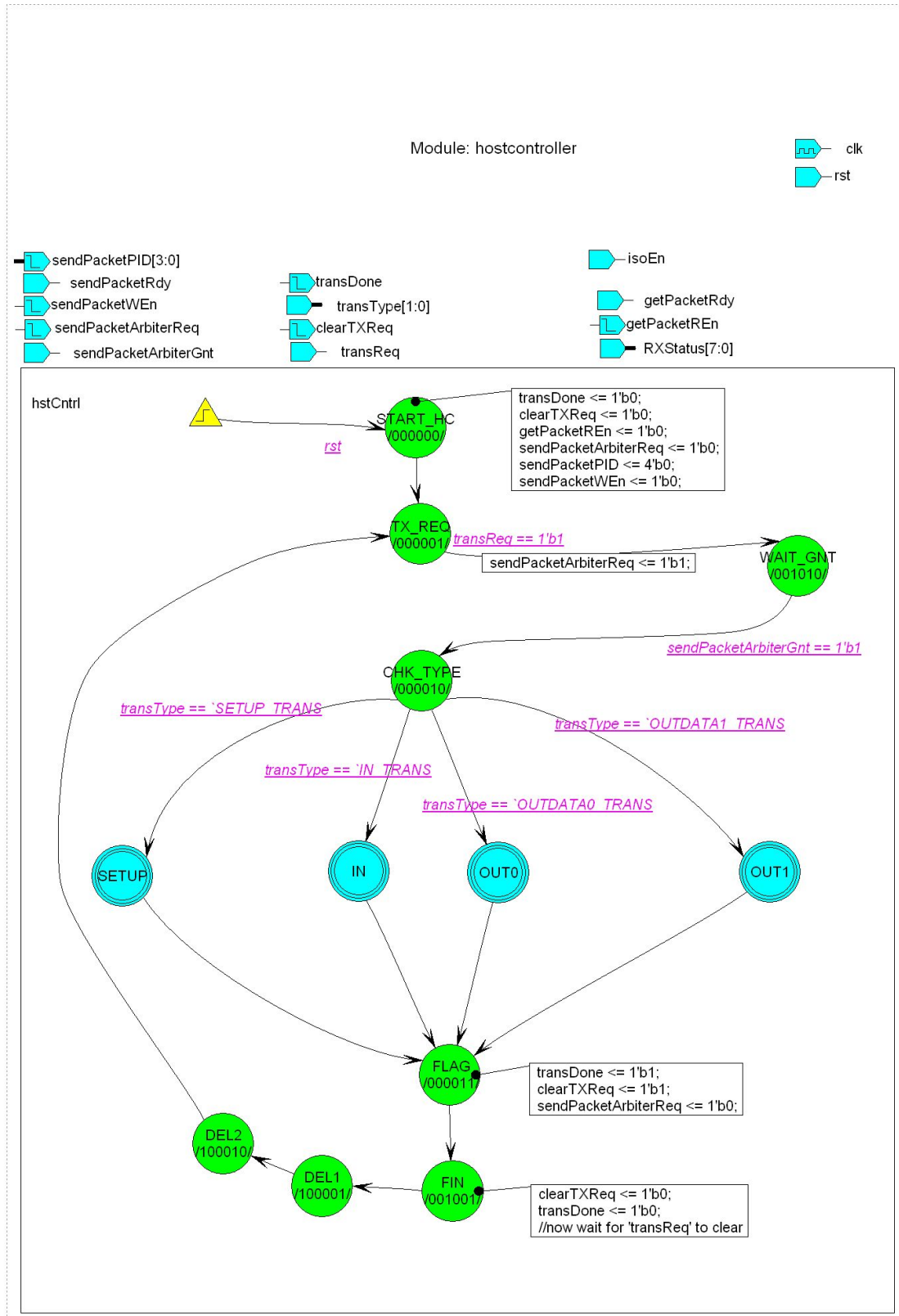
- SOFCtrlData[7:0]
- SOFCtrlCnt[7:0]
- SOFCtrlWEn
- SOFCtrlGnt
- SOFCtrlReq
- directCtrlData[7:0]
- directCtrlCnt[7:0]
- directCtrlWEn
- directCtrlGnt
- directCtrlReq
- sendPacketData[7:0]
- sendPacketCnt[7:0]
- sendPacketWEn
- sendPacketGnt
- sendPacketReq
- HCTXPortCnt[7:0]
- HCTXPortWEnable
- HCTXPortData[7:0]

```
// SOFController/directCtrl/sendPacket mux
always @(muxCtrl or SOFCtrlWEn or SOFCtrlData or SOFCtrlCnt or
directCtrlWEn or directCtrlData or directCtrlCnt or
directCtrlWEn or directCtrlData or directCtrlCnt or
sendPacketWEn or sendPacketData or sendPacketCnt)
begin
case (muxCtrl)
SOF_CTRL_MUX :
begin
HCTXPortWEnable <= SOFCtrlWEn;
HCTXPortData <= SOFCtrlData;
HCTXPortCnt <= SOFCtrlCnt;
end
DIRECT_CTRL_MUX :
begin
HCTXPortWEnable <= directCtrlWEn;
HCTXPortData <= directCtrlData;
HCTXPortCnt <= directCtrlCnt;
end
SEND_PACKET_MUX :
begin
HCTXPortWEnable <= sendPacketWEn;
HCTXPortData <= sendPacketData;
HCTXPortCnt <= sendPacketCnt;
end
default :
begin
HCTXPortWEnable <= 1'b0;
HCTXPortData <= 8'h00;
HCTXPortCnt <= 8'h00;
end
endcase
end
```

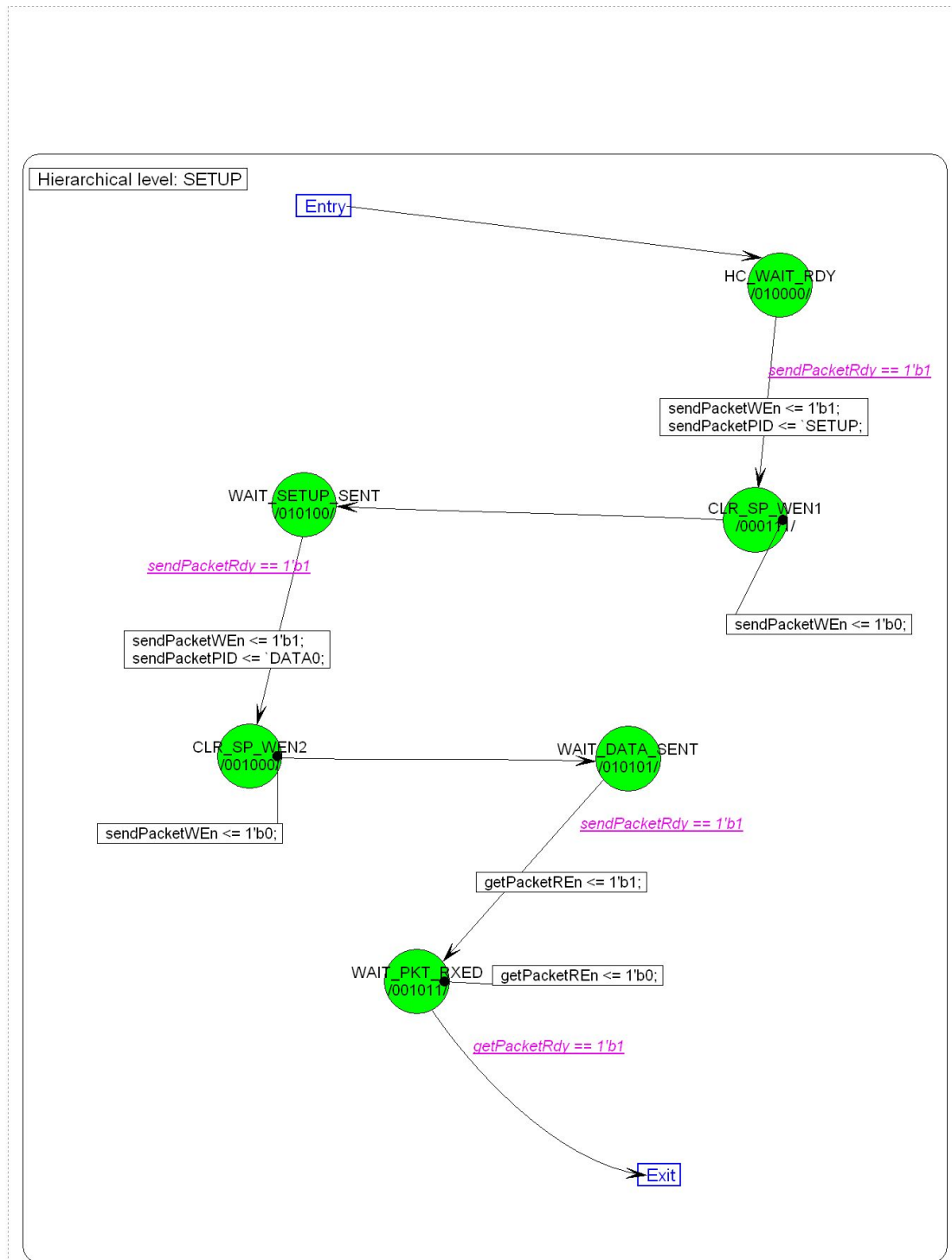




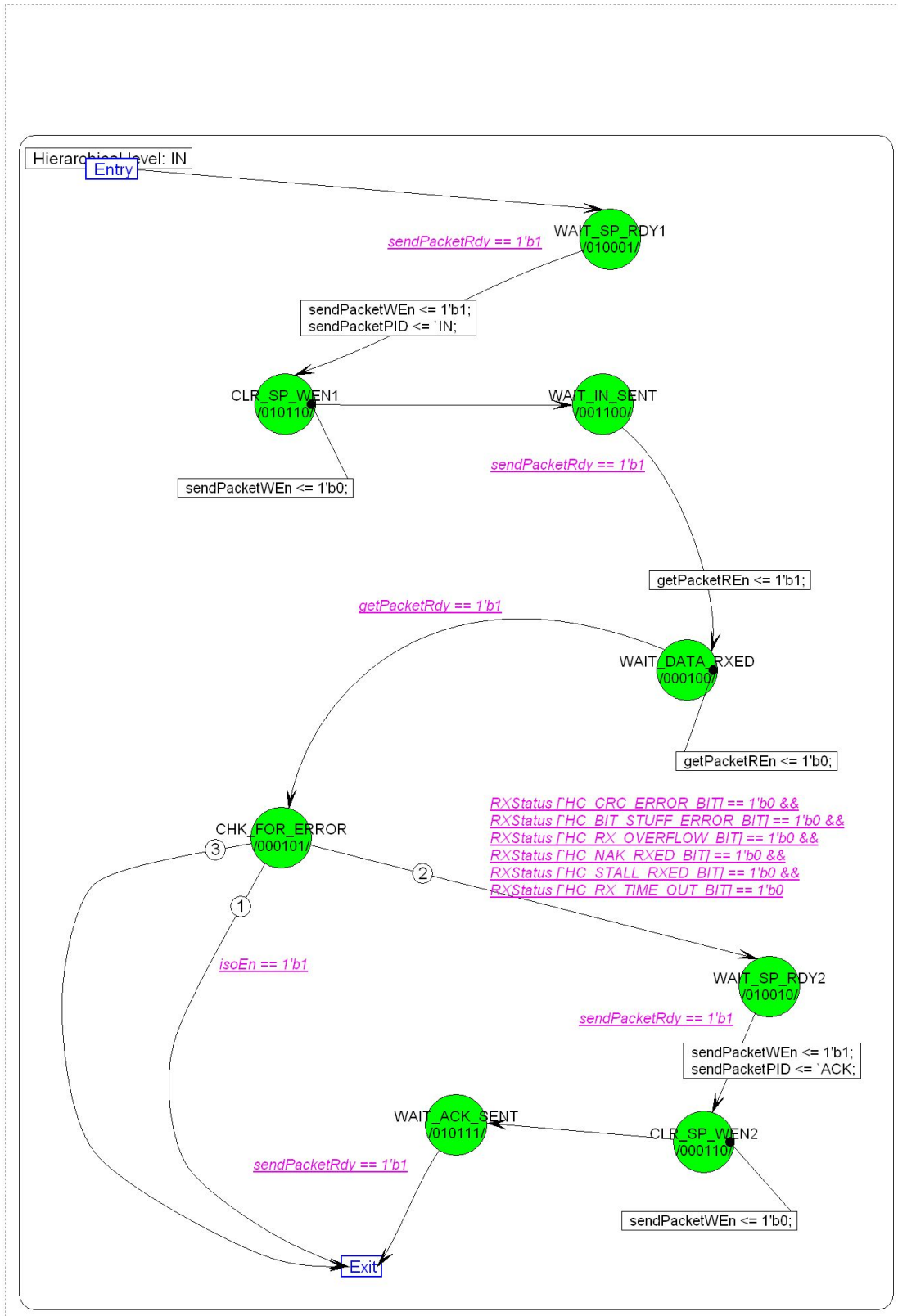
2.5 hostcontroller.asf



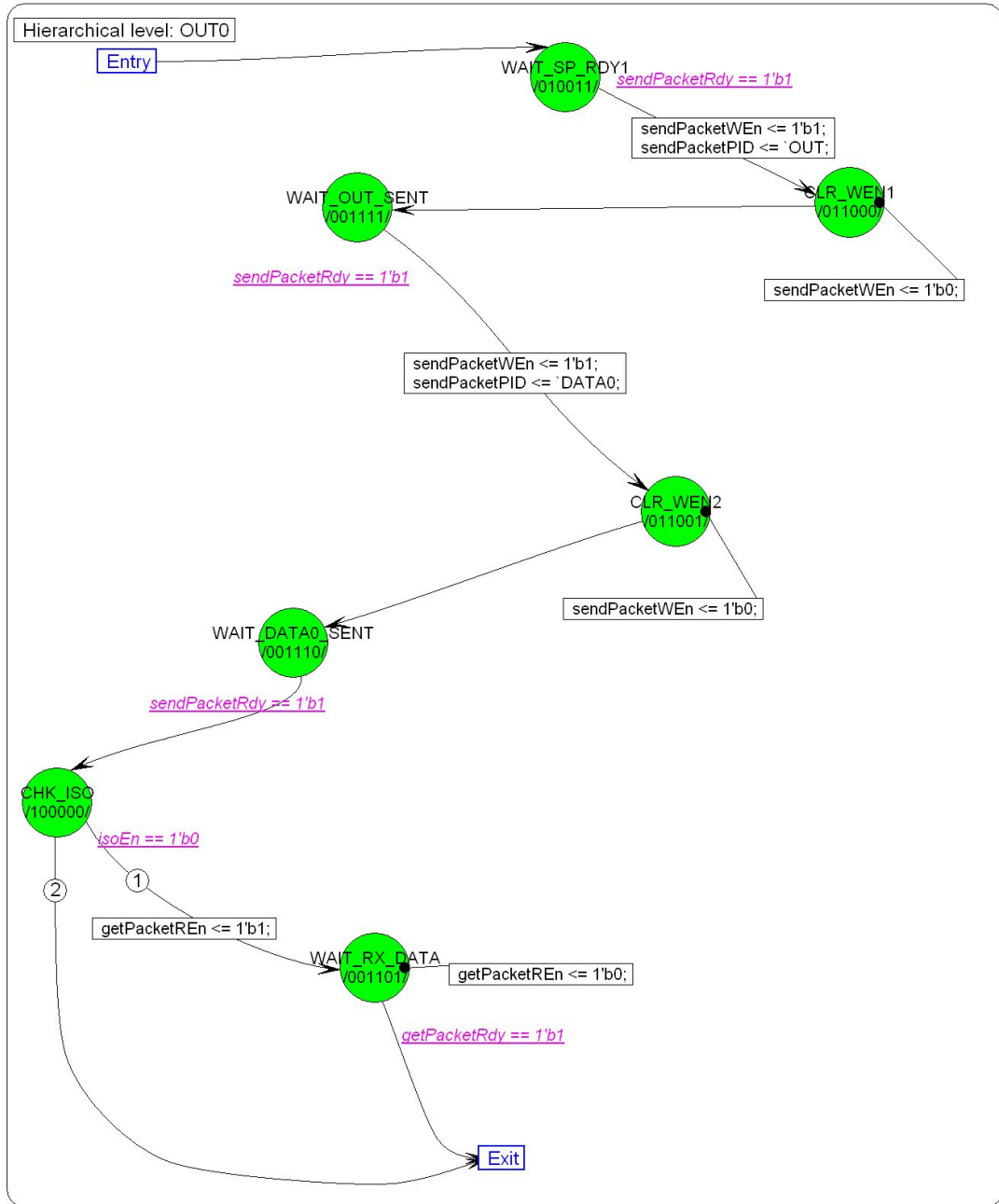
## 2.5.1 SETUP



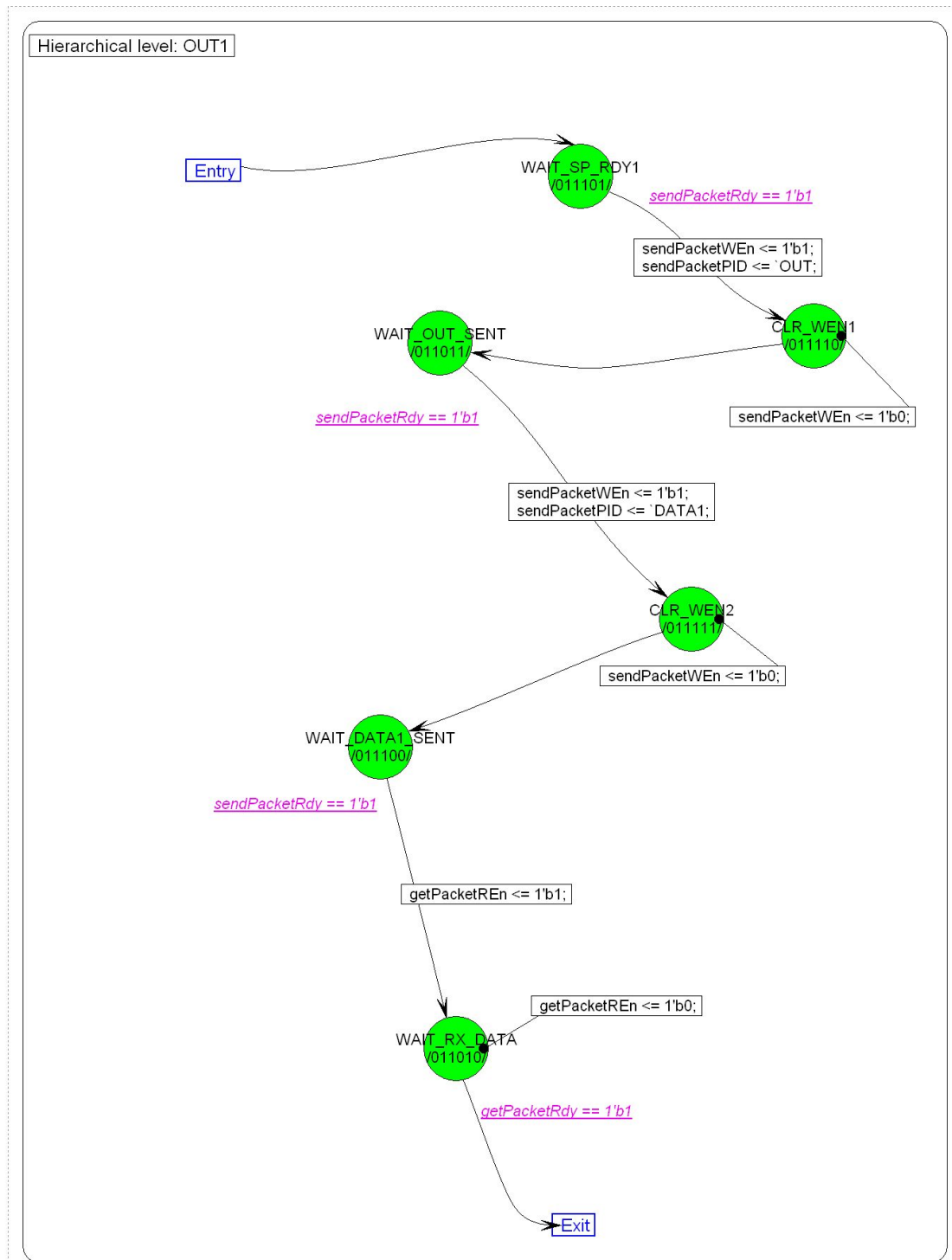
2.5.2 IN



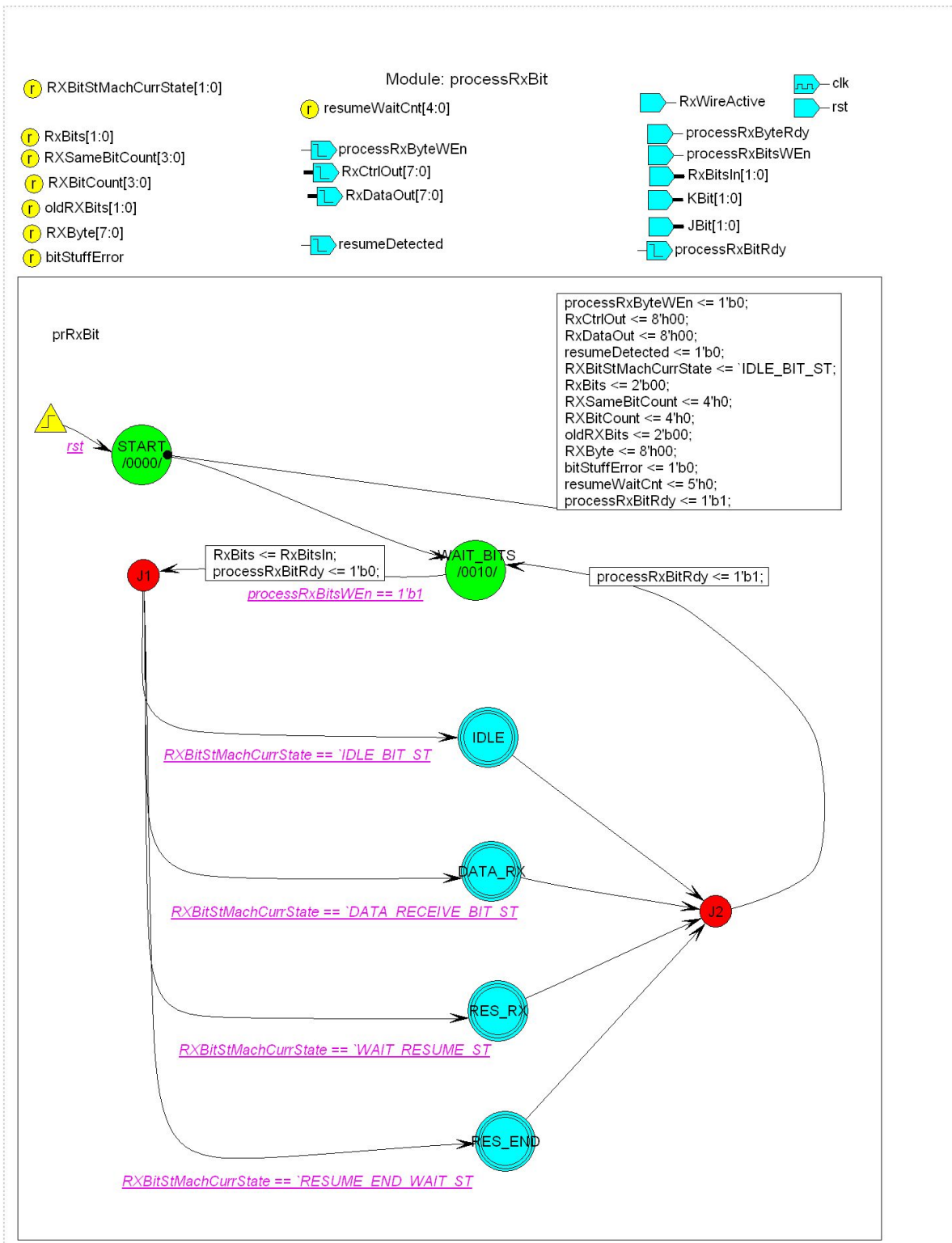
### 2.5.3 OUT0



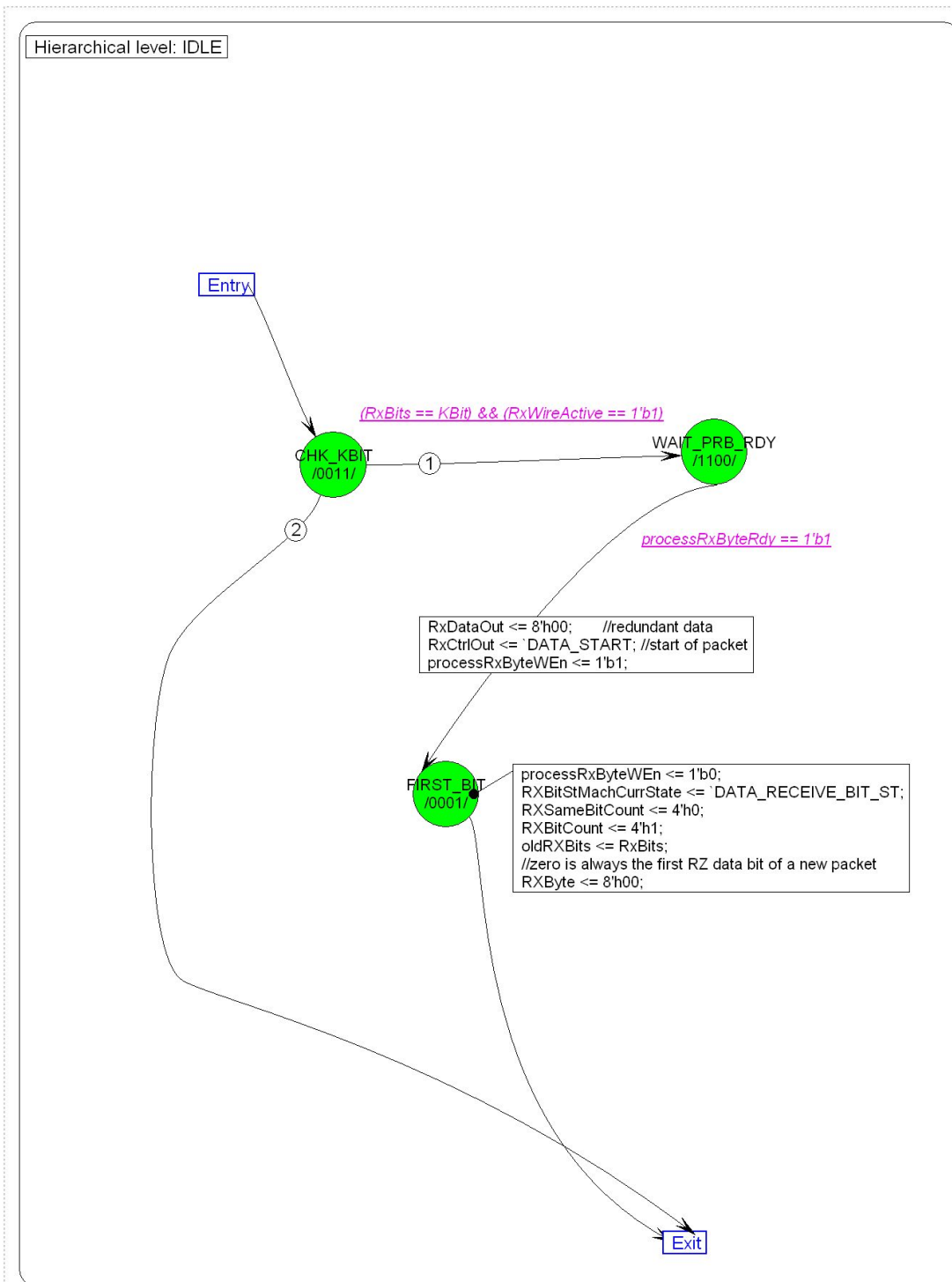
## 2.5.4 OUT1



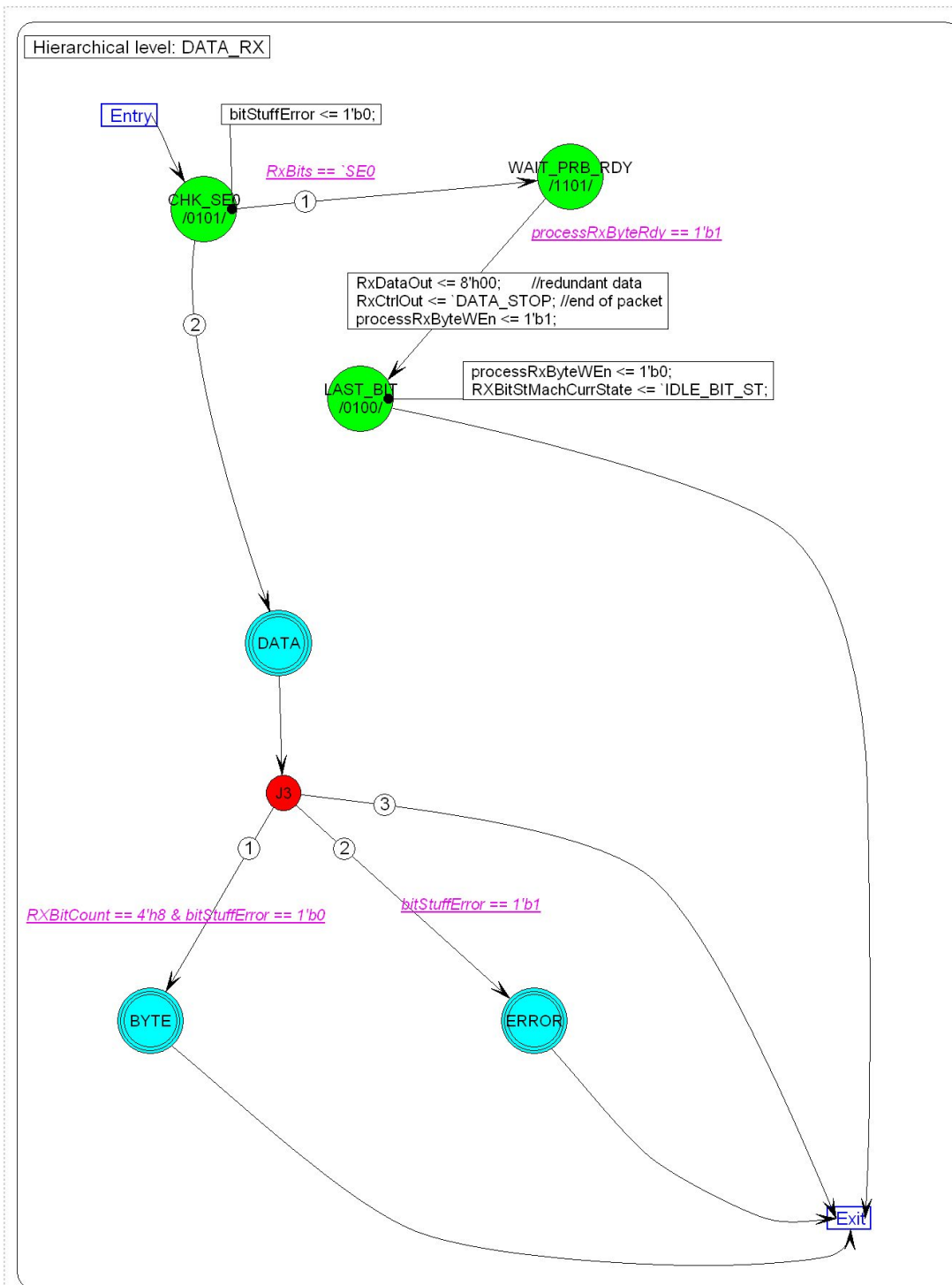
## 2.6 processRxBit.asf



## 2.6.1 IDLE



## 2.6.2 DATA\_RX

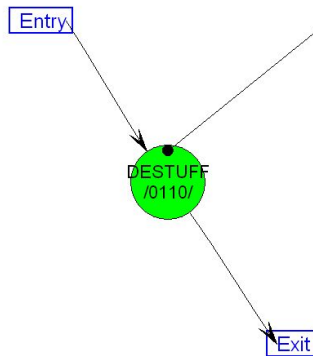




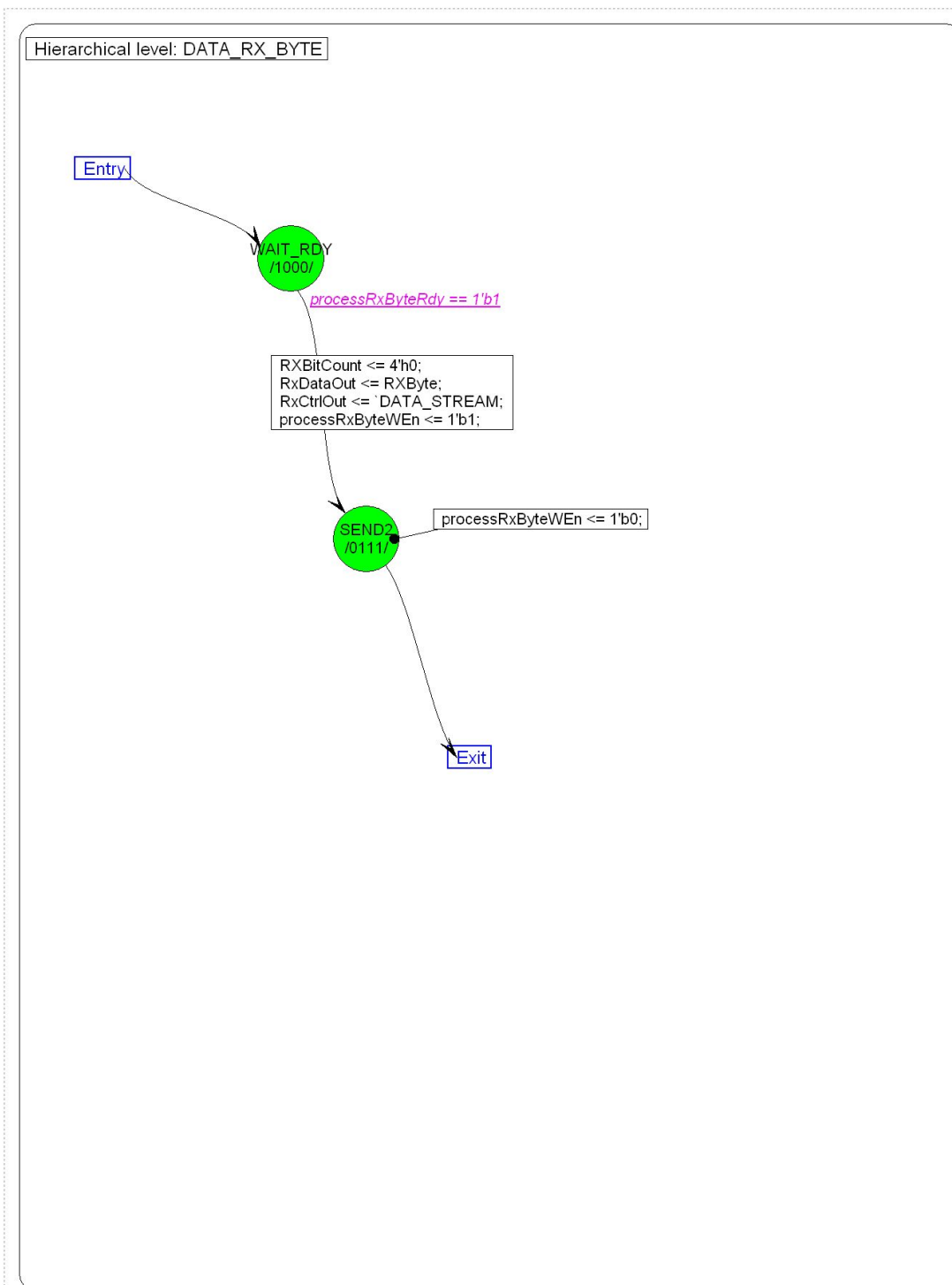
## 2.6.2.1 DATA

Hierarchical level: DATA\_RX\_DATA

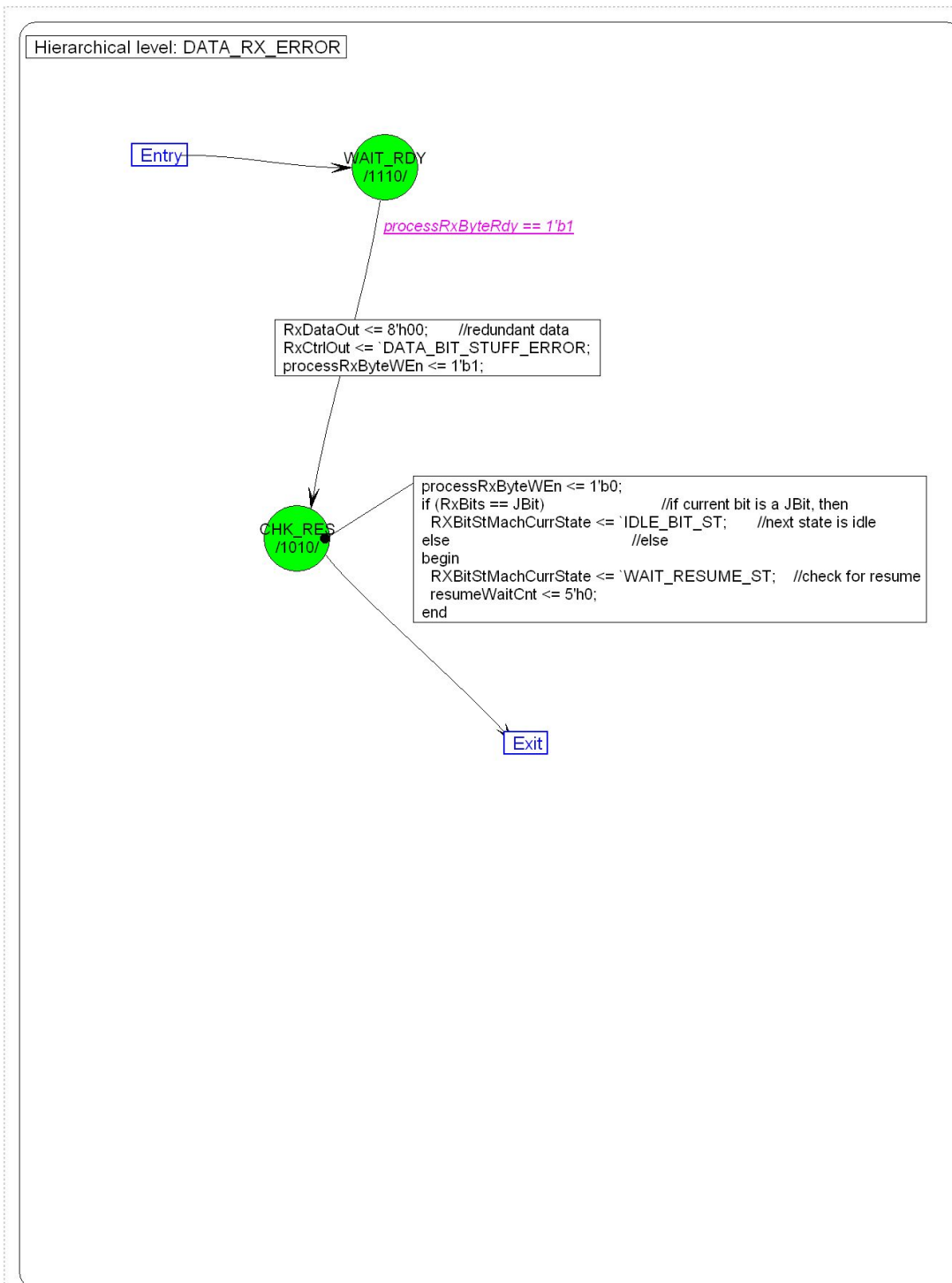
```
if (RxBits == oldRXBits) //if the current 'RxBits' are the same as the old 'RxBits', then
begin
  RXSameBitCount <= RXSameBitCount + 1'b1; //inc 'RXSameBitCount'
  if (RXSameBitCount == `MAX_CONSEC_SAME_BITS) //if 'RXSameBitCount' == 6 there has been a bit stuff error
    bitStuffError <= 1'b1; //flag 'bitStuffError'
  else //else no bit stuffing error
  begin
    RXBitCount <= RXBitCount + 1'b1;
    if (RXBitCount != `MAX_CONSEC_SAME_BITS_PLUS1) begin
      processRxBitRdy <= 1'b1; //early indication of ready
    end
    RXByte <= { 1'b1, RXByte[7:1]}; //RZ bit = 1 (ie no change in 'RxBits')
  end
end
else //else current 'RxBits' are different from old 'RxBits'
begin
  if (RXSameBitCount != `MAX_CONSEC_SAME_BITS) //if this is not the RZ 0 bit after 6 consecutive RZ 1s, then
  begin
    RXBitCount <= RXBitCount + 1'b1;
    if (RXBitCount != 4'h7) begin
      processRxBitRdy <= 1'b1; //early indication of ready
    end
    RXByte <= {1'b0, RXByte[7:1]}; //RZ bit = 0 (ie current 'RxBits' is different than old 'RxBits')
  end
  end
  RXSameBitCount <= 4'h0; //reset 'RXSameBitCount'
end
oldRXByte <= RxByte;
```



## 2.6.2.2 BYTE



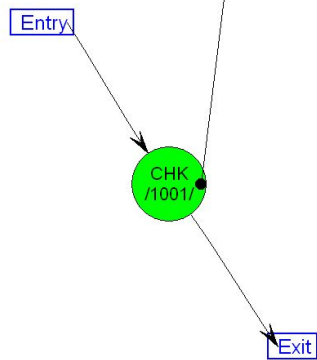
### 2.6.2.3 ERROR



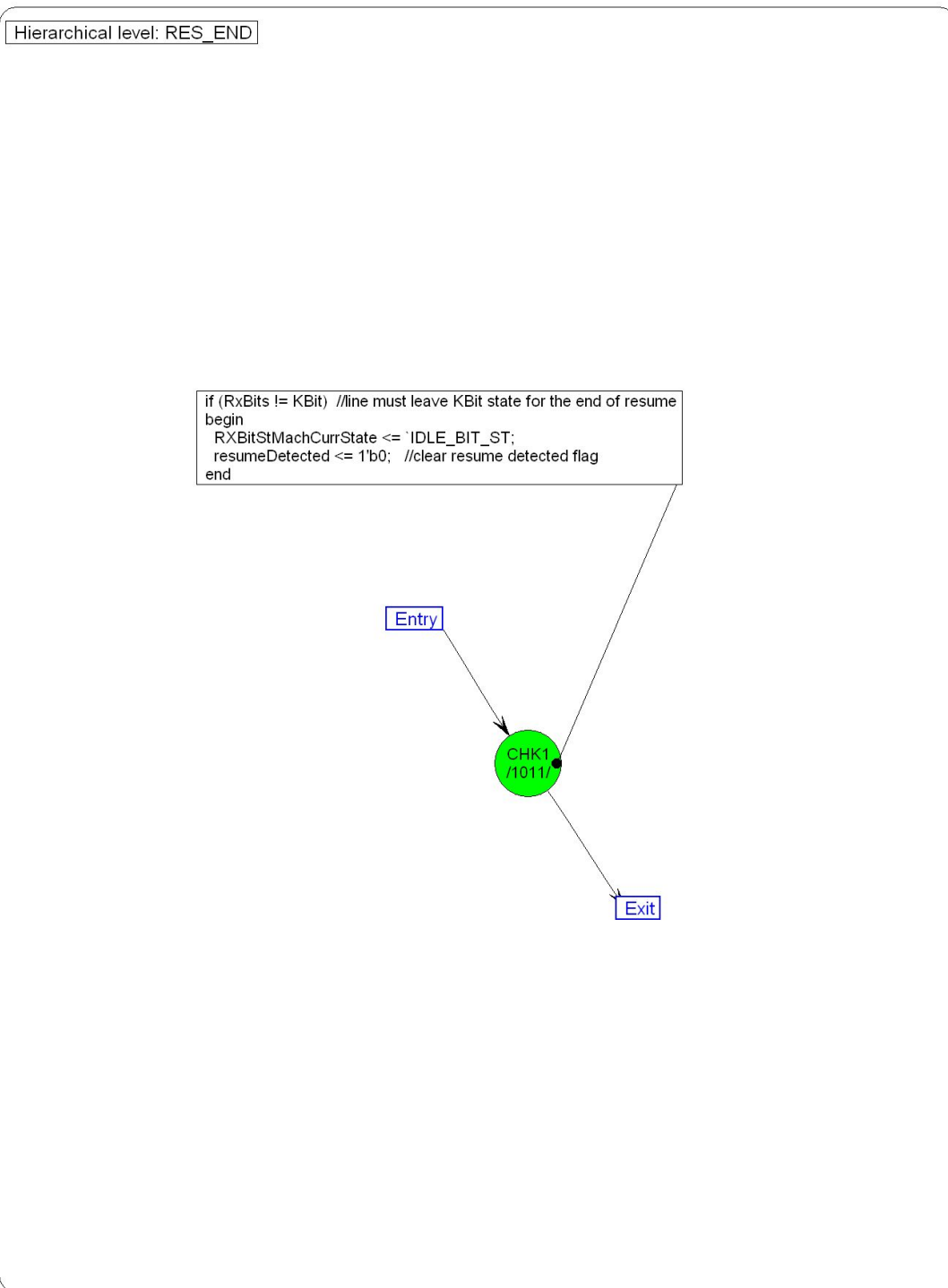
## 2.6.3 RES\_RX

Hierarchical level: RES\_RX

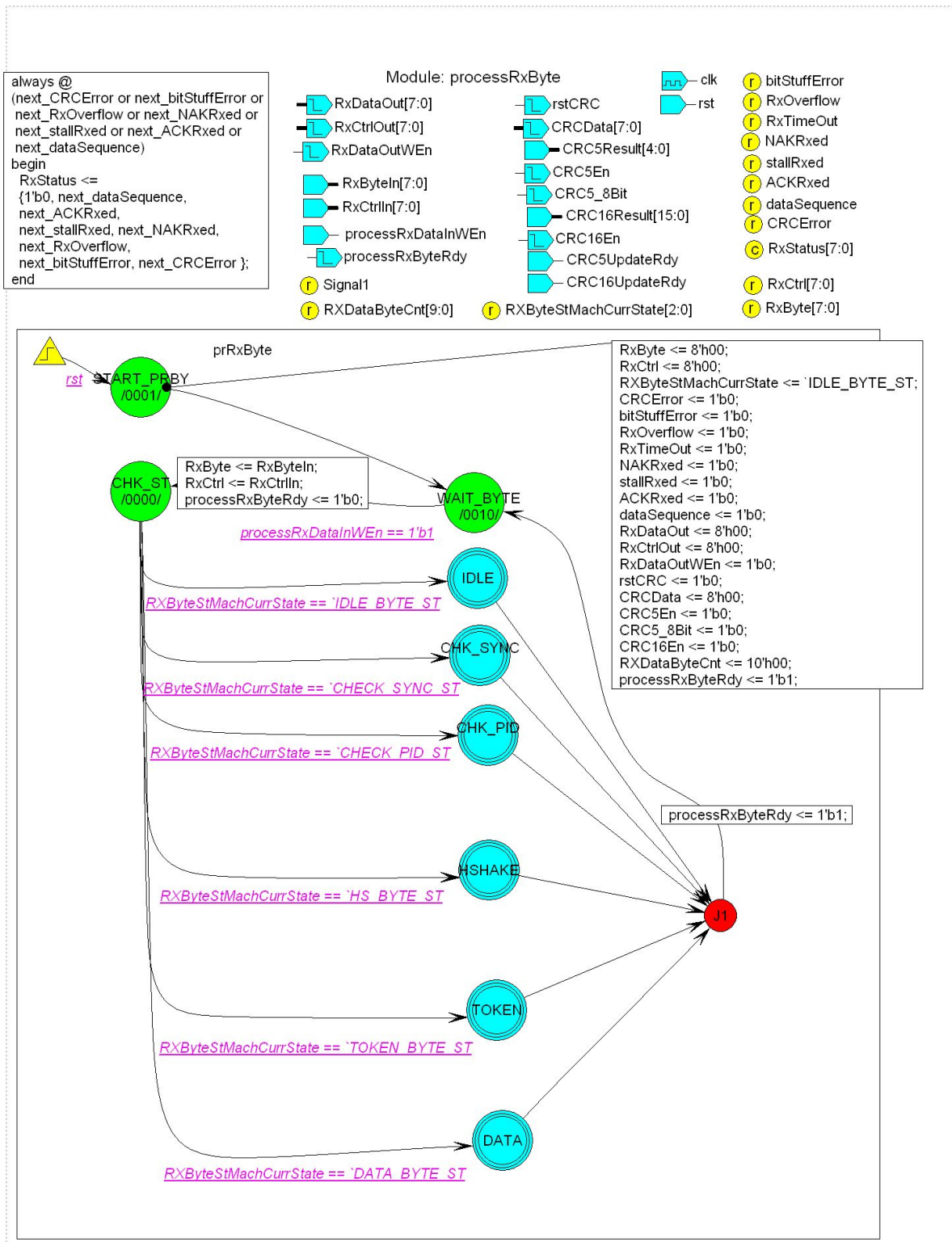
```
if (RxBits != KBit) //can only be a resume if line remains in Kbit state
  RXBitStMachCurrState <= `IDLE_BIT_ST;
else
  begin
    resumeWaitCnt <= resumeWaitCnt + 1'b1;
    //if we've waited long enough, then
    if (resumeWaitCnt == `RESUME_RX_WAIT_TIME)
      begin
        RXBitStMachCurrState <= `RESUME_END_WAIT_ST;
        resumeDetected <= 1'b1; //report resume detected
      end
    end
  end
```



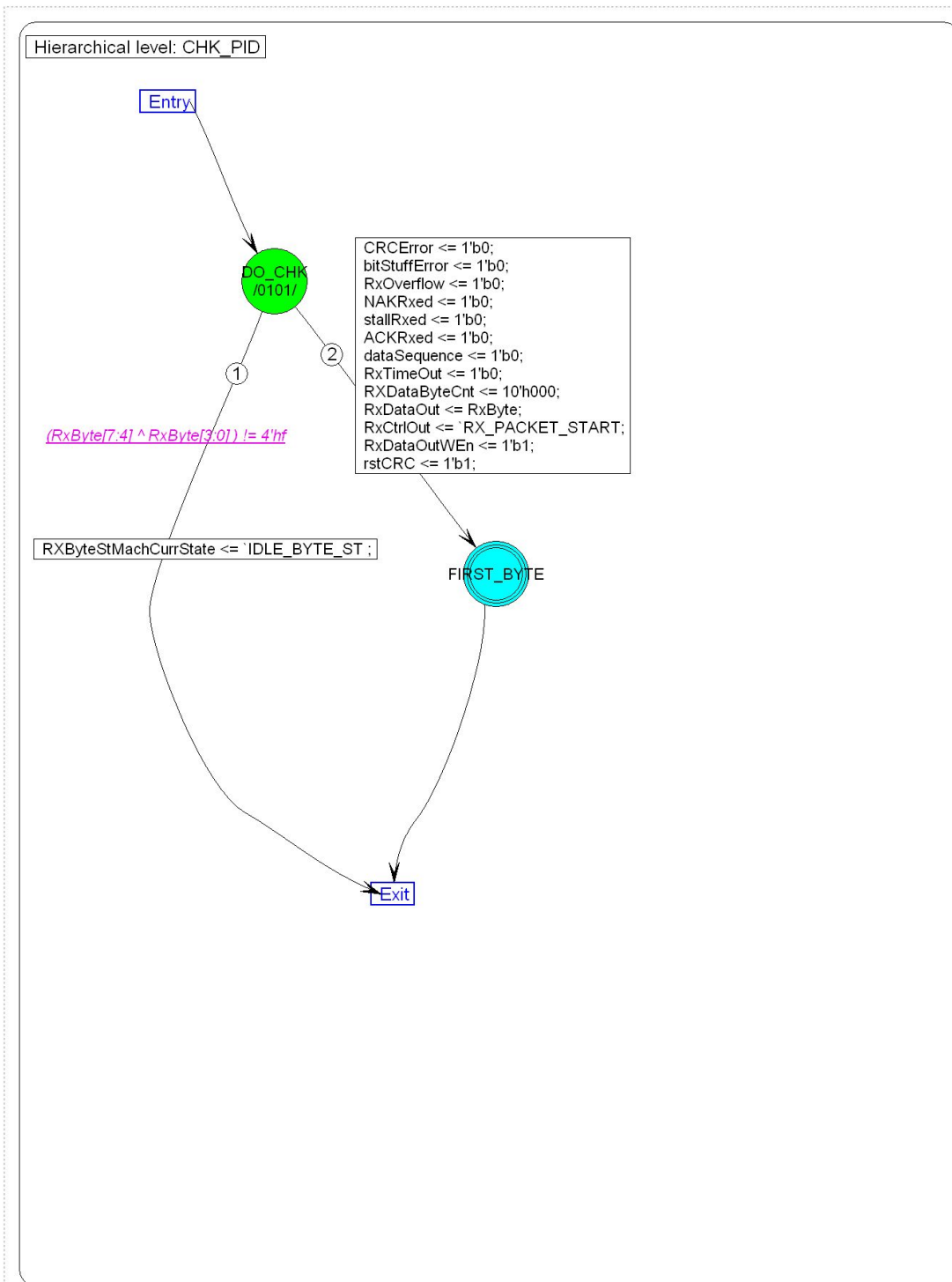
## 2.6.4 RES\_END



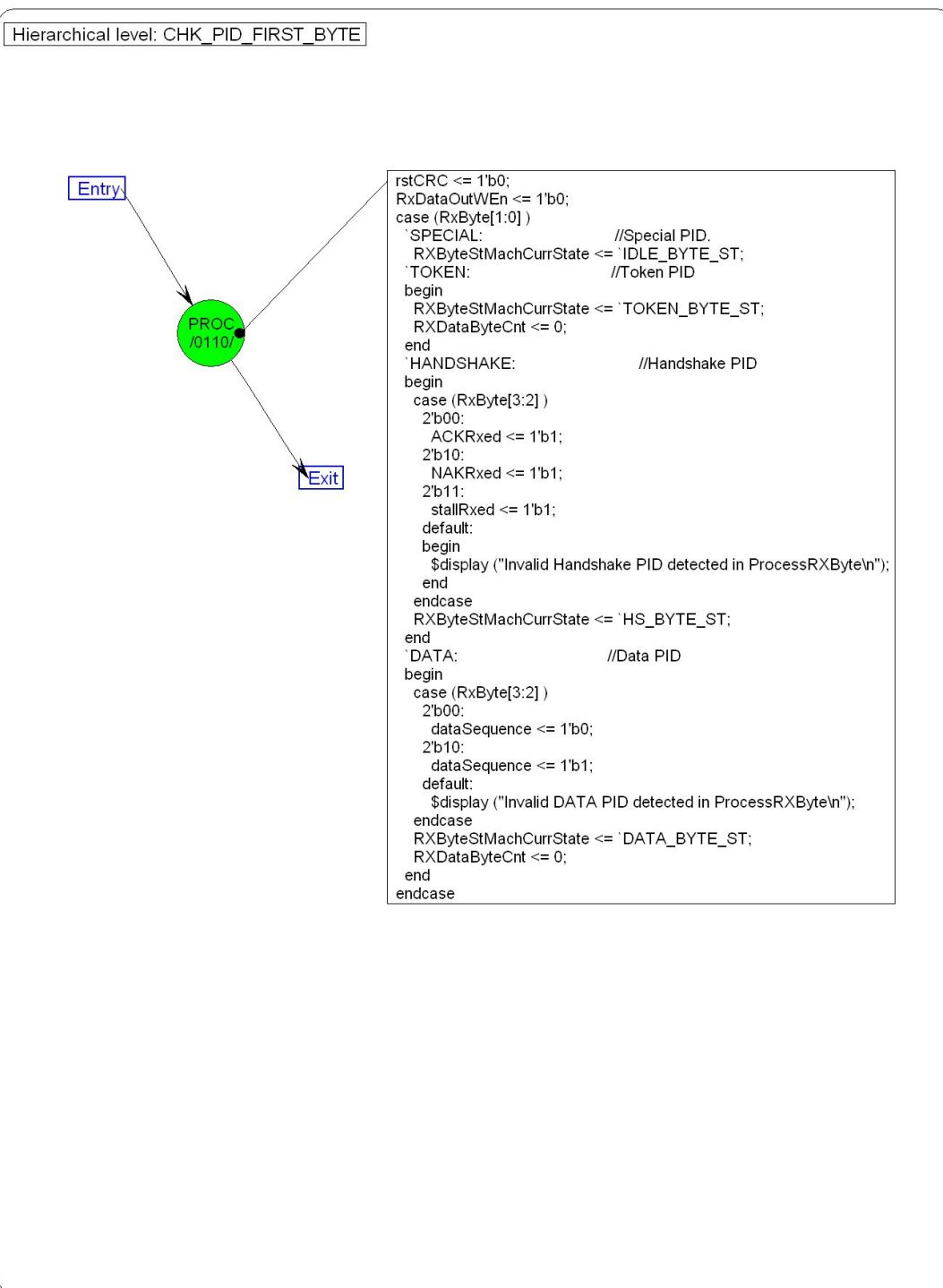
## 2.7 processRxByte.asf



## 2.7.1 CHK\_PID

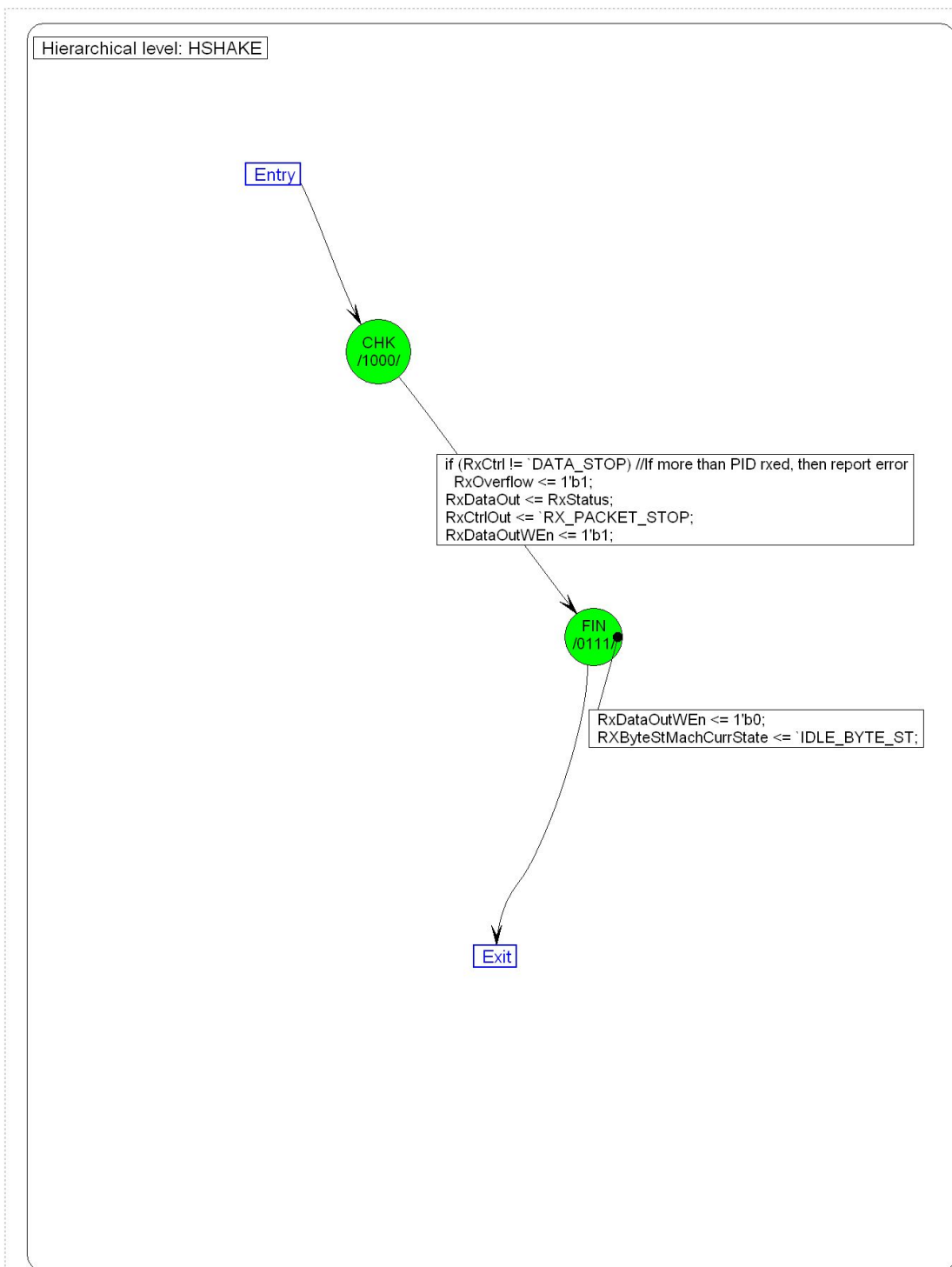


## 2.7.1.1 FIRST\_BYTE

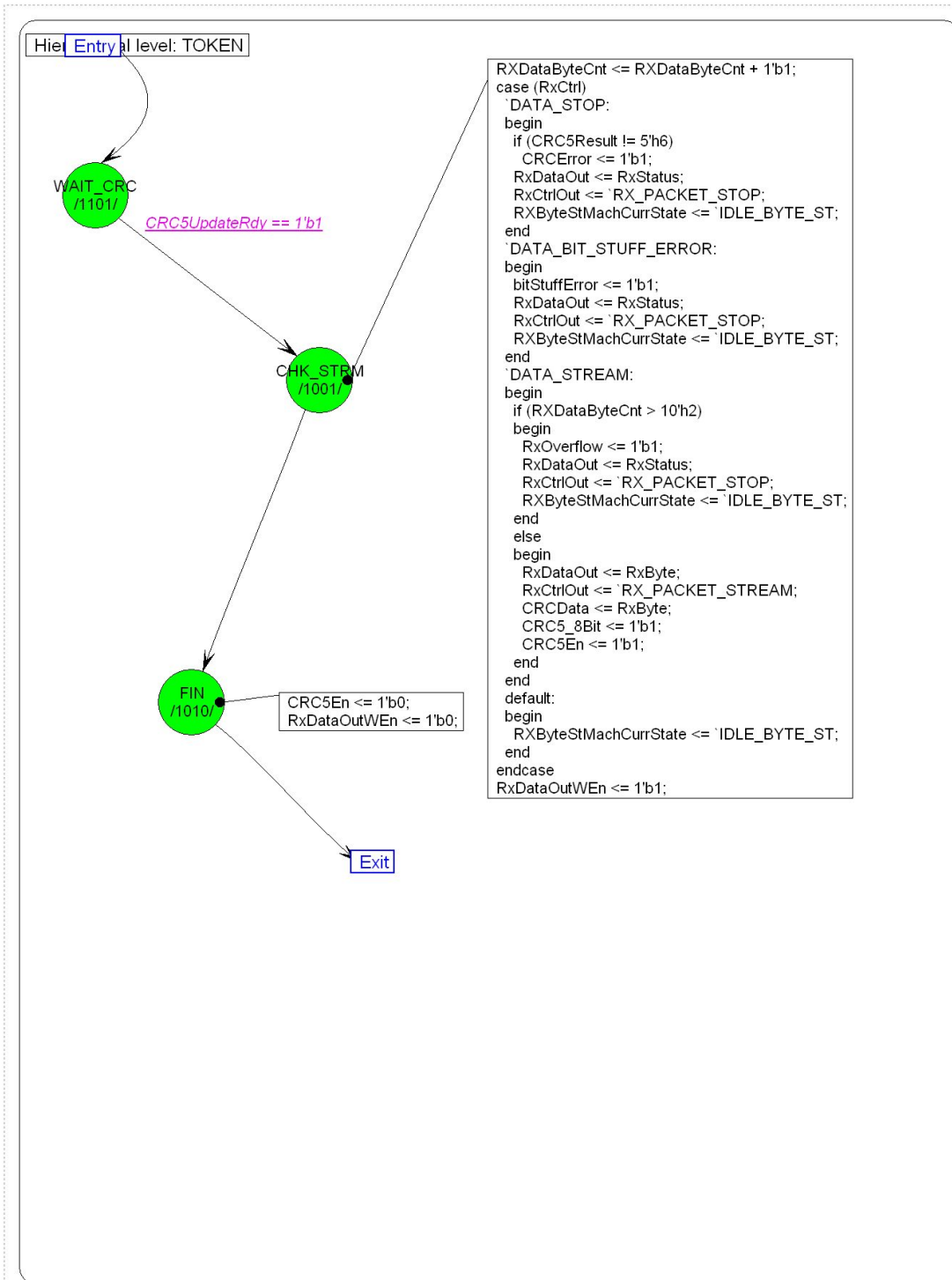




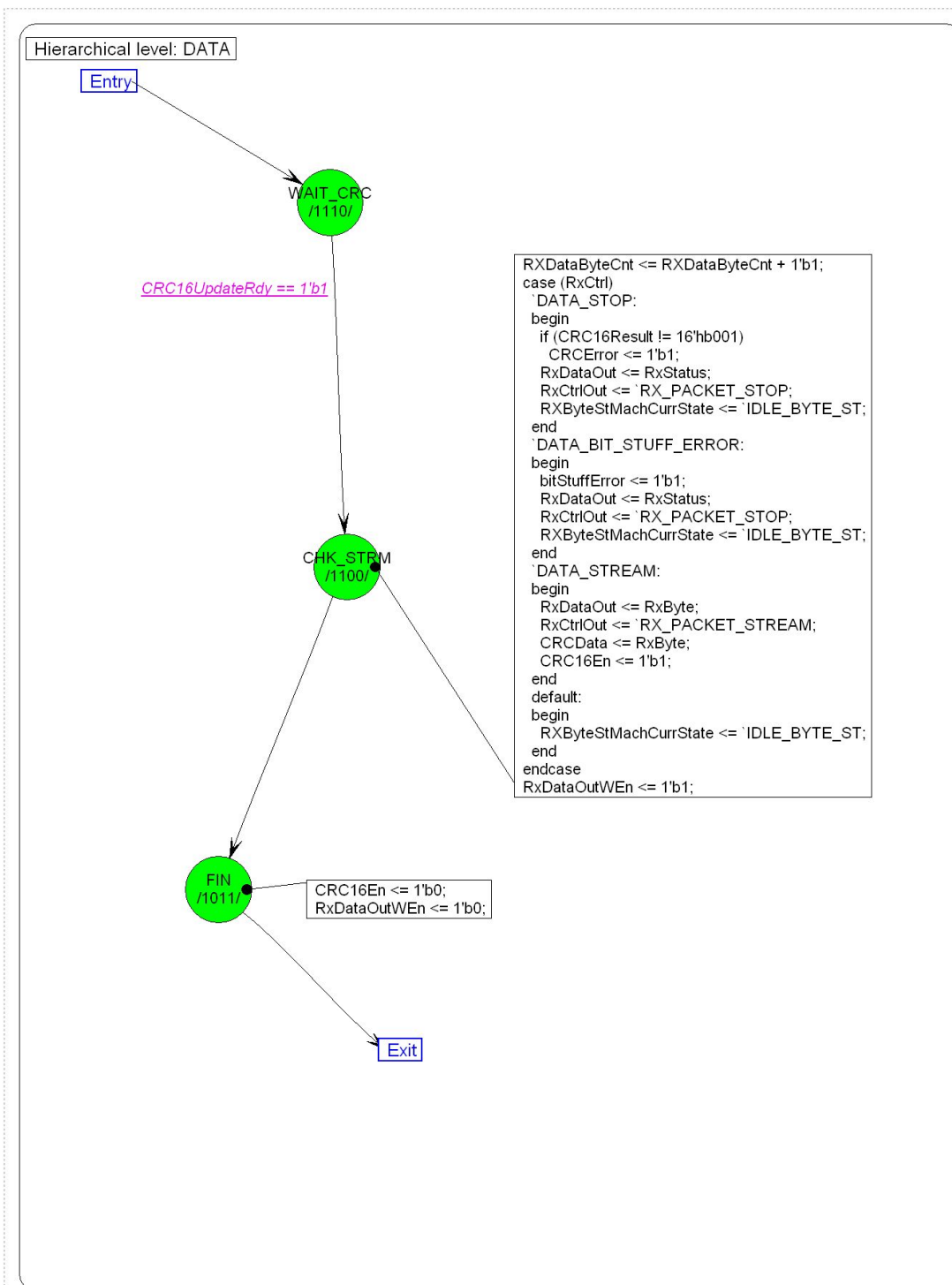
## 2.7.2 HSHAKE



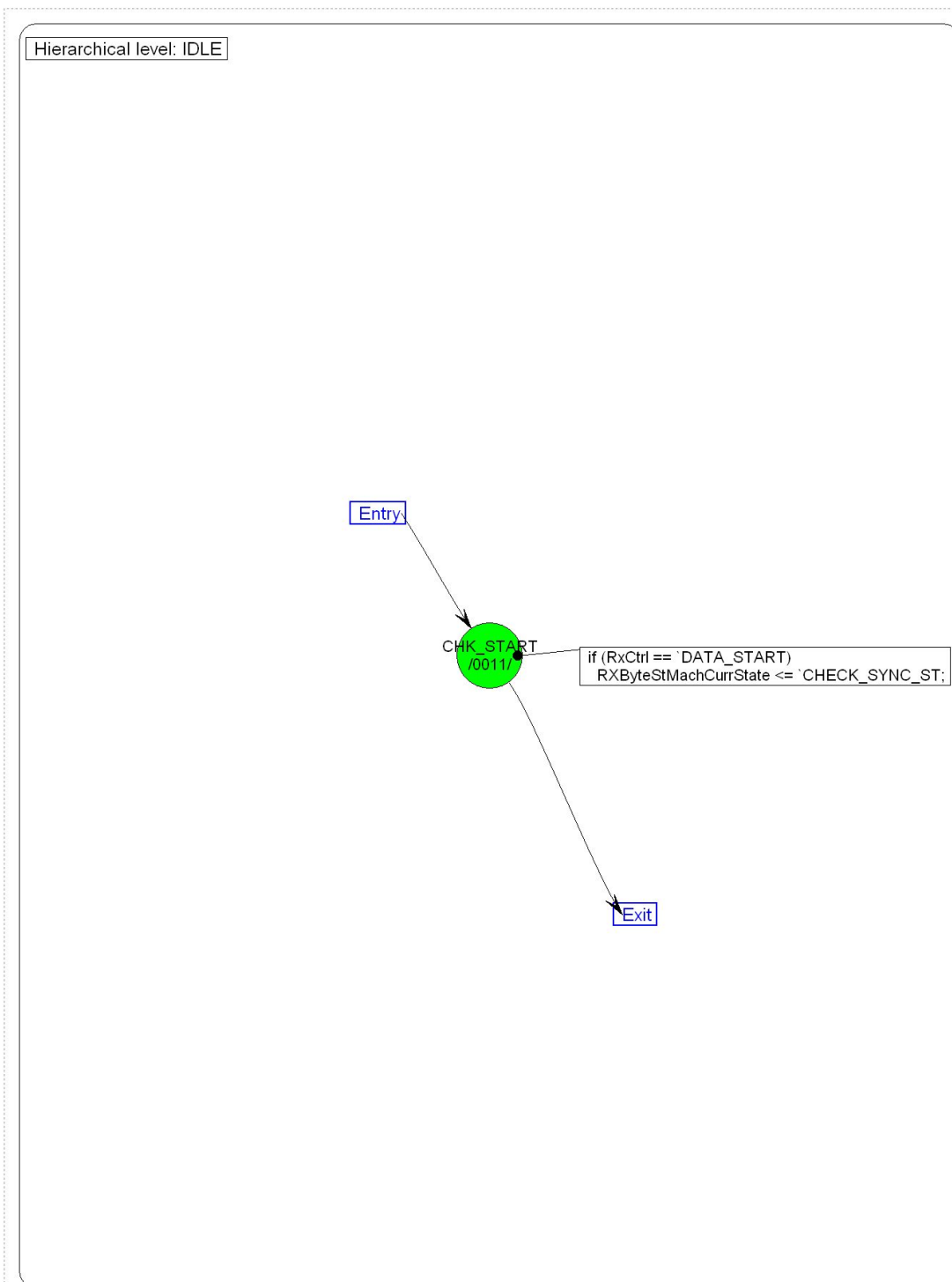
### 2.7.3 TOKEN



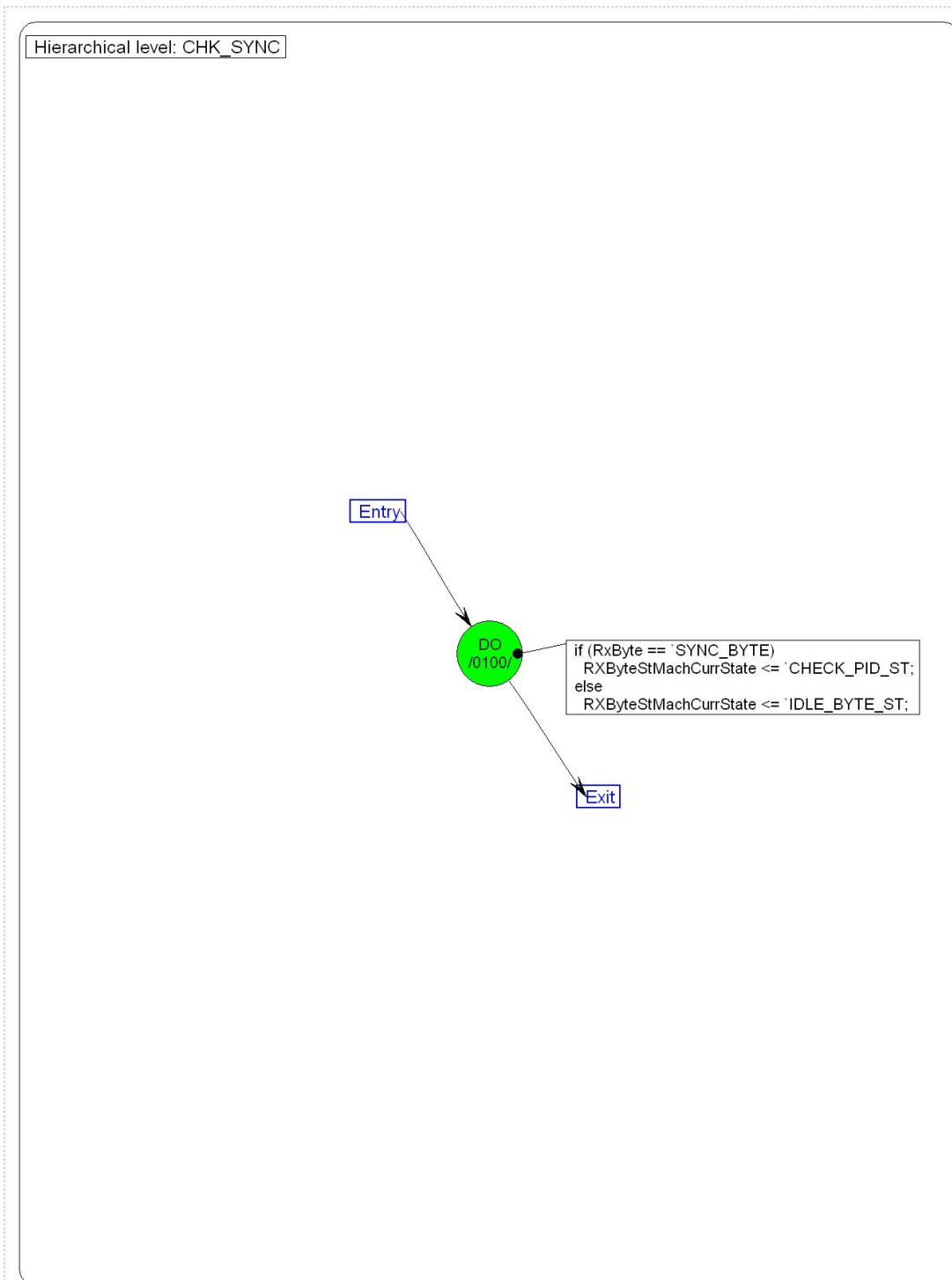
## 2.7.4 DATA



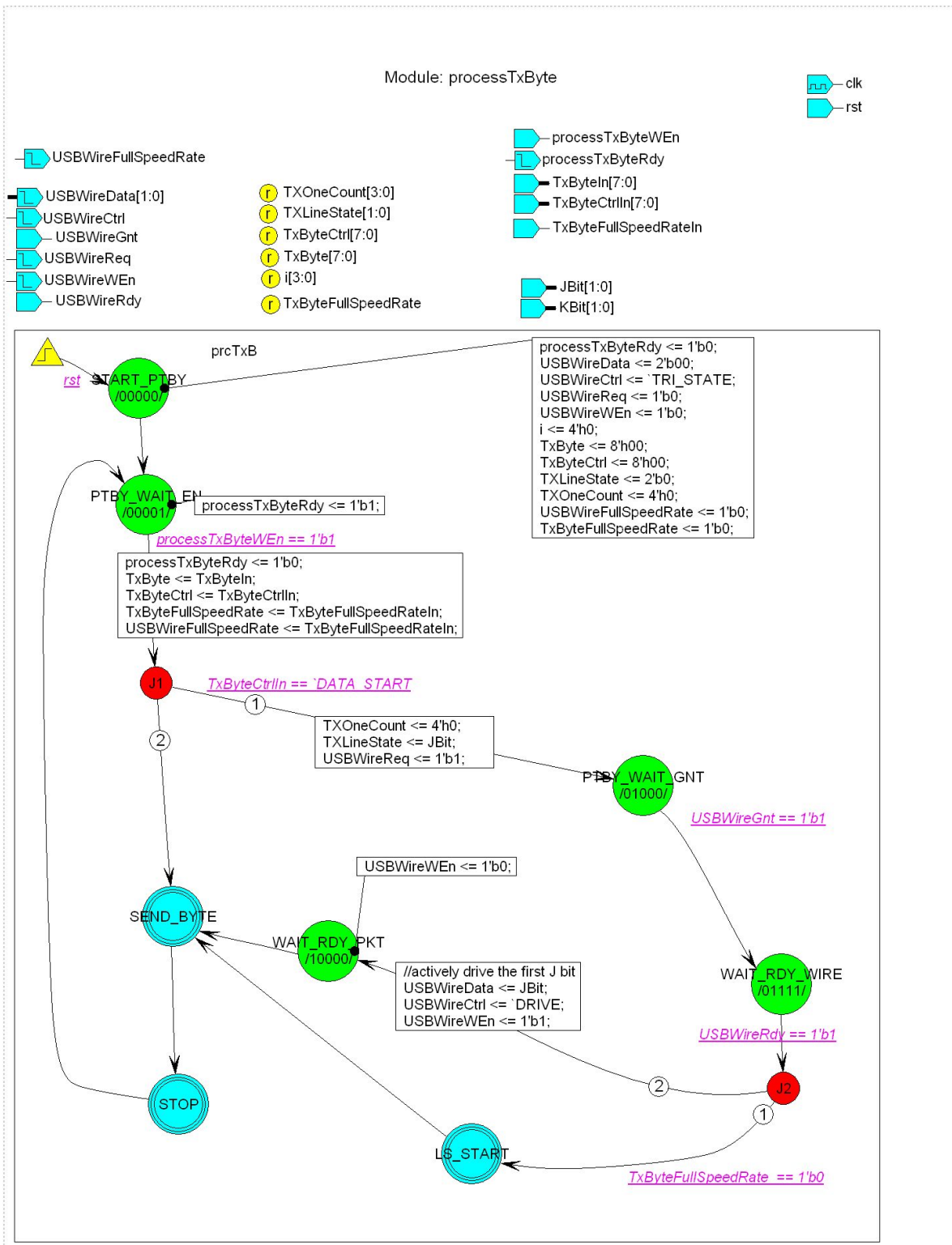
## 2.7.5 IDLE



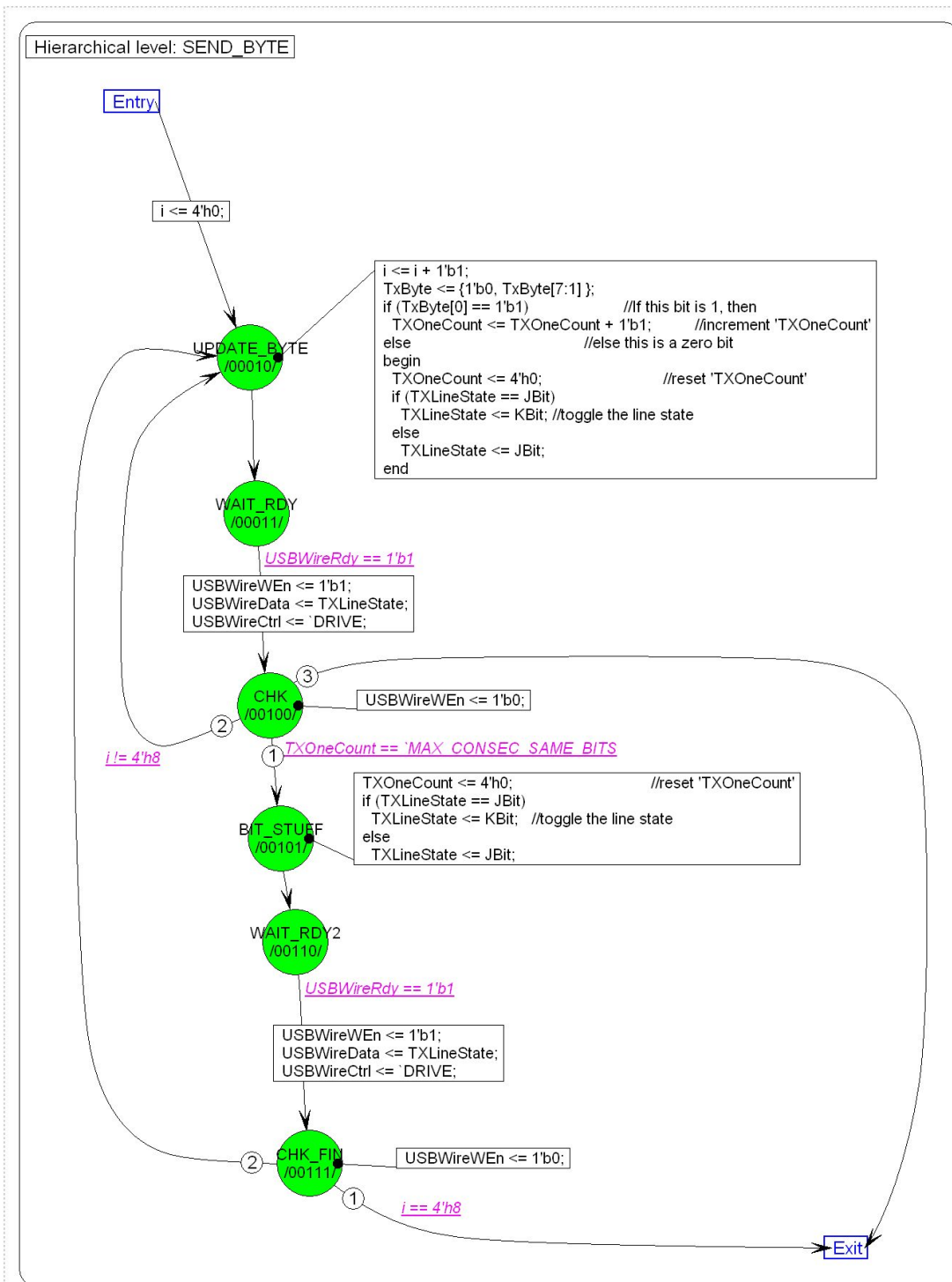
## 2.7.6 CHK\_SYNC



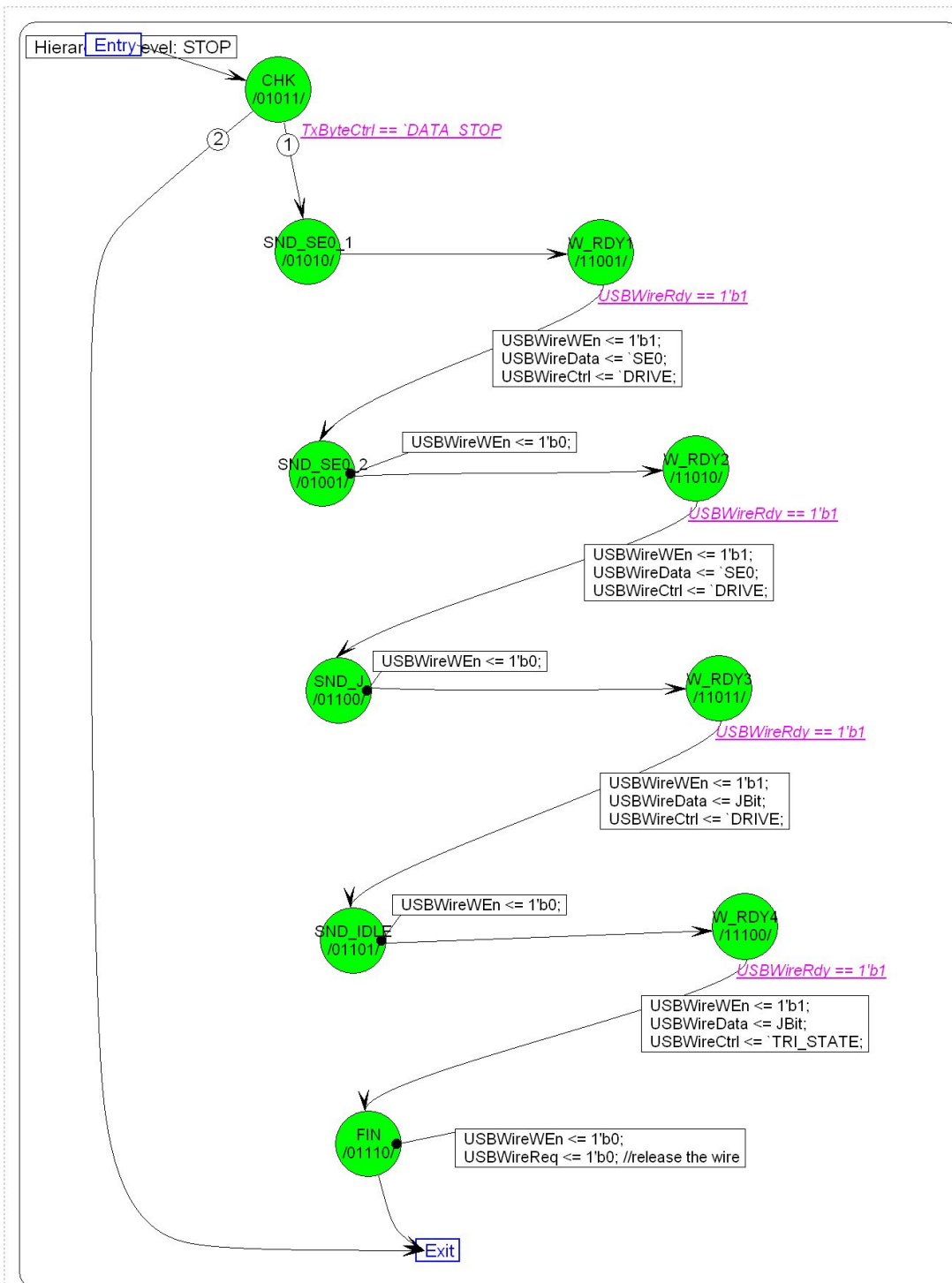
## 2.8 processTxByte.asf



## 2.8.1 SEND\_BYTE

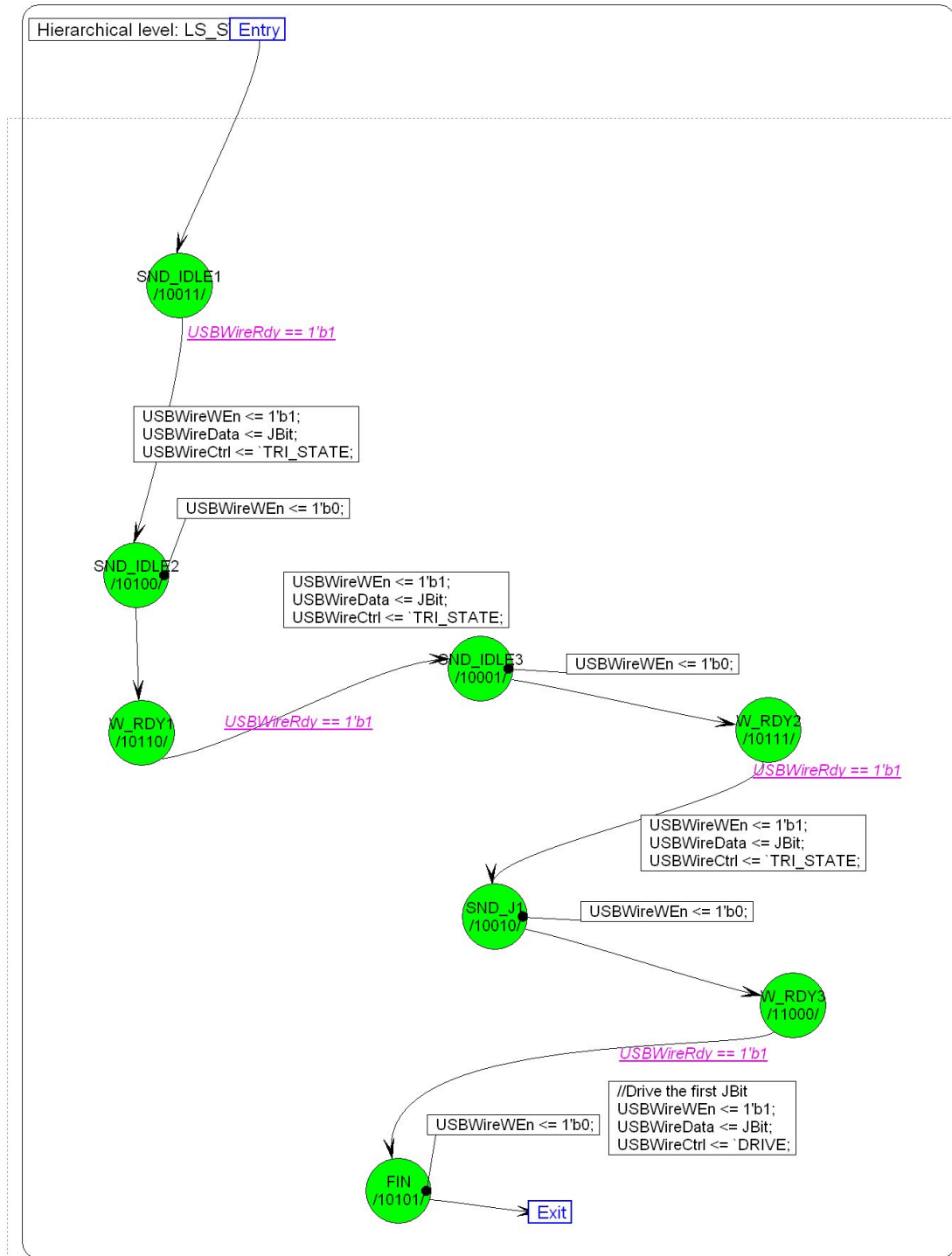


## 2.8.2 STOP

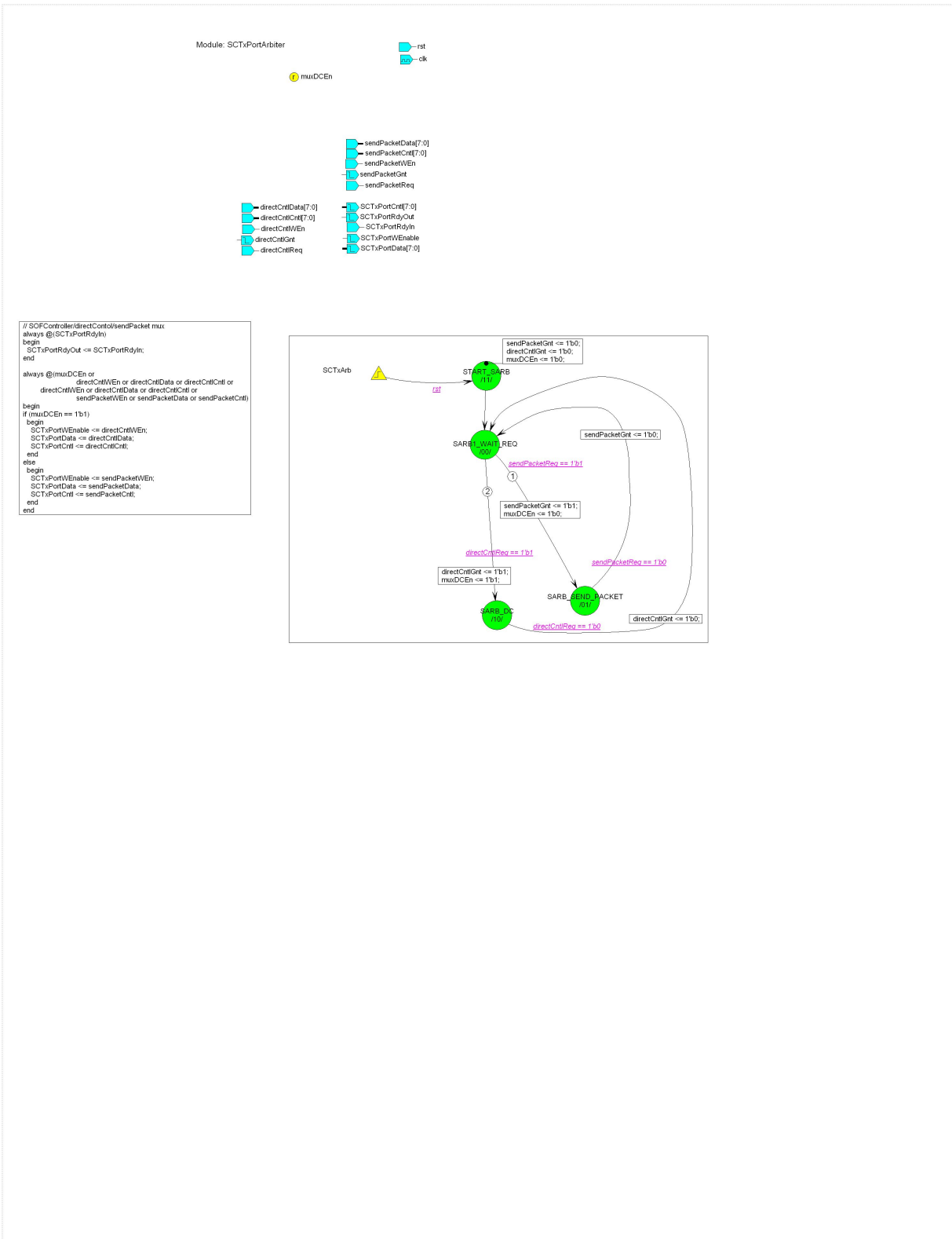




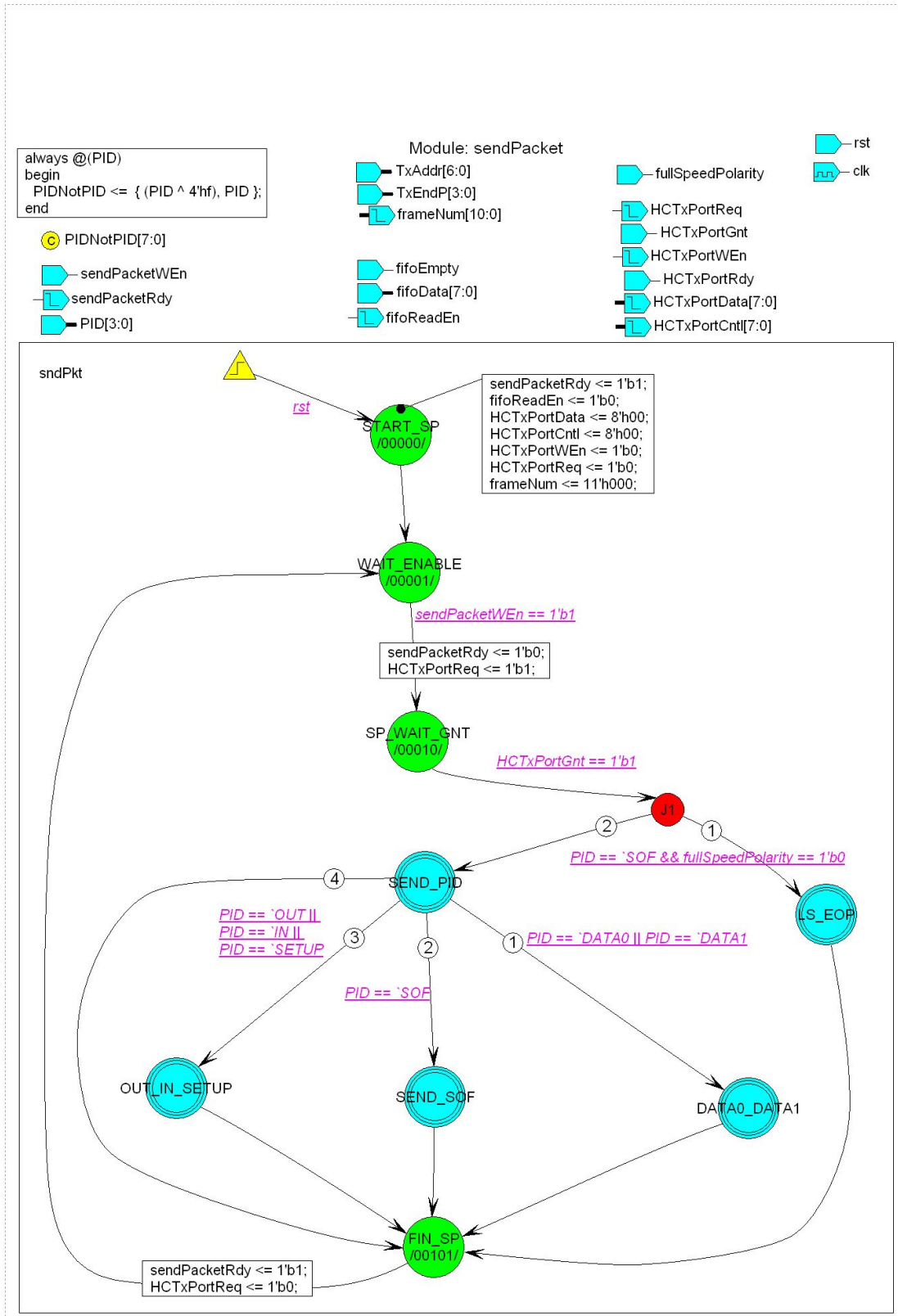
### 2.8.3 LS\_START



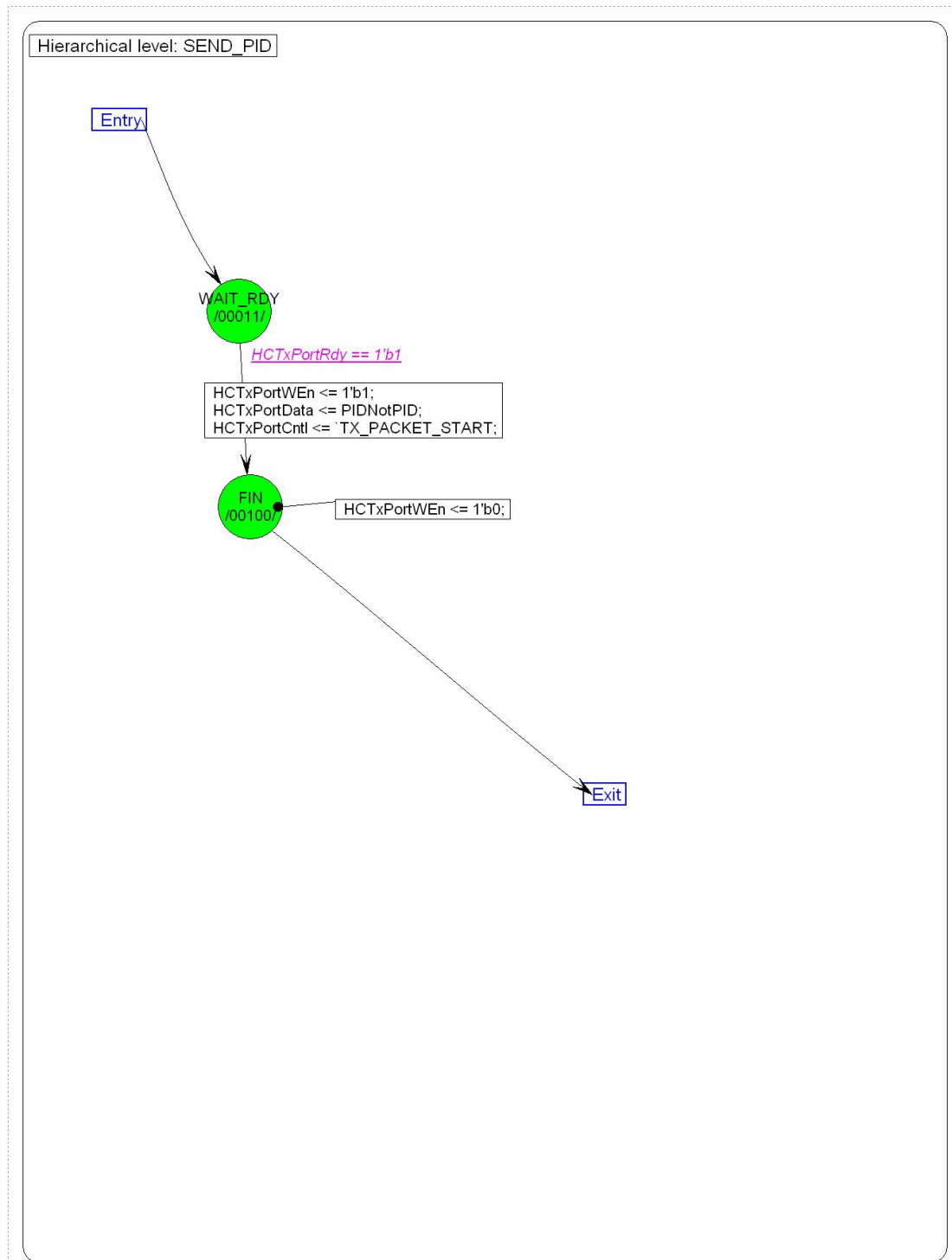
## 2.9 sctxportarbitr.asf



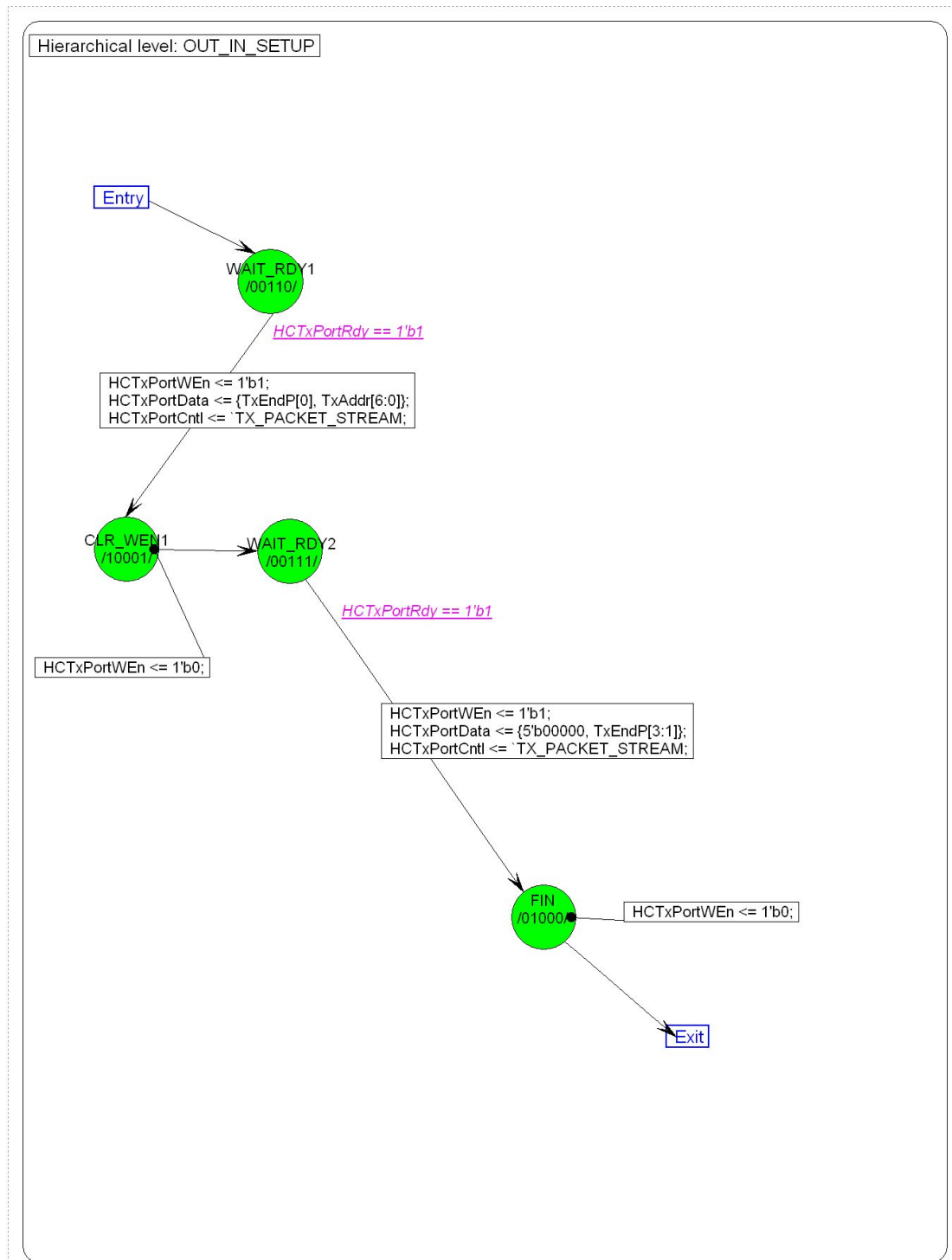
## 2.10 sendpacket.asf



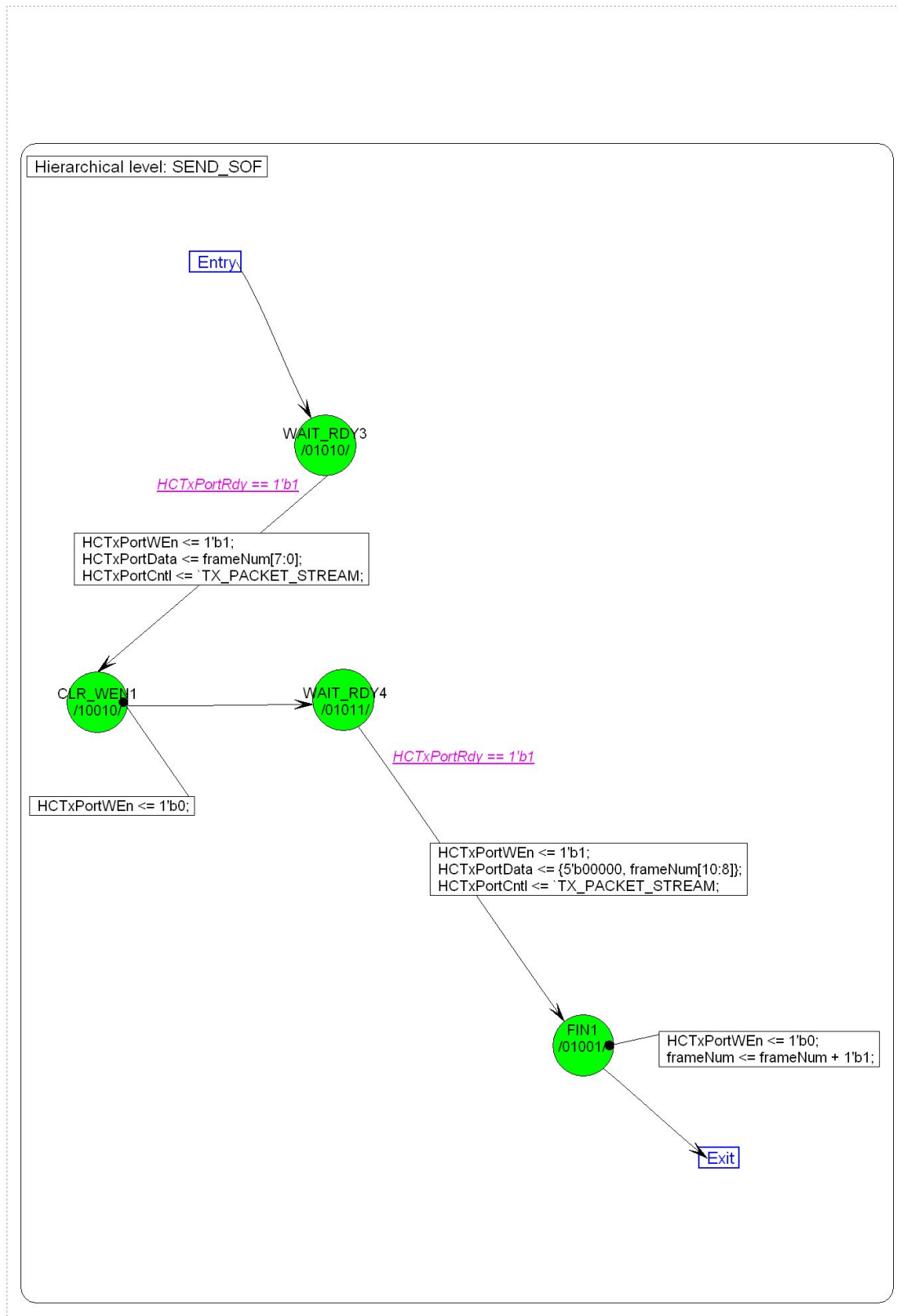
## 2.10.1 SEND\_PID



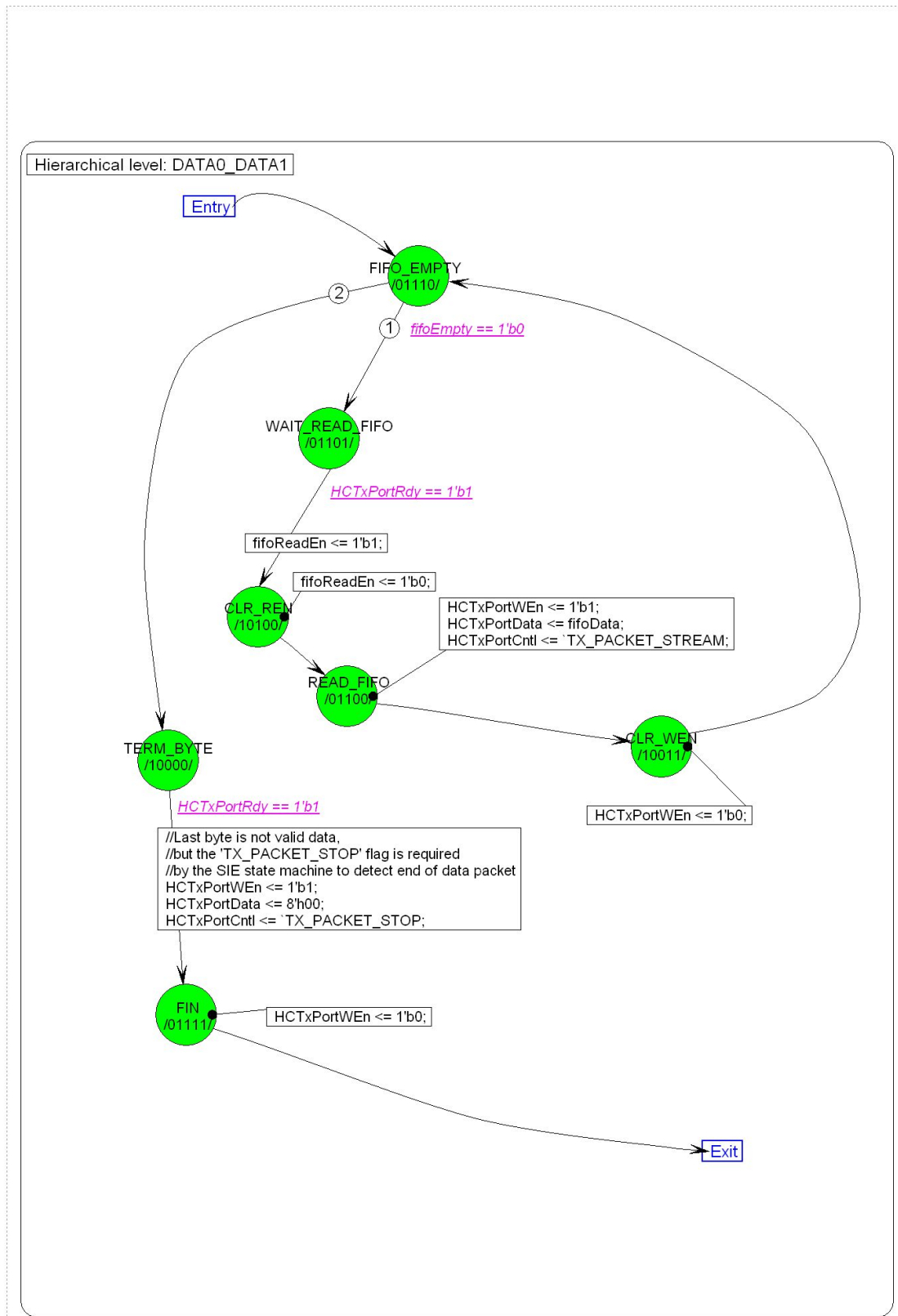
## 2.10.2 OUT\_IN\_SETUP



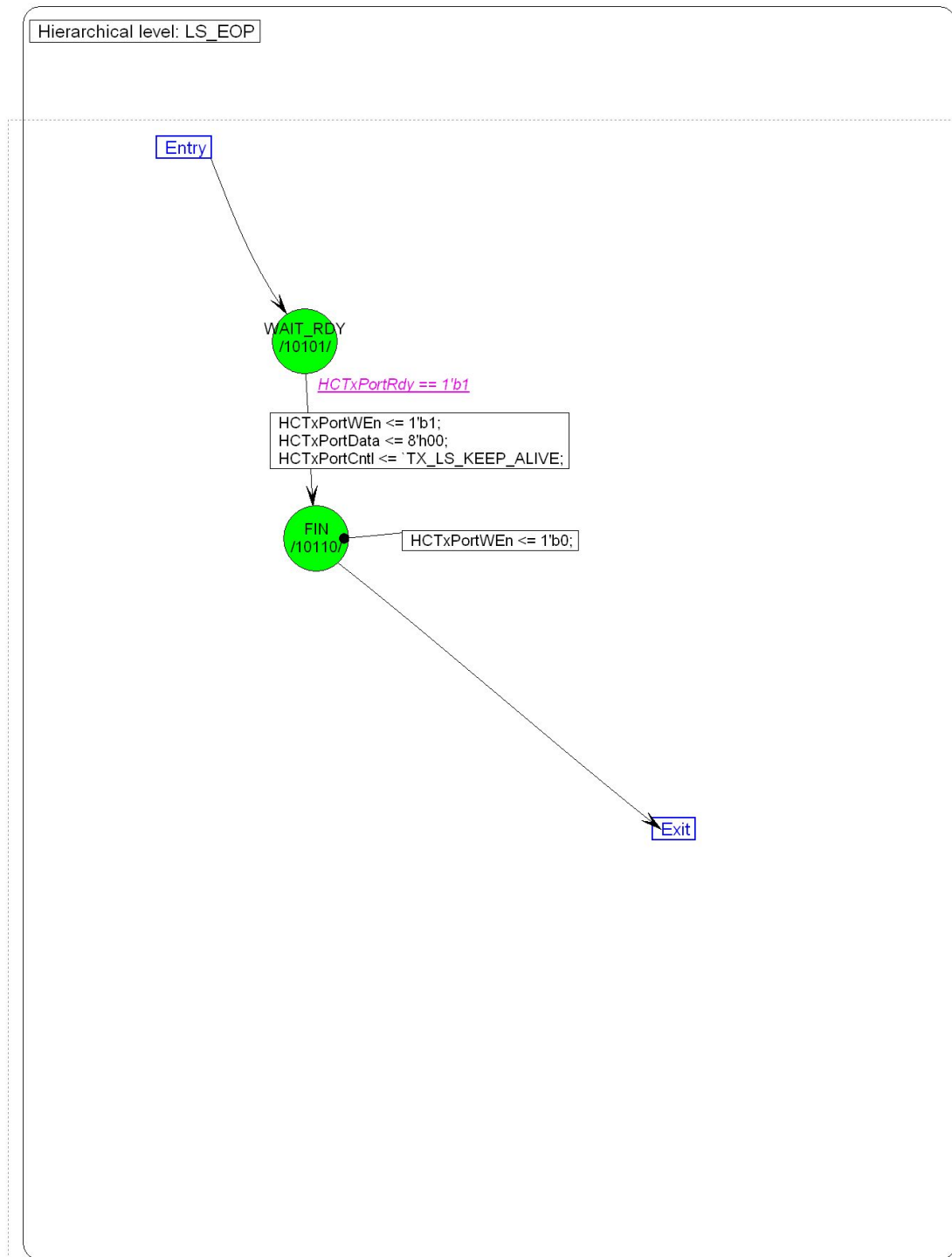
### 2.10.3 SEND\_SOF



## 2.10.4 DATA0\_DATA1

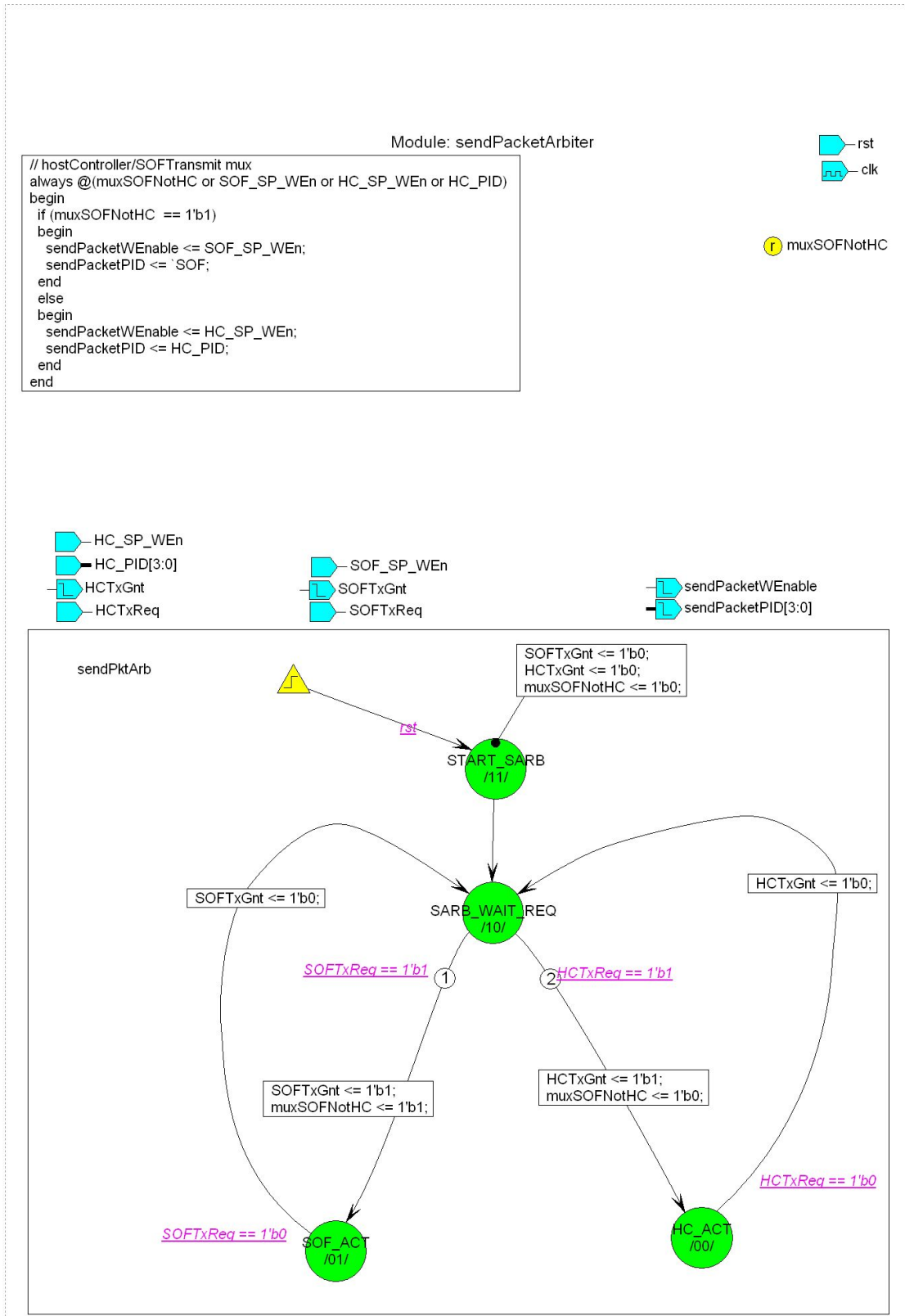


## 2.10.5 LS\_EOP

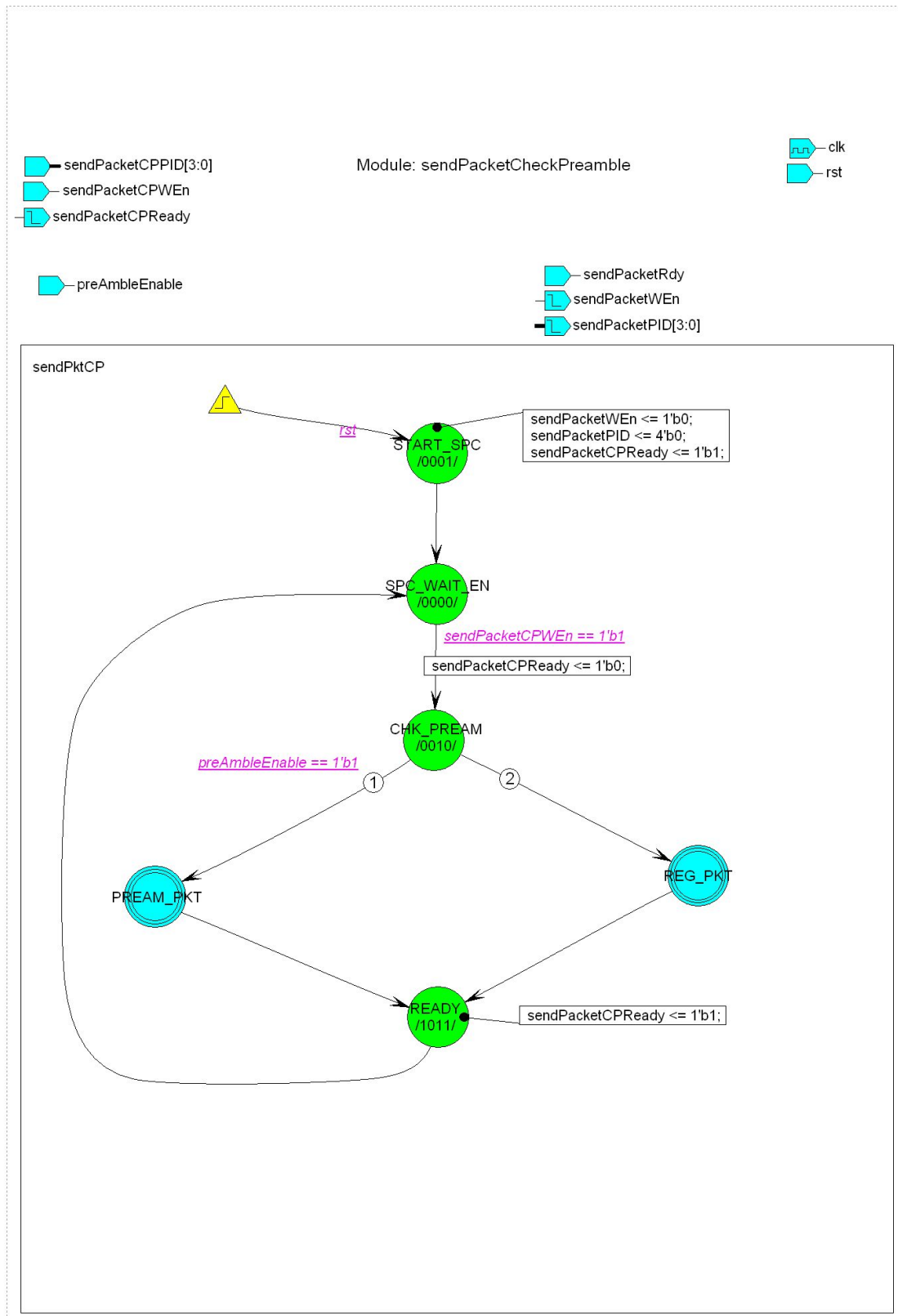




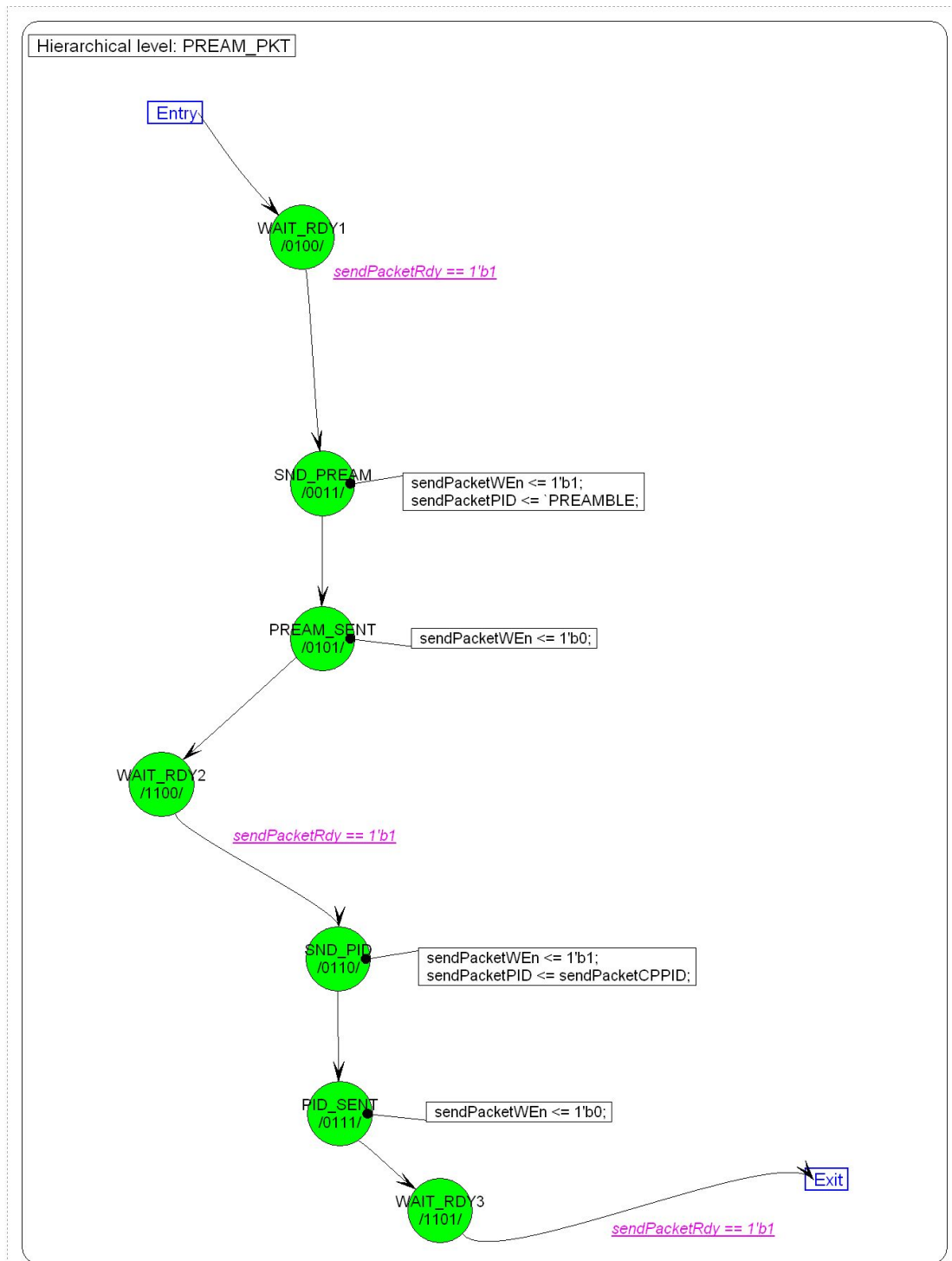
## 2.11 sendpacketarbiter.asf



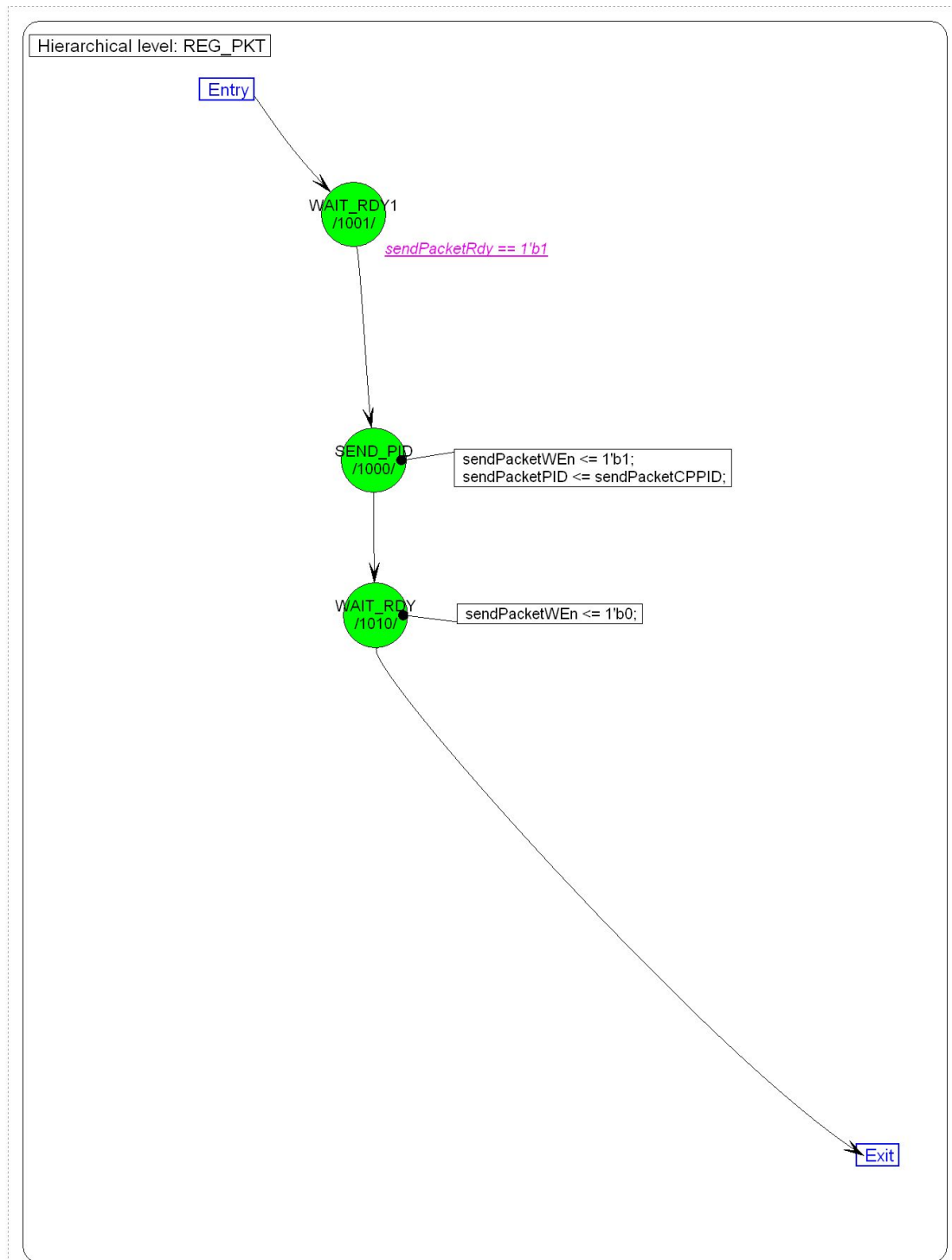
## 2.12 sendpacketcheckpreamble.asf



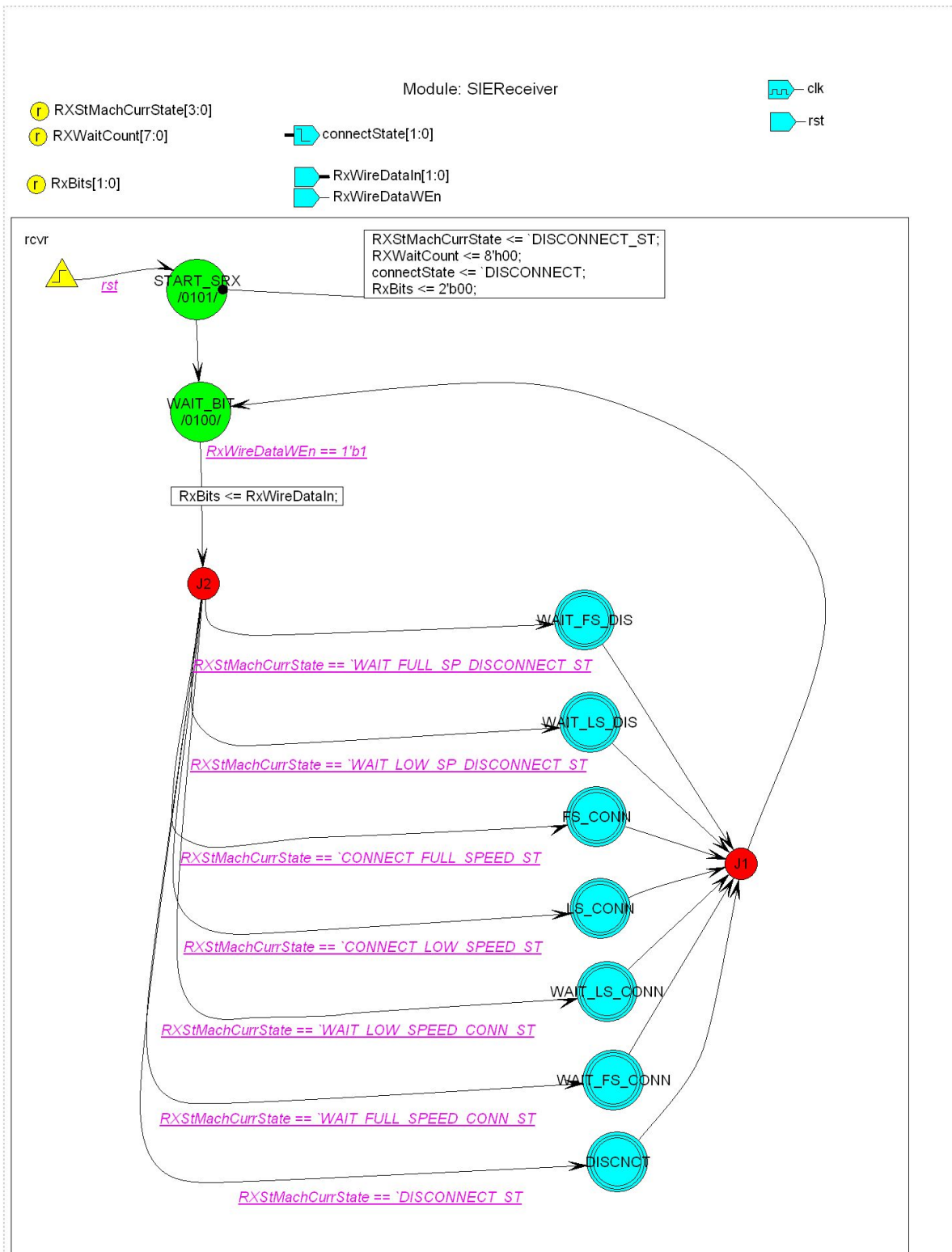
## 2.12.1 PREAM\_PKT



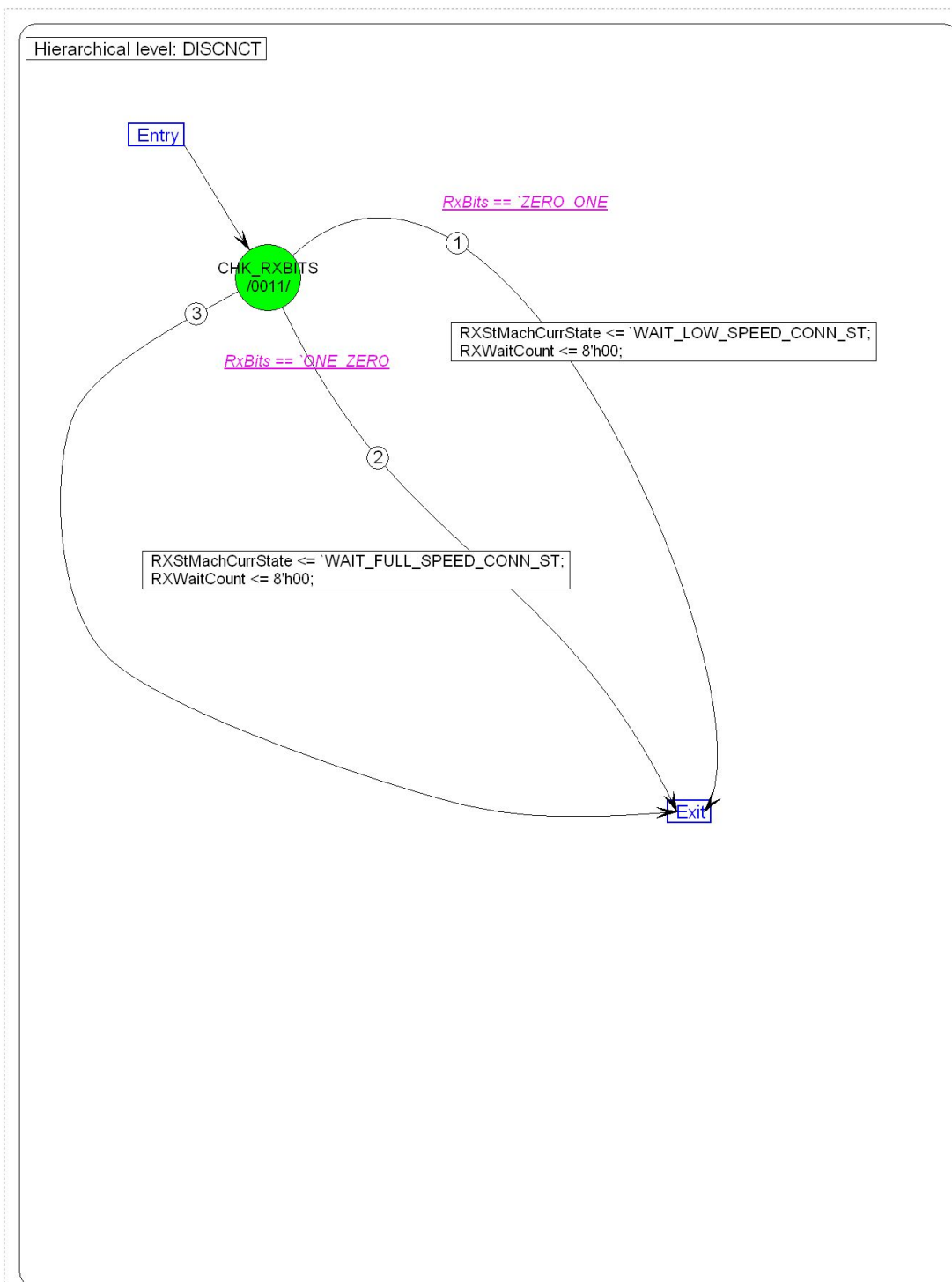
## 2.12.2 REG\_PKT



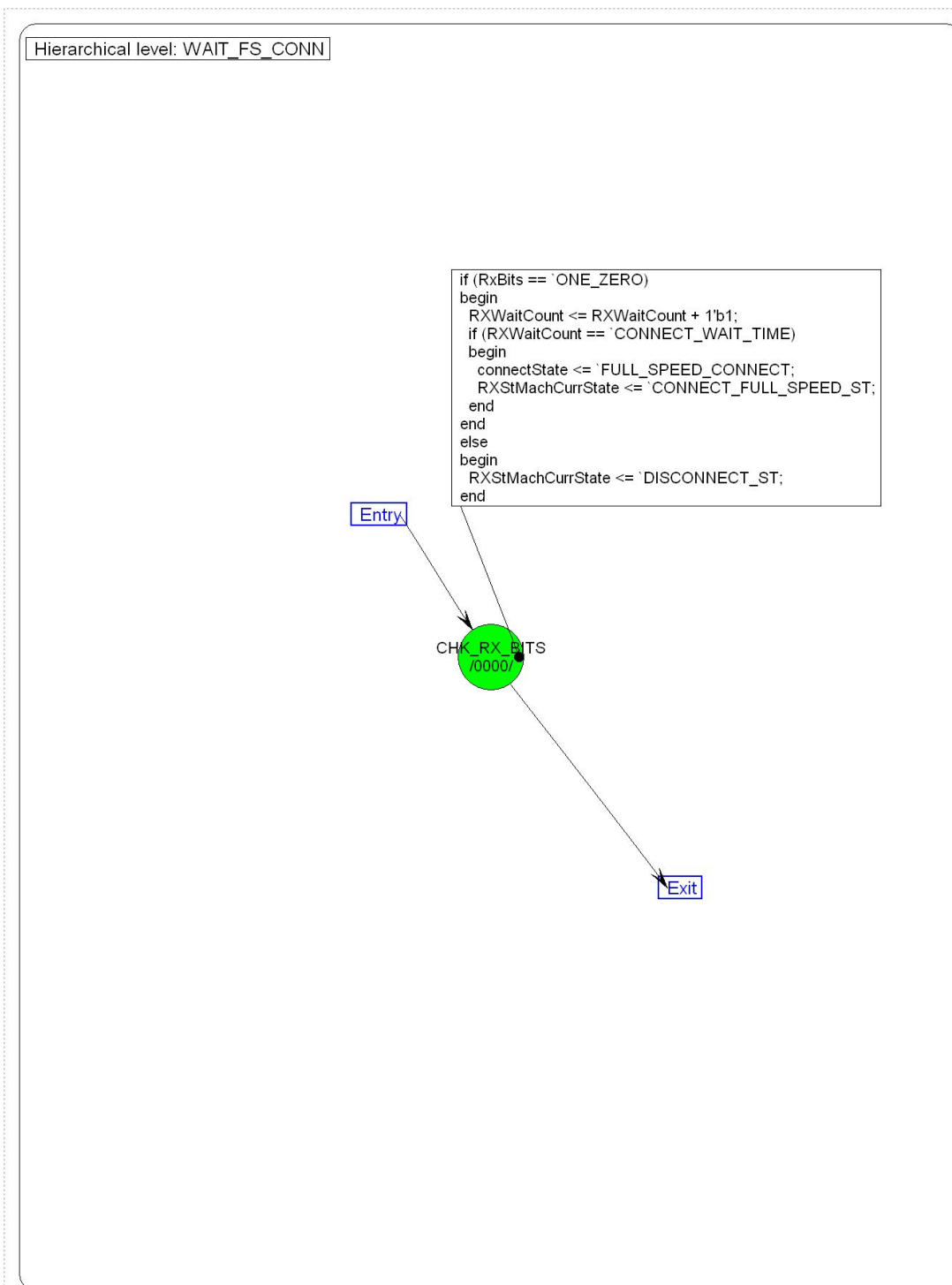
2.13 siereceiver.asf



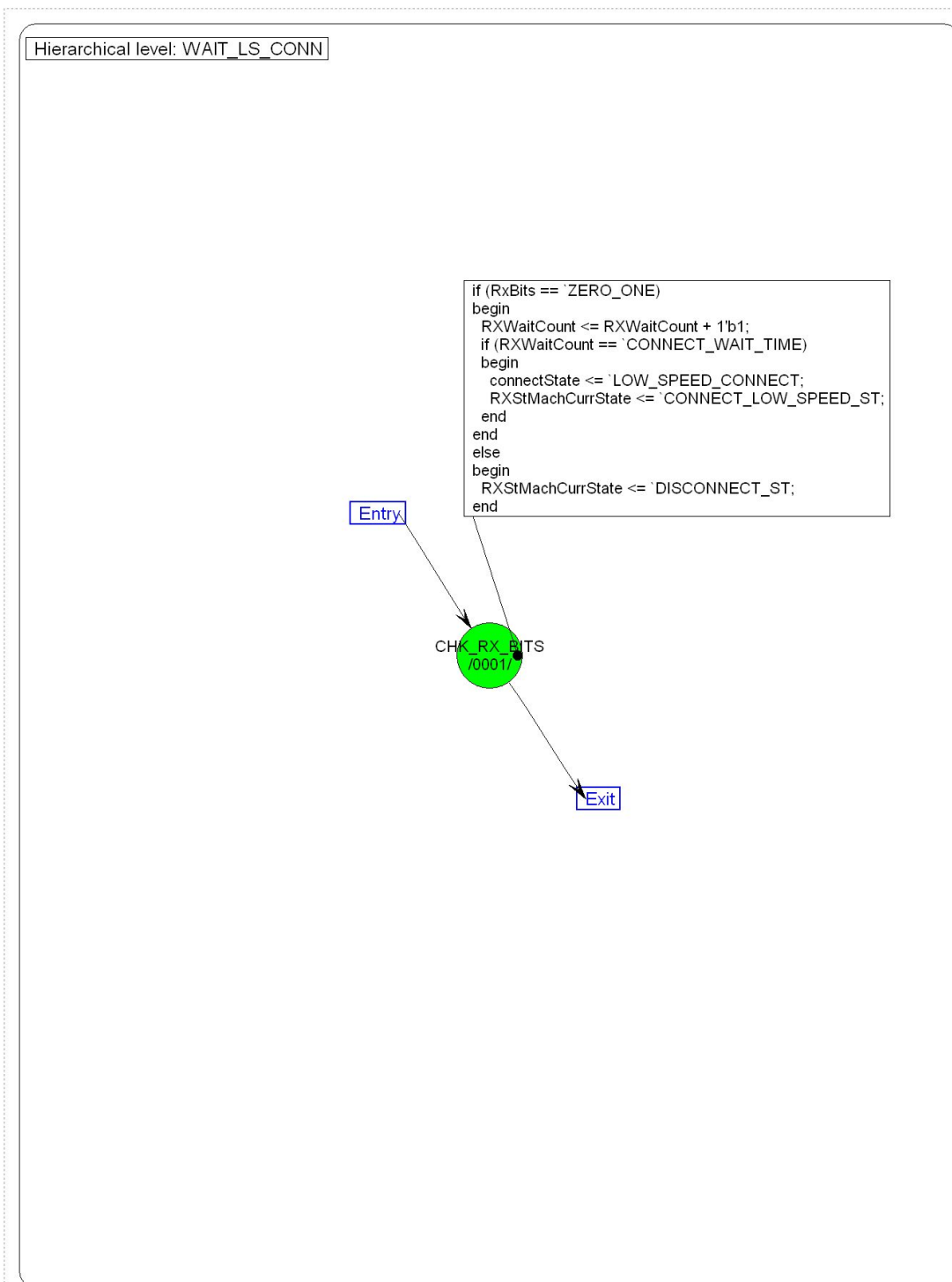
## 2.13.1 DISCNCT



## 2.13.2 WAIT\_FS\_CONN

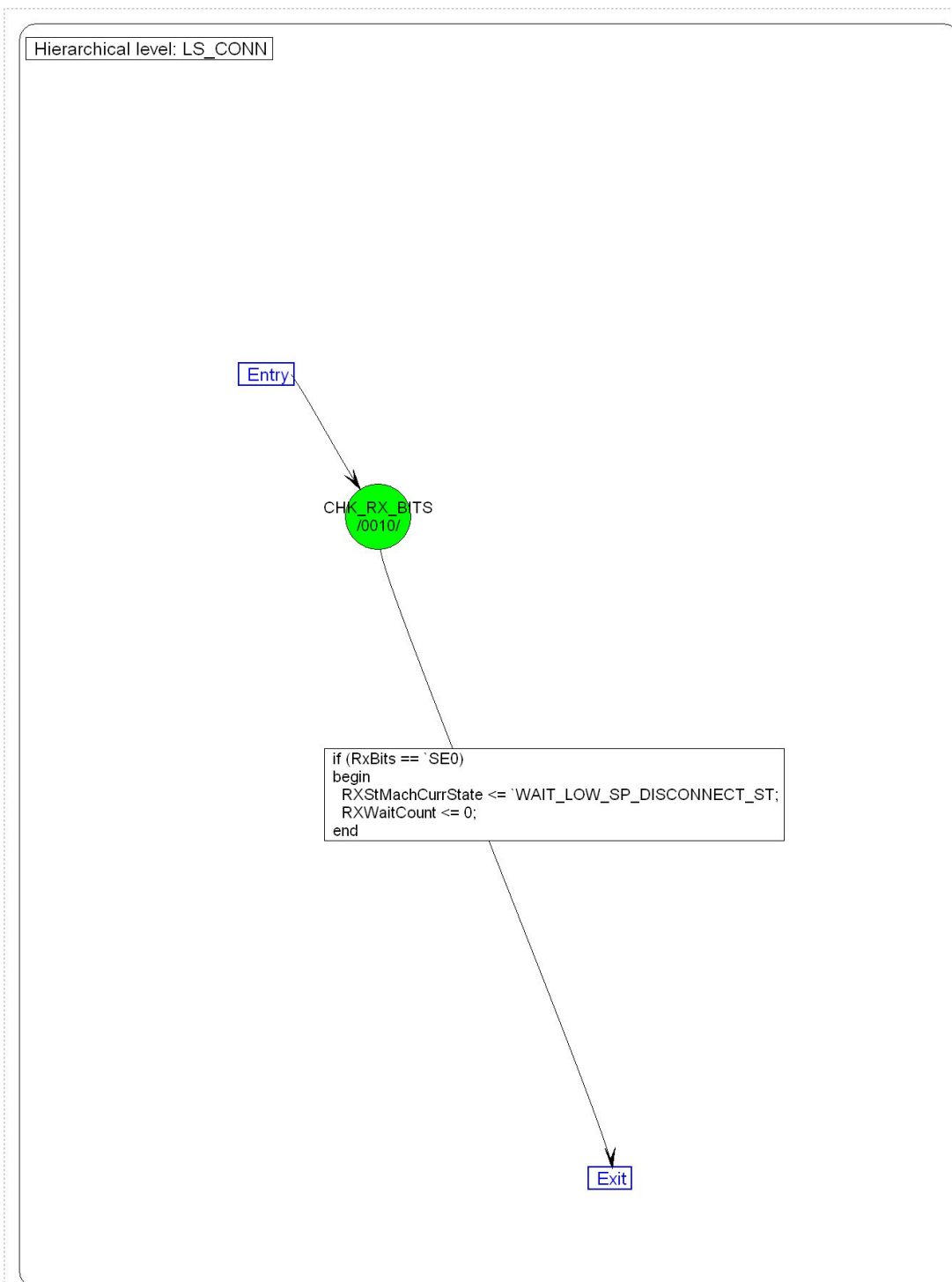


### 2.13.3 WAIT\_LS\_CONN

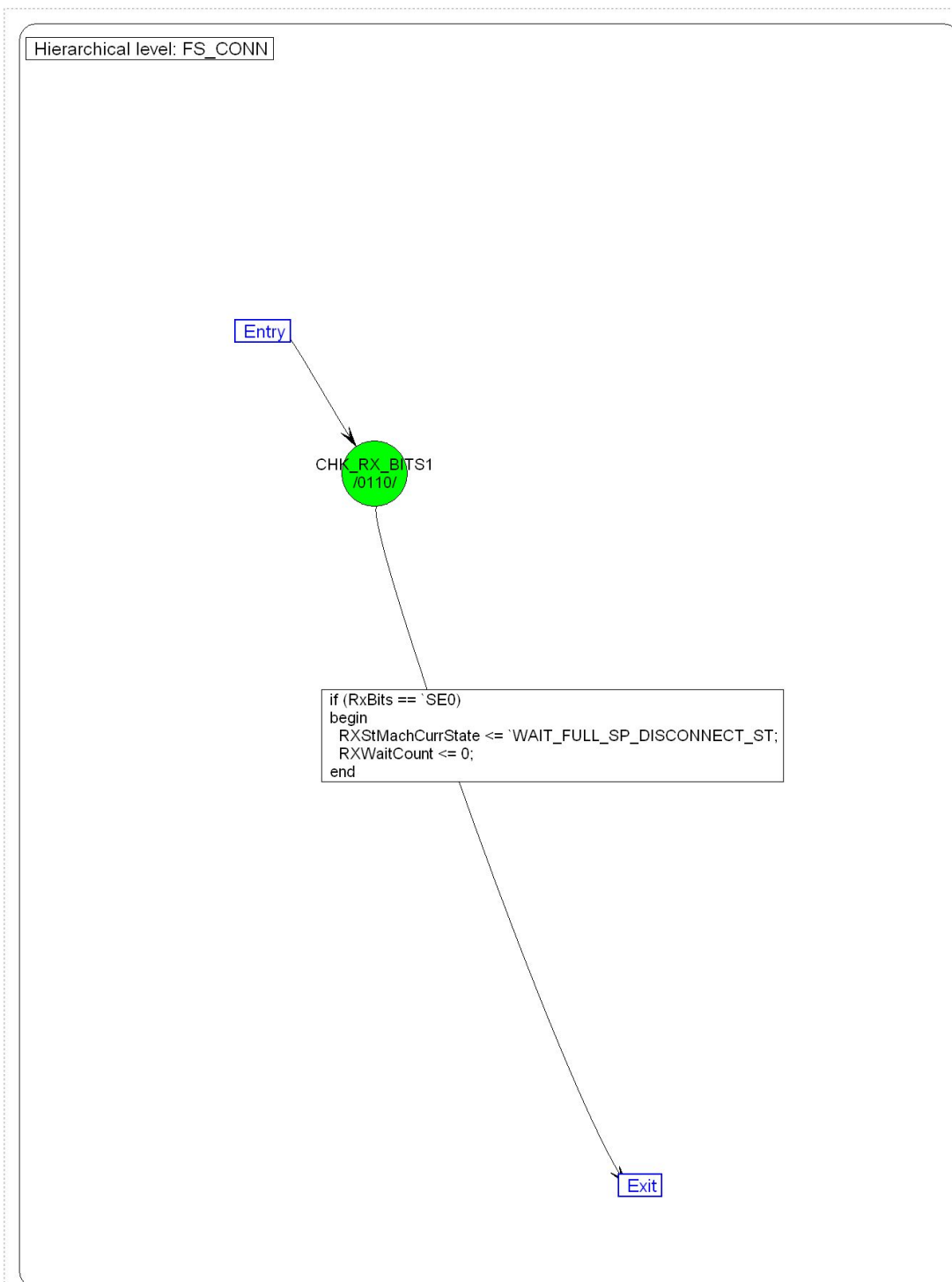




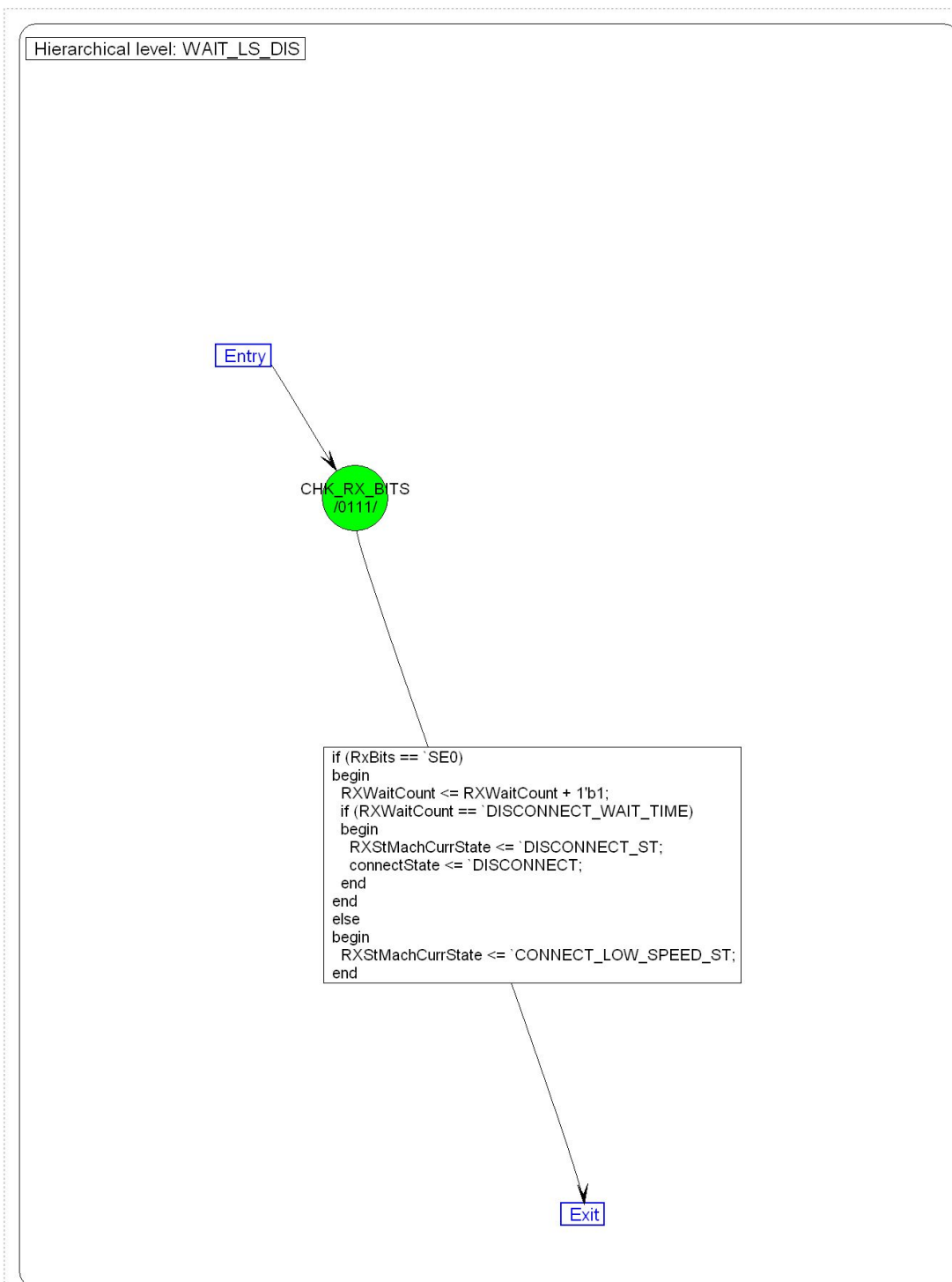
## 2.13.4 LS\_CONN



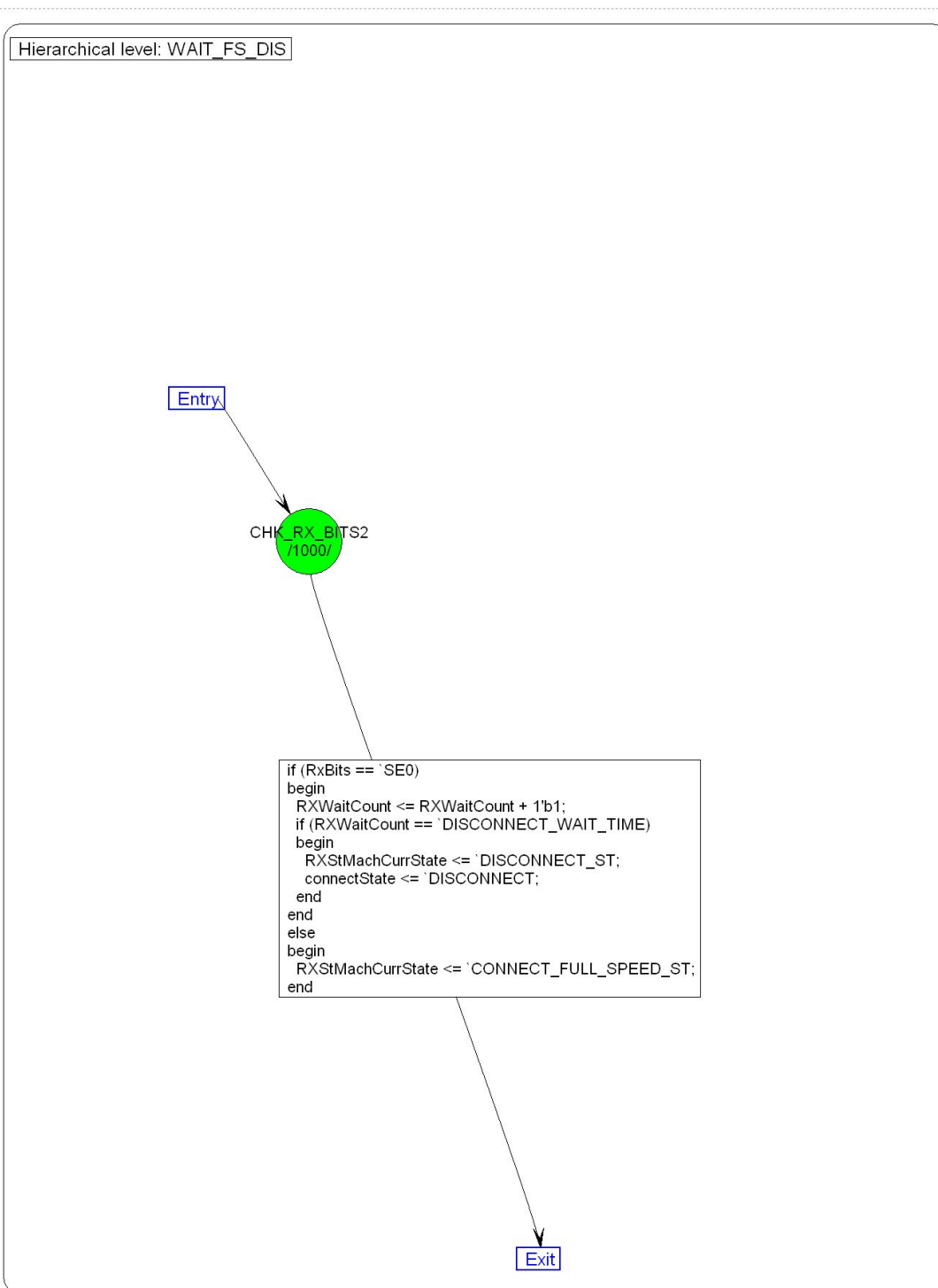
## 2.13.5 FS\_CONN



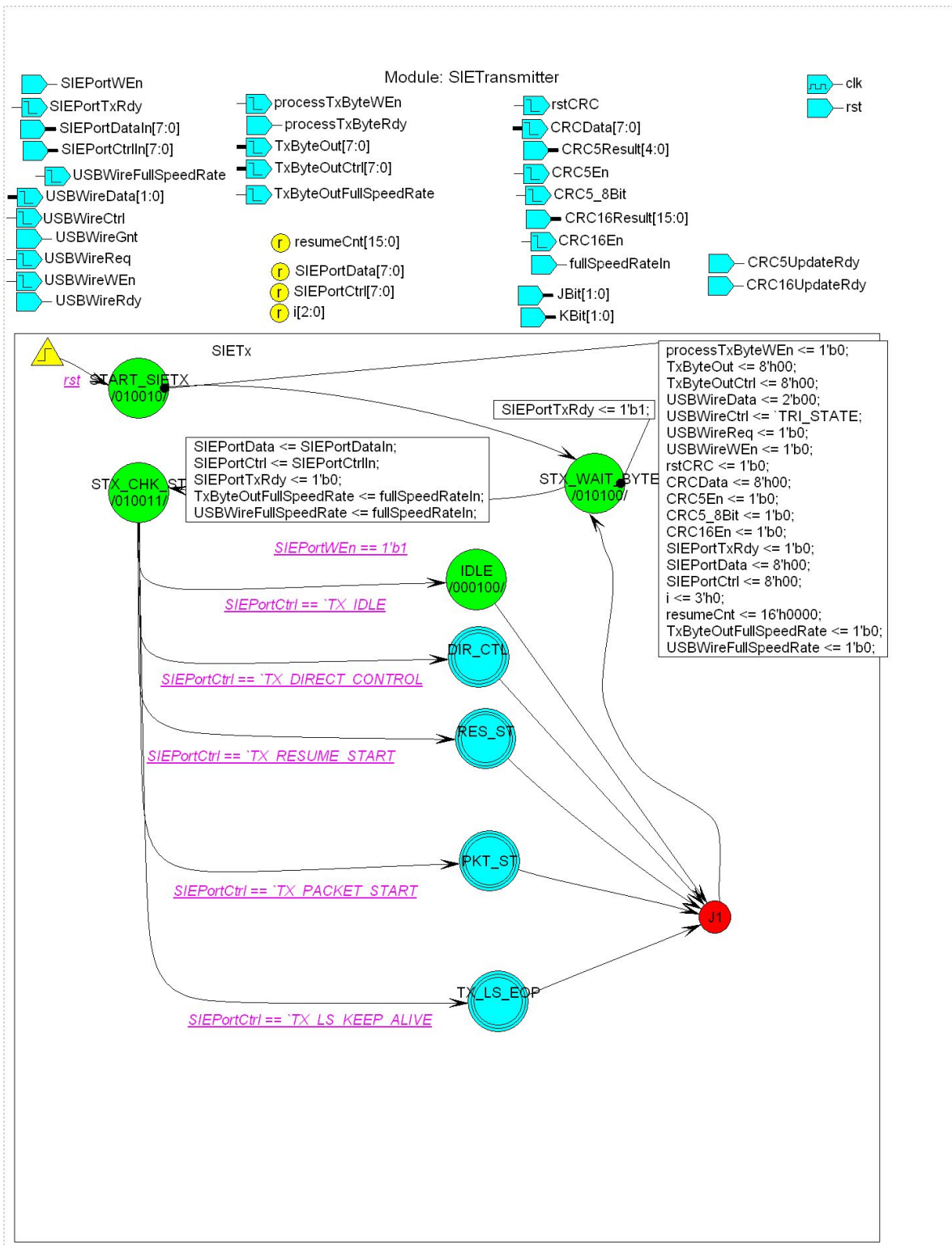
## 2.13.6 WAIT\_LS\_DIS



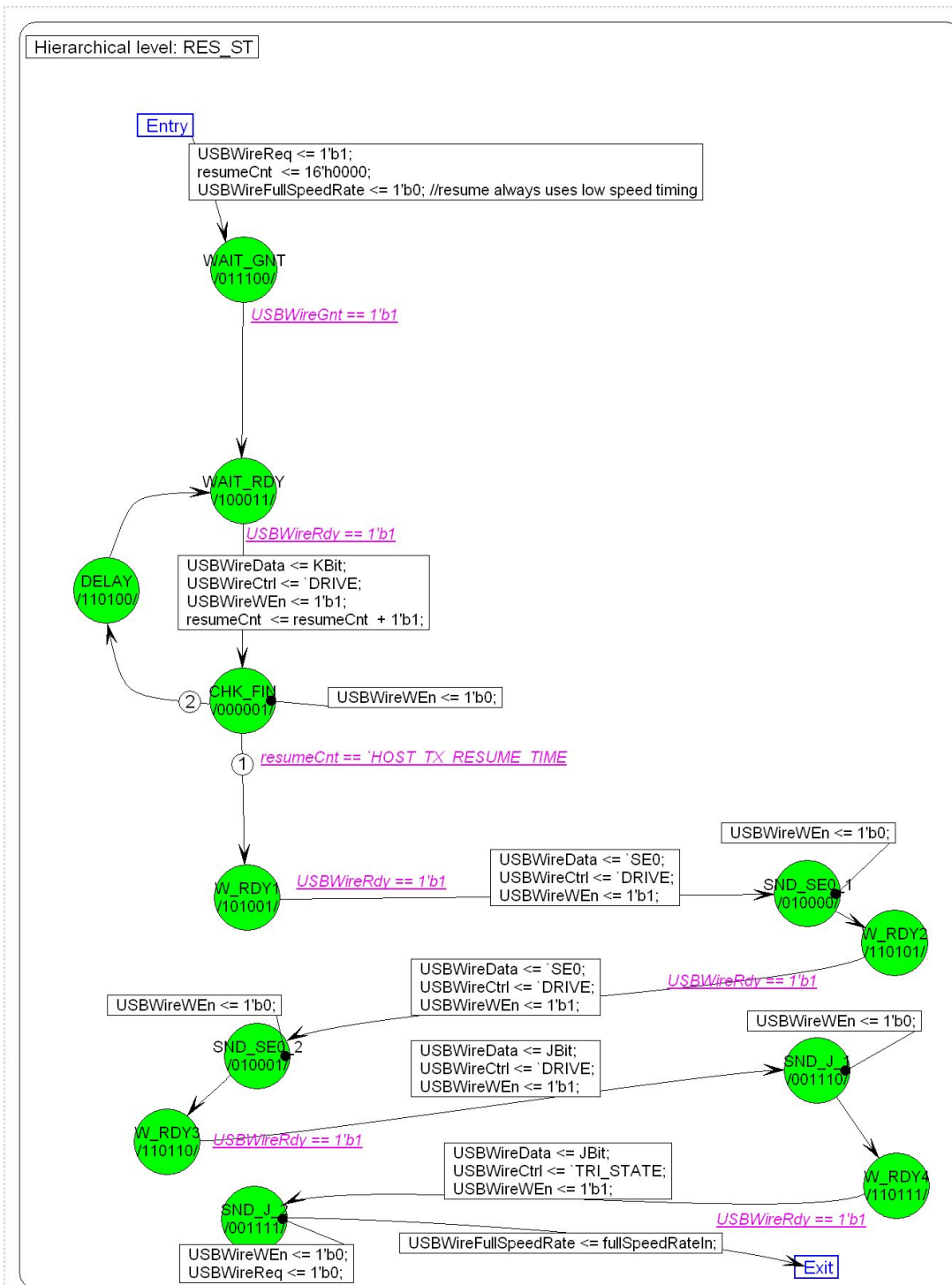
## 2.13.7 WAIT\_FS\_DIS



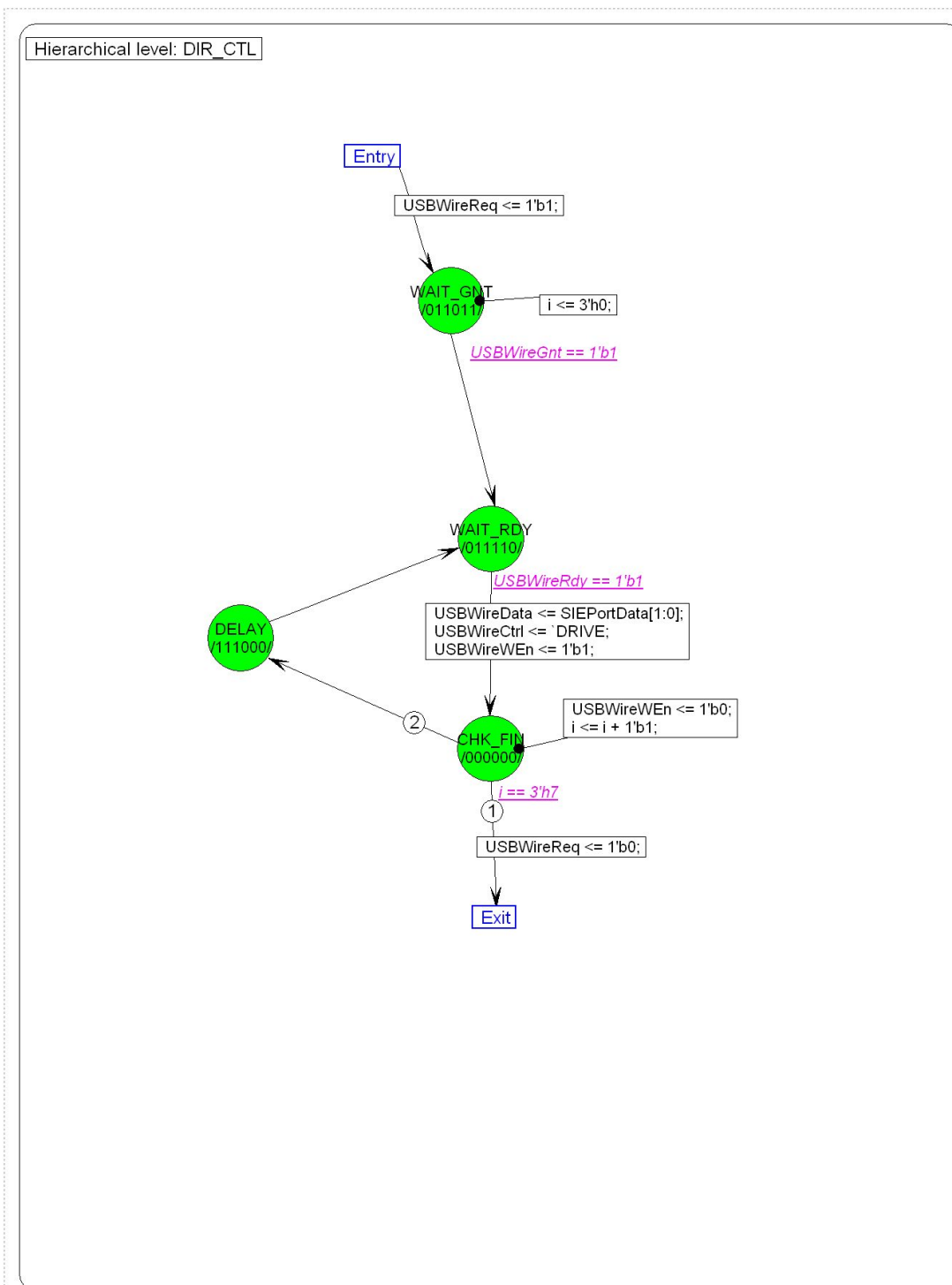
## 2.14 SIETransmitter.asf



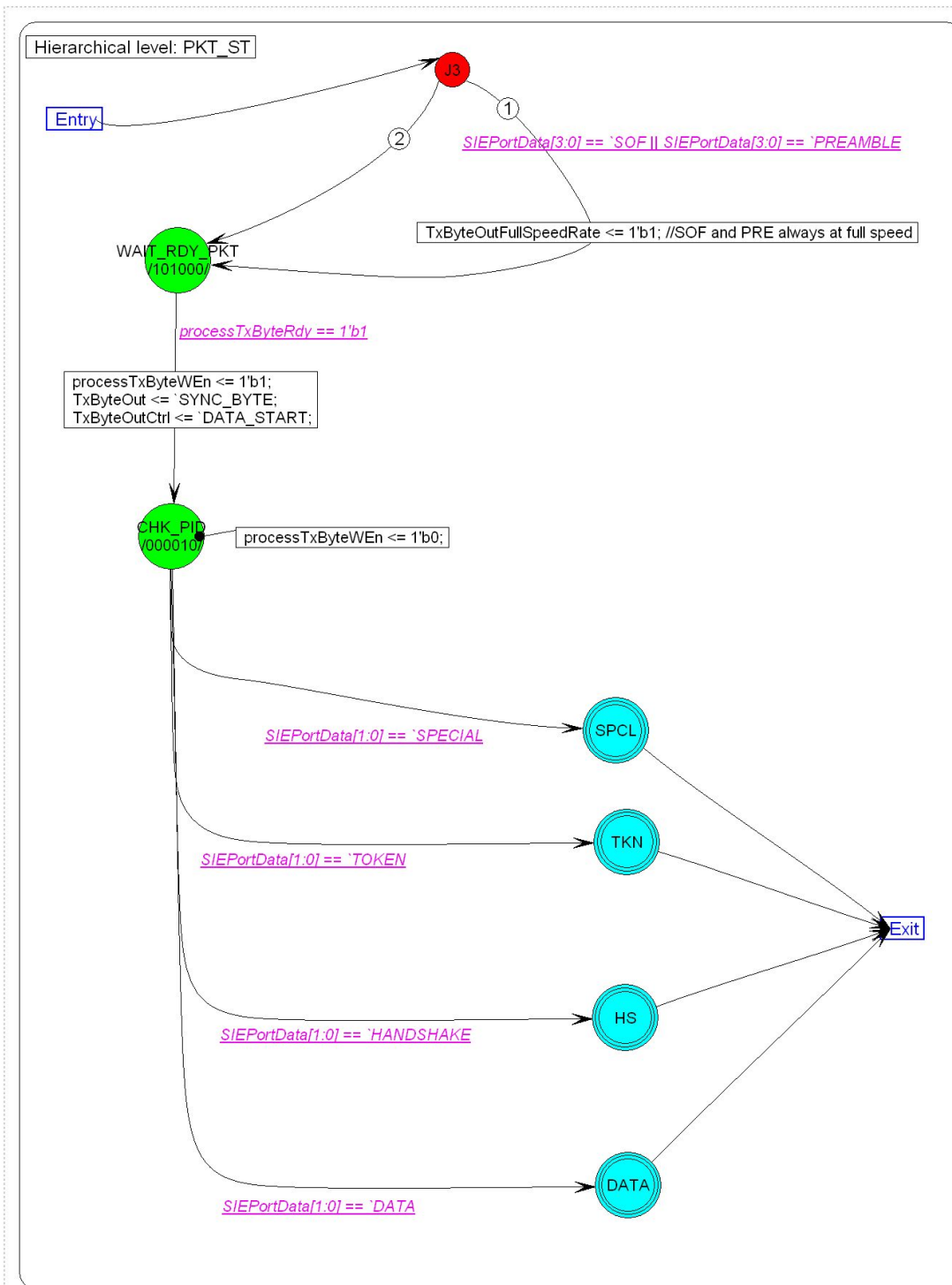
## 2.14.1 RES\_ST



## 2.14.2 DIR\_CTL

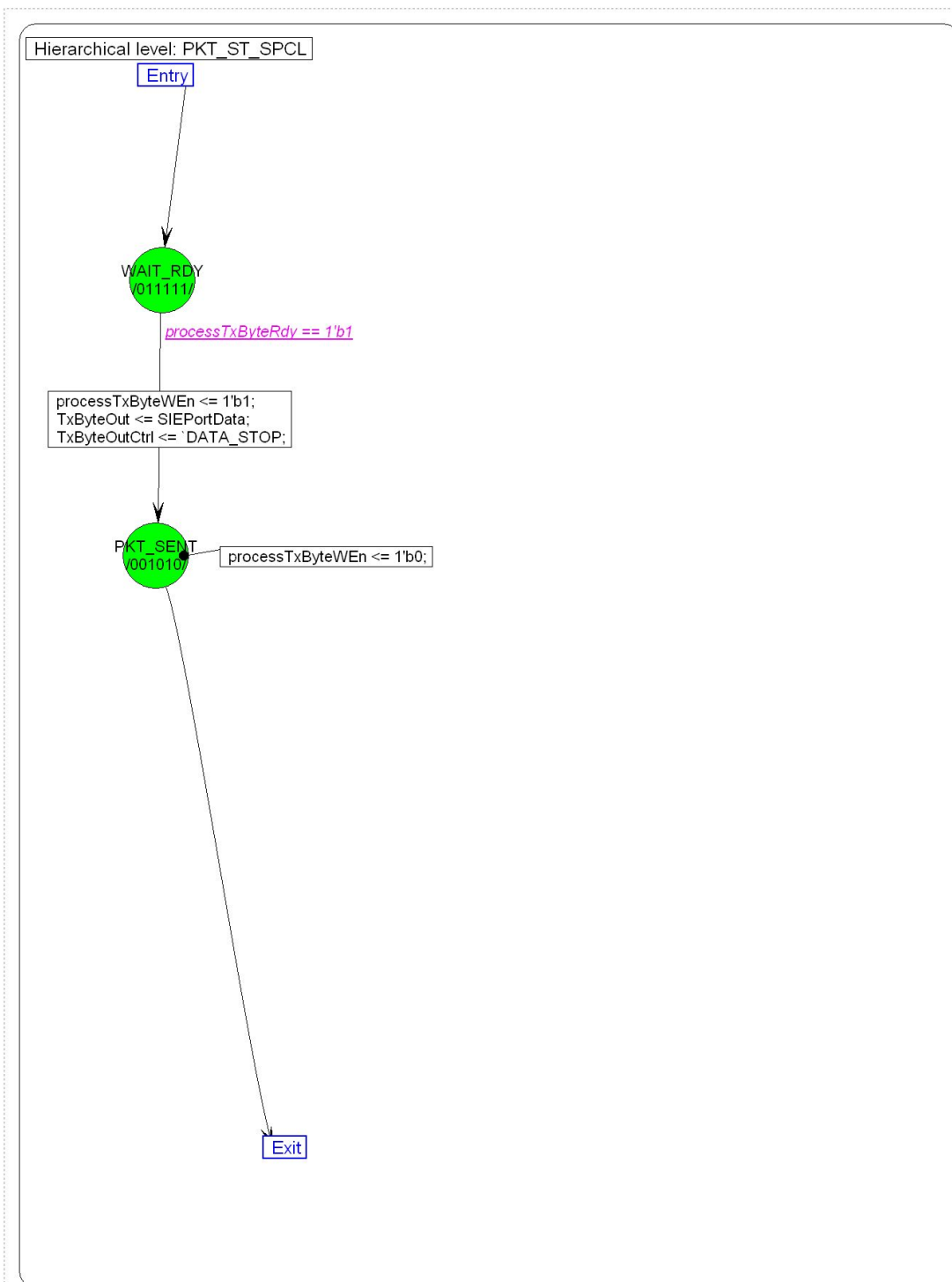


### 2.14.3 PKT\_ST

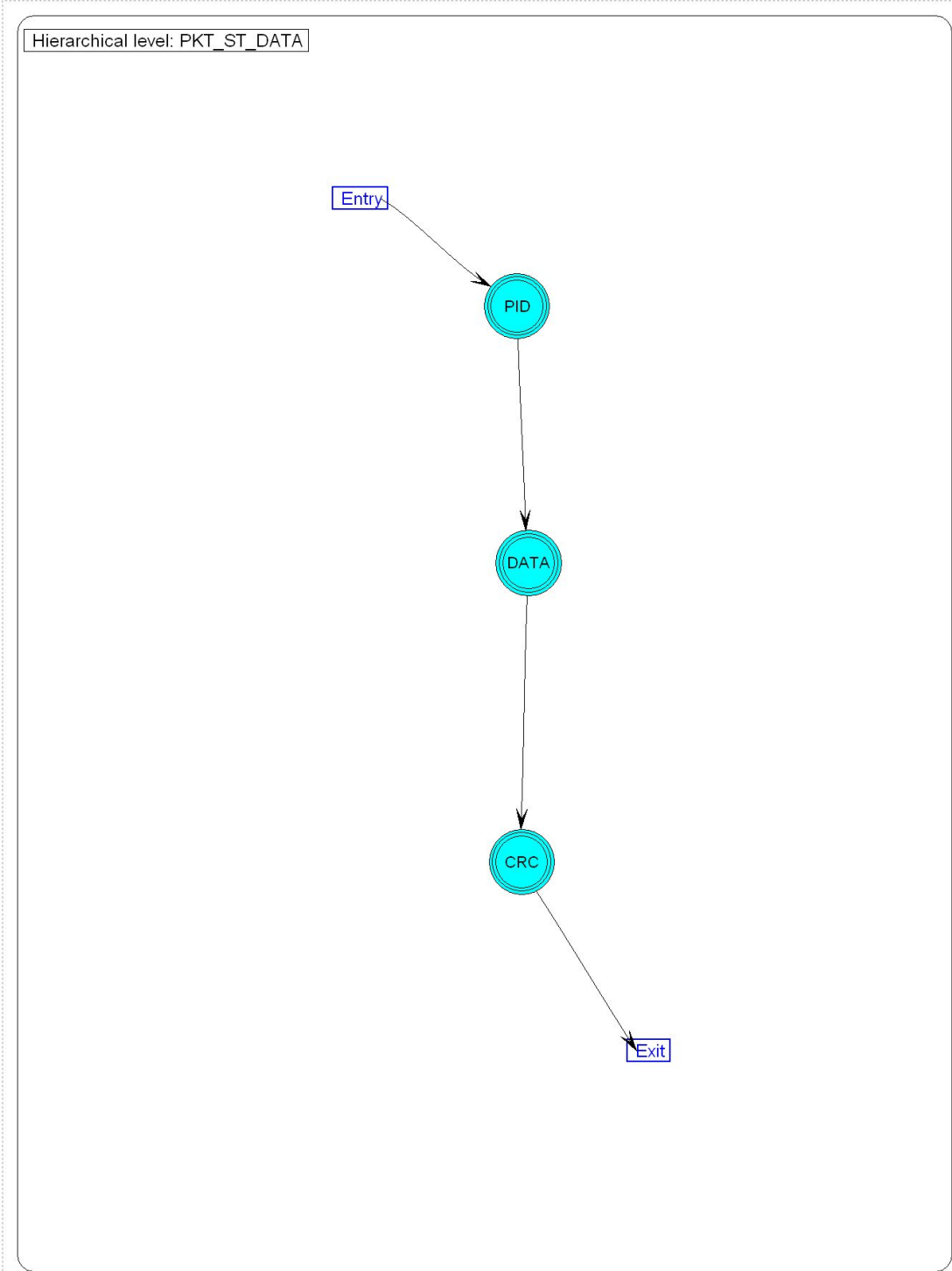




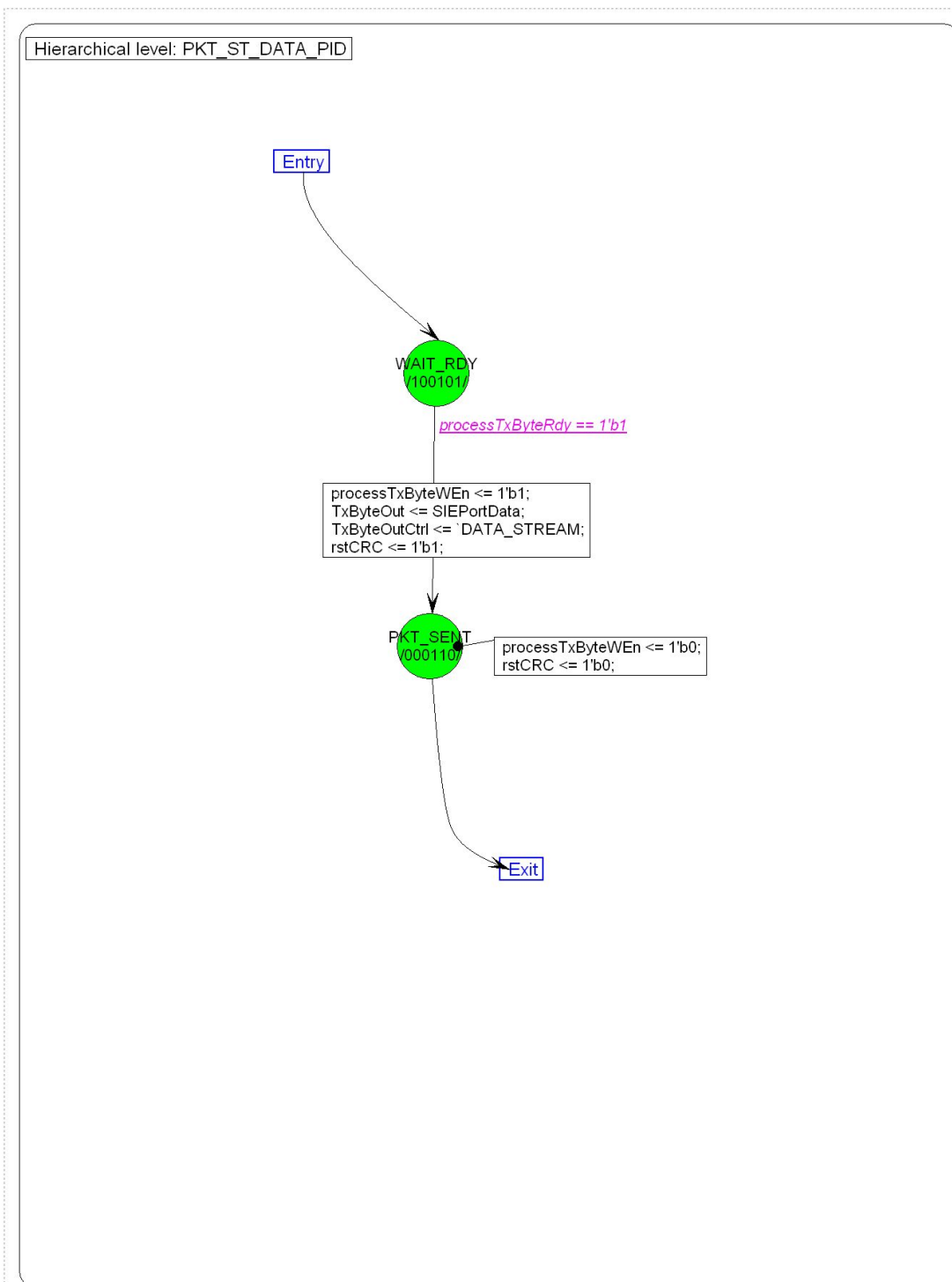
### 2.14.3.1 SPCL



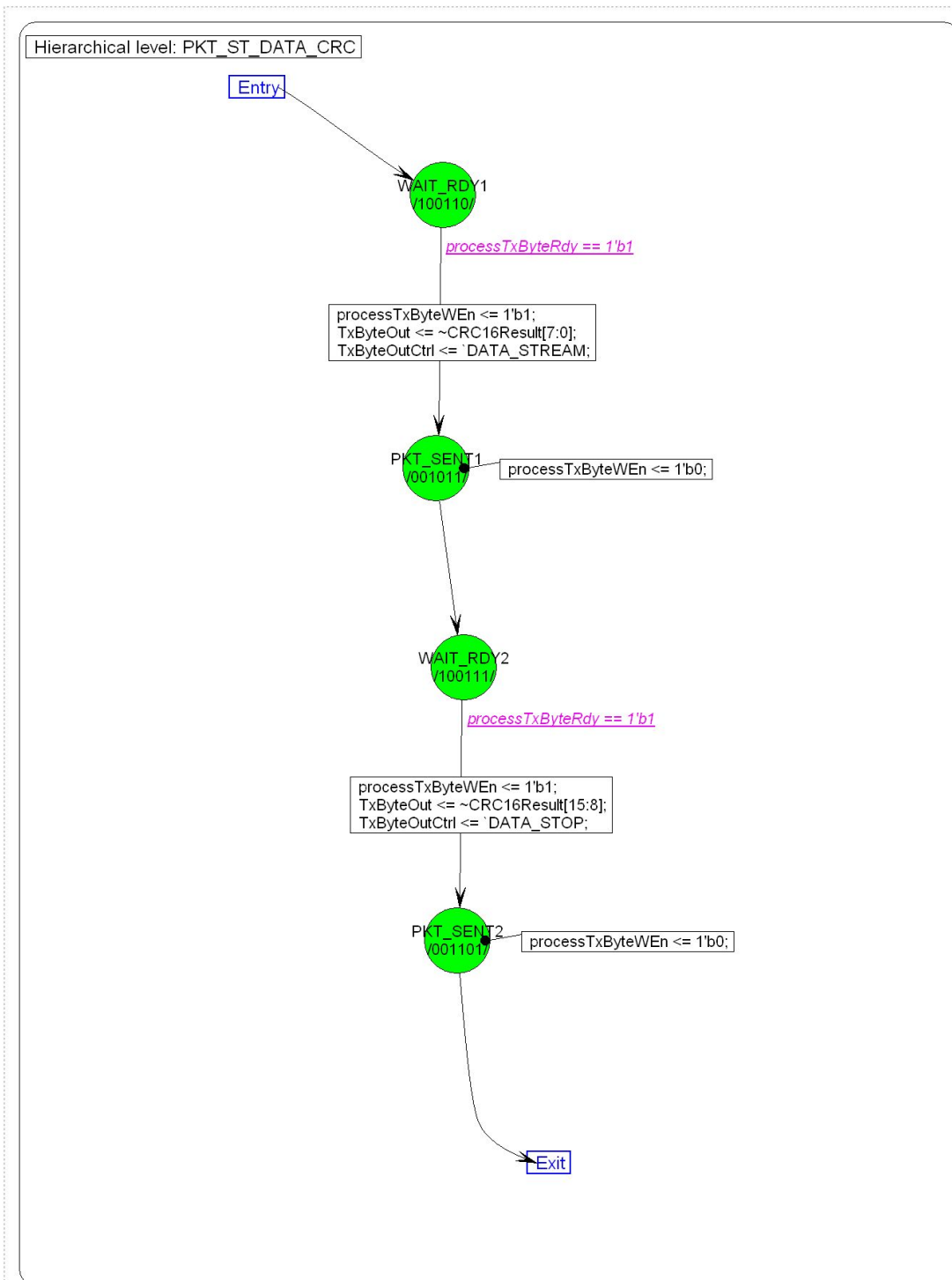
2.14.3.2 DATA



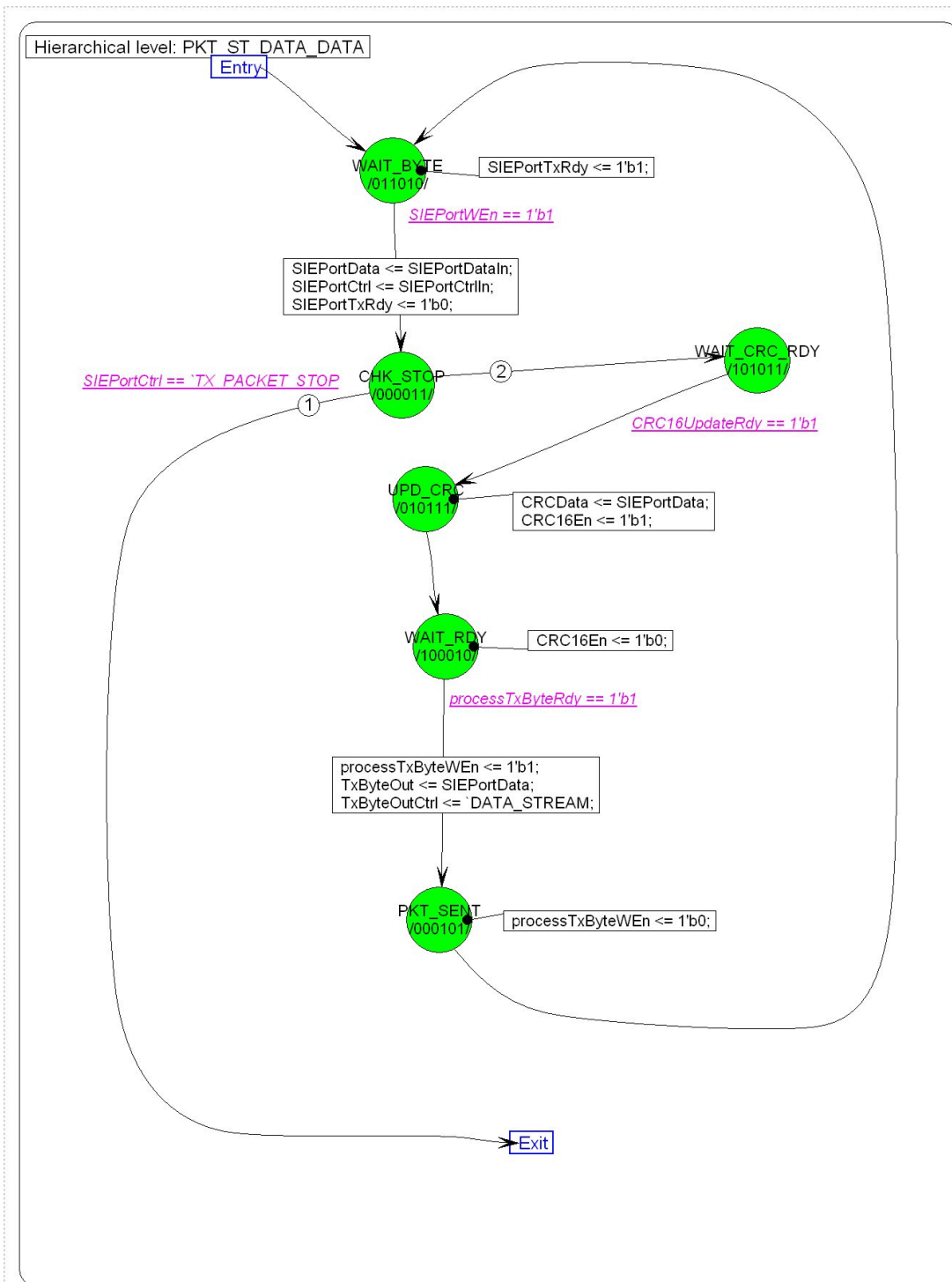
### 2.14.3.2.1 PID



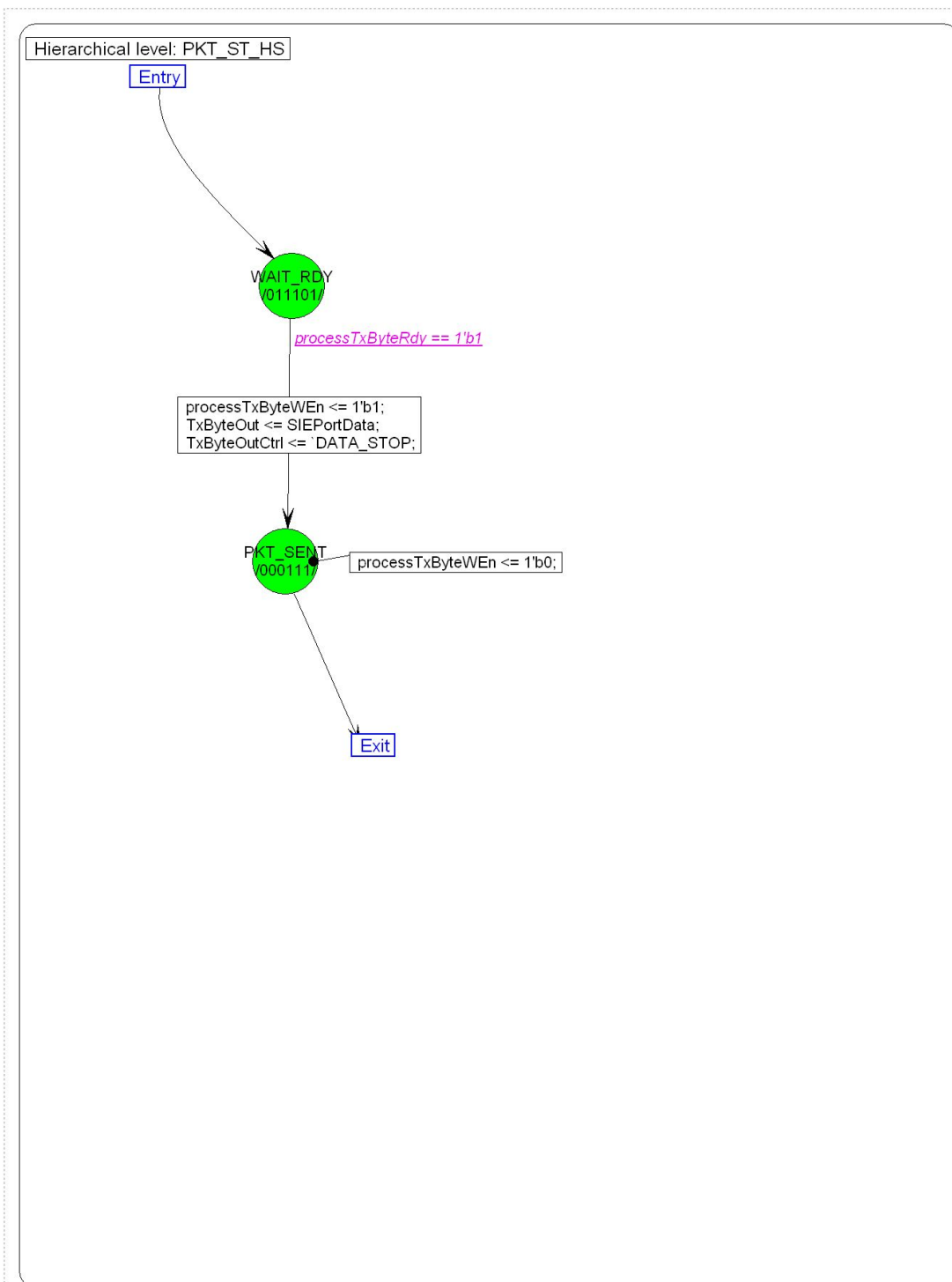
### 2.14.3.2.2 CRC



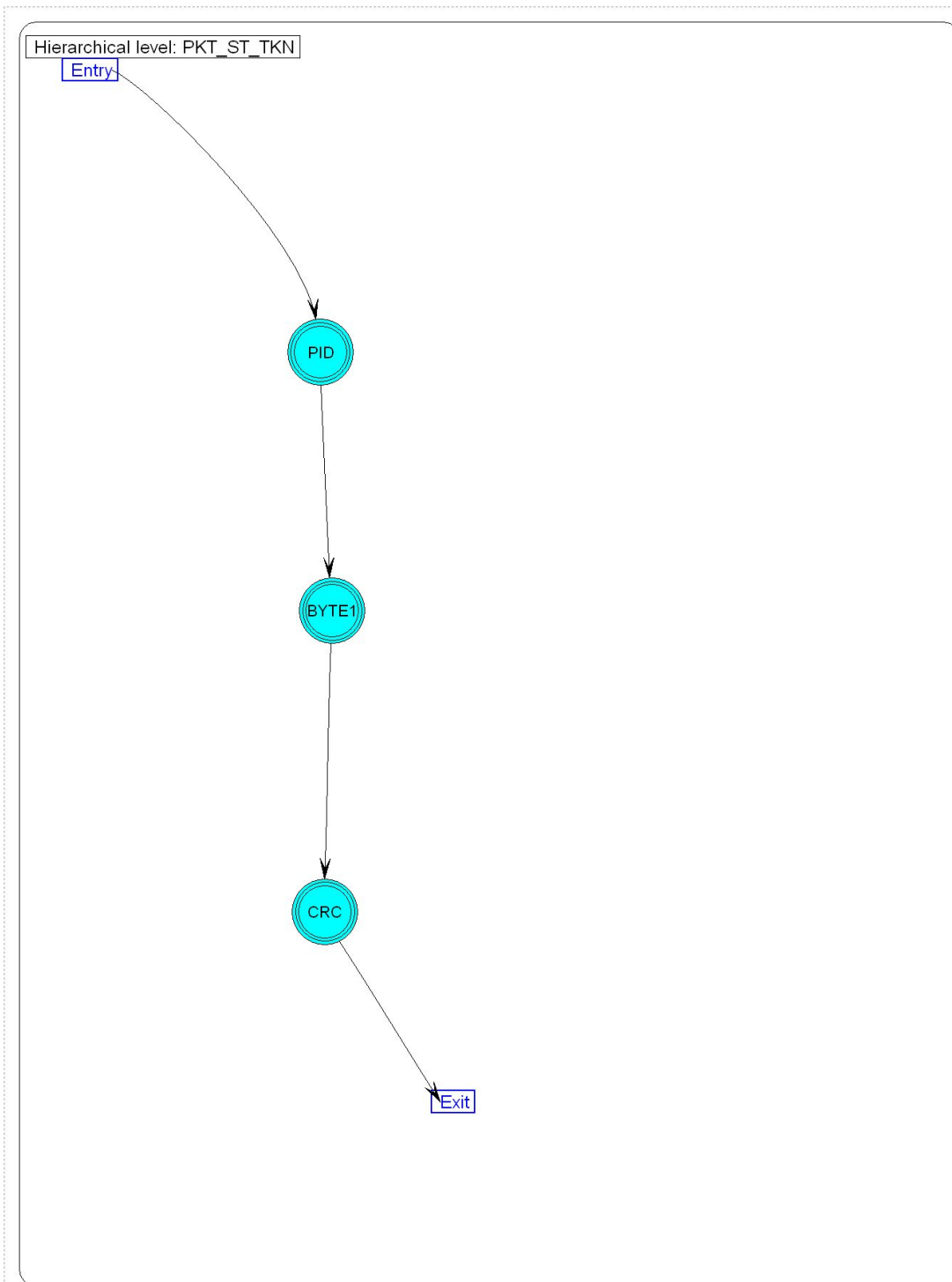
### 2.14.3.2.3 DATA



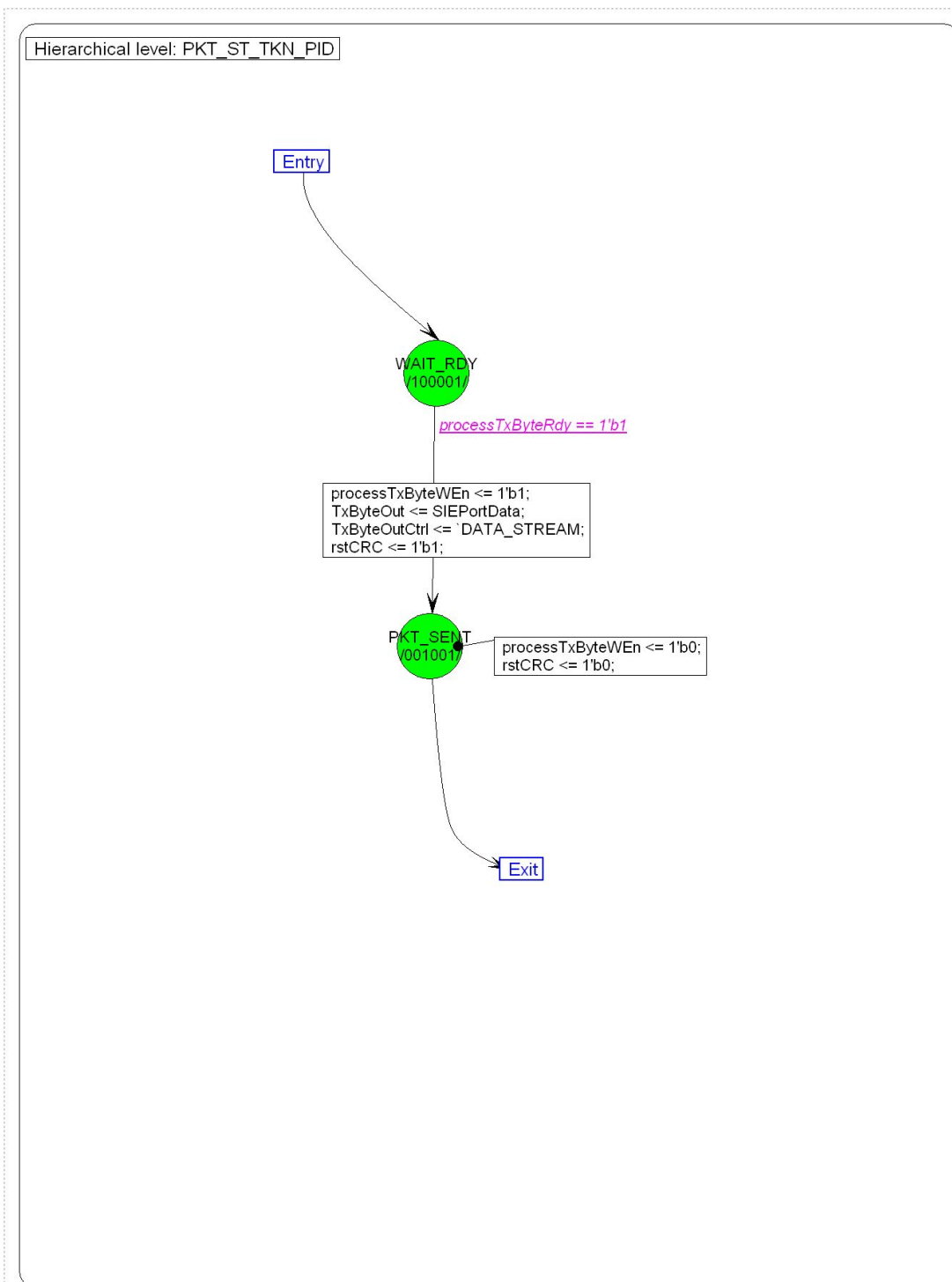
### 2.14.3.3 HS



### 2.14.3.4 TKN

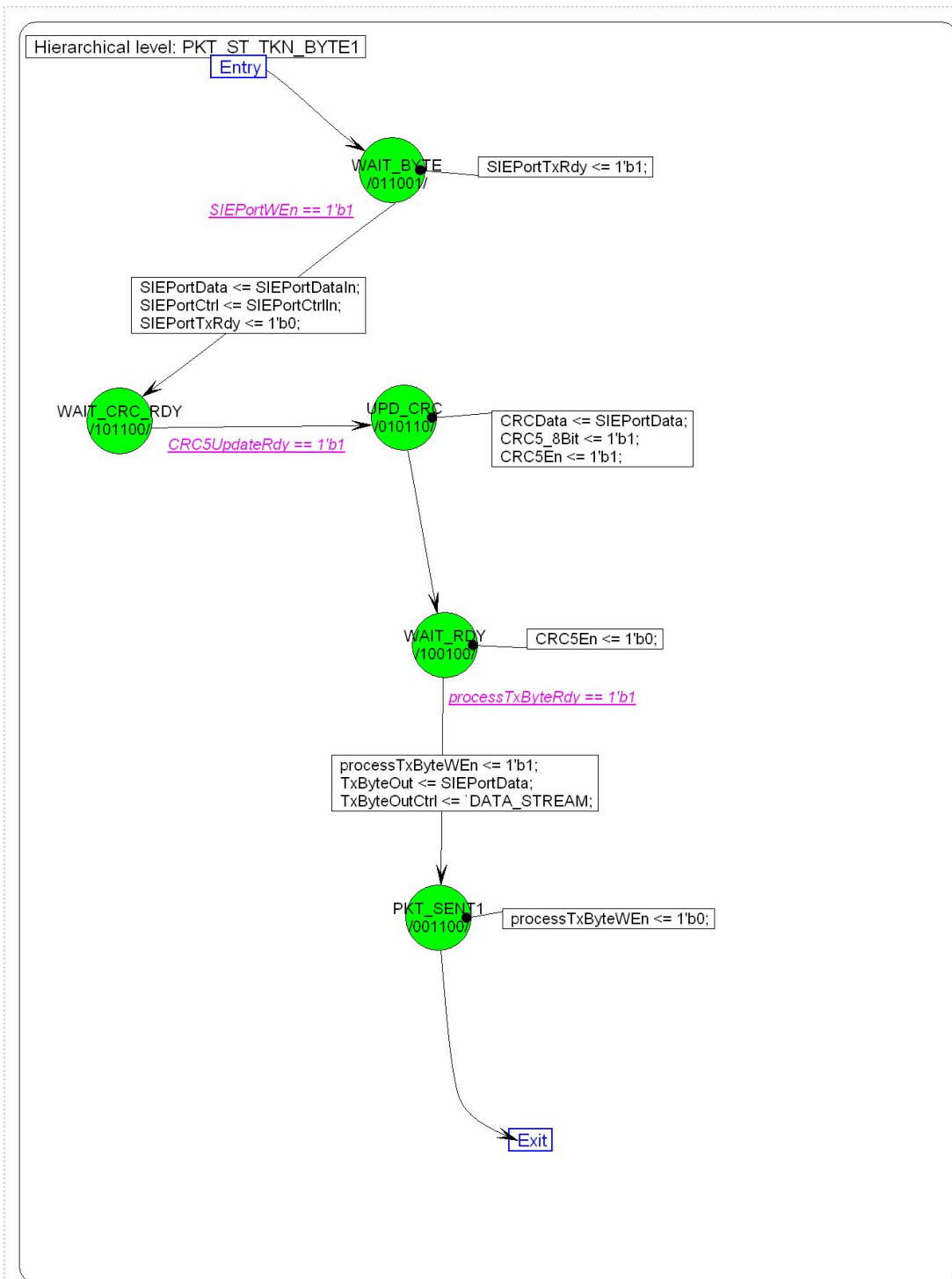


### 2.14.3.4.1 PID

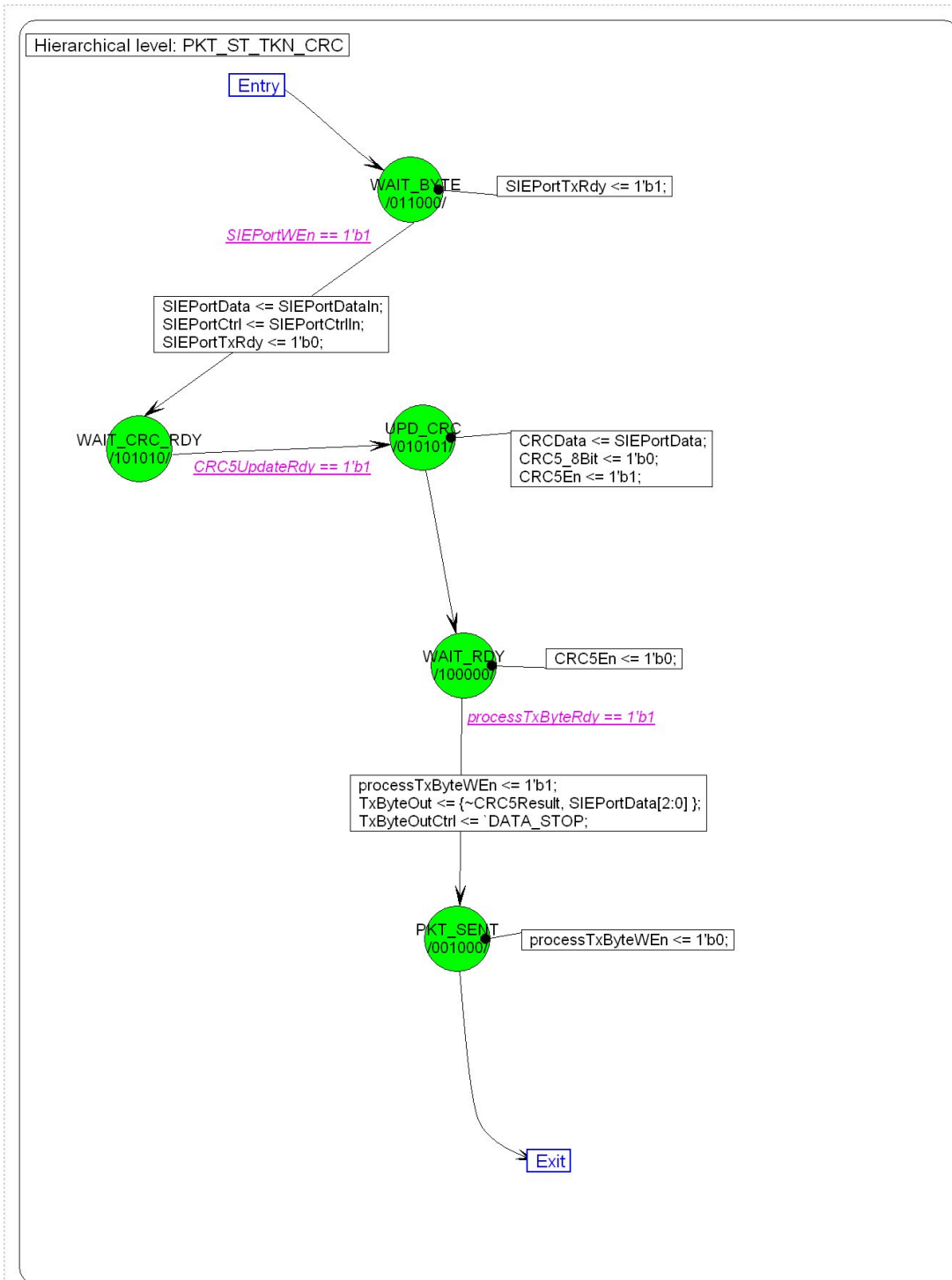




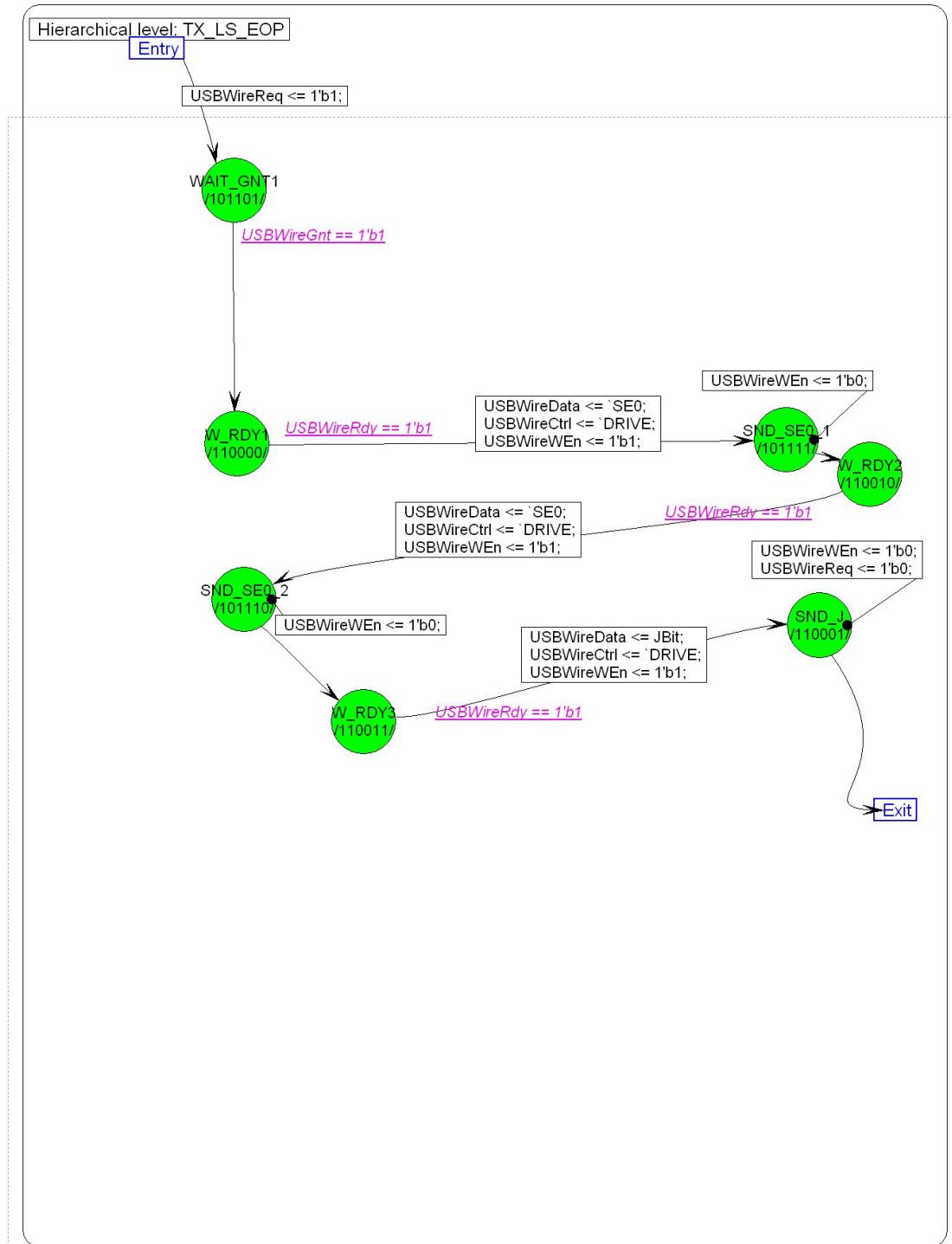
2.14.3.4.2 BYTE1



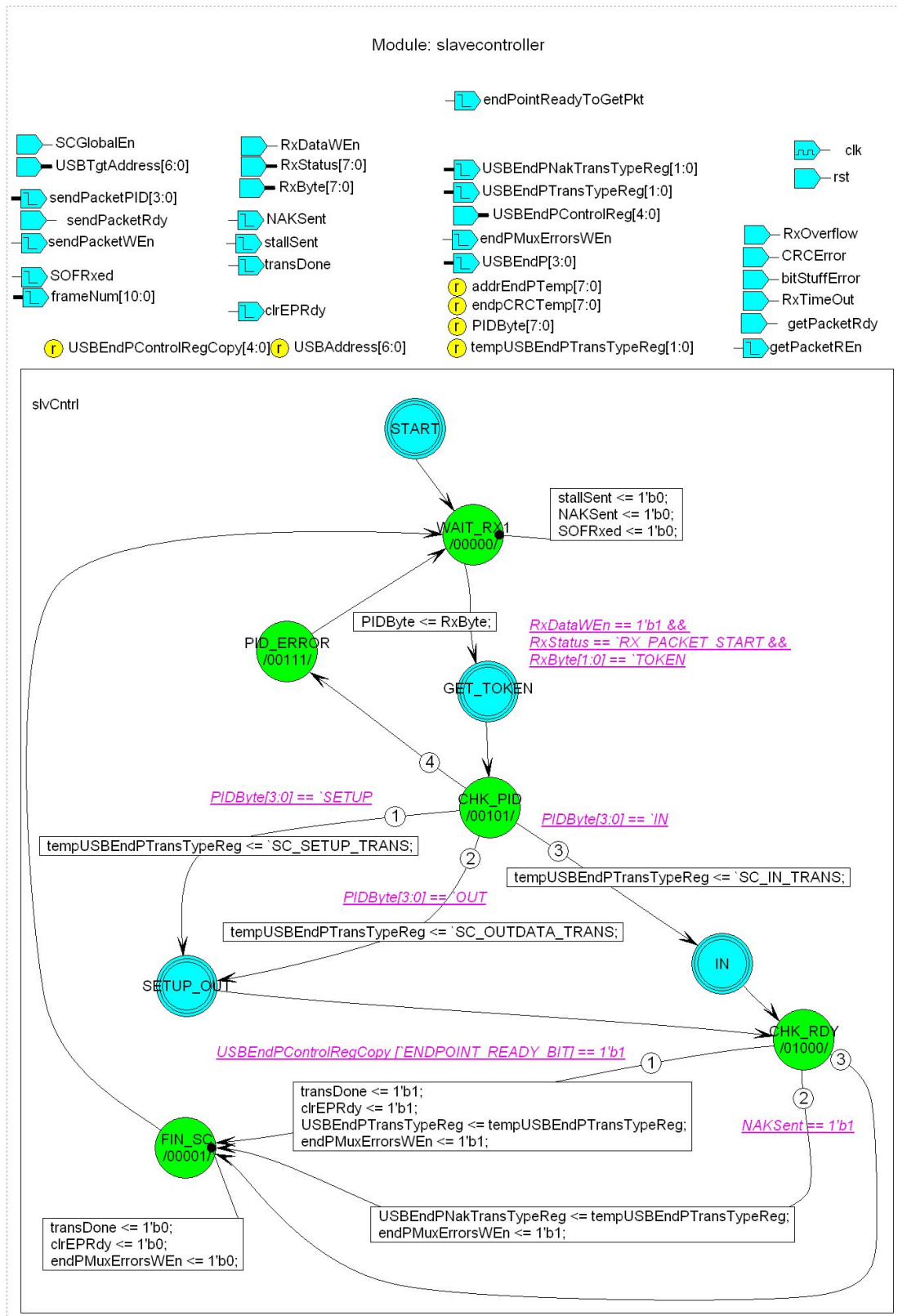
### 2.14.3.4.3 CRC



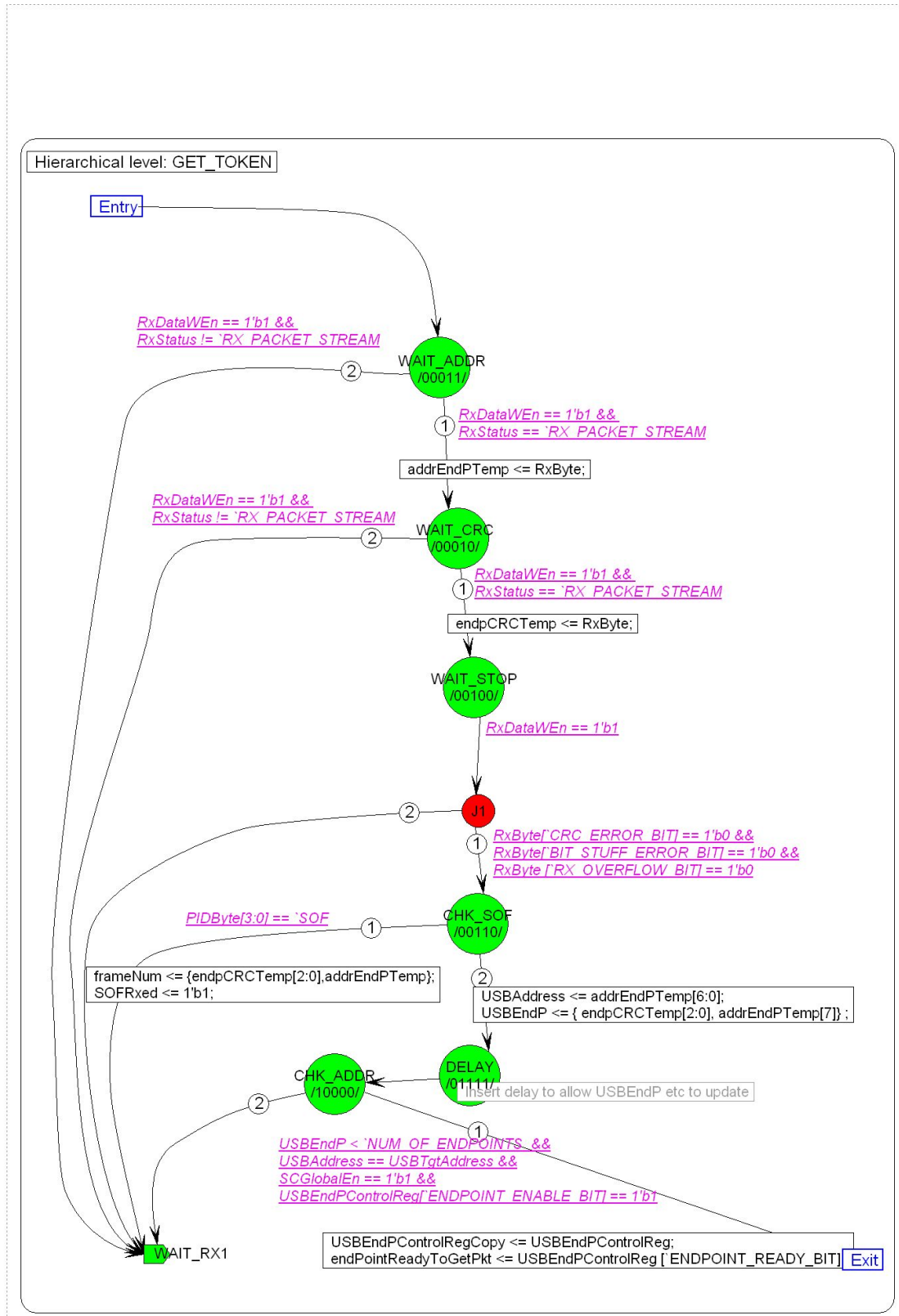
## 2.14.4 TX\_LS\_EOP



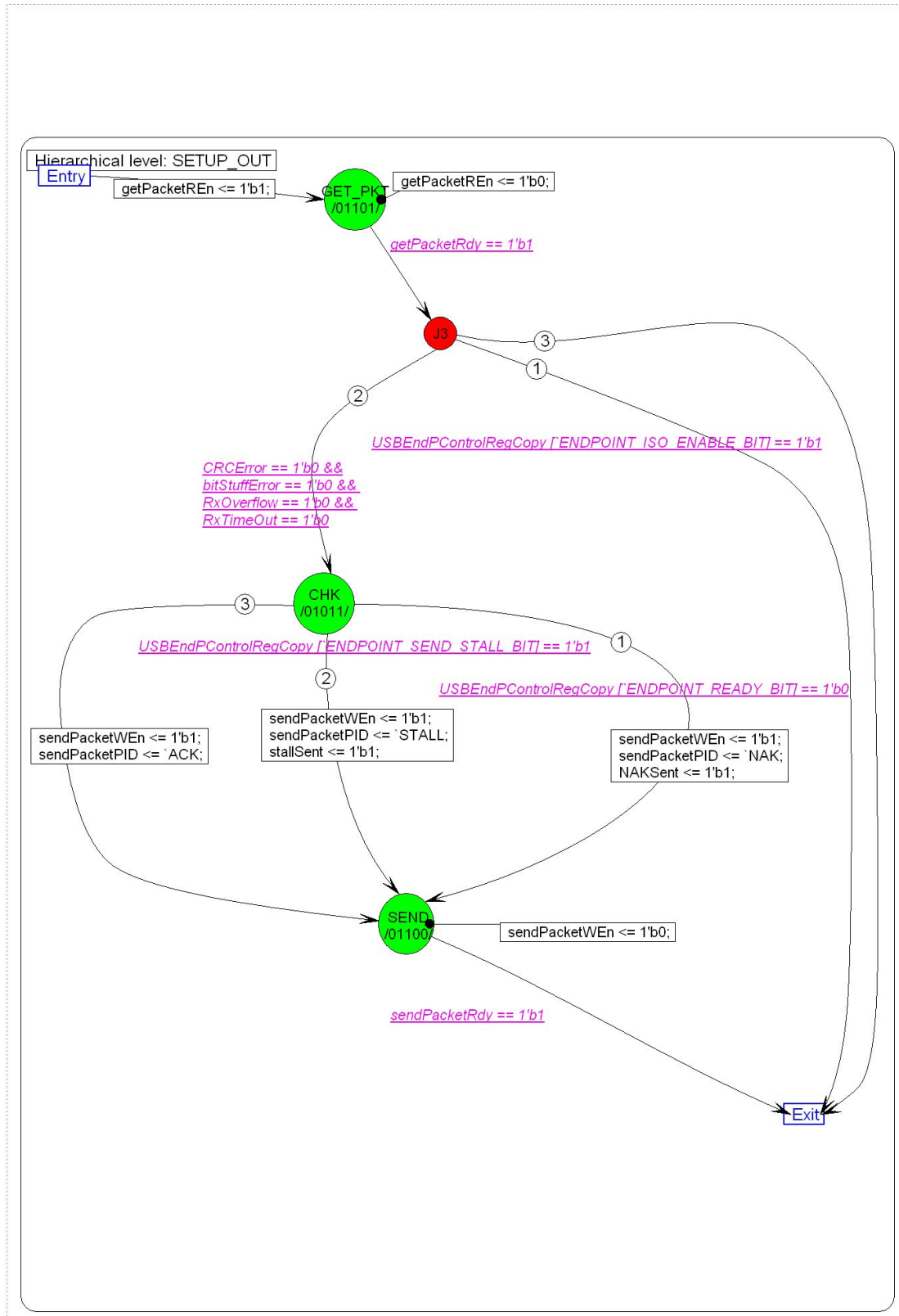
## 2.15 slavecontroller.asf



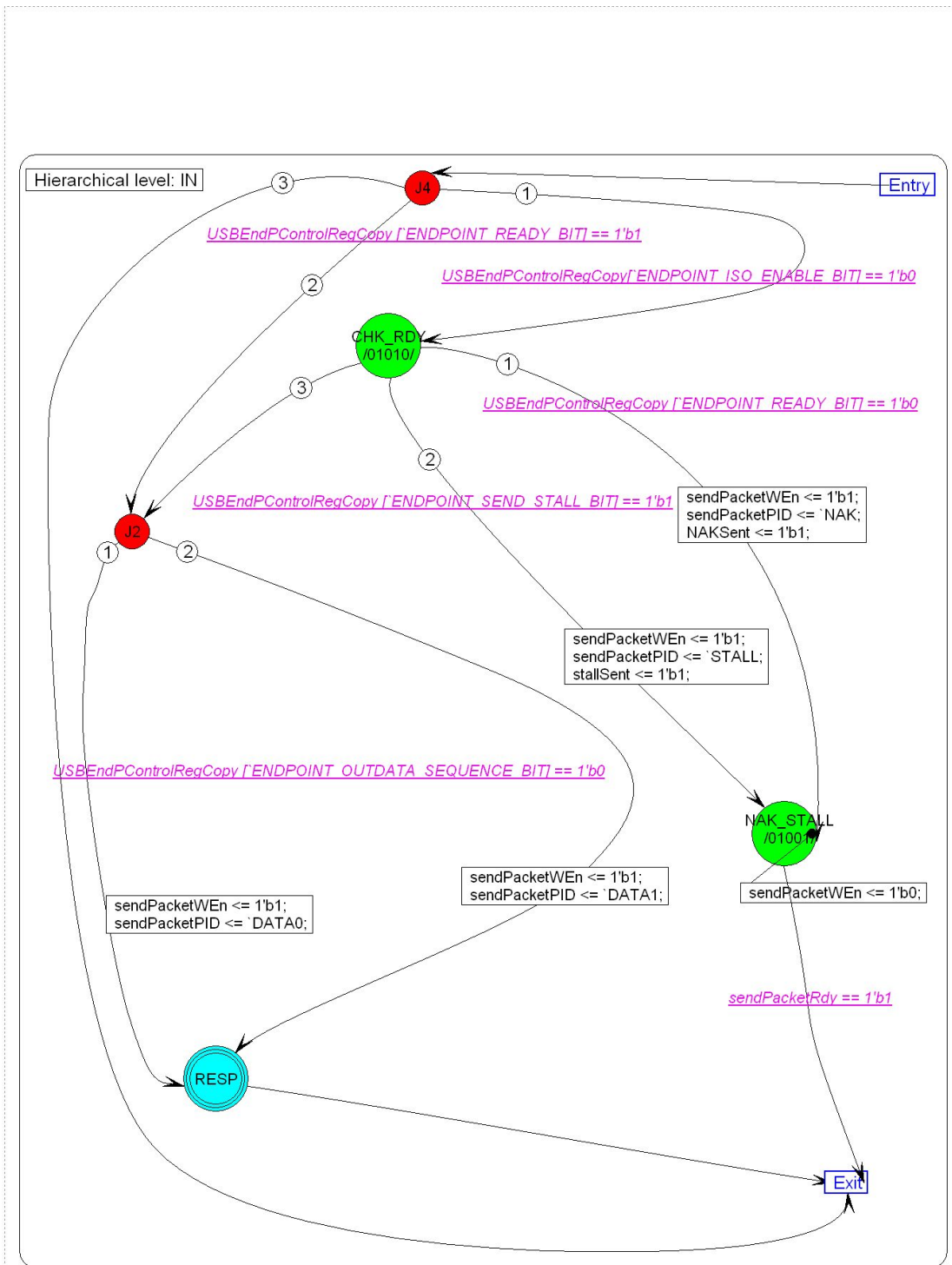
## 2.15.1 GET\_TOKEN



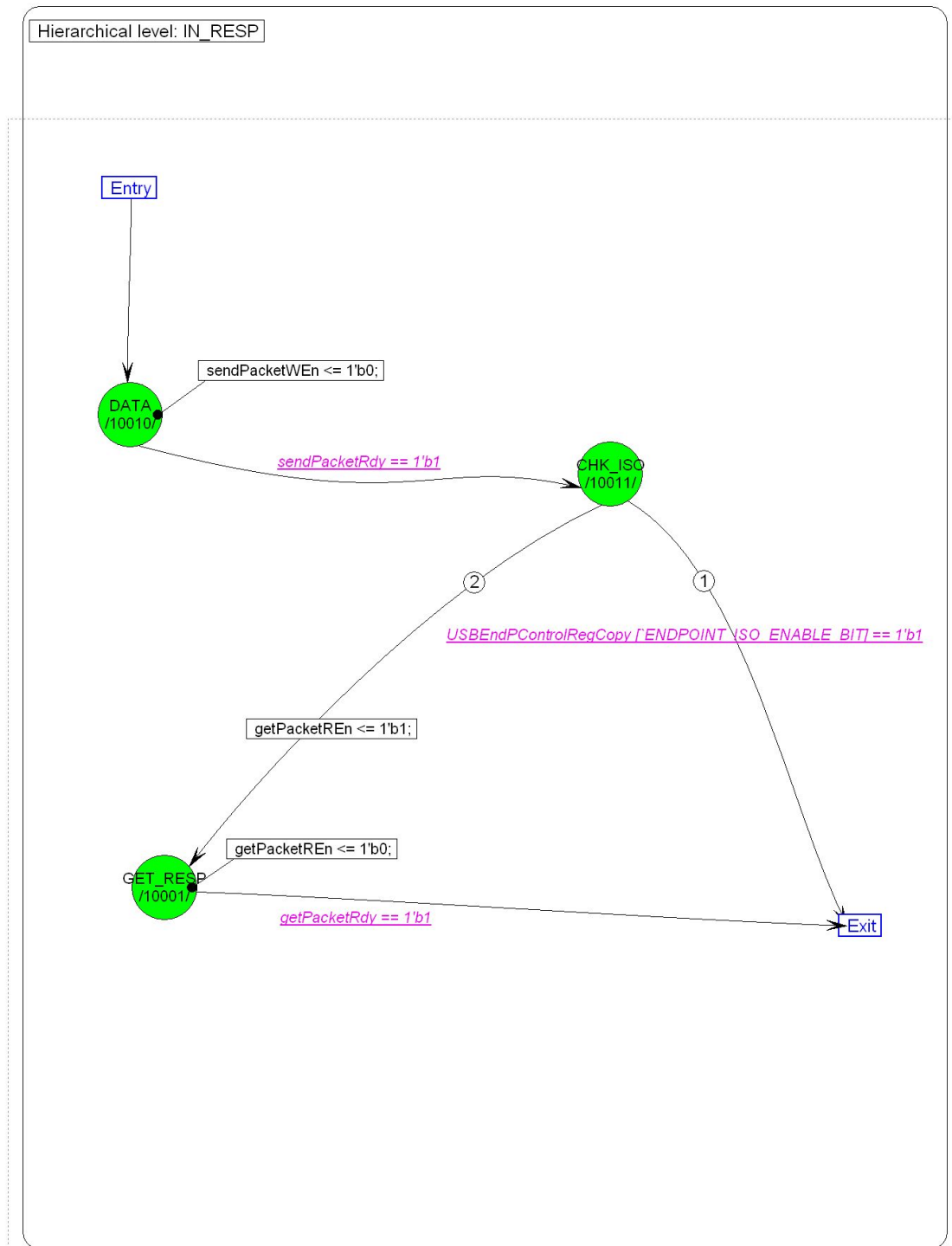
## 2.15.2 SETUP\_OUT



2.15.3 IN

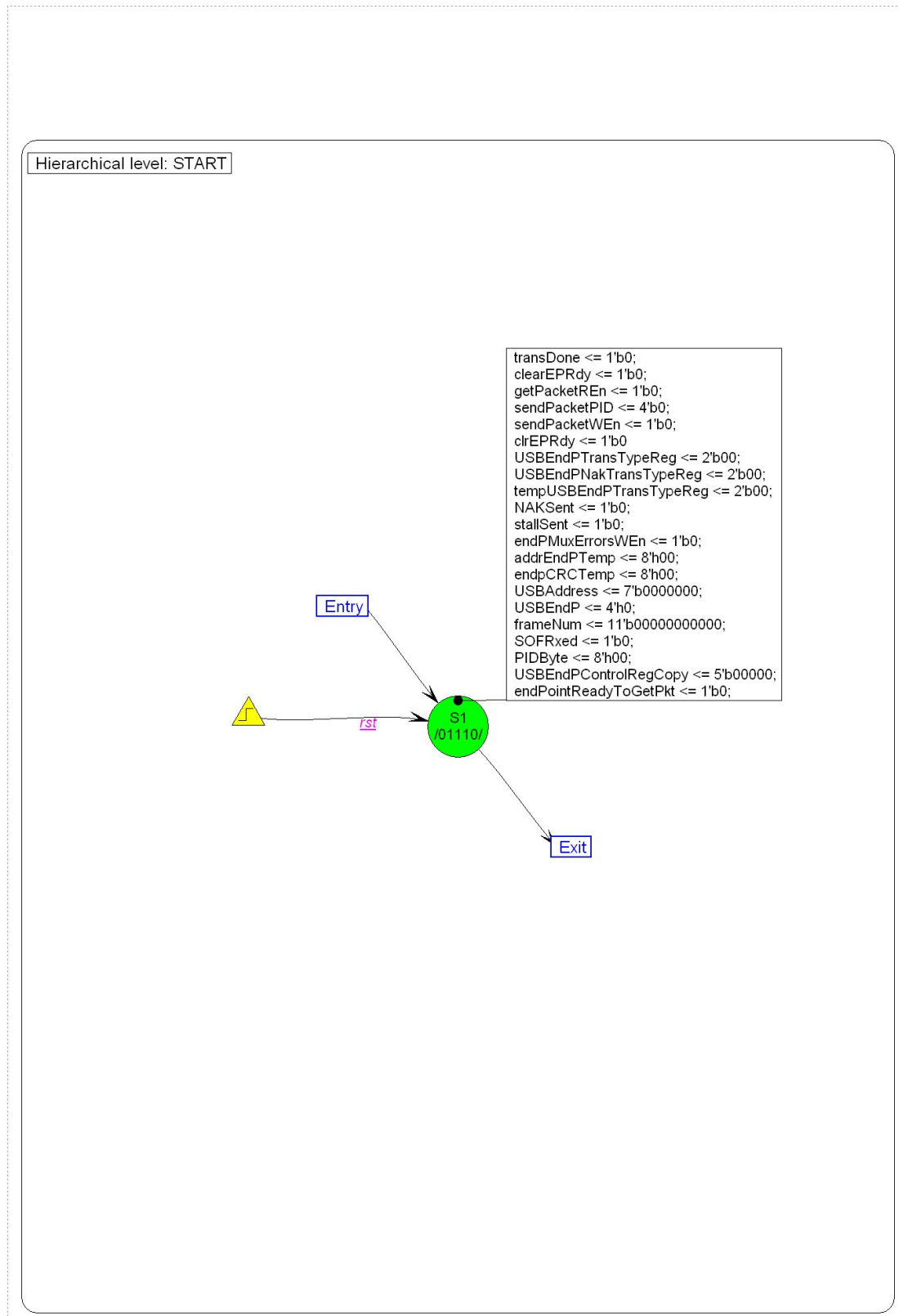


### 2.15.3.1 RESP

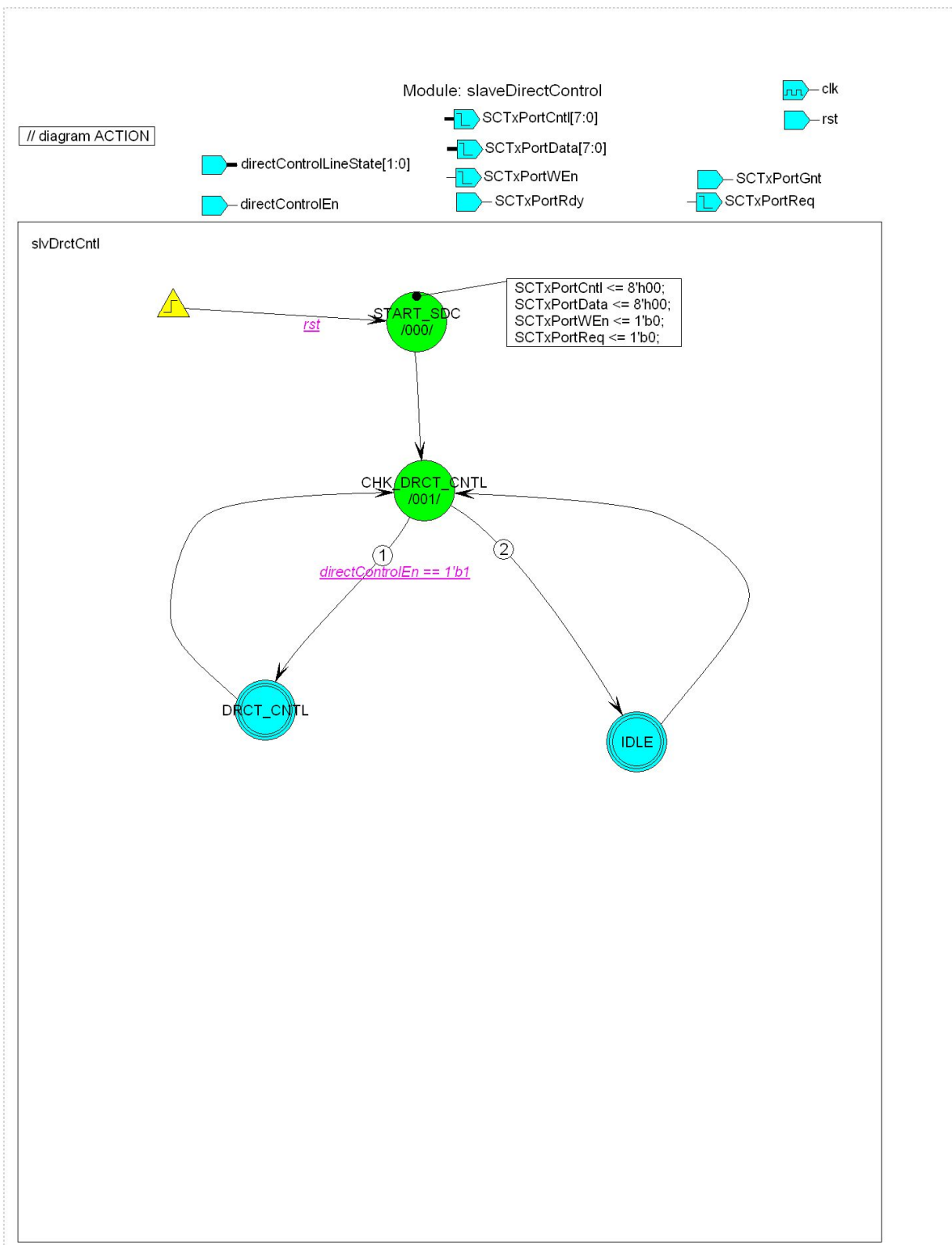




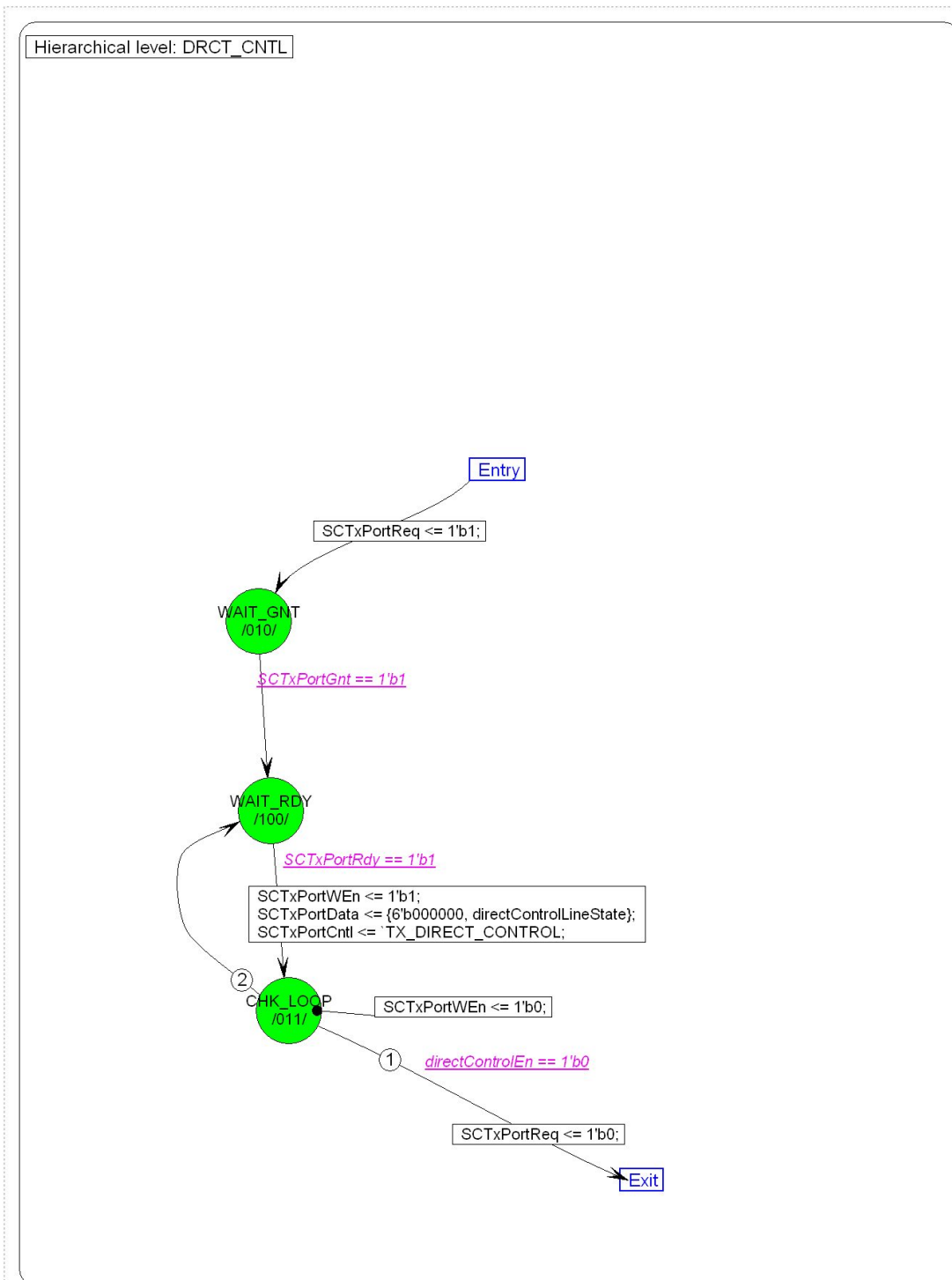
## 2.15.4 START



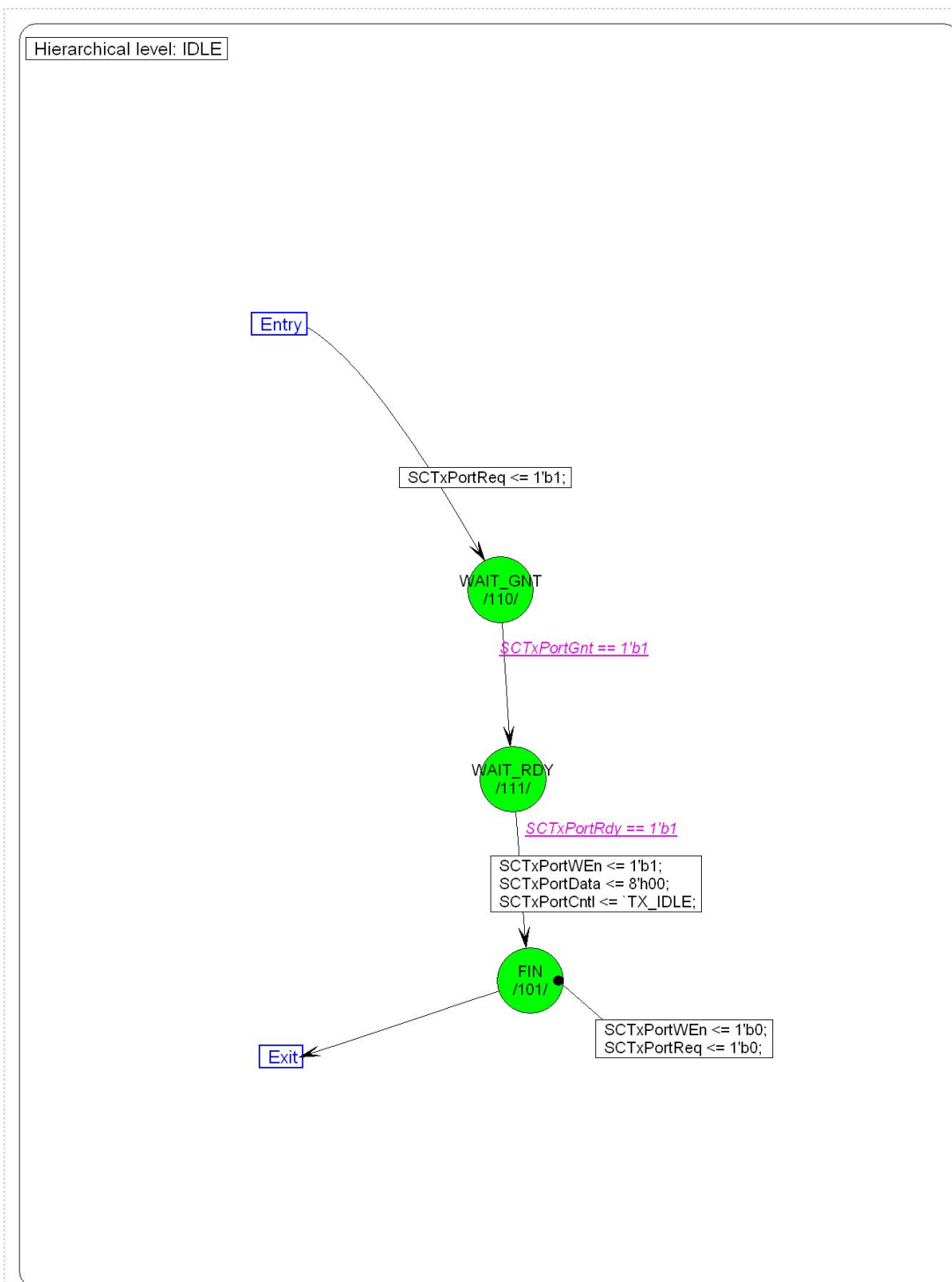
2.16 slaveDirectcontrol.asf



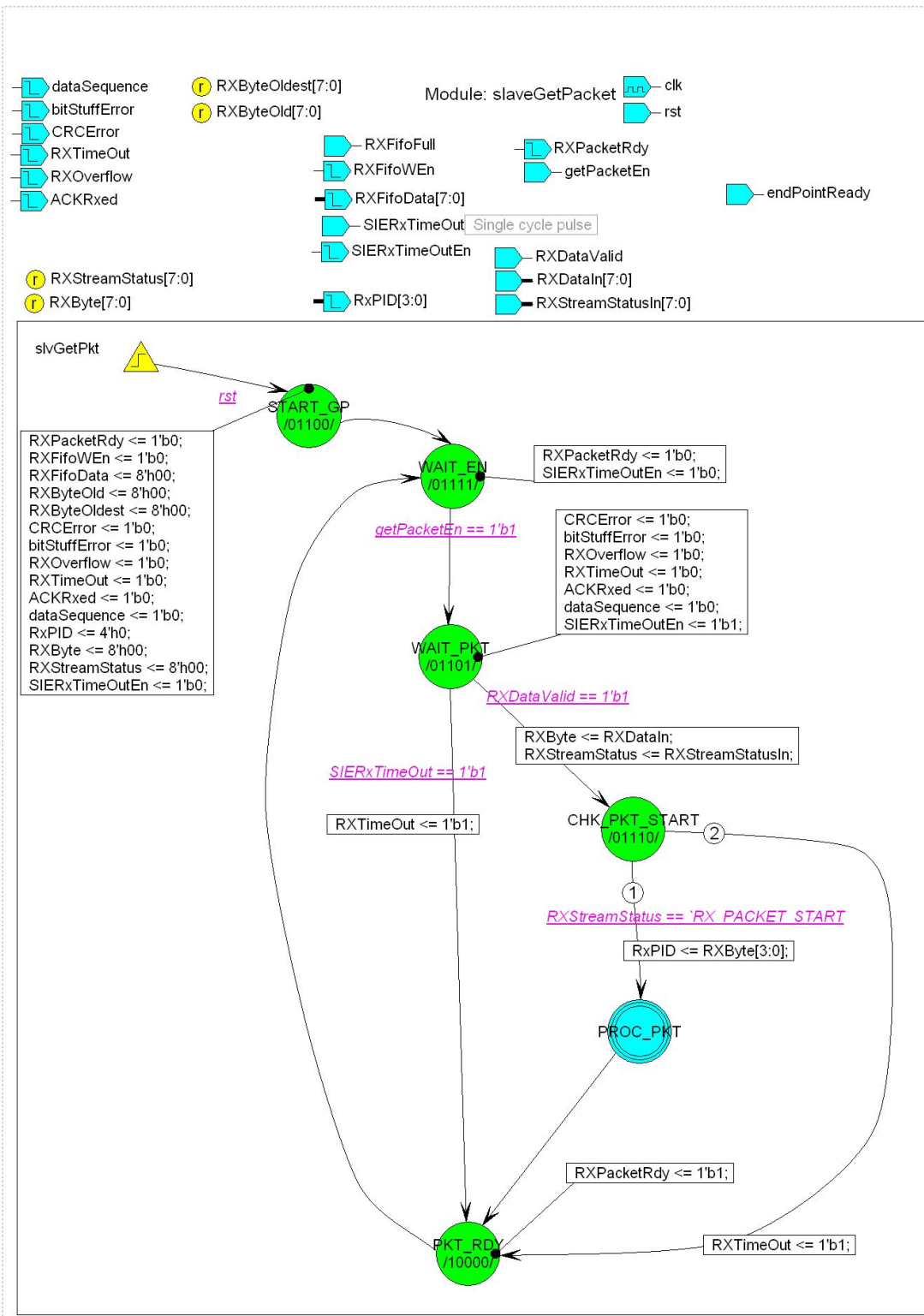
## 2.16.1 DRCT\_CNTL



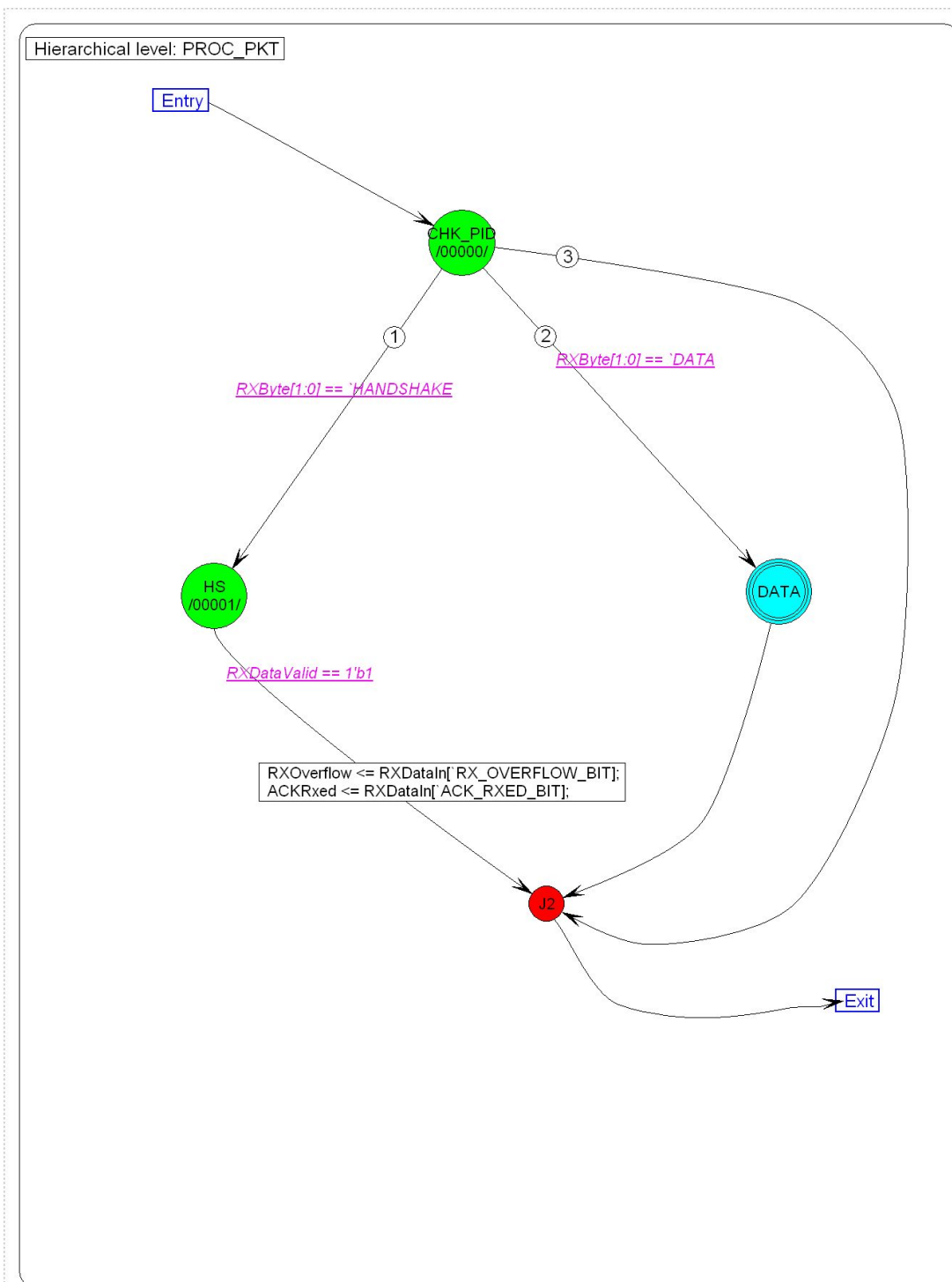
## 2.16.2 IDLE



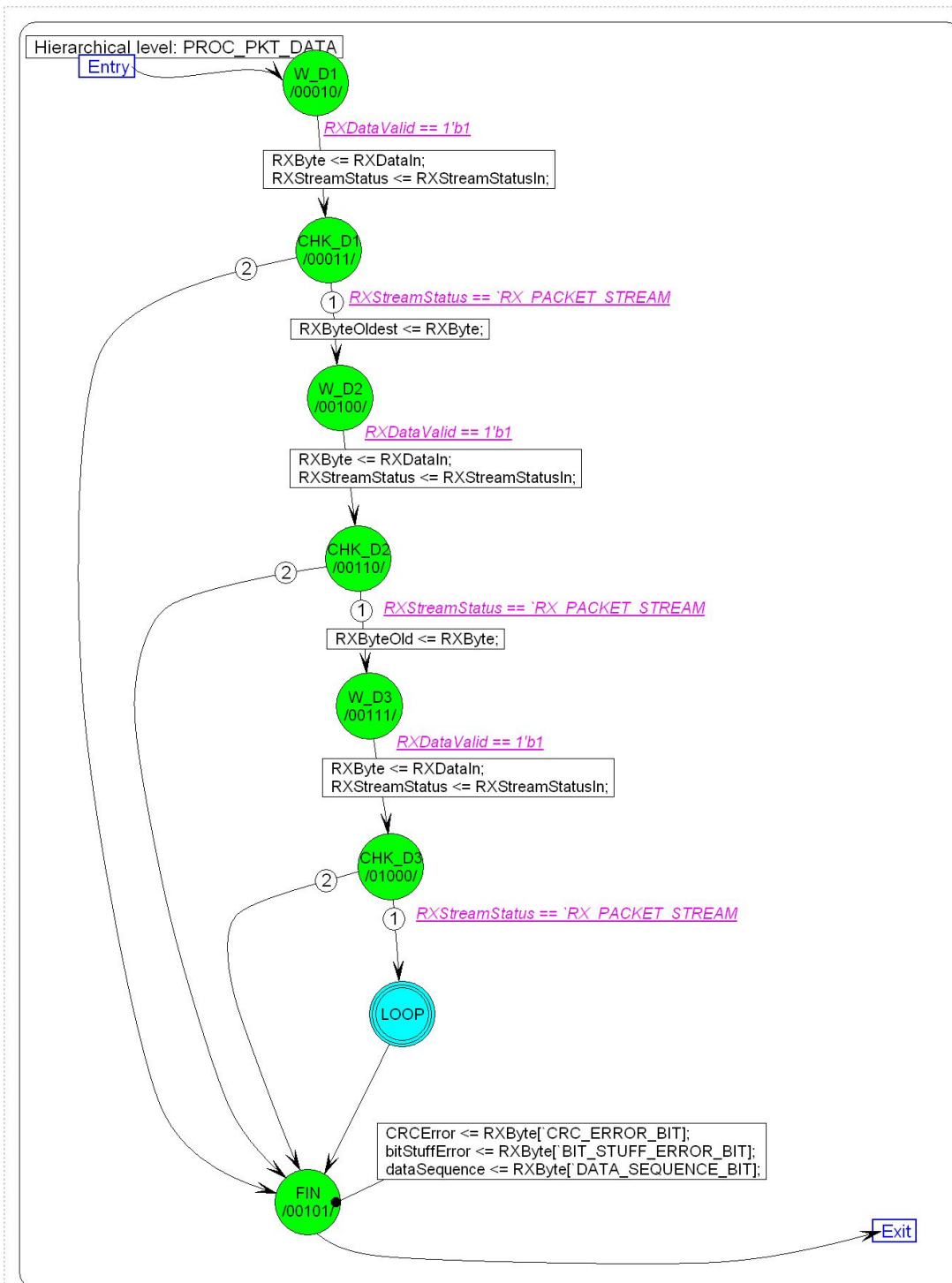
## 2.17 slaveGetpacket.asf



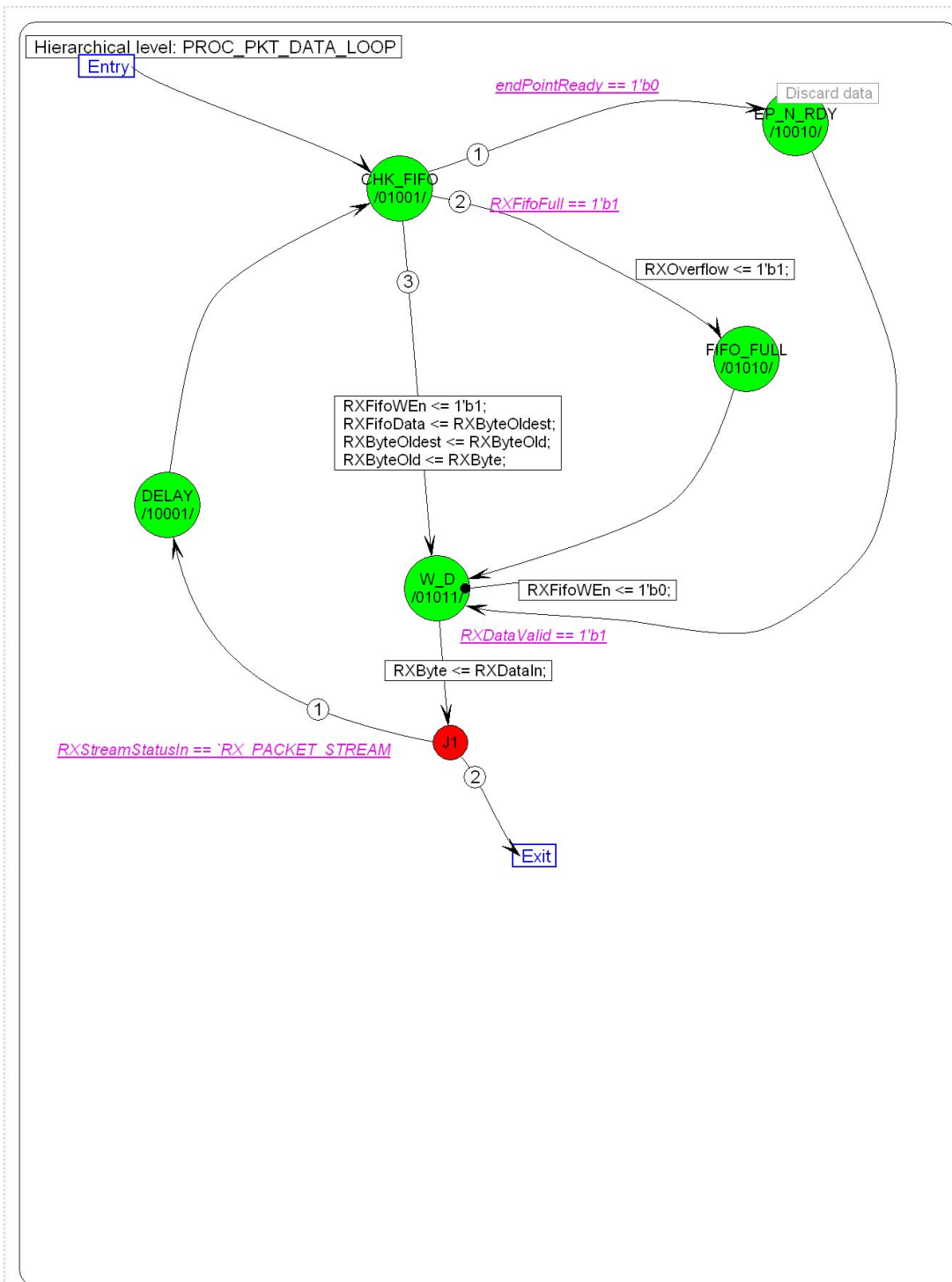
## 2.17.1 PROC\_PKT



### 2.17.1.1 DATA

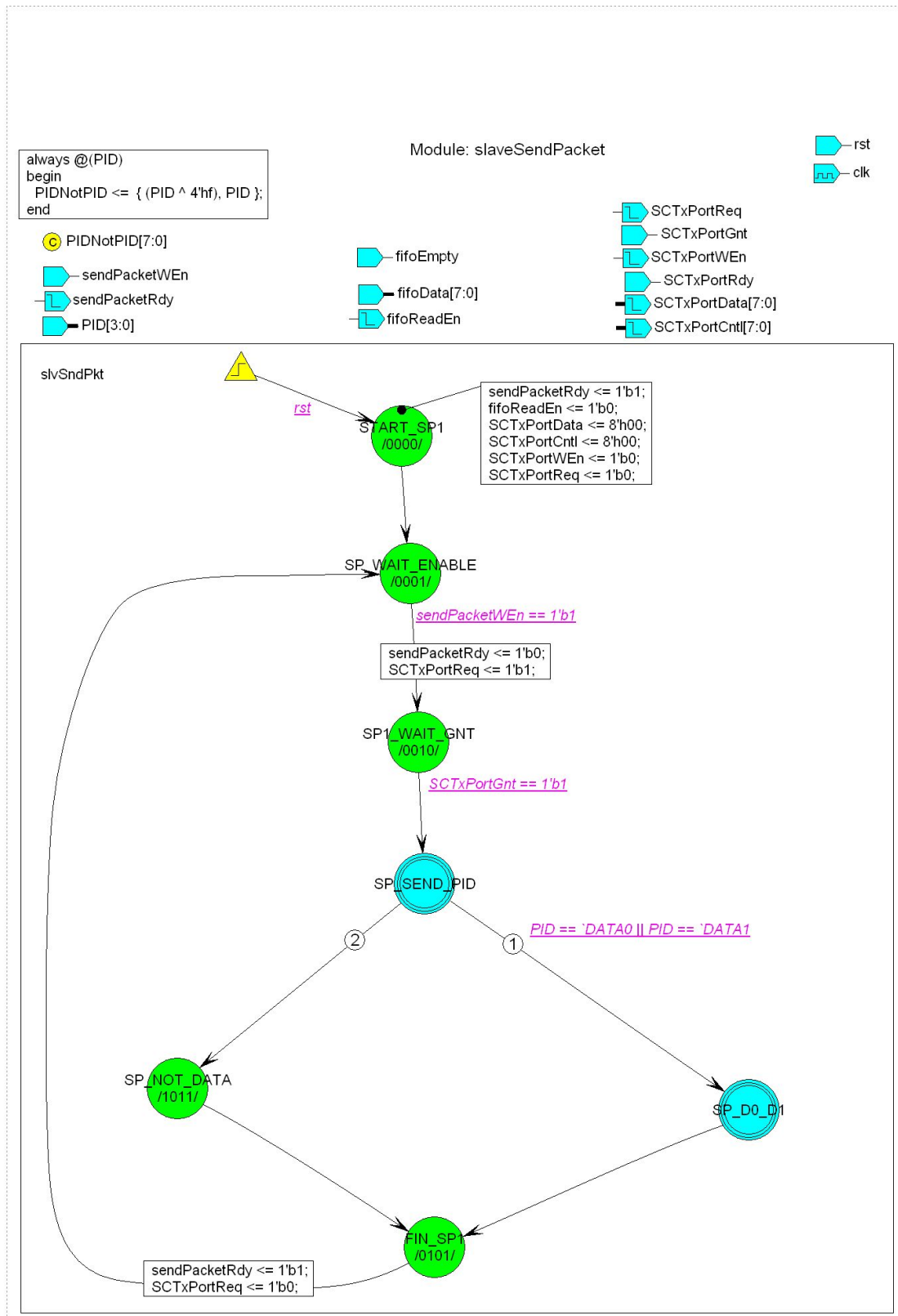


### 2.17.1.1.1 LOOP

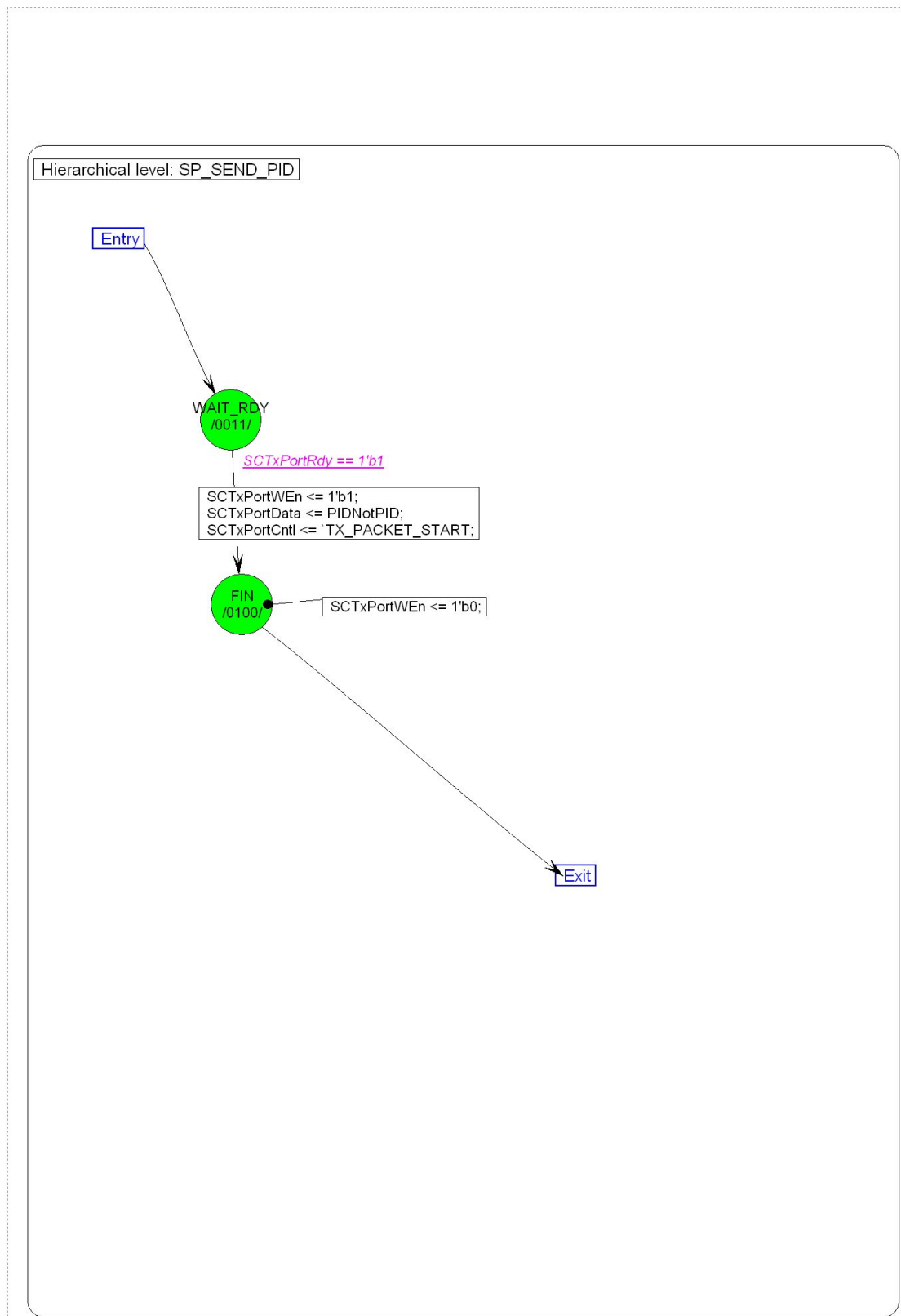




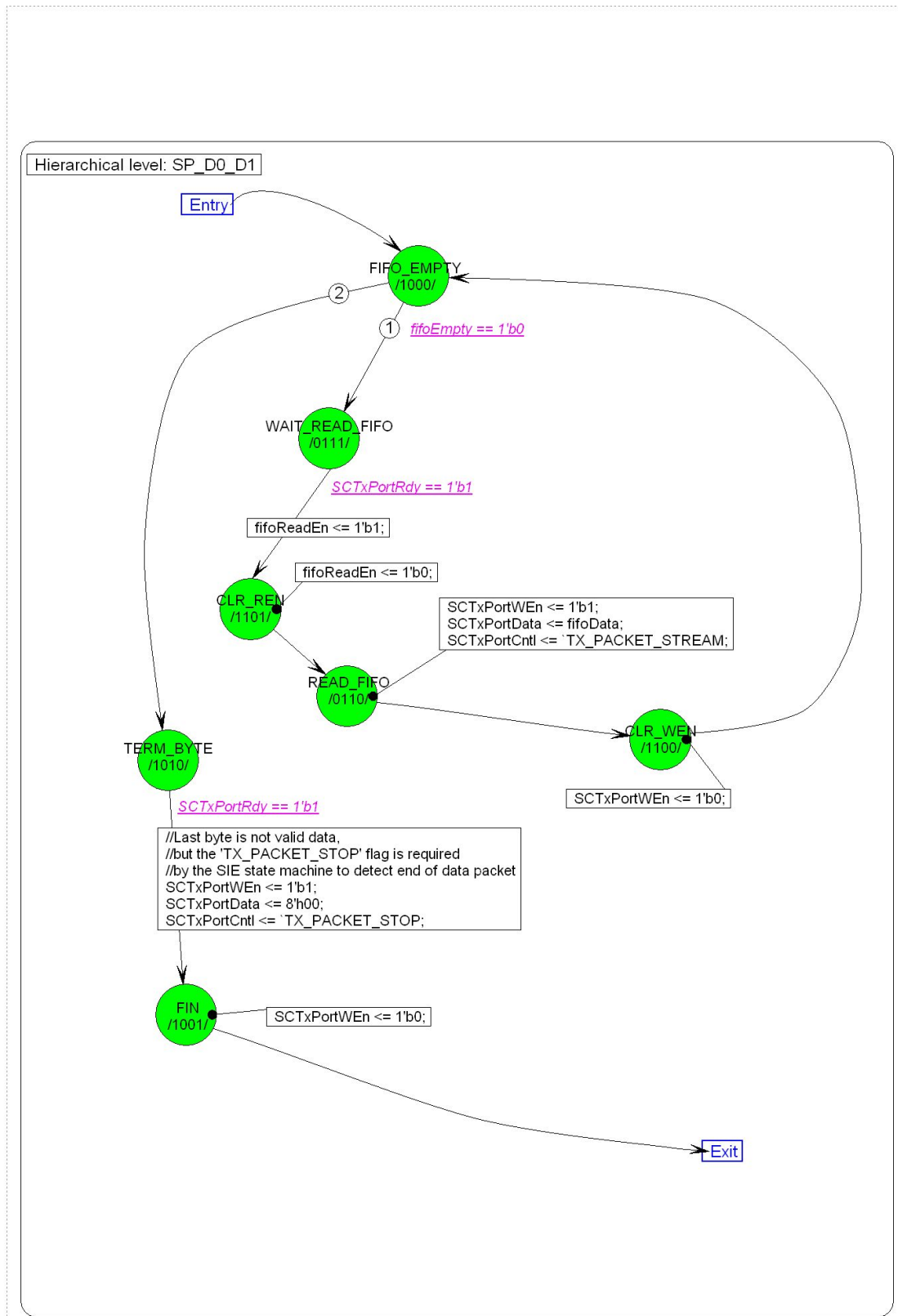
## 2.18 slaveSendpacket.asf



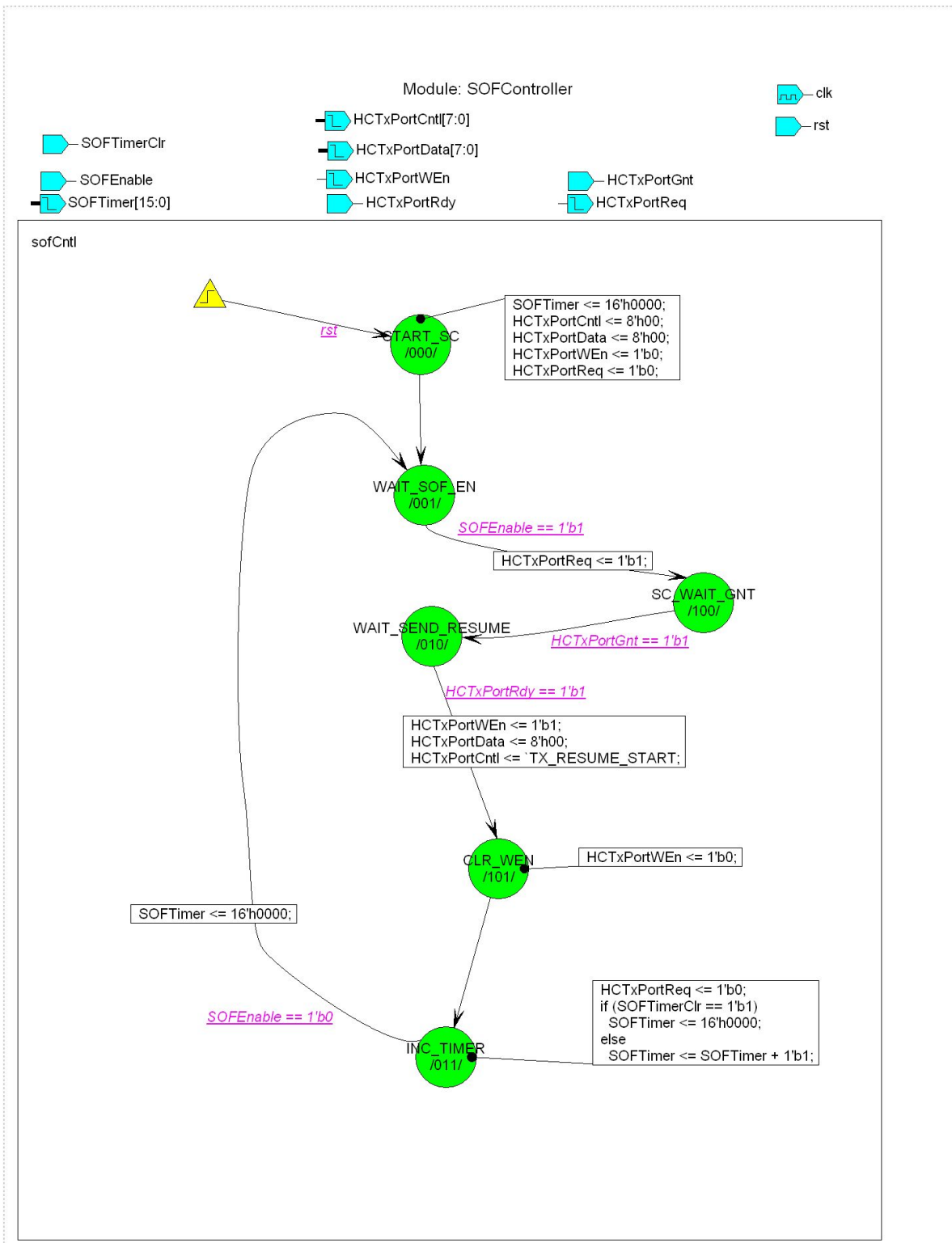
## 2.18.1 SP\_SEND\_PID



## 2.18.2 SP\_D0\_D1



2.19 sofcontroller.asf



2.20 softransmit.asf

