Versatile memory controller User Guide

Michael Unneback
ORSoC

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1 Introduction

This design implements a versatile memory controller. If used in combination with the versitale library, available from OpenCores, different types of system can easily be designed, including use cases where the system bus is in one clock domain and the memory controller in an other.

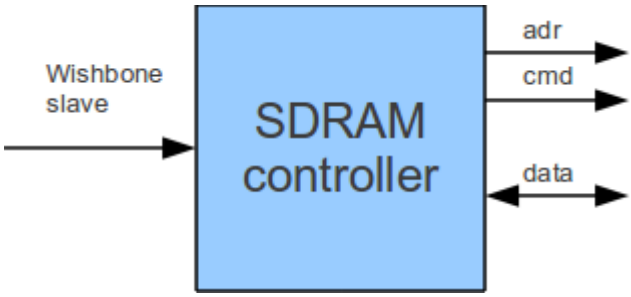
1.1 Dependencies to other IP cores

This design uses the following IP coreas available from OpenCores project verstile library.

- vl_cnt_shreg_ce_clear
- vl_dff_ce_clear
- vl_cnt_lfsr_zq
- vl_dff
- vl_o_dff
- vl_io_dff_oe

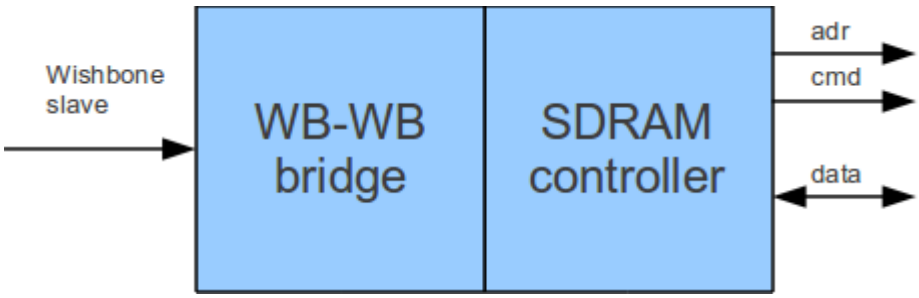
2 Block Diagram

2.1 Synchronous design



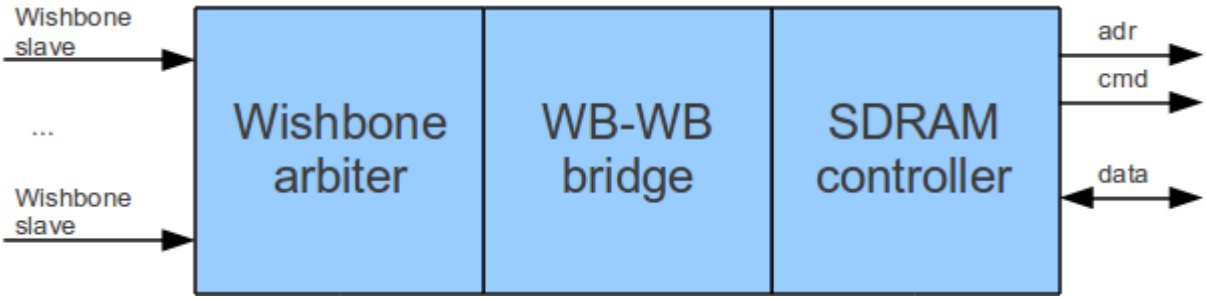
Synchronous design where wishbone clock domain is equal to SDRAM and SDRAM controller clock domain.

2.2 Asynchronous design



Asynchronous design where wishbone and SDRAM clock domain are independant. A wishbone rev B3 compatilble bridge is available in project versatile_library from OpenCores, http://www.opencores.org.

2.3 Asynchronous design with multiple wishbone interfaces



Asynchronous design where wishbone and SDRAM clock domain are independant. Multiple wishbone port with use of a wishbone arbiter.

3 SDR SDRAM controller

3.1 Module defines

Name	Description
NO_BURST	Define if burst cycles not used
WRAP4	Define to support 4 word wrap burst
WRAP8	Define to support 8 word wrap burst
WRAP16	Define to support 16 word wrap burst

3.2 Module parameters

Name	Default value	Description
ba_size	2	Bank adress vector size
row_size	13	Row adress vector size
col_size	9	Column adress vector size
cl	2	CAS latency

Parameters ba_size, col_size and row_size should be set depending on memory configuration. The following table holds figures for some SDRAM memories.

Manufacturer	Partnumber	ba_size	row_size	col_size	Memory size
Micron	MT48LC4M16	2	12	8	8Mbyte
Micron	MT48LC8M16	2	12	9	16Mbyte
Micron	MT48LC16M16	2	13	9	32Mbyte
Micron	MT48LC32M16	2	13	10	64Mbyte

Parameter cl should be set to either 2 or 3 depending on SDRAM clock.

3.3 Module IO signals

3.3.1 Wishbone signals

Name	Dir	Width	Description
dat_i	I	32	Input data vector
adr_i	I		Adress vector
sel_i	I	4	Byte select signals
bte_i	I	2	Bus tag identifier
we_i	I	1	Write enable
cyc_i	I	1	Active cycle indicator
stb_i	I	1	Strobe
dat_o	O	32	Output data vector
ack_o	O	1	Acknowledge signal

Wishbone signal bte_i is optional and is only used for designs supporting burst transfer.

3.3.2 SDRAM signals

Name	Dir	Width	Description
ba	O	ba_size	Bank adress vector

a	O	13	Adress vector
cmd	O	3	SDRAM command, ras_n, cas_n, we_n
cke	O	1	Clock enable
cs_n	O	1	Chip select, active low
dqm	O	2	Data mask
dq_i	I	16	Data input vector
dq_o	O	16	Data output vector
dq_oe	O	1	Data output enable

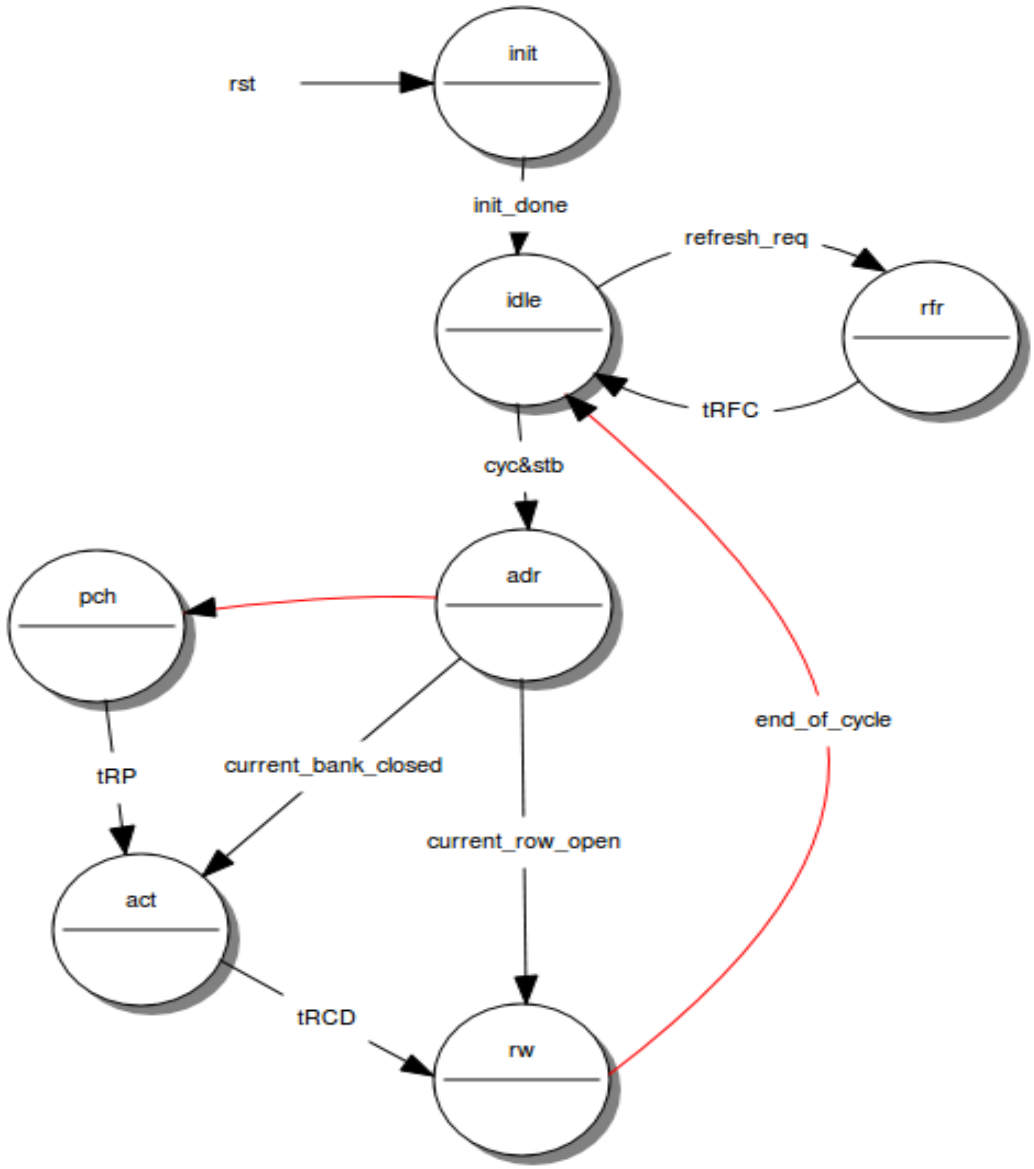
3.3.3 System signals

Name	**Dir**	**Width**	**Description**
clk	I	1	SDRAM system clock
rst	I	1	Asynchronous reset, active hig

4 SDR SDRAM 16 bit data bus controller

4.1 State machine implementation

Design is based on a state machine as described below.



A counter is incremented on each cycle the state machine reside in any given state. When changing state a counter clear is issued. The counter state vector is used for two things

- controlling outputs, ie defining cmd and other control signals
- to make sure timing reqiurements are fulfilled, ie define time from precharge to activate

4.1.1 State - init

The init state is responsible to make sure that a proper start-up and initialization of the SDRAM is performed. The following sequence should be applied:

1. assert CKE low

2. provide stable clock
3. bring CKE high
4. perform PRECHARGE ALL command and wait for tRP
5. issue AUTO RERFESH and wait for tRFC
6. issue AUTO RERFESH and wait for tRFC
7. LOAD MODE REGISTER and wait for tMR

After this state machine advances to idle state

4.1.2 State - idle

In state idle implementation awaits two different condition, appearing in order of priority

1. refresh request => next state is rfr
2. cyc_i & stb_i => next state is adr

4.1.3 State - adr

Depending on status of open bank and open rows choice is taken whether to precharge and activate, activate or go directly to read write state. Reason for this as a separate state is to be able to have comparison result as a registered signal to achive an higher clock frequency.

4.1.4 State - pch

Open row in current bank is deactivated. State machine waits in pch state to fulfill tRP.

4.1.5 State - act

Row in current bank is activated. State machine waits in act state to fulfill tRCD.

4.1.6 State - rw

A two word read or write burst is started. If wishbone cycle is of type burst column will get incremented with possible wrap around and a new burst started for each 32 bit word.

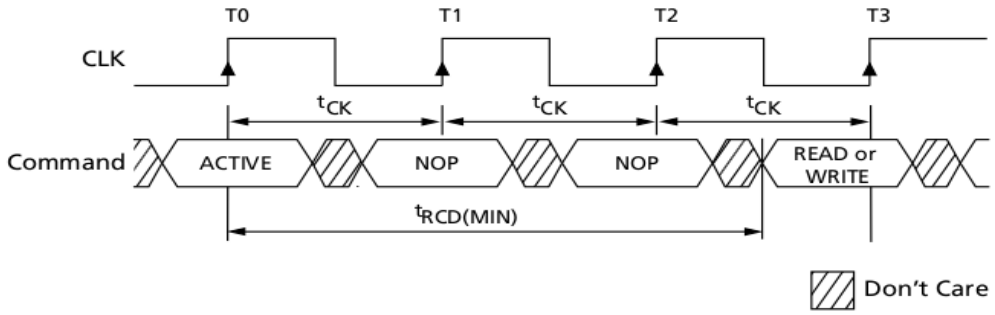
4.2 Timing

The follwoing timing requirements must be fulfilled:

- tMR - Load Mode Register period
- tRCD - Active to read/write delay
- tRP - Precharge command period
- tRFC - Auto refresh period
- tREF - refresh period

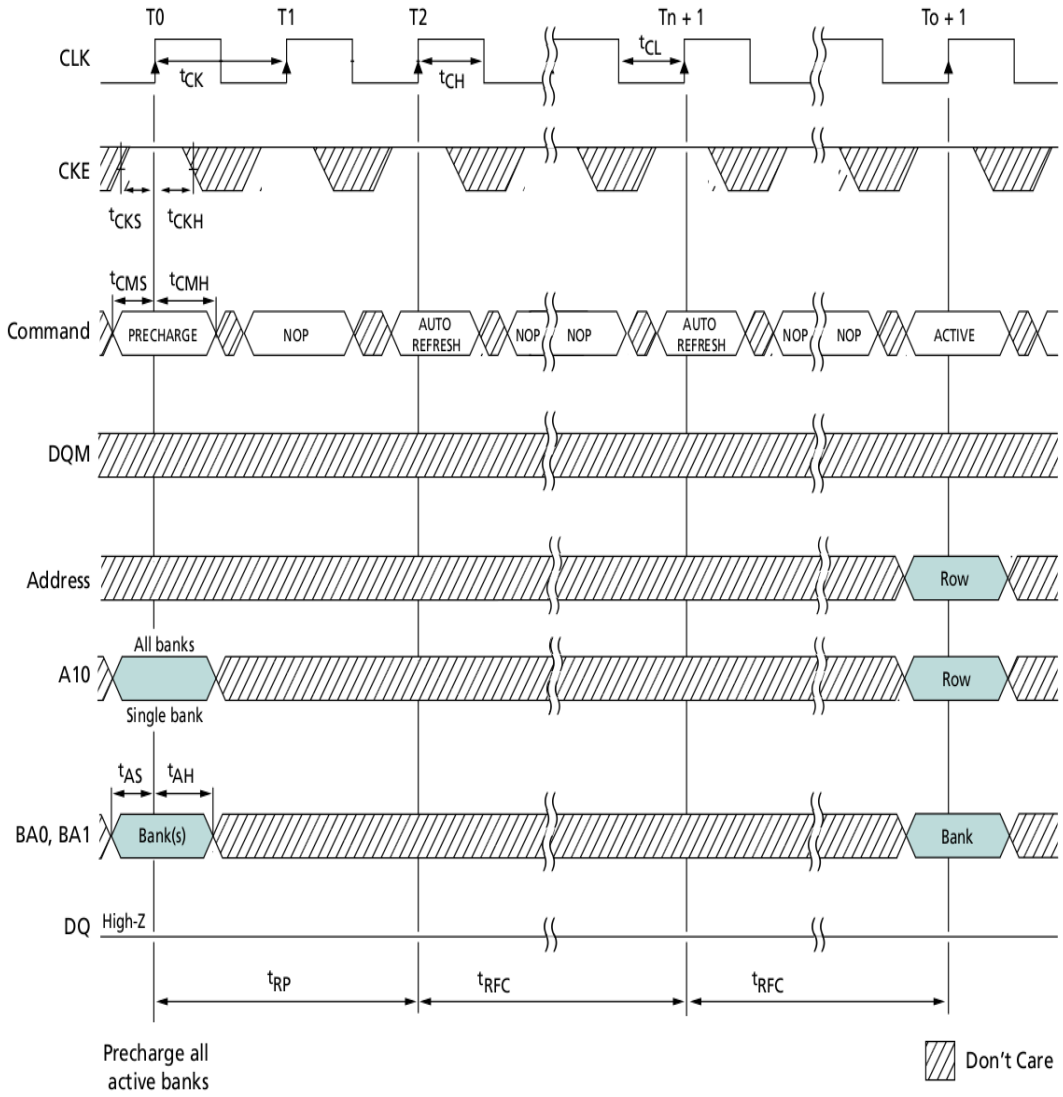
In the SDRAM datasheet the above timing figures will be given in ns and should be converted to number of clock cycles. All of the above timing figures, except tREF, are implemented as parameters in the design and should be set depending on SDRAM figures and actual clock period. All parameters have default values of 2 clock cycles.

4.2.1 Bank/Row activation - tRCD



Minimum time between activation of and read or write command.

4.2.2 Auto refresh mode



Minumum time between precharge and auto refresh and active command.

4.2.3 Refresh period - tREF

The auto refresh period, tREF must be met. During auto refresh an internal address counter is used and adress signals are treated as don't care. During the refresh period each row must be refreshed.
For example consider a SDRAM with tREF = 64 ms and row size of 8K. An auto refresh command should be issued once every 64 ms / 8192 = 7.813 us.
The refresh interval counter is implemented as an LFSR style counter for minimal area and maximum performance. To accurately set the wrap value for this counter use the application VersatileCounter found in the versatile library project at opencores. This program gives the wrap value for a given vector length. Assuming an SDRAM clock frequency of 133 MHz which equals a period time of 7.5 ns we should issue an auto refresh every 7.813 us / 7.5 ns = 1041 cycle. We need a state vector of 11 bits in the counter.
To get the wrap value we use the application

```
./VersatileCounter.php 11 1041
11111110101
```

5 Example: Timing setup

5.1 Requirements

SDRAM device to use:

- Micron MT48LC32M16-7E

Parameter	Symbol	Min	Max	Unit
Auto refresh period	tRFC	66	-	ns
Precharge command period	tRP	15	-	ns
Active to read or write delay	tRCD	15	-	ns
Load mode register command to active or refresh	tMRD	2	-	tCK
Refresh periods (8192 rows)	tREF	66	-	ms

Intended operating frequency is 75 MHz, tCK = 13.333 ns

5.2 Parameter settings

Symbol	Value
tRFC	5
tRP	2
tRCD	2
tMRD	2

Refresh rate is 66 ms / 8192 = 8.057 us
Number of clock cycles between refresh request 8.057 us / 13.333 ns = 604

To get the wrap value we use the application from Versatile Library

```
./VersatileCounter.php 10 604
0101001110
```

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