VGA/LCD Core v2.0 Specifications

Author: Richard Herveille
richard@asics.ws

Document rev. 0.7
October 25, 2001

This page left intentionally blank

Revision History

Rev.	Date	Author	Description
0.1	10/04/01	Richard Herveille	First Draft
0.1a	20/04/01	Richard Herveille	Changed *proposal* to *specifications* Added Appendix A Extended Register Specifications
0.2	21/05/01	Richard Herveille	First official release Added OpenCores logo Changed Chapter 1, Introduction Finished Chapter 2, IO ports Finished Chapter 3, Registers Extended Chapter 4, Operation Changed Chapter 5, Architecture Added Appendix B
0.3	28/05/01	Richard Herveille	Fixed some inconsistencies.
0.4	03/06/01	Richard Herveille	Changed all references to address related subjects (core fix & documentation fix). Added Appendix C
0.4a	04/06/01	Richard Herveille	Fixed some minor typing errors in the document (credits: Rudolph Usselmann)
0.5	15/07/01	Richard Herveille	Added Color Lookup Table bank switching. Added embedded CLUT section. Revised horizontal & vertical timing section.
0.6	31/07/01	Richard Herveille	Added Power-on-Reset description. Changed CBSE & VBSE bits functionality. Added Bank Switch Section. Added VGA & CLUT section to Appendix B. Changed introduction page.
0.7	10/19/01	Richard Herveille	Major VGA/LCD Core changes; core v2.0. Changed Manual to reflect core changes. Removed all references to external CLUT v2.0 core has CLUT internally.

1 Introduction

The OpenCores VGA/LCD Controller Core provides VGA capabilities for embedded systems. It supports both CRT and LCD displays with user programmable resolutions and video timings. Making it compatible with almost all available LCD and CRT displays. The core supports a number of color modes, including 24bpp, 16bpp, 8bpp gray-scale, and 8bpp-pseudo color. The video memory is located outside the primary core, thus providing the most flexible memory solution. It can be located on-chip or off-chip, shared with the system's main memory (VGA on demand) or be dedicated to the VGA system. The color lookup table is, as of VGA/LCD Core V2.0, incorporated into the Color Processor block

Pixel data is fetched automatically via the Wishbone master interface, making this an ideal "program-and-forget" video solution. More demanding video applications like streaming video or video games can benefit from the video-bank-switching function, which reduces flicker and cluttered images by automatically switching between video-memory pages and/or color lookup tables on a vertical retrace.

The core can interrupt the host on each horizontal and/or vertical synchronization pulse. The horizontal, vertical and composite synchronization polarization levels, as well as the blanking polarization level are user programmable.

Features:

- CRT and LCD display support
- Separate VSYNC/HSYNC and combined CSYNC synchronization signals
- Composite BLANK signal
- User programmable video timing
- User programmable video resolutions
- 24bpp and 16bpp color modes
- 8bpp gray-scale and 8bpp pseudo-color modes
- Support of video-bank switching during vertical retrace
- Triple display support
- Interrupt generation
- WISHBONE Rev. B2 compliant slave and master
- 32bit host interface
- Operates from a wide range of input clock frequencies
- Static synchronous design
- Fully synthesizable

2

IO ports

2.1 Core Parameters

Parameter	Type	Default	Description
ARST_LVL	Bit	1'b0	Asynchronous reset level
LINE_FIFO_AWIDTH	Integer	7	Line Fifo Size

2.1.1 ARST_LVL

The asynchronous reset level can be set to either active high (1'b1) or active low (1'b0).

2.1.2 LINE_FIFO_AWIDTH

The line FIFO size can be altered by changing the amount of address-bits the FIFO logic should use. The line FIFO depth (amount of entries) can be calculated as follows:

$$entries = 2^{LINE\_FIFO\_AWIDTH}$$

2.2 WISHBONE Syscon Interface Connections

Port	Width	Direction	Description
wb_clk_i	1	Input	Master clock input
wb_rst_i	1	Input	Synchronous active high reset
rst_i	1	Input	Asynchronous reset
wb_inta_o	1	Output	Interrupt request signal

2.2.1 wb_clk_i

All internal WISHBONE logic is registered to the rising edge of the [wb_clk_i] clock input. The frequency range over which the core can operate depends on the technology used and the pixel clock needed; [wb_clk_i] may not be slower than the pixel clock [clk_p_i].

2.2.2 wb_rst_i

The active high synchronous reset input [wb_rst_i] forces the core to restart. All internal registers are preset and all state-machines are set to an initial state.

2.2.3 rst_i

The asynchronous reset input [rst_i] forces the core to restart. All internal registers are preset and all state-machines are set to an initial state. The reset level, either active high or active low, is set by the ARST_LVL parameter.

rst_i is not a WISHBONE compatible signal. It is provided for FPGA implementations. Using [rst_i] instead of [wb_rst_i] can result in lower cell-usage and higher performance, because most FPGAs provide a dedicated asynchronous reset path. Use either [rst_i] or [wb_rst_i].

The core requires a power-on reset which allows all internal registers to propagate to a known state. The power-on reset must be held asserted until all clocks are stable. When all clocks are stable the reset signal must remain asserted for at least 3 clock cycles of the slowest available clock (clk_p_i).

2.2.4 wb_inta_o
The interrupt request output is asserted when the core needs service from the host system.

2.3 WISHBONE Slave Interface Connections

Port	Width	Direction	Description
wbs_adr_i	12	Input	Lower address bits
wbs_dat_i	32	Input	Slave Data bus input
wbs_dat_o	32	Output	Slave Data bus output
wbs_sel_i	4	Input	Byte select signals
wbs_we_i	1	Input	Write enable input
wbs_stb_i	1	Input	Strobe signal/Core select input
wbs_cyc_i	1	Input	Valid bus cycle input
wbs_ack_o	1	Output	Bus cycle acknowledge output
wbs_err_o	1	Output	Bus cycle error output

2.3.1 wbs_adr_i
The address array input [wbs_adr_i] is used to pass a binary coded address to the core. The most significant bit is at the higher number of the array.

2.3.2 wbs_dat_i
The data array input [wbs_dat_i] is used to pass binary data to the core. All data transfers are 32bit wide.

2.3.3 wbs_dat_o
The data array output [wbs_dat_o] is used to pass binary data from the core to the MASTER. All data transfers are 32bit wide.

2.3.4 wbs_sel_i
The byte select array input [wbs_sel_i] indicates where valid data is placed on the [wbs_dat_i] input array during writes to the core, and where it is expected on the [wbs_dat_o] output array during reads from the core. The core requires all accesses to be 32bit wide (wbs_sel_i[3:0] = ‘1111’b).

2.3.5 wbs_we_i
The write enable input [wbs_we_i], when asserted indicates whether the current bus cycle is a read or write cycle. The signal is asserted during write cycles and negated during read cycles.

2.3.6 wbs_stb_i
The strobe input [wbs_stb_i] is asserted when the core is being addressed. The core only responds to WISHBONE cycles when [wbs_stb_i] is asserted, except for [wb_rst_i] and [rst_i] reset signals, which are always responded to.

2.3.7 wbs_cyc_i
The cycle input [wbs_cyc_i], when asserted indicates that a valid bus cycle is in progress. The logical AND function of [wbs_cyc_i] and [wbs_stb_i] indicates a valid transfer cycle to/from the core.

2.3.8 wbs_ack_o
The acknowledge output [wbs_ack_o], when asserted indicates the normal termination of a valid bus cycle.

2.3.9 wbs_err_o
The error output [wbs_err_o], when asserted indicates an abnormal termination of a bus cycle. The [wbs_err_o] output signal is asserted when the host tries to access the controller's internal registers using non 32bit aligned data; i.e. wbs_sel_I[3:0] not equal to '1111'b.

2.4 WISHBONE Master Interface Connections

Port	Width	Direction	Description
wbn_adr_o	32	Output	Address bus output
wbm_dat_i	32	Input	Data bus input
wbm_sel_o	4	Output	Byte select signals
wbm_we_o	1	Output	Write enable output
wbm_stb_o	1	Output	Strobe signal
wbm_cyc_o	1	Output	Valid bus cycle output
wbm_cab_o	1	Output	Consecutive address burst output
wbm_ack_i	1	Input	Bus cycle acknowledge input
wbm_err_i	1	Input	Bus cycle error Input

2.4.1 wbm_adr_o
The address array input [wbm_adr_o] is used to pass a binary coded address from the core to the external video memory. The most significant bit is at the higher number of the array.

2.4.2 wbm_dat_i
The master data array input [wbm_dat_i] is used to pass binary data to the core. All data transfers are 32bit wide.

2.4.3 wbm_sel_o
The byte select array output [wbm_sel_o] indicates where valid data is expected on the [wbm_dat_i] input array. The core support 32bit wide accesses only(wbm_sel_o[3:0] = '1111'b).

2.4.4 wbm_we_o
The write enable output [wbm_we_o], when asserted indicates whether the current bus cycle is a read or write cycle. The core only reads from the external memory, [wbm_we_o] is therefore always negated ('0').

2.4.5 wbm_stb_o
The strobe output [wbm_stb_o] is asserted when the core wants to read from the external video memory.

2.4.6 wbm_cyc_o
The cycle output [wbm_cyc_o] is asserted when the core wants to read from the external video memory.

2.4.7 wbm_cab_o
The consecutive address burst output [wbm_cab_o] is asserted when the core wants to perform a linear address burst read from the video memory.

2.4.8 wbm_ack_i
The acknowledge input [wbm_ack_i], when asserted indicates the normal termination of a valid bus cycle.

2.4.9 wbm_err_i
The error input [wbm_err_i], when asserted indicates an abnormal termination of a bus cycle. When the [wbm_err_i] signal is asserted the core stops the current transfer. The state of the core after the assertion of [wbm_err_i] is undefined.

2.5 VGA Port Connections

Port	Width	Direction	Description
clk_p_I	1	Input	Pixel Clock
hsync_pad_o	1	Output	Horizontal Synchronization Pulse
vsync_pad_o	1	Output	Vertical Synchronization Pulse
csync_pad_o	1	Output	Composite Synchronization Pulse
blank_pad_	1	Output	Blank signal

o			
r_pad_o	8	Output	Red Color Data
g_pad_o	8	Output	Green Color Data
b_pad_o	8	Output	Blue Color Data

2.5.1 clk_p_i
All internal video logic is registered to the rising edge of the [clk_p_i] clock input. The frequency range over which the core can operate depends on the technology used and the pixel clock needed; [clk_p_i] may not be faster than the WISHBONE clock [wb_clk_i].

2.5.2 hsync_pad_o
The horizontal synchronization pulse is asserted when the raster scan ray needs to return to the start position (the left side of the screen).

2.5.3 vsync_pad_o
The vertical synchronization pulse is asserted when the raster scan ray needs to return to the vertical start position (the top of the screen).

2.5.5 csync_pad_o
The composite synchronization pulse is a combined horizontal and vertical synchronization signal.

2.5.6 blank_pad_o
The blank output is asserted during the period no image is projected on the screen; the back porch, synchronization pulses and the front porch.

2.5.7 r_pad_o, g_pad_o, b_pad_o
Red, green and blue pixel data. The RGB lines contain invalid data while the BLANK signal [blank_pad_o] is asserted.

3

Registers

3.1 Registers list

Name	wbs_adr_i[11:0]	Width	Access	Description
CTRL	0x000	32	R/W	Control Register
STAT	0x004	32	R/W	Status Register
HTIM	0x008	32	R/W	Horizontal Timing Register
VTIM	0x00C	32	R/W	Vertical Timing Register
HVLEN	0x010	32	R/W	Horizontal and Vertical Length Register
VBARa	0x014	32	R/W	Video Memory Base Address Register A
VBARb	0x018	32	R/W	Video Memory Base Address Register B

3.2 Control Register [CTRL]

Bit #	Access	Description
31:16	R/W	*reserved*
15	R/W	BL, Blanking Polarization Level 0: Positive 1: Negative
14	R/W	CSL, Composite Synchronization Pulse Polarization Level 0: Positive 1: Negative
13	R/W	VSL, Vertical Synchronization Pulse Polarization Level 0: Positive 1: Negative
12	R/W	HSL, Horizontal Synchronization Pulse Polarization Level 0: Positive 1: Negative
11	R/W	PC, 8bit Pseudo Color 0: 8bit gray scale 1: 8bit pseudo color
10,9	R/W	CD, Color Depth 11: reserved 10: 24bit per pixel 01: 16bit per pixel 00: 8bit per pixel
8,7	R/W	VBL, Video memory Burst Length

		11b: 8 cycles 10b: 4 cycles 01b: 2 cycles 00b: 1 cycle
6	R/W	CBSWE, CLUT Bank Switching Enable
5	R/W	VBSWE, Video Bank Switching Enable
4	R/W	CBSIE, CLUT Bank Switch Interrupt Enable
3	R/W	VBSIE, Video Bank Switch Interrupt Enable
2	R/W	HIE, Horizontal Interrupt Enable
1	R/W	VIE, Vertical Interrupt Enable
0	R/W	VEN, Video Enable

Reset Value: 0x00000000

3.2.1 BL

The Blanking Polarization Level defines the voltage level the BLANK output has when the blank signal is asserted. When BL is cleared (‘0’) BLANK is at a high voltage level when the blank signal is asserted and at a low voltage level when not (i.e. BLANK is active high). When BL is set (‘1’) BLANK is at a low voltage level when the blank signal is asserted and at a high voltage level when not (i.e. BLANK is active low).

3.2.2 CBSIE

When the Clut Bank Switch Interrupt Enable bit is set (‘1’) and a bank switch is requested, the host is interrupted. The Bank Switch interrupt is independent of the Clut Bank Switch Enable bit setting. Setting this bit while the Clut Bank Switch Interrupt Pending (CBSINT) flag is set generates an interrupt. Clearing this bit while CBSINT is set disables the interrupt request, but does not clear the interrupt pending flag.

3.2.3 CBSWE

When the CLUT Bank Switch Enable bit is set (‘1’) and a complete video frame has been read into the line buffer, the core switches between the two available color lookup tables located at the memory addresses set in the CLUT Memory Base Address register. The Active CLUT Memory Page (ACMP) flag reflects the current active Color Lookup Table. The core automatically clears this bit after the bank switch. Software should set this bit each time a bank switch is desired.

3.2.4 CD

The Color Depth bits define the number of bits per pixel (bpp), either 8, 16 or 24bpp.

3.2.5 CSL

The Composite Sync Polarization Level defines the voltage level the CSYNC output has when the composite sync signal is asserted. When CSL is cleared (‘0’) CSYNC is at a high voltage level when the composite sync signal is asserted and at a low voltage level when not (i.e. CSYNC is active high). When CSL is set (‘1’) CSYNC is at a low voltage level when the composite sync signal is asserted and at a high voltage level when not (i.e. CSYNC is active low).

3.2.6 HIE
When the Horizontal Interrupt Enable bit is set (‘1’) and a horizontal interrupt is pending, the host system is interrupted. Setting this bit while the Horizontal Interrupt Pending (HINT) flag is set generates an interrupt. Clearing this bit while HINT is set disables the interrupt request, but does not clear the interrupt pending flag.

3.2.7 HSL
The Horizontal Sync Polarization Level defines the voltage level the HSYNC output has when the horizontal sync signal is asserted. When HSL is cleared (‘0’) HSYNC is at a high voltage level when the horizontal sync signal is asserted and at a low voltage level when not (i.e. HSYNC is active high). When HSL is set (‘1’) HSYNC is at a low voltage level when the horizontal sync signal is asserted and at a high voltage level when not (i.e. HSYNC is active low).

3.2.8 PC
When in 8bpp mode the pixel-data can be used as black and white information (256 gray scales) or as an index to a color lookup table (pseudo color mode). When the 8PC bit is set (‘1’) the core operates in pseudo color mode and the pixel-data is used to read the color data from the CLUT. When the 8PC bit is cleared (‘0’) the pixel-data is placed on the red, green and blue outputs, effectively producing a black and white image with 256 different gray-scales.

3.2.9 VBSIE
When the Video Bank Switch Interrupt Enable bit is set (‘1’) and a bank switch is requested, the host is interrupted. The Bank Switch interrupt is independent of the Video Bank Switch Enable bit setting. Setting this bit while the Video Bank Switch Interrupt Pending (VBSINT) flag is set generates an interrupt. Clearing this bit while VBSINT is set disables the interrupt request, but does not clear the interrupt pending flag.

3.2.10 VBSWE
When the Video Bank Switch Enable bit is set (‘1’) and a complete video frame has been read into the line buffer, the core switches between the two available video pages located at the memory addresses set in the Video Memory Base Address (VBAR) registers. The Active Video Memory Page (AVMP) flag reflects the current active video page. The core automatically clears this bit after the bank switch. Software should set this bit each time a bank switch is desired.

3.2.11 VBL
The Video Burst Length bits define the number of transfers during a single block read access to the video memory.

3.2.12 VEN
The video circuit is disabled when the Video Enable bit is cleared (‘0’). The video circuit is enabled when the Video Enable bit is set (‘1’). This bit must be cleared before changing any register contents. After (re)programming all registers this bit may be set.

3.2.13 VIE
When the Vertical Interrupt Enable bit is set (‘1’) and a vertical interrupt is pending, the host system is interrupted. Setting this bit while the Vertical Interrupt Pending (VINT) flag is set generates an interrupt. Clearing this bit while VINT is set disables the interrupt request, but does not clear the interrupt pending flag.

3.2.14 VSL
The Vertical Sync Polarization Level defines the voltage level the VSYNC output has when the vertical sync signal is asserted. When VSL is cleared (‘0’) VSYNC is at a high voltage level when the vertical sync signal is asserted and at a low voltage level when not (i.e. VSYNC is active high). When VSL is set (‘1’) VSYNC is at a low voltage level when the vertical sync signal is asserted and at a high voltage level when not (i.e. VSYNC is active low).

3.3 Status Register [STAT]

Bit #	Access	Description
31:18	R	*Reserved*
17	R	ACMP, Active CLUT Memory Page
16	R	AVMP, Active Video Memory Page
15:8	R	*Reserved*
7	R/W	CBSINT, CLUT Bank Switch Interrupt Pending
6	R/W	VBSINT, Bank Switch Interrupt Pending
5	R/W	HINT, Horizontal Interrupt Pending
4	R/W	VINT, Vertical Interrupt Pending
1	R/W	LUINT, Line Fifo Under-run Interrupt Pending
0	R/W	SINT, System Error Interrupt Pending

Reset Value: 0x00000000

3.3.1 ACMP
The Active CLUT Memory Page flag is cleared (‘0’) when the active Color Lookup Table is CLUT0, it is set (‘1’) when the active Color Lookup Table CLUT1. This flag is cleared when the Video Enable bit is cleared. See CLUT Base Address Register for more information on CLUT0 and CLUT1.

3.3.2 AVMP
The Active Video Memory Page flag is cleared (‘0’) when the active memory page is located at Video Base Address A (VBARa), it is set (‘1’) when the active memory page is located at Video Base Address B (VBARb). This flag is cleared when the Video Enable bit is cleared.

3.3.3 CBSINT
The Clut Bank Switch Interrupt Pending flag is set (‘1’) when all clut-data from the current active memory page has been read. When the CBSIE bit is set (‘1’) and CBSINT

is asserted, the host system is interrupted. Software must clear the interrupt by writing a '0' to this bit.

3.3.4 HINT
The Horizontal Interrupt Pending flag is set ('1') when the horizontal synchronization pulse (HSYNC) is asserted. When the HIE bit is set ('1') and HINT is asserted, the host system is interrupted. Software must clear the interrupt by writing a '0' to this bit.

3.3.5 LUINT
The Line Fifo Under-run Interrupt Pending flag is set ('1') when pixels are read from the line-fifo while it is empty. This can be caused by a locked bus, reading from an illegal video memory or to few entries in the FIFO. When LUINT is asserted the host system is interrupted. Software must clear the interrupt by writing a '0' to this bit.

3.3.6 SINT
The System Error Interrupt Pending flag is set ('1') when [wbm_err_i] is asserted during a read from the video memory. When SINT is asserted the host system is interrupted. Software must clear the interrupt by writing a '0' to this bit.

3.3.7 VBSINT
The Video Bank Switch Interrupt Pending flag is set ('1') when all video-data from the current active memory page has been read. When the VBSIE bit is set ('1') and VBSINT is asserted, the host system is interrupted. Software must clear the interrupt by writing a '0' to this bit.

3.3.8 VINT
The Vertical Interrupt Pending flag is set ('1') when the vertical synchronization pulse (VSYNC) is asserted. When the VIE bit is set ('1') and VINT is asserted, the host system is interrupted. Software must clear the interrupt by writing a '0' to this bit.

3.4 Horizontal Timing Register [HTIM]

Bit #	Access	Description
31:24	R/W	Thsync, Horizontal synchronization pulse width
23:16	R/W	Thgdel, Horizontal gate delay time
15:0	R/W	Thgate, Horizontal gate time

Reset Value: 0x00000000

3.4.1 Thsync
The horizontal synchronization pulse width in pixels -1.

3.4.2 Thgdel
The horizontal gate delay width in pixels -1.

3.4.3 Thgate

The horizontal gate width in pixels -1. The horizontal gate width is dependent on the programmed Video memory Burst Length [VBL] and the Color Depth [CD]. The horizontal gate width has to be dividable by the burst length and the number of pixels per memory access; see table below.

CD	Thgate dividable by:
00b	$4 * VBL$
01b	$2 * VBL$
10b	$\frac{4}{3} * VBL$

3.5 Vertical Timing Register [VTIM]

Bit #	Access	Description
31:24	R/W	Tvsync, Vertical synchronization pulse width
23:16	R/W	Tvgdel, Vertical gate delay time
15:0	R/W	Tvgate, Vertical gate time

Reset Value: 0x00000000

3.5.1 Tvsync
The vertical synchronization pulse width in horizontal lines -1.

3.5.2 Tvgdel
The vertical gate delay time in horizontal lines -1.

3.5.3 Tvgate
The vertical gate width in horizontal lines -1.

3.6 Horizontal and Vertical Length Register [HVLEN]

Bit #	Access	Description
31:16	R/W	Thlen, Horizontal length
15:0	R/W	Tvlen, Vertical length

Reset Value: 0x00000000

3.6.1 Thlen
The total horizontal line time in pixels –2.

3.6.2 Tvlen
The total vertical line time in horizontal lines -2.

3.7 Video Base Address [VBARa] [VBARb]

Bit #	Access	Description
31:2	R/W	VBA, Video Base Address
1:0	R	*Always zero*

Reset Value: 0x00000000

3.7.1 Video Base Address

The Video Base Address Register defines the starting point of the video memory. The image is stored in consecutive memory locations, starting at this address. The byte-memory location of a pixel can be calculated as follows:

Adr = ((Y * Thgate) + X) * bytes_per_pixel;

The core supports memories with burst capabilities. Burst transfers of 1, 2, 4 and 8 accesses are supported. The lower address bits must reflect the value entered in the Video Memory Burst Length bits as shown in the table below.

VBL	VBAR[4:0]*
00b	xxx00b
01b	xx000b
10b	x0000b
11b	00000b

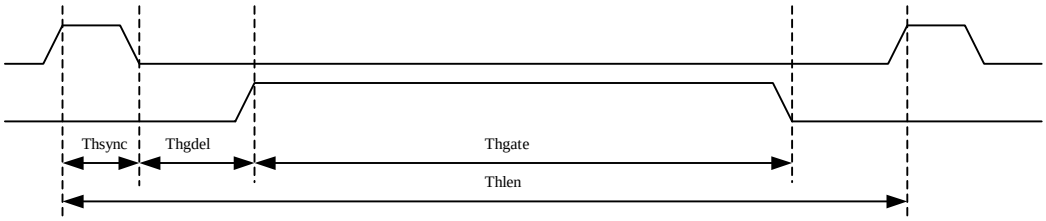
* x = don’t care

4

Operation

4.1 Video Timing

4.1.1 Horizontal Video Timing



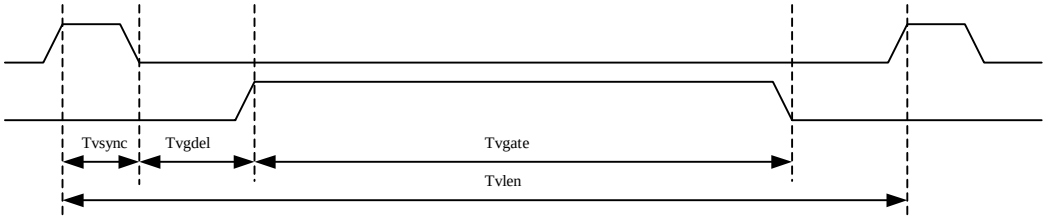
4.1.1.1 Thsync
The Horizontal Synchronization Time is the duration of the horizontal synchronization pulse in pixel clock ticks.

4.1.1.2 Thgdel
The Horizontal Gate Delay Time is the duration of the time between the end of the horizontal synchronization pulse and the start of the horizontal gate in pixel clock ticks. The image can be shifted left/right over the screen by modifying Thgdel. In video timing diagrams this is mostly referred to as the back porch.

4.1.1.3 Thgate
The Horizontal Gate Time is the duration of the visible area of a video line in pixel clock ticks. In video timing diagrams this is mostly referred to as the active time.

4.1.1.4 Thlen
The Horizontal Length Time is the duration of a complete video line in pixel clock ticks, beginning at the start of the horizontal synchronization pulse till the start of the next horizontal synchronization pulse.

4.1.2 Vertical Video Timing



4.1.2.1 Tvsync

The Vertical Synchronization Time is the duration of the vertical synchronization pulse in horizontal lines.

4.1.2.2 Tvgdel

The Vertical Gate Delay Time is the duration of the time between the end of the vertical synchronization pulse and the start of the vertical gate in horizontal lines. The image can be shifted up/down the screen by modifying Tvgdel. In video timing diagrams this is mostly referred to as the back porch.

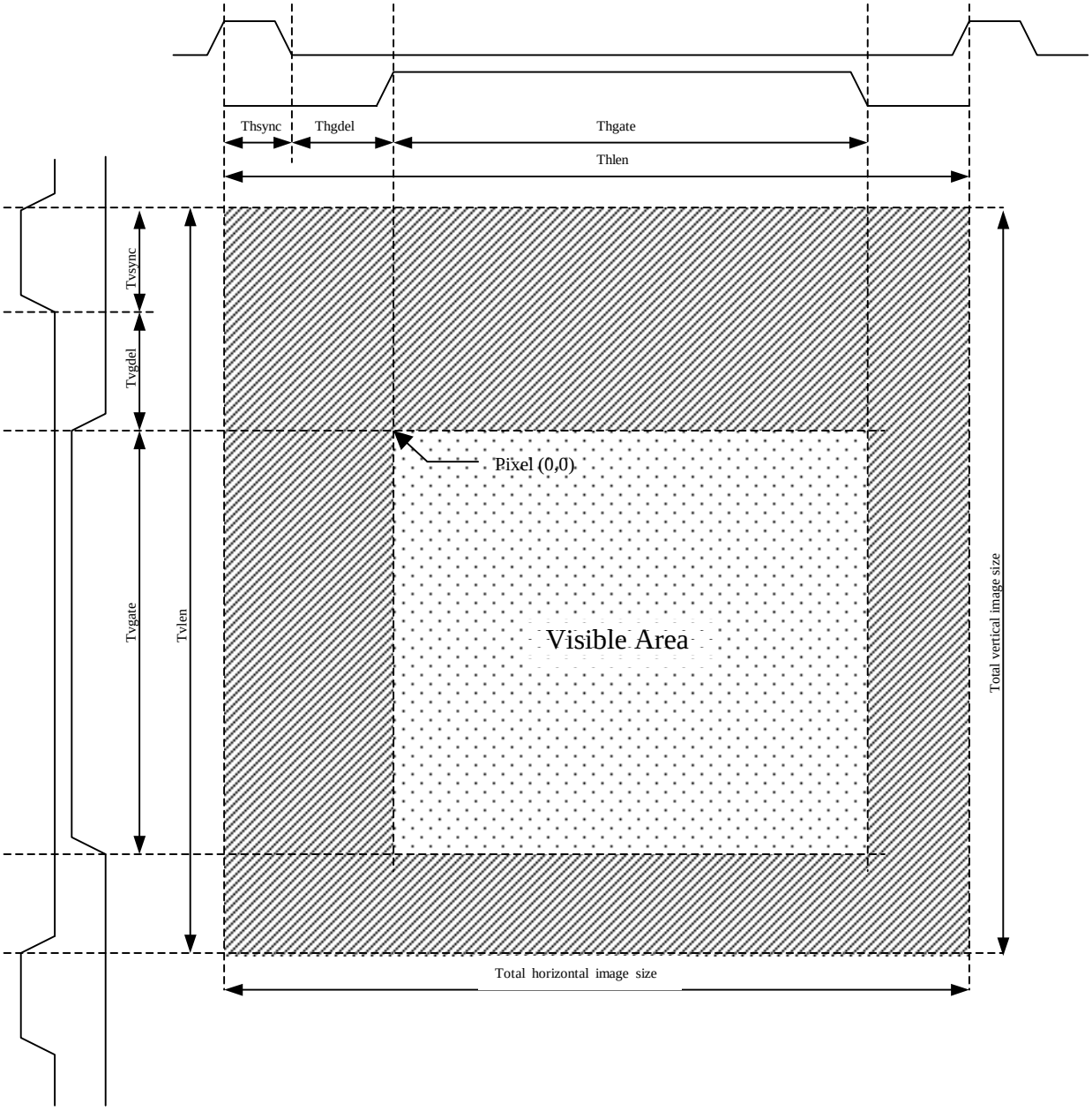
4.1.2.3 Tvgate

The Vertical Gate Time is the duration of the visible area of a video frame in horizontal lines. In video timing diagrams this is mostly referred to as the active time.

4.1.2.4 Tvlen

The Vertical Length Time is the duration of a complete video frame in horizontal lines, beginning at the start of the vertical synchronization pulse till the start of the next vertical synchronization pulse.

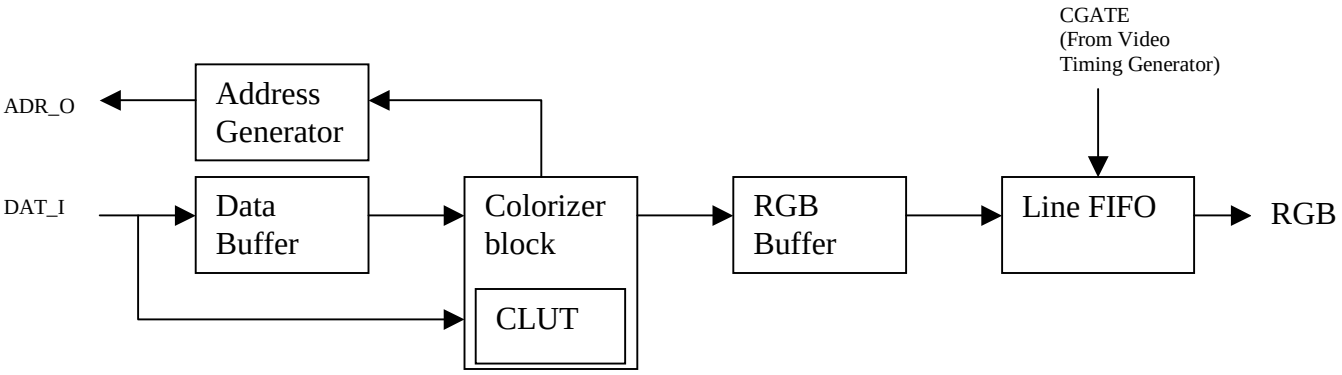
4.1.3 Combined Video Frame Timing



The video frame is composed of Tvlen video lines, each Thlen pixels long. The logical AND function of the horizontal gate and the vertical gate defines the visible area, the rest of the image is blanked.

4.2 Pixel Color Generation

4.2.1 Color Processor Internals



A block called the Color Processor, together with the Wishbone Master interface and the Line Fifo handles the pixel color generation. The internal structure of the Color Processor, including the Line Fifo and parts of the Wishbone Master interface is shown in the figure above.

4.2.1.1 Address Generator

The address generator is part of the Wishbone Master interface. It generates the video memory addresses, performs video memory bank switching and keeps track of the number of pixels to read. When all pixels are read the video memory bank is switched, the video memory offset (i.e. pixel counter) is reset and, when enabled, the bank switch interrupt is generated. The bank switch interrupt is only dependent on the amount of pixels read, i.e. it has no fixed timing relation to HSYNC or VSYNC.

4.2.1.2 Data Buffer

The data buffer temporarily stores the data read from the video memory. It can contain 16 32bits entries. The system tries to keep the data buffer at least half full. The data is read from the video memory by a consecutive address burst; i.e. [wbm_cab_o] is asserted. The burst length is determined by the Video memory Burst Length [VBL] bits in the control registers. It is possible that multiple burst accesses are executed within a single access cycle.
All data is stored consecutive and all available bits are used, independent of color depth. In 8bpp mode a 32bits word stores 4 pixels, in 16bpp mode a 32bit word stores 2 pixels and in 24bpp a 32bits word stores 1 1/3 pixel.

4.2.1.3 Colorizer

The colorizer translates the data stored in the data buffer into colors. See the examples below.

The table below shows the Data Buffer contents used in the examples. Only 8 out of the 16 possible entries are shown. The buffer is read from the top to the bottom; i.e. 0x01234567 is the first data read, 0x89abcdef is the second etc.

Data Buffer contents
0x01234567
0x89abcdef
0x01234567
0x89abcdef
0x01234567
0x89abcdef
0x01234567
0x89abcdef

24bpp example.

In 24bits per pixel mode the RGB-colors are generated as shown in the following sequence:
Da(31:8), Da(7:0)Db(31:16), Db(15:0)Dc(31:24), Dc(23:0)

The table below shows the RGB-colors that are generated from the sample data in the Data Buffer.

Color Data	R	G	B
0x12345	0x01	0x23	0x45
0x6789ab	0x67	0x89	0xab
0xcdef01	0xcd	0xef	0x01
0x234567	0x23	0x45	0x67
0x89abcd	0x89	0xab	0xcd
0xef0123	0xef	0x01	0x23
0x456789	0x45	0x67	0x89
0xabcdef	0xab	0xcd	0xef
0x012345	0x01	0x23	0x45
0x6789ab	0x67	0x89	0xab
0xcdef…	0xcd	0xef	…

TrippleDisplay mode

The system is capable of driving up to three different displays at the same time. The system operates in TrippleDisplay mode when it is setup for 24bpp mode, but each of the three colors contains gray-scale information for a single display.

16bpp example.
In 16bits per pixel mode the upper 16bits carry the data for the first pixel and the lower 16bits carry the data for the second pixel. The 24bit RGB data is extracted from the 16bit color data as follows:
R(7:0) = color_data(15:11), 000b
G(7:0) = color_data(10:5), 00b
B(7:0) = color_data(4:0), 000b

The table below shows the RGB-colors that are generated from the sample data in the Data Buffer. Only the first 4 pixels are shown.

Color Data	R	G	B
0x0123	0x00	0x24	0x18
0x4567	0x40	0xac	0x38
0x89ab	0x88	0x34	0x58
0xcdef	0xc8	0xbc	0x78

8bpp gray-scale example.
In 8bits per pixel gray-scale mode the color data for each of the three colors are equal. The information stored in one byte is sent to all three colors, effectively producing a black-and-white image with 256 gray-scales.

The table below shows the RGB-colors that are generated from the sample data in the Data Buffer. Only the first 4 pixels are shown.

Color Data	R	G	B
0x01	0x01	0x01	0x01
0x23	0x23	0x23	0x23
0x45	0x45	0x45	0x45
0x67	0x67	0x67	0x67

8bpp pseudo-color example.
In 8bits per pixel pseudo-color mode the color data represents an offset in the internal color-lookup-table (CLUT). The CLUT contains the RGB color information. This way it is possible to generate an image with 256 different colors with minimal memory requirements. R = clut_data_out(23:16)
G = clut_data_out(15:8)
B = clut_data_out(7:0)

The table below shows CLUT address for the first 4 pixels.

Color Data	CLUT offset
0x01	0x01
0x23	0x23
0x45	0x45
0x67	0x67

4.2.1.4 Color Lookup Table

The Color Lookup Table (or CLUT) is a 512x24bit single clock synchronous static memory. Divided into two separate CLUTS each 256x24bit large. Either one of them is accessed by the colorizer, depending on the Active CLUT Memory Page [ACMP] flag in the status register. When the ACMP flag is cleared (‘0’) CLUT0 is accessed, when the ACMP flag is set (‘1’) CLUT1 is accessed.

The CLUT memory is mapped into the core’s address range. It can be externally accessed (read and write) via the slave interface; starting at address 0x800. CLUT0 is located at memory range 0x800 – 0xBFC, CLUT1 is located at memory range 0xC00 – 0xFFC. All external accesses to the CLUT are 32bits, but the CLUT itself is only 24bits wide. The top-most bits[31:24] are ignored for write accesses and are always zero for read accesses.

4.2.1.5 RGB buffer

The RGB buffer temporarily stores the RGB values generated by the Colorizer. It can contain 4 24bits entries. The RGB buffer is used to simplify the Colorizer and the Line Fifo. The Colorizer always generates RGB values for 4 pixels, which are stored in the RGB buffer until there is room in the Line Fifo. The Colorizer waits until the RGB buffer is empty before storing new RGB values in it.

4.2.1.6 Line Fifo

The Line Fifo is a dual clocked FIFO, its two clock inputs are controlled by the Wishbone clock [wb_clk_i] and the VGA dot-clock [clk_p_i]. It stores the RGB values before they are send to the VideoDAC or the LCD.

4.3 Bank switching

4.3.1 Introduction

The bank switching system is implemented as a double buffering scheme, also known as a Ping-Pong system. The core reads pixel information from one memory bank while the second bank is being filled. When the second bank has been filled, the host sets the Video Bank Switch Enable bit [VBSE] and/or the Color Lookup Table Bank Switch Enable bit [CBSE]. The core finishes reading the current bank, until the entire frame has been read. It then switches to the second bank and starts reading the new frame. The core automatically resets the VBSE and CBSE bits to avoid accidentally switching to the previous bank. A Video Bank Switch Interrupt is generated when the core switches between the two video memory banks and a CLUT Bank Switch Interrupt is generated when the core switches between the two Color Lookup Tables.

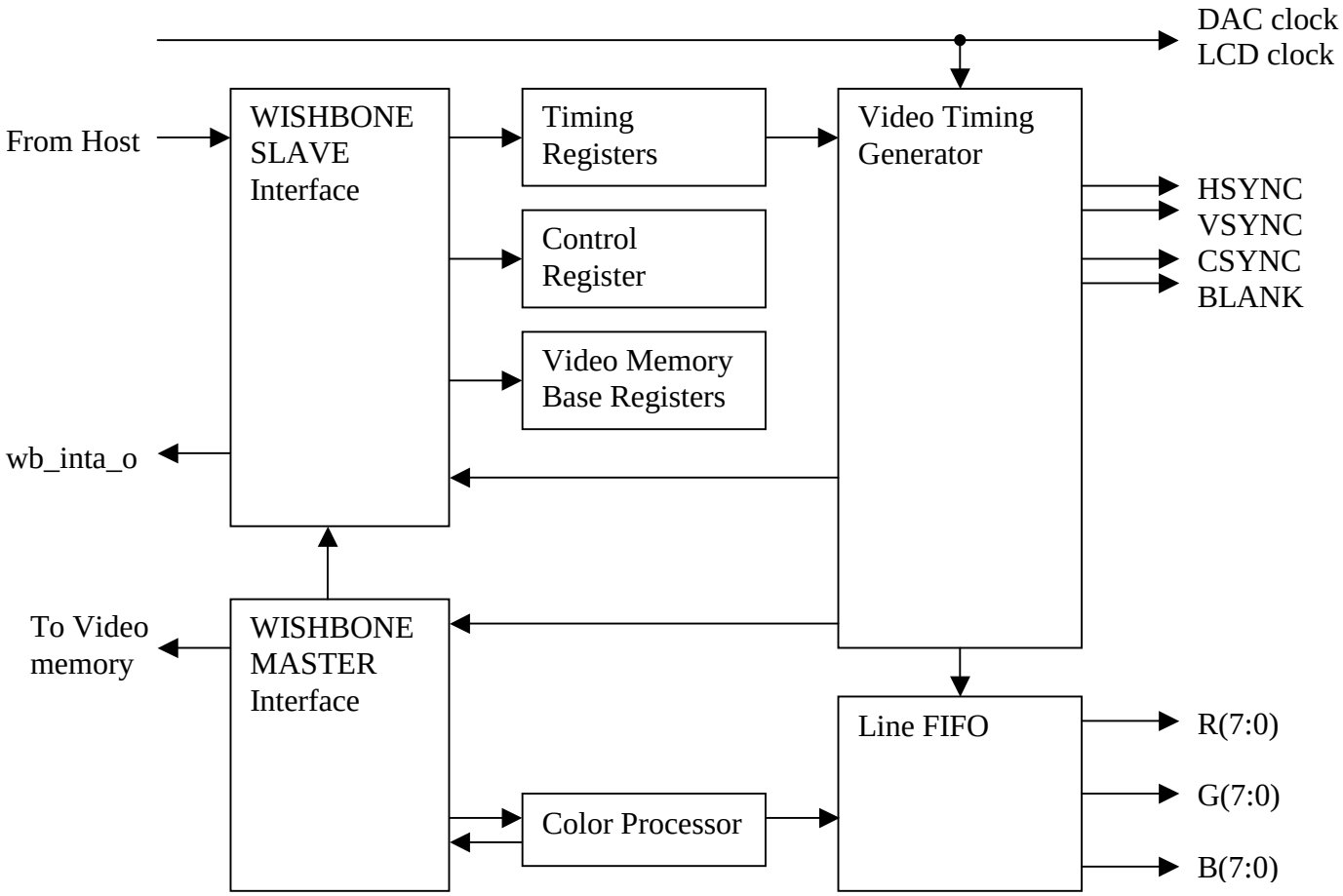
4.3.2 Host notes

The host should not set the VBSE or CBSE bits until all frame information has been written to the video memory. The host system should wait for the Bank Switch Interrupt before filling the previous memory bank.

4.3.3 Sequence:

1) Fill video bank0
2) Fill video bank1
3) Set VBSE, CBSE, BSIE
4) Wait for interrupt
5) Fill video bank0
6) Set VBSE, CBSE
7) Wait for interrupt
8) Fill video bank1
9) Set VBSE, CBSE
10) Goto step 4

5 Architecture



Color Processor

The Color Processor translates the received pixel data to RGB color information. When in 24bit-color mode this is a pass-through function. In 16bit-color mode this is a linear translation: 5bit Red, 6bit Green and 5bit Blue. When in 8bit gray-scale mode the same data is placed on the red, green and blue color outputs, effectively generating a black-and-white image. When in 8bit pseudo color mode the received pixel data is send through the internal color lookup table.

Line FIFO

The dual-clocked Line FIFO ensures a continuos data stream towards the VGA or LCD display and ensures a correct transformation from the Wishbone clock domain to the VGA clock domain.

Video Memory Base Registers

The Video Memory Base Registers contain the starting addresses of the external video memory banks.

Video Timing Generator

The Video Timing Generator generates the horizontal synchronization pulse [HSYNC], the vertical synchronization pulse [VSYNC], the corresponding interrupt signals [HINT] and [VINT], the composite synchronization pulse [CSYNC], the blanking signal [BLANK] and the read request to the Line FIFO.

Appendix A

VGA Modes

This appendix describes some common VGA modes.

A.1 Vertical Timing information common VGA modes

Mode	Resolution	Refresh rate	Line Width	Sync Pulse		Back porch		Active time		Front porch		Frame Total	
			usec	usec	lin	usec	lin	usec	lin	usec	lin	usec	lin
QVGA	320x240	60 Hz											
VGA	640x480	60 Hz	31.78	63	2	953	30	15382	484	285	9	16683	525
VGA	640x480	72 Hz	26.41	79	3	686	26	12782	484	184	7	13735	520
VGA	800x600	56 Hz	28.44	56	1	568	20	17177	604		-1*	17775	625
VGA	800x600	60 Hz	26.40	106	4	554	21	15945	604		-1*	16579	628
VGA	800x600	72 Hz	20.80	125	6	436	21	12563	604	728	35	13853	666

- The Active Time includes 4 overscan border lines. Some timing tables include these into the back and front porch.
- When the Active Time is increased, it passes the rising edge of the vsync signal. Hence the –1 Front Porch.

A.2 Horizontal Timing information common VGA modes

Mode	Resolution	Refresh rate	Pixel Clock	Sync Pulse		Back porch	Active time	Front porch	Line Total
			MHz	usec	Pix	pix	pix	pix	pix
QVGA	320x240	60 Hz							
VGA	640x480	60 Hz	25.175	3.81	96	45	646	13	800
VGA	640x480	72 Hz	31.5	1.27	40	125	646	21	832
VGA	800x600	56 Hz	36	2	72	125	806	21	1024
VGA	800x600	60 Hz	40	3.2	128	85	806	37	1056
VGA	800x600	72 Hz	50	2.4	120	61	806	53	1040

- The Active Time includes 6 overscan border lines. Some timing tables include these into the back and front porch.

Partially taken from Jere Makela, Software design for a video conversion equipment, Master's Thesis, Helsinki Univerity of Technology.

Appendix B

Target Dependent Implementations

The parts of the system which could be target dependent for FPGA implementations and are absolutely target dependent for ASIC implementations are the dual clocked RAM block for the Line FIFO and the single clock RAM block for the internal CLUT.

The RAM blocks are instantiated by the generic_spram.v and generic_dpram.v files. These files contain a FPGA synthesizable model, which has been tested with Exemplar's LeonardoSpectrum and Synplicity's Synplify for Altera (FLEX, ACEX, APEX) and Xilinx devices (Virtex, Spartan). They also contain modules for some ASIC technologies.

The technology is set by a define statement in the vga_defines.v file.
`define VENDOR_FPGA → use FPGA synthesizable model
`define VENDOR_ARTISAN → use Artisan memories
`define VENDOR_VIRTUALSILICON → use VirtualSilicon memories
.
.
.

Check the generic_spram.v and generic_dpram.v files for more information.

Appendix C

Core Structure