VGA/LCD Core Specifications

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Revision History

Rev.	Date	Author	Description
0.1	10/04/01	Richard Herveille	First Draft
0.1a	20/04/01	Richard Herveille	Changed *proposal* to *specifications* Added Appendix A Extended Register Specifications
0.2	21/05/01	Richard Herveille	First official release Added OpenCores logo Changed Chapter 1, Introduction Finished Chapter 2, IO ports Finished Chapter 3, Registers Extended Chapter 4, Operation Changed Chapter 5, Architecture Added Appendix B
0.3	28/05/01	Richard Herveille	Fixed some inconsistencies.
0.4	03/06/01	Richard Herveille	Changed all references to address related subjects (core fix & documentation fix). Added Appendix C
0.4a	04/06/01	Richard Herveille	Fixed some minor typing errors in the document (credits: Rudolph Usselmann)
0.5	15/07/01	Richard Herveille	Added Color Lookup Table bank switching. Added embedded CLUT section.

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Introduction

The VGA/LCD core provides elementary VGA capabilities for embedded systems. It supports both CRT and LCD displays, with user programmable resolutions and timings.

The core supports 24bit and 16bit color modes and 8bit gray-scale and 8bit pseudo-color modes. The pseudo color mode uses external memory for color look-up tables. The external CLUT can either be on-chip or off-chip memory, depending on the system integrator's demands.

The external video memory can be shared with the system memory (Video-On-Demand) or can be a separate memory, dedicated to the core.

Features:

- **CRT and LCD display support**
- **User programmable resolutions**
- **User programmable video timing**
- **24bit and 16bit color modes**
- **8bit gray-scale and 8bit pseudo-color modes**
- **Supports video memory bank switching**
- **TripleDisplay support**

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IO ports

2.1 WISHBONE Common Interface Connections

Port	Width	Direction	Description
CLK_I	1	Input	Master clock input
RST_I	1	Input	Synchronous active high reset
NRESET	1	Input	Asynchronous active low reset
INTA_O	1	Output	Interrupt request signal

2.1.1 CLK_I
All internal WISHBONE logic is registered to the rising edge of the [CLK_I] clock input. The frequency range over which the core can operate depends on the technology used and the pixel clock needed; [CLK_I] may not be slower than the pixel clock [PCLK].

2.1.2 RST_I
The active high synchronous reset input [RST_I] forces the core to restart. All internal registers are preset and all state-machines are set to an initial state.

2.1.3 nRESET:
The active low asynchronous reset input [nRESET] forces the core to restart. All internal registers are preset and all state-machines are set to an initial state.

nRESET is not a WISHBONE compatible signal. It is provided for FPGA implementations. Since most FPGAs provide a dedicated reset path using [nRESET] instead of [RST_I] can result in lower cell-usage and higher performance. Either use [nRESET] or [RST_I].

2.1.4 INTA_O
The interrupt request output is asserted when the core needs service from the host system.

2.2 WISHBONE Slave Interface Connections

Port	Width	Direction	Description
ADR_I	3	Input	Lower address bits
SDAT_I	32	Input	Slave Data bus input
SDAT_O	32	Output	Slave Data bus output
SEL_I	4	Input	Byte select signals
WE_I	1	Input	Write enable input

STB_I	1	Input	Strobe signal/Core select input
CYC_I	1	Input	Valid bus cycle input
ACK_O	1	Output	Bus cycle acknowledge output
ERR_O	1	Output	Bus cycle error output

2.2.1 ADR_I
The address array input [ADR_I] is used to pass a binary coded address to the core. The most significant bit is at the higher number of the array.

2.2.2 SDAT_I
The data array input [SDAT_I] is used to pass binary data to the core. All data transfers are 32bit wide.

2.2.3 SDAT_O
The data array output [SDAT_O] is used to pass binary data from the core to the MASTER. All data transfers are 32bit wide.

2.2.4 SEL_I
The byte select array input [SEL_I] indicates where valid data is placed on the [DAT_I] input array during writes to the core, and where it is expected on the [DAT_O] output array during reads from the core. The core requires all accesses to be 32bit wide [SEL_I(3:0)] = ‘1111’b.

2.2.5 WE_I
The write enable input [WE_I], when asserted indicates whether the current bus cycle is a read or write cycle. The signal is asserted during write cycles and negated during read cycles.

2.2.6 STB_I
The strobe input [STB_I] is asserted when the core is being addresses. The core only responds to WISHBONE signals when [STB_I] is asserted, except for [RST_I] and [nRESET] reset signals, which are always responded to.

2.2.7 CYC_I
The cycle input [CYC_I], when asserted indicates that a valid bus cycle is in progress. The logical AND function of [STB_I] and [CYC_I] indicates a valid transfer cycle to/from the core.

2.2.8 ACK_O
The acknowledge output [ACK_O], when asserted indicates the normal termination of a valid bus cycle.

2.2.9 ERR_O

The error output [ERR_O], when asserted indicates an abnormal termination of a bus cycle. The [ERR_O] output signal is asserted when the host tries to access the controller's internal registers using non 32bit aligned data; i.e. SEL_I(3:0) not equal to 1111b.

2.3 WISHBONE Master Interface Connections

Port	Width	Direction	Description
ADR_O	30	Output	Address bus output
MDAT_I	32	Input	Data bus input
SEL_O	4	Output	Byte select signals
WE_O	1	Output	Write enable output
STB_O	1	Output	Strobe signal
CYC_O	1	Output	Valid bus cycle output
CAB_O	1	Output	Consecutive address burst output
ACK_I	1	Input	Bus cycle acknowledge input
ERR_I	1	Input	Bus cycle error Input

2.3.1 ADR_O
The address array input [ADR_I] is used to pass a binary coded address from the core to the external video or CLUT memory. The most significant bit is at the higher number of the array.

2.3.2 MDAT_I
The master data array input [MDAT_I] is used to pass binary data to the core. All data transfers are 32bit wide.

2.3.3 SEL_O
The byte select array output [SEL_O] indicates where valid data is expected on the [DAT_I] input array. The core support 32bit wide accesses only [SEL_O(3:0)] = '1111'b.

2.3.4 WE_O
The write enable output [WE_O], when asserted indicates whether the current bus cycle is a read or write cycle. The core only support reads from the external memory/memories, [WE_O] is therefore always negated ('0').

2.3.5 STB_O
The strobe output [STB_O] is asserted when the core wants to read from the external video or CLUT memory.

2.3.6 CYC_O
The cycle output [CYC_O] is asserted when the core wants to read from the external video or CLUT memory.

2.3.7 CAB_O
The consecutive address burst output [CAB_O] is asserted when the core wants to perform a burst read from the video memory.

2.3.8 ACK_I
The acknowledge input [ACK_I], when asserted indicates the normal termination of a valid bus cycle.

2.3.9 ERR_I
The error input [ERR_I], when asserted indicates an abnormal termination of a bus cycle. When the [ERR_I] signal is asserted the core stops the current transfer. The state of the core after the assertion of ERR_I is undefined.

2.4 External Connections

Port	Width	Direction	Description
PCLK	1	Input	Pixel Clock
HSYNC	1	Output	Horizontal Synchronization Pulse
VSYNC	1	Output	Vertical Synchronization Pulse
CSYNC	1	Output	Composite Synchronization Pulse
BLANK	1	Output	Blank signals
R	8	Output	Red Color Data
G	8	Output	Green Color Data
B	8	Output	Blue Color Data

2.4.1 PCLK
All internal video logic is registered to the rising edge of the [PCLK] clock input. The frequency range over which the core can operate depends on the technology used and the pixel clock needed; [PCLK] may not be faster than the WISHBONE clock [CLK_I].

2.4.2 HSYNC
The horizontal synchronization pulse is asserted when the raster scan ray needs to return to the start position (the left side of the screen).

2.4.3 VSYNC
The vertical synchronization pulse is asserted when the raster scan ray needs to return to the vertical start position (the top of the screen).

2.4.5 CSYNC
The composite synchronization pulse is a combined horizontal and vertical synchronization signal.

2.4.6 BLANK
The blank output is asserted during the period no image is projected on the screen; the back porch, synchronization pulses and the front porch.

2.4.7 R, G, B

Red, green and blue pixel data. The RGB lines contain invalid data while BLANK is asserted.

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Registers

3.1 Registers list

Name	ADR_I(4:2)	Width	Access	Description
CTRL	0x00	32	R/W	Control Register
STAT	0x01	32	R/W	Status Register
HTIM	0x02	32	R/W	Horizontal Timing Register
VTIM	0x03	32	R/W	Vertical Timing Register
HVLEN	0x04	32	R/W	Horizontal and Vertical Length Register
VBARa	0x05	32	R/W	Video Memory Base Address Register A
VBARb	0x06	32	R/W	Video Memory Base Address Register B
CBAR	0x07	32	R/W	Color Lookup Table Base Address Register

3.2 Control Register [CTRL]

Bit #	Access	Description
31:16	R/W	*reserved*
15	R/W	BL, Blanking Polarization Level 0: Positive 1: Negative
14	R/W	CSL, Composite Synchronization Pulse Polarization Level 0: Positive 1: Negative
13	R/W	VSL, Vertical Synchronization Pulse Polarization Level 0: Positive 1: Negative
12	R/W	HSL, Horizontal Synchronization Pulse Polarization Level 0: Positive 1: Negative
11	R/W	PC, 8bit Pseudo Color 0: 8bit gray scale 1: 8bit pseudo color
10,9	R/W	CD, Color Depth 11: reserved 10: 24bit per pixel 01: 16bit per pixel 00: 8bit per pixel
8,7	R/W	VBL, Video memory Burst Length

		11b: 8 cycles 10b: 4 cycles 01b: 2 cycles 00b: 1 cycle
6	R/W	*Reserved*
5	R/W	CBSWE, CLUT Bank Switching Enable
4	R/W	VBSWE, Video Bank Switching Enable
3	R/W	BSIE, Bank Switch Interrupt Enable
2	R/W	HIE, Horizontal Interrupt Enable
1	R/W	VIE, Vertical Interrupt Enable
0	R/W	VEN, Video Enable

Reset Value: 0x00000000

3.2.1 BL

The Blanking Polarization Level defines the voltage level the BLANK output has when the blank signal is asserted. When BL is cleared (‘0’) BLANK is at a high voltage level when the blank signal is asserted and at a low voltage level when not (i.e. BLANK is active high). When BL is set (‘1’) BLANK is at a low voltage level when the blank signal is asserted and at a high voltage level when not (i.e. BLANK is active low).

3.2.2 BSIE

When the Bank Switch Interrupt Enable bit is set (‘1’) and a bank switch is requested, the host is interrupted. The Bank Switch interrupt is independent of the Bank Switch Enable bits settings. Setting this bit while the Bank Switch Interrupt Pending (BSINT) flag is set generates an interrupt. Clearing this bit while BSINT is set disables the interrupt request, but does not clear the interrupt pending flag.

3.2.3 CBSWE

When the CLUT Bank Switch Enable bit is set (‘1’) and a complete video frame has been read into the line buffer, the core switches between the two available color lookup tables located at the memory addresses set in the CLUT Memory Base Address register. The Active CLUT Memory Page (ACMP) flag reflects the current active Color Lookup Table. When the CLUT Bank Switch Enable bit is cleared (‘0’) the core continues using the currently active CLUT.

3.2.4 CD

The Color Depth bits define the number of bits per pixel (bpp), either 8, 16 or 24bpp.

3.2.5 CSL

The Composite Sync Polarization Level defines the voltage level the CSYNC output has when the composite sync signal is asserted. When CSL is cleared (‘0’) CSYNC is at a high voltage level when the composite sync signal is asserted and at a low voltage level when not (i.e. CSYNC is active high). When CSL is set (‘1’) CSYNC is at a low voltage level when the composite sync signal is asserted and at a high voltage level when not (i.e. CSYNC is active low).

3.2.6 HIE
When the Horizontal Interrupt Enable bit is set (‘1’) and a horizontal interrupt is pending, the host system is interrupted. Setting this bit while the Horizontal Interrupt Pending (HINT) flag is set generates an interrupt. Clearing this bit while HINT is set disables the interrupt request, but does not clear the interrupt pending flag.

3.2.7 HSL
The Horizontal Sync Polarization Level defines the voltage level the HSYNC output has when the horizontal sync signal is asserted. When HSL is cleared (‘0’) HSYNC is at a high voltage level when the horizontal sync signal is asserted and at a low voltage level when not (i.e. HSYNC is active high). When HSL is set (‘1’) HSYNC is at a low voltage level when the horizontal sync signal is asserted and at a high voltage level when not (i.e. HSYNC is active low).

3.2.8 PC
When in 8bpp mode the pixel-data can be used as black and white information (256 gray scales) or as an index to a color lookup table (pseudo color mode). When the 8PC bit is set (‘1’) the core operates in pseudo color mode and the pixel-data is used to read the color data from the CLUT. When the 8PC bit is cleared (‘0’) the pixel-data is placed on the red, green and blue outputs, effectively producing a black and white image with 256 different gray-scales.

3.2.9 VBSW
When the Video Bank Switch Enable bit is set (‘1’) and a complete video frame has been read into the line buffer, the core switches between the two available video pages located at the memory addresses set in the Video Memory Base Address (VBAR) registers. The Active Video Memory Page (AVMP) flag reflects the current active video page. When the Video Bank Switch Enable bit is cleared (‘0’) the core continues using the currently active video page.

3.2.10 VBL
The Video Burst Length bits define the number of transfers during a single block read access to the video memory.

3.2.11 VEN
The video circuit is disabled when the Video Enable bit is cleared (‘0’). The video circuit is enabled when the Video Enable bit is set (‘1’). This bit must be cleared before changing any register contents. After (re)programming all registers this bit may be set.

3.2.12 VIE
When the Vertical Interrupt Enable bit is set (‘1’) and a vertical interrupt is pending, the host system is interrupted. Setting this bit while the Vertical Interrupt Pending (VINT) flag is set generates an interrupt. Clearing this bit while VINT is set disables the interrupt request, but does not clear the interrupt pending flag.

3.2.13 VSL

The Vertical Sync Polarization Level defines the voltage level the VSYNC output has when the vertical sync signal is asserted. When VSL is cleared (‘0’) VSYNC is at a high voltage level when the vertical sync signal is asserted and at a low voltage level when not (i.e. VSYNC is active high). When VSL is set (‘1’) VSYNC is at a low voltage level when the vertical sync signal is asserted and at a high voltage level when not (i.e. VSYNC is active low).

3.3 Status Register [STAT]

Bit #	Access	Description
31:18	R	*Reserved*
17	R	ACMP, Active CLUT Memory Page
16	R	AVMP, Active Video Memory Page
15:7	R	*Reserved*
6	R/W	BSINT, Bank Switch Interrupt Pending
5	R/W	HINT, Horizontal Interrupt Pending
4	R/W	VINT, Vertical Interrupt Pending
1	R/W	LUINT, Line Fifo Under-run Interrupt Pending
0	R/W	SINT, System Error Interrupt Pending

Reset Value: 0x00000000

3.3.1 ACMP

The Active CLUT Memory Page flag is cleared (‘0’) when the active Color Lookup Table is CLUT0, it is set (‘1’) when the active Color Lookup Table CLUT1. This flag is cleared when the Video Enable bit is cleared. See CLUT Base Address Register for more information on CLUT0 and CLUT1.

3.3.2 AVMP

The Active Video Memory Page flag is cleared (‘0’) when the active memory page is located at Video Base Address A (VBARa), it is set (‘1’) when the active memory page is located at Video Base Address B (VBARb). This flag is cleared when the Video Enable bit is cleared.

3.3.3 BSINT

The Bank Switch Interrupt Pending flag is set (‘1’) when all data from the current active memory page has been read. When the BSIE bit is set (‘1’) and BSINT is asserted, the host system is interrupted. Software must clear the interrupt by writing a ‘0’ to this bit.

3.3.4 HINT

The Horizontal Interrupt Pending flag is set (‘1’) when the horizontal synchronization pulse (HSYNC) is asserted. When the HIE bit is set (‘1’) and HINT is asserted, the host system is interrupted. Software must clear the interrupt by writing a ‘0’ to this bit.

3.3.5 LUINT

The Line Fifo Under-run Interrupt Pending flag is set (‘1’) when pixels are read from the line-fifo while it is empty. This can be caused by a locked bus, reading from an illegal video memory or to few entries in the FIFO. When LUINT is asserted the host system is interrupted. Software must clear the interrupt by writing a ‘0’ to this bit.

3.3.6 SINT
The System Error Interrupt Pending flag is set (‘1’) when ERR_I is asserted during a read from the video memory or the color lookup table. When SINT is asserted the host system is interrupted. Software must clear the interrupt by writing a ‘0’ to this bit.

3.3.7 VINT
The Vertical Interrupt Pending flag is set (‘1’) when the vertical synchronization pulse (VSYNC) is asserted. When the VIE bit is set (‘1’) and VINT is asserted, the host system is interrupted. Software must clear the interrupt by writing a ‘0’ to this bit.

3.4 Horizontal Timing Register [HTIM]

Bit #	Access	Description
31:24	R/W	Thsync, Horizontal synchronization pulse width
23:16	R/W	Thgdel, Horizontal gate delay time
15:0	R/W	Thgate, Horizontal gate time

Reset Value: 0x00000000

3.4.1 Thsync
The horizontal synchronization pulse width in pixels –1.

3.4.2 Thgdel
The horizontal gate delay width in pixels –1.

3.4.3 Thgate
The horizontal gate width in pixels –1.

3.5 Vertical Timing Register [VTIM]

Bit #	Access	Description
31:24	R/W	Tvsync, Vertical synchronization pulse width
23:16	R/W	Tvgdel, Vertical gate delay time
15:0	R/W	Tvgate, Vertical gate time

Reset Value: 0x00000000

3.5.1 Tvsync
The vertical synchronization pulse width in horizontal lines.

3.5.2 Tvgdel
The vertical gate delay time in horizontal lines.

3.5.3 Tvgate
The vertical gate width in horizontal lines.

3.6 Horizontal and Vertical Length Register [HVLEN]

Bit #	Access	Description
31:16	R/W	Thlen, Horizontal length
15:0	R/W	Tvlen, Vertical length

Reset Value: 0x00000000

3.6.1 Thlen
The total horizontal line time in pixels –2.

3.6.2 Tvlen
The total vertical line time in horizontal lines.

3.7 Video Base Address [VBARa] [VBARb]

Bit #	Access	Description
31:2	R/W	VBA, Video Base Address
1:0	R	*Always zero*

Reset Value: 0x00000000

3.7.1 Video Base Address
The Video Base Address Register defines the starting point of the video memory. The image is stored in consecutive memory locations, starting at this address. The byte-memory location of a pixel can be calculated as follows:

Adr = ((Y * Thgate) + X) * bytes_per_pixel;

The core supports memories with burst capabilities. Burst transfers of 1, 2, 4 and 8 accesses are supported. The lower address bits must reflect the value entered in the Video Memory Burst Length bits as shown in the table below.

VBL	VBAR (4:2)*
00b	xxxb
01b	xx0b
10b	x00b
11b	000b

* x = don’t care

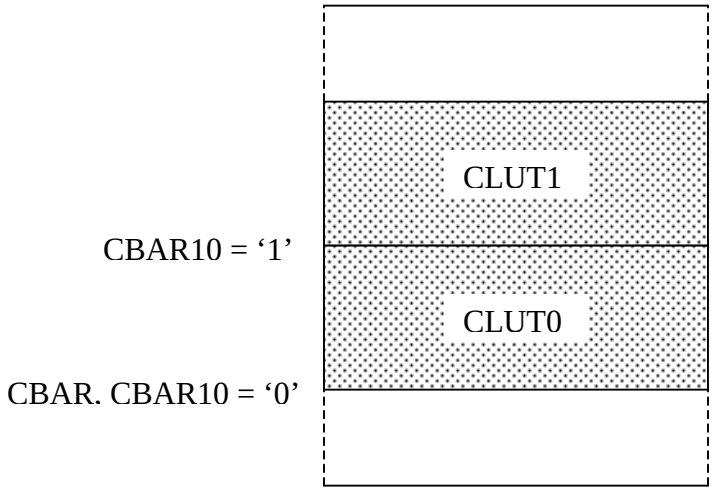
3.8 CLUT Base Address [CBAR]

Bit #	Access	Description
31:11	R/W	CBA, Color Lookup Table Base Address
10:0	R	*Always zero*

Reset Value: 0x00000000

The Color Lookup Table Base Address Register defines the upper 21bits of the CLUT addresses. The two available Color Lookup Tables share the same base address. Switching between the two addresses is done by toggling address bit 10. CLUT0 is located at address (CBA, x“000”), whereas CLUT1 is located at address (CBA, “400”).

Although the Color Lookup Tables are accessed as 32bit memories, only the lower 24bits are used. The upper 8 bits (31:24) are ignored.



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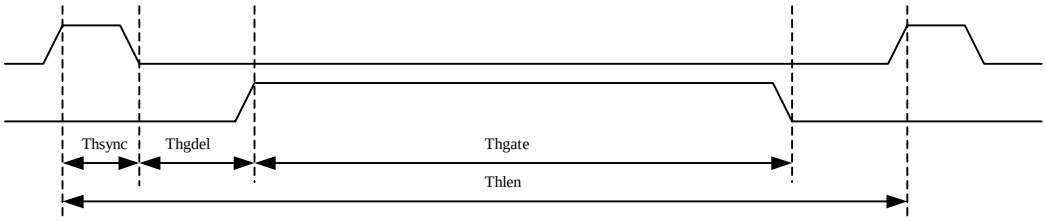
Operation

4.1 Video Timing

4.1.1 Horizontal Video Timing



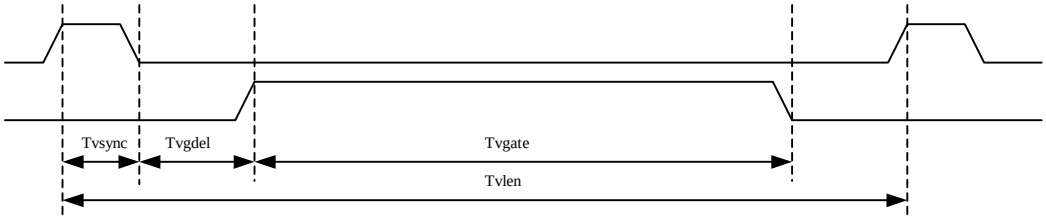
4.1.1.1 Thsync
The Horizontal Synchronization Time is the duration of the horizontal synchronization pulse in pixel clock ticks.

4.1.1.2 Thgdel
The Horizontal Gate Delay Time is the duration of the time between the end of the horizontal synchronization pulse and the start of the horizontal gate in pixel clock ticks. The image can be shifted left/right over the screen by modifying Thgdel. In video timing diagrams this is mostly referred to as the back porch.

4.1.1.3 Thgate
The Horizontal Gate Time is the duration of the visible area of a video line in pixel clock ticks. In video timing diagrams this is mostly referred to as the active time.

4.1.1.4 Thlen
The Horizontal Length Time is the duration of a complete video line in pixel clock ticks, beginning at the start of the horizontal synchronization pulse till the start of the next horizontal synchronization pulse.

4.1.2 Vertical Video Timing



4.1.2.1 Tvsync

The Vertical Synchronization Time is the duration of the vertical synchronization pulse in horizontal lines.

4.1.2.2 Tvgdel

The Vertical Gate Delay Time is the duration of the time between the end of the vertical synchronization pulse and the start of the vertical gate in horizontal lines. The image can be shifted up/down the screen by modifying Tvgdel. In video timing diagrams this is mostly referred to as the back porch.

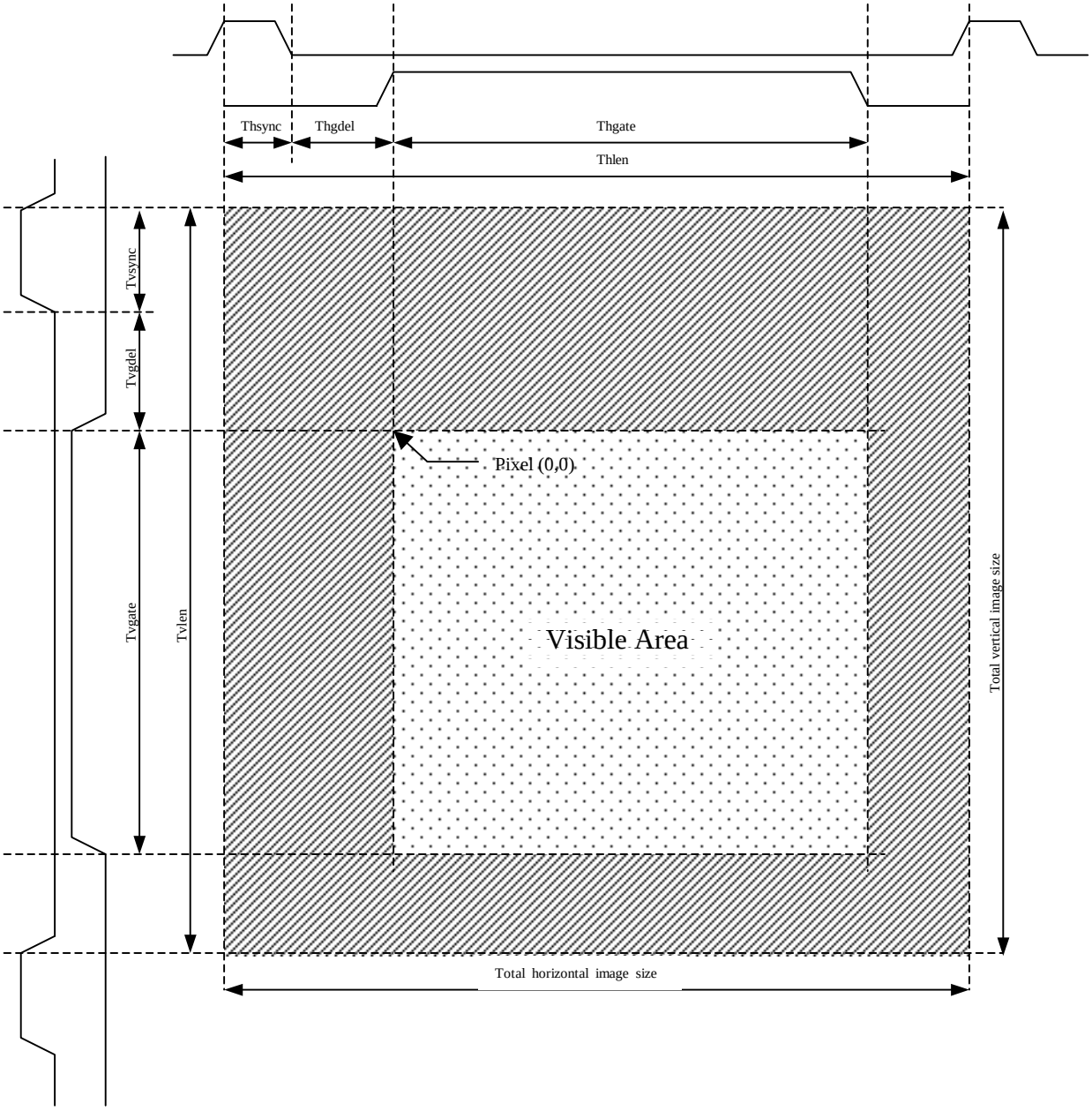
4.1.2.3 Tvgate

The Vertical Gate Time is the duration of the visible area of a video frame in horizontal lines. In video timing diagrams this is mostly referred to as the active time.

4.1.2.4 Tvlen

The Vertical Length Time is the duration of a complete video frame in horizontal lines, beginning at the start of the vertical synchronization pulse till the start of the next vertical synchronization pulse.

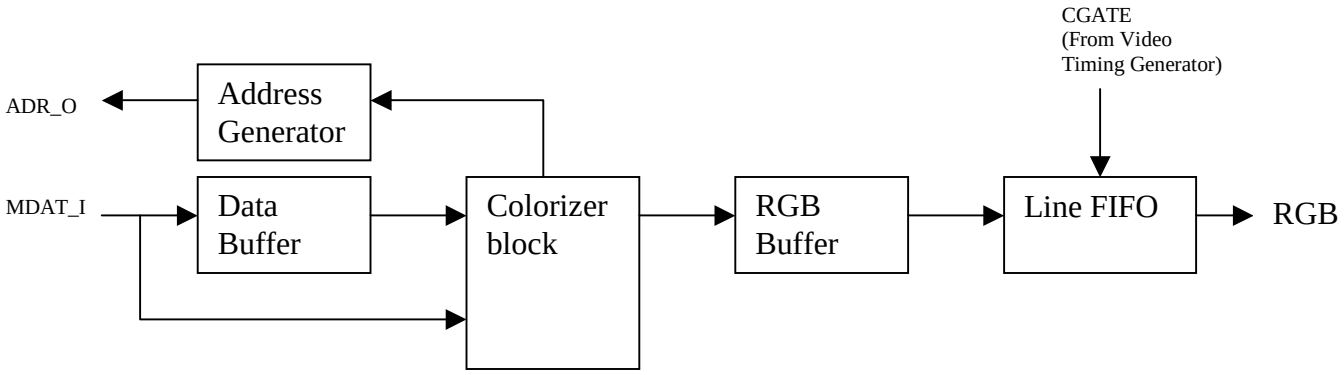
4.1.3 Combined Video Frame Timing



The video frame is composed of Tvlen video lines, each Thlen pixels long. The logical AND function of the horizontal gate and the vertical gate defines the visible area, the rest of the image is blanked.

4.2 Pixel Color Generation

4.2.1 Color Processor Internals



A block called the Color Processor, together with the Wishbone Master interface and the Line Fifo handles the pixel color generation. The internal structure of the Color Processor, including the Line Fifo and parts of the Wishbone Master interface is shown in the figure above.

4.2.1.1 Address Generator

The address generator is part of the Wishbone Master interface. It generates the video memory and color-lookup-table addresses, performs video memory bank switching and keeps track of the number of pixels to read. When all pixels are read the video memory bank is switched, the video memory offset (i.e. pixel counter) is reset and, when enabled, the bank switch interrupt is generated. The bank switch interrupt is only dependent on the amount of pixels read, i.e. it has no fixed timing relation to HSYNC or VSYNC.

4.2.1.2 Data Buffer

The data buffer temporarily stores the data read from the video memory. It can contain 16 32bits entries. The system tries to keep the data buffer at least half full. The data is read from the video memory by a consecutive address burst; [CAB_O] is asserted. The burst length is determined by the Video memory Burst Length [VBL] bits in the control registers. It is possible that multiple burst accesses are executed within a single access cycle. The memory controller should interpret these as separate burst accesses.

NOTE: Because all video memory read accesses are burst accesses, the number of pixel addresses (not pixels!) must be a multiple of the Video memory Burst Length.

All data is stored consecutive and all available bits are used, independent of color depth. In 8bpp mode a 32bits word stores 4 pixels, in 16bpp mode a 32bit word stores 2 pixels and in 24bpp a 32bits word stores 1 1/3 pixel.

4.2.1.3 Colorizer

The colorizer translates the data stored in the data buffer into colors. See the examples below.

The table below shows the Data Buffer contents used in the examples. Only 8 out of the 16 possible entries are shown. The buffer is read from the top to the bottom; i.e. 0x01234567 is the first data read, 0x89abcdef is the second etc.

Data Buffer contents
0x01234567
0x89abcdef
0x01234567
0x89abcdef
0x01234567
0x89abcdef
0x01234567
0x89abcdef

24bpp example.

In 24bits per pixel mode the RGB-colors are generated as shown in the following sequence:
Da(31:8), Da(7:0)Db(31:16), Db(15:0)Dc(31:24), Dc(23:0)

The table below shows the RGB-colors that are generated from the sample data in the Data Buffer.

Color Data	R	G	B
0x12345	0x01	0x23	0x45
0x6789ab	0x67	0x89	0xab
0xcdef01	0xcd	0xef	0x01
0x234567	0x23	0x45	0x67
0x89abcd	0x89	0xab	0xcd
0xef0123	0xef	0x01	0x23
0x456789	0x45	0x67	0x89
0xabcdef	0xab	0xcd	0xef
0x012345	0x01	0x23	0x45
0x6789ab	0x67	0x89	0xab
0xcdef…	0xcd	0xef	…

TrippleDisplay mode

The system is capable of driving up to three different displays at the same time. The system operates in TrippleDisplay mode when it is setup for 24bpp mode, but each of the three colors contains gray-scale information for a single display.

16bpp example.
In 16bits per pixel mode the upper 16bits carry the data for the first pixel and the lower 16bits carry the data for the second pixel. The 24bit RGB data is extracted from the 16bit color data as follows:
R(7:0) = color_data(15:11), 000b
G(7:0) = color_data(10:5), 00b
B(7:0) = color_data(4:0), 000b

The table below shows the RGB-colors that are generated from the sample data in the Data Buffer. Only the first 4 pixels are shown.

Color Data	R	G	B
0x0123	0x00	0x24	0x18
0x4567	0x40	0xac	0x38
0x89ab	0x88	0x34	0x58
0xcdef	0xc8	0xbc	0x78

8bpp gray-scale example.
In 8bits per pixel gray-scale mode the color data for each of the three colors are equal. The information stored in one byte is sent to all three colors, effectively producing a black-and-white image with 256 gray-scales.

The table below shows the RGB-colors that are generated from the sample data in the Data Buffer. Only the first 4 pixels are shown.

Color Data	R	G	B
0x01	0x01	0x01	0x01
0x23	0x23	0x23	0x23
0x45	0x45	0x45	0x45
0x67	0x67	0x67	0x67

8bpp pseudo-color example.
In 8bits per pixel pseudo-color mode the color data represents an offset in an external color-lookup-table (CLUT). The CLUT contains the RGB color information. This way it is possible to generate an image with 256 different colors with minimal memory requirements. The core accesses the CLUT memory as a 32bits wide memory, but uses only the lower 24bits.
R = clut_data_out(23:16)
G = clut_data_out(15:8)
B = clut_data_out(7:0)

The table below shows CLUT address for the first 4 pixels. The CLUT base address is set in the CBAR register.

Color Data	CLUT offset
0x01	0x01
0x23	0x23

0x45 0x67	0x45 0x67

4.2.1.4 RGB buffer

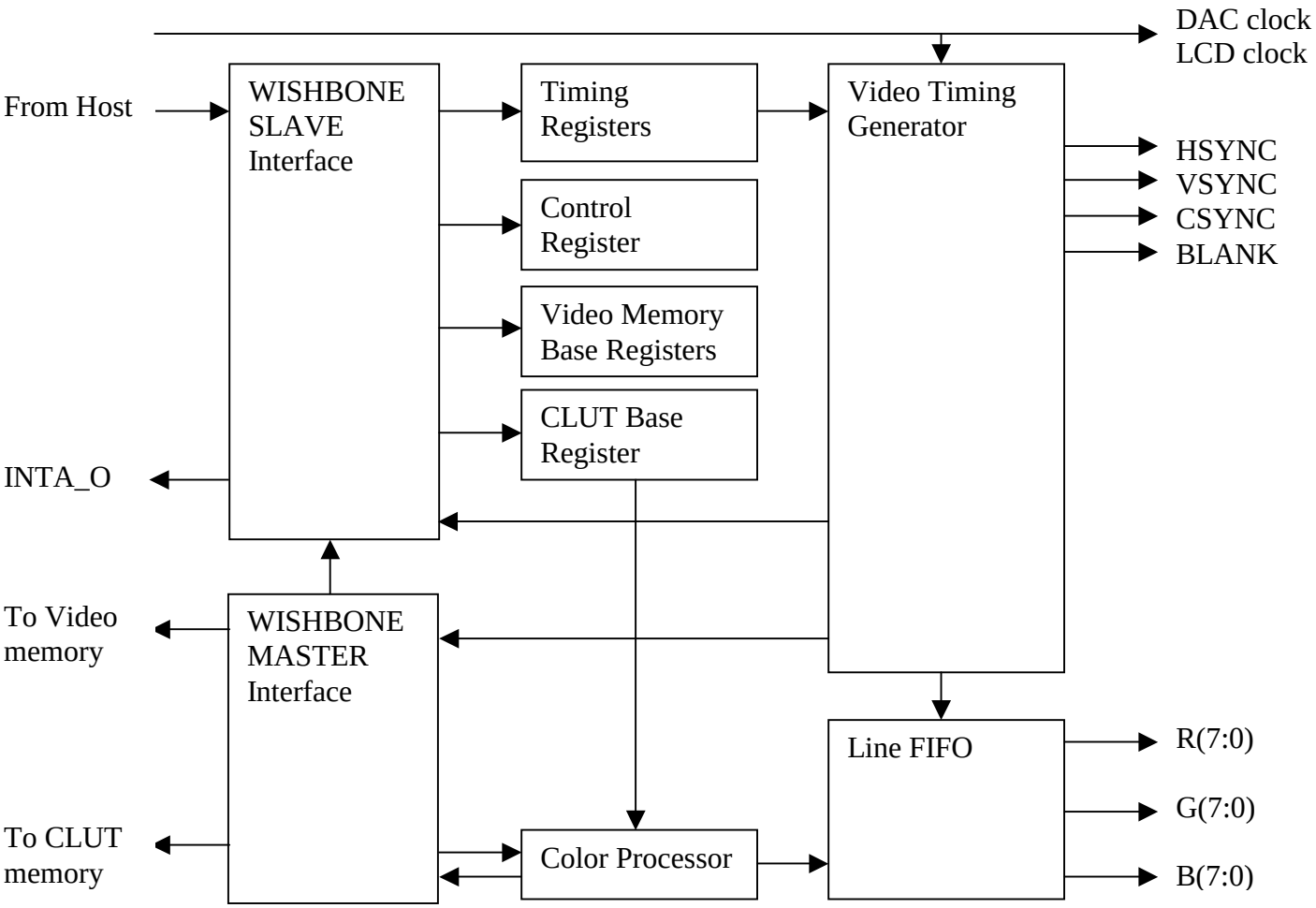
The RGB buffer temporarily stores the RGB values generated by the Colorizer. It can contain 4 24bits entries. The RGB buffer is used to simplify the Colorizer and the Line Fifo. The Colorizer always generates RGB values for 4 pixels, which are stored in the RGB buffer until there is room in the Line Fifo. The Colorizer waits until the RGB buffer is empty before storing new RGB values in it.

4.2.1.5 Line Fifo

The Line Fifo is a dual clocked FIFO, its two clock inputs are controlled by the Wishbone clock and the VGA dot-clock. It stores the RGB values before they are send to the VideoDAC or the LCD.

The FIFO is implemented using an embedded dual-clocked RAM. See appendix B for implementing target specific

5 Architecture



CLUT Base Register

The Color Lookup Table Base Register contains the starting address of the external color lookup table for 8bit pseudo color mode.

Color Processor

The Color Processor translates the received pixel data to RGB color information. When in 24bit-color mode this is a pass-through function. In 16bit-color mode this is a linear translation: 5bit Red, 6bit Green and 5bit Blue. When in 8bit gray-scale mode the same data is placed on the red, green and blue color outputs, effectively generating a black-

and-white image. When in 8bit pseudo color mode the received pixel data is send through an external color lookup table starting at the memory location pointed to by the CLUT Base Register.

Line FIFO

The dual-clocked Line FIFO ensures a continuos data stream towards the VGA or LCD display and ensures a correct transformation from the Wishbone clock domain to the VGA clock domain.

Video Memory Base Registers

The Video Memory Base Registers contain the starting addresses of the external video memory banks.

Video Timing Generator

The Video Timing Generator generates the horizontal synchronization pulse [HSYNC], the vertical synchronization pulse [VSYNC], the corresponding interrupt signals [HINT] and [VINT], the composite synchronization pulse [CSYNC], the blanking signal [BLANK] and the read request to the Line FIFO.

Appendix A

VGA Modes

This appendix describes some common VGA modes.

A.1 Vertical Timing information common VGA modes

Mode	Resolution	Refresh rate	Line Width	Sync Pulse		Back porch		Active time		Front porch		Frame Total	
			usec	usec	lin	usec	lin	usec	lin	usec	lin	usec	lin
QVGA	320x240	60 Hz											
VGA	640x480	60 Hz	31.78	63	2	953	30	15382	484	285	9	16683	525
VGA	640x480	72 Hz	26.41	79	3	686	26	12782	484	184	7	13735	520
VGA	800x600	56 Hz	28.44	56	1	568	20	17177	604		-1*	17775	625
VGA	800x600	60 Hz	26.40	106	4	554	21	15945	604		-1*	16579	628
VGA	800x600	72 Hz	20.80	125	6	436	21	12563	604	728	35	13853	666

- The Active Time includes 4 overscan border lines. Some timing tables include these into the back and front porch.
- When the Active Time is increased, it passes the rising edge of the vsync signal. Hence the –1 Front Porch.

A.2 Horizontal Timing information common VGA modes

Mode	Resolution	Refresh rate	Pixel Clock	Sync Pulse		Back porch	Active time	Front porch	Line Total
			MHz	usec	Pix	pix	pix	pix	pix
QVGA	320x240	60 Hz							
VGA	640x480	60 Hz	25.175	3.81	96	45	646	13	800
VGA	640x480	72 Hz	31.5	1.27	40	125	646	21	832
VGA	800x600	56 Hz	36	2	72	125	806	21	1024
VGA	800x600	60 Hz	40	3.2	128	85	806	37	1056
VGA	800x600	72 Hz	50	2.4	120	61	806	53	1040

- The Active Time includes 6 overscan border lines. Some timing tables include these into the back and front porch.

Partially taken from Jere Makela, Software design for a video conversion equipment, Master's Thesis, Helsinki Univerity of Technology.

Appendix B

Target Dependent Implementations

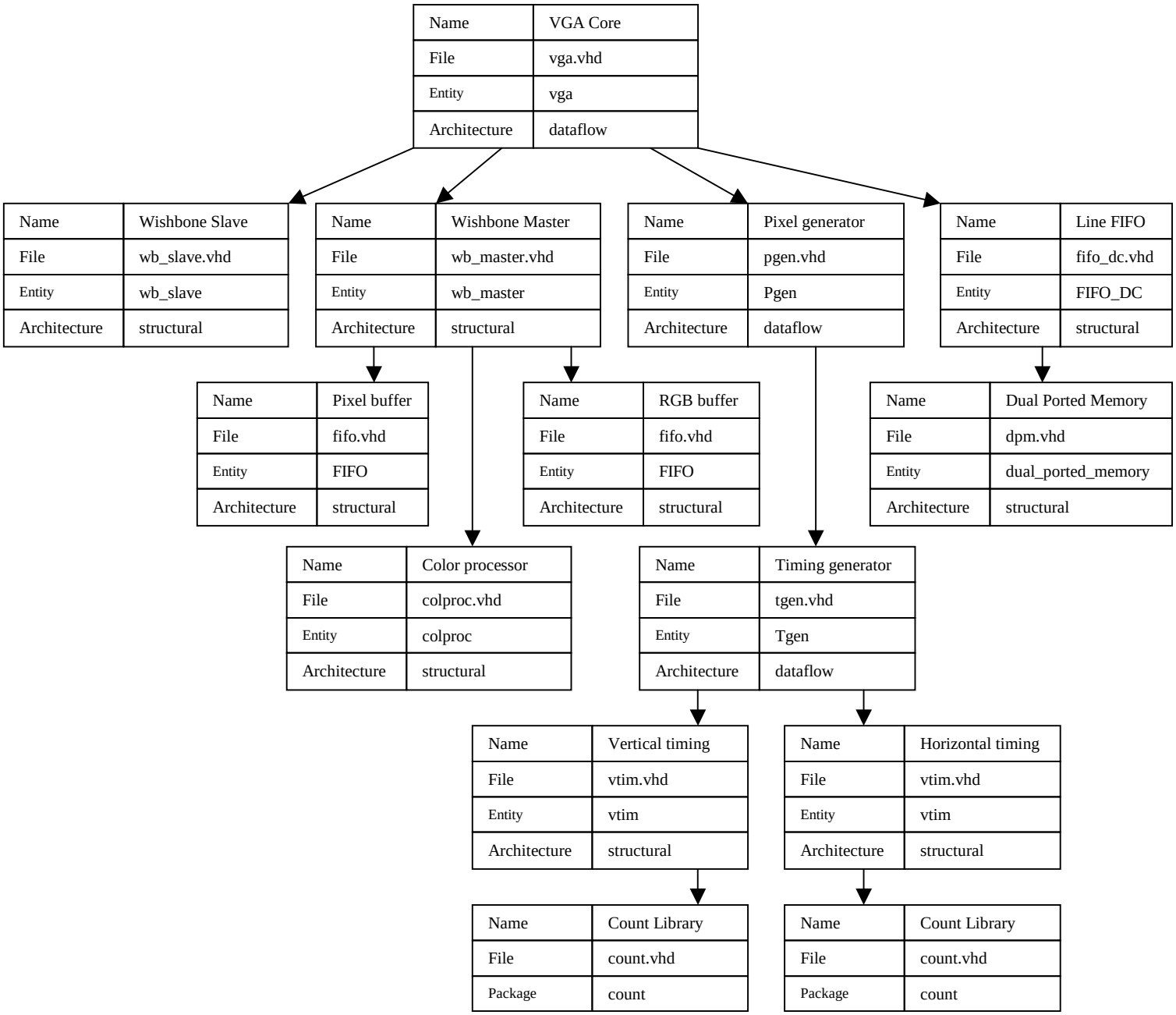
The only part of the system which could be target dependent for FPGA implementations and is absolutely target dependent for ASIC implementations is the dual clocked RAM block for the Line FIFO.

The RAM block is a 256x24bit dual clocked static RAM. It is initialized in dpm.vhd. Target specific RAM blocks must be inserted by editing this file. The source file contains a generic model for a dual-clocked memory block, which should be compatible with common FPGAs. It also contains an example of a target specific module and detailed information on how to implement it. Whatever solution you choose, the functionality as described by the generic model must be maintained.

Appendix C

Core Structure

VGA Core



VGA & CLUT Core