Key Design Features

- 12-bit signed output data samples
- 32-bit phase accumulator (tuning word)
- Phase resolution of $2\pi/2^{32}$
- Frequency resolution of $Fs/2^{32}$ (Fs = sample frequency)
- ≈ 70 dB Signal-to-Noise Ratio (SNR)
- ≈ 70 dB Spurious Free Dynamic Range (SFDR)
- Simultaneous SIN, COS, Square and Sawtooth output waveforms
- 2 clock-cycle latency
- Sample rates of 500 MHz+[1]

Applications

- Digital oscillators
- Digital modulation
- Digital up/down conversion
- Generation of Quadrature (Complex) signals
- Versatile waveform generation

Pin-out Description

Pin name	*I/O*	*Description*	*Active state*
clk	in	Sample clock	rising edge
reset	in	Asynchronous reset	low
phase_inc [31:0]	in	Phase increment as an unsigned 32-bit number (controls frequency of output waveform)	data
sin_out [11:0]	out	Sine wave output (16-bit signed number)	data
cos_out [11:0]	out	Cosine wave output (16-bit signed number)	data
squ_out [11:0]	out	Square wave output (16-bit signed number)	data
saw_out [11:0]	out	Sawtooth wave output (16-bit signed number)	data

Block Diagram

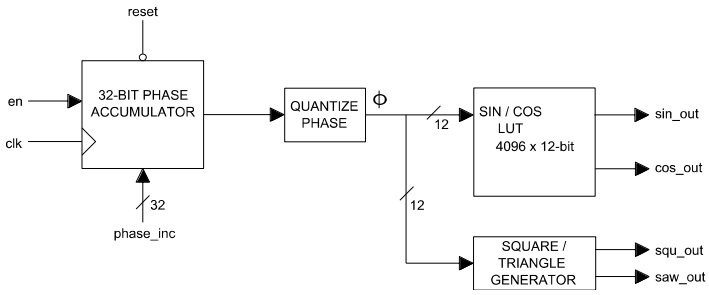

Figure 1: NCO Architecture

General Description

WAVEFORM_GEN is a 12-bit Numerically Controlled Oscillator with simultaneous SIN, COS, SQUARE and SAWTOOTH output waveforms.

On each rising-edge of the sample clock, the phase in the phase accumulator is incremented by the value *phase_inc*. This phase is quantized to 12-bits and passed as an address to a look-up table which converts the phase into a waveform.

The look-up table is implemented as an array of 4096 x 12-bit samples over the range 0 to 2Pi. All output values are 12-bit signed numbers.

Phase increment

The frequency of the output waveforms are controlled by the phase increment on a clock-by-clock basis. A change in the phase increment during normal circuit operation will affect a change in the output waveforms 2 sample clocks later. The phase increment may be calculated using the formula:

$$\Phi_{inc} = (F_{out} \cdot 2^{32}) / F_s + 0.5$$

Where F_{out} is the desired waveform output frequency and F_s is the sampling frequency. Note that the *integer* value of the phase increment must be used. As an example, consider a 100 MHz sample clock with a desired output frequency of 6.197 MHz. The phase increment would be calculated as $(6.197 * 2^{32})/100 + 0.5 = 266159123$.

The minimum and maximum frequencies the NCO can generate are given by the following formulas:

$$F_{min} = F_s / 2^{32} \quad , \quad F_{max} = F_s / 2$$

As an example, a 100 MHz sample clock would allow a minimum NCO frequency of 0.0233 Hz. This is sometimes called the frequency resolution. Conversely, the maximum frequency the NCO can generate is given by the Nyquist/Shannon sampling theorem (Fs/2).

1 Xilinx Virtex 5 FPGA used as a benchmark

Source File Description

All source files are provided as text files coded in VHDL. The following table gives a brief description of each file.

Source file	***Description***
sincos_lut.vhd	SIN/COS look-up table
waveform_gen.vhd	Top-level block
waveform_gen_bench.vhd	Top-level test bench

Functional Testing

An example VHDL testbench is provided for use in a suitable VHDL simulator. The compilation order of the source code is as follows:

1. sincos_lut.vhd
2. waveform_gen.vhd
3. wvaeform_gen_bench.vhd

The VHDL testbench instantiates the WAVEORM_GEN component and the user may modify the phase increment in order to generate the desired output waveform. The example provided generates a 1.7 MHz waveform with a 100 MHz sample clock.

The simulation must be run for at least 30 us during which time the NCO will output the SIN, COS, SQUARE and SAWTOOTH waveforms. Output samples are captured in the text file *waveform_out.txt.* Figures 2 to 5 show plots of the resulting waveforms.

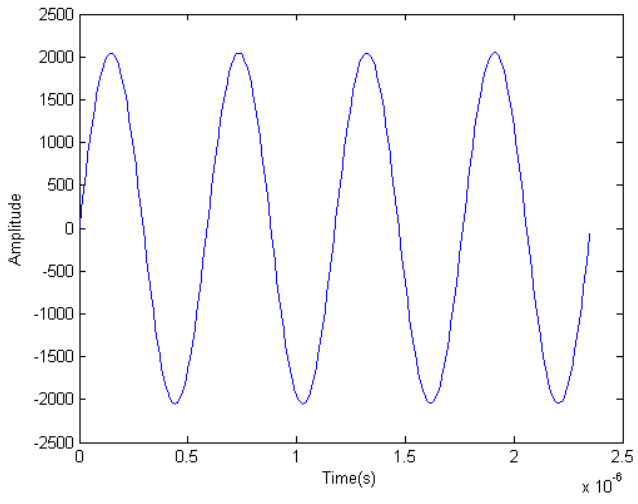

Figure 2: SIN waveform output (1.7 MHz)

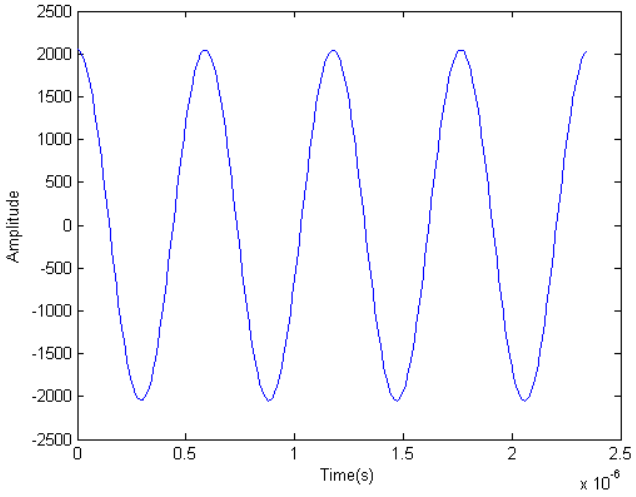

Figure 3: COS waveform output (1.7 MHz)

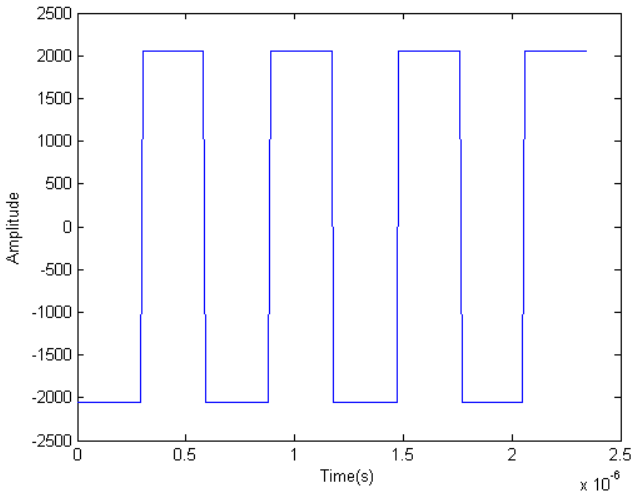

Figure 4: Square waveform output (1.7 MHz)

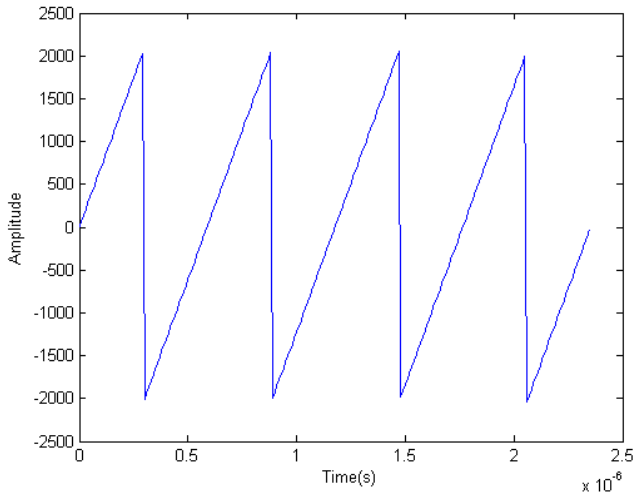

Figure 5: Sawtooth waveform output (2.73 MHz)

Performance

The following plot shows the resulting output spectrum for the 1.7MHz SIN and COS output samples. The SFDR is ~71 dB with the largest magnitude spur of -8.7 dB at around 35 MHz. The spur is highlighted with the red circle.

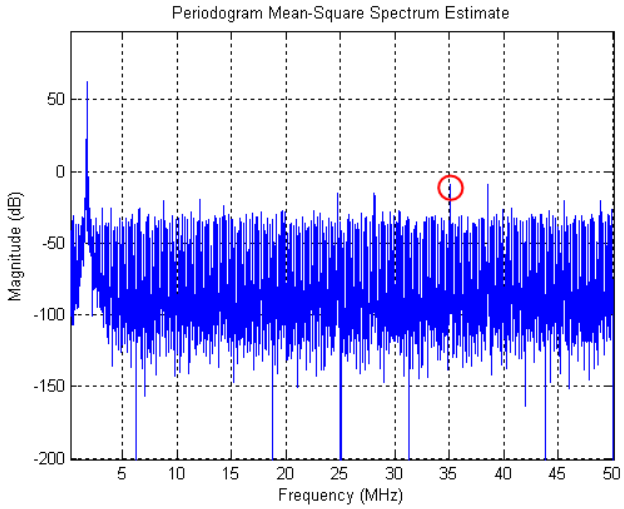

Figure 6: Output spectrum – Single 1.7 MHz tone

Synthesis

The files required for synthesis and the design hierarchy is shown below:

- waveform_gen.vhd
  - waveform_gen.vhd

The VHDL core is designed to be technology independent. However, as a benchmark, synthesis results have been provided for the Xilinx Virtex 5 and the Altera Stratix III series of FPGA devices. The lowest and highest speed grade devices have been chosen in both cases for comparison. Resource usage is specified after Place and Route.

VIRTEX 5

Resource type	***Quantity used***
Slice register	44
Slice LUT	32
Block RAM	3
DSP48	0
Clock frequency (worst case)	437 MHz
Clock frequency (best case)	569 MHz

STRATIX III

Resource type	***Quantity used***
Register	44
ALUT	32
Block Memory bit	98304
DSP block 18	0
Clock frequency (worse case)	368 MHz
Clock frequency (best case)	500 MHz

Revision History

Revision	***Change description***	***Date***
1.0	Initial revision	23/10/2008