WISHBONE Verilog Behaviorals

User Manual

W. Washington
wwashington@opencores.org

Change Log

Date	Version	Change
1-14-01	0.1	Creation Date – W. Washington

Introduction

This document describes the Verilog behaviorals written to support the WISHBONE System-On-Chip SoC interface architecture developed by Silicore.

The behaviorals consist of four types of models:

- A master
- A slave
- An arbiter
- A bus monitor

No attempt was made to insure any of the Verilog is suitable for synthesis.

Verilog Models

Master Model

The master model supports the following transfer sizes: 8, 16 and 32 bits.

The master model supports the following bus cycle types:

- Single Read
- Single Write
- Block Read
- Block Write
- Read-Modify-Write (RMW)

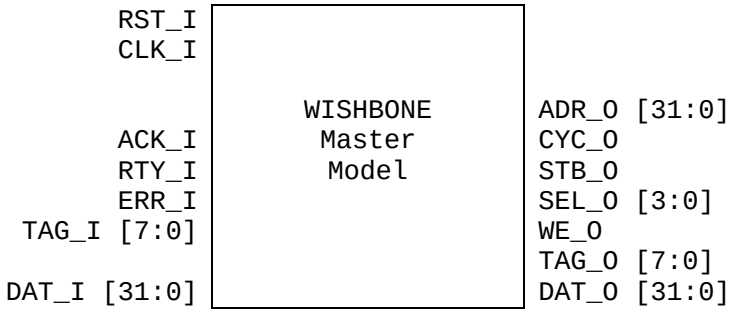

Figure 1 WISHBONE Master Model Signals

Master Transfer Sizes

The address region determines a bus cycle's transfer size. The default configuration is shown in Table X.

Table 1 Default Address to Operand Size

Address Range	Operand Size
00000000 - 1FFFFFFF	8
20000000 – 3FFFFFFF	16
40000000 – 5FFFFFFF	32
60000000 – 7FFFFFFF	64
80000000 – 9FFFFFFF	8
A0000000 - BFFFFFFF	16
C0000000 - DFFFFFFF	32
E0000000 - FFFFFFFF	64

Master Tasks

The master model supports the following tasks.

Table 2 Master Task Routines

Task	Description
task rd; input [31:0] adr; output [31:0] result;	Performs a single read cycle. adr = read address result = data returned by slave device
task wr; input [31:0] adr; input [31:0] dat; input [3:0] sel;	Performs a single write cycle. adr = write address dat = write data sel = byte selects
task blkrd; input [31:0] adr; input end_flag; output [31:0] result;	Performs a block read cycle. adr = read address end_flag = last access in block result = data returned by slave device
task blkwr; input [31:0] adr; input [31:0] dat; input [3:0] sel; input end_flag;	Performs a block write cycle. adr = write address dat = write data sel = byte selects end_flag = last access in block
task rmw; input [31:0] adr; input [31:0] dat; input [3:0] sel; output [31:0] result;	Performs a read-modify-write cycle. adr = write address dat = write data sel = byte selects result = data returned by slave device