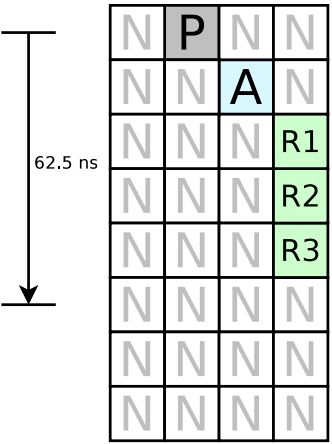
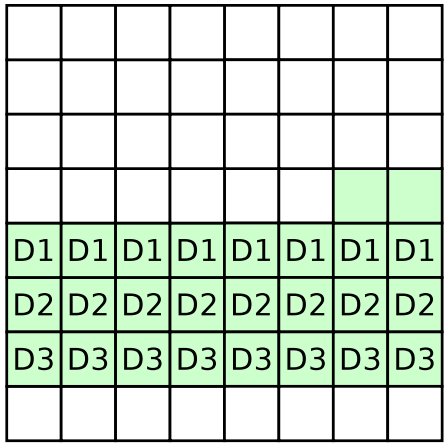
Command Interface



Data Lines



Assuming that the bank is activated on another row, we'll need to wait tRP, the precharge command period, which is 5 clocks in this case. Thus, to get guaranteed access, there may be a 5 clock delay here.

tRCD, activate to internal read or write is another 5 clocks.

tAA, nCL, internal read command to first data is 5 clocks.

As long as we are reading data from an active row of any active bank, we should be able to sustain read transfers of 128-bits per clock. We'll precharge and activate the next bank along the way, so we can sustain this rate indefinitely, ... or at least until the next refresh cycle.

Read/Write Access/Transfer Time

Minimum = 37.5+12.5N ns

Maximum = 62.5+12.5N ns

This read time accounts only for the time on the DDR3 bus, and does not include any time on the wishbone bus or in the controller to get to or or from this DDR3 bus.

P	Precharge the bank
A	Activate a bank
Rx	Is a read command
N	Is a NOOP command

	An empty data cycle
	Empty data cycle, SDRAM is driving DQS strobe lines
Dx	Read data cycle, SDRAM is driving DQS