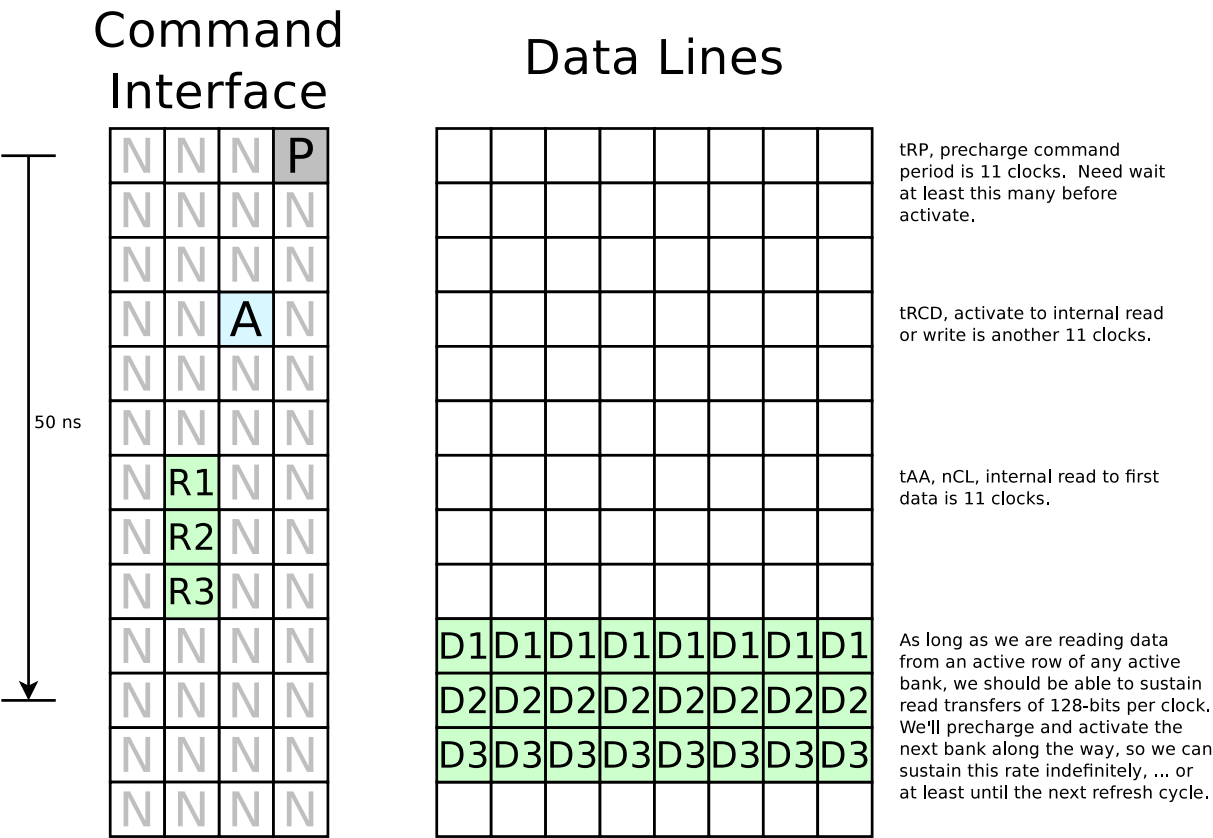
Command Interface
Data Lines
50 ns
N N N P
N N N N
N N N N
N N A N
N N N N
N N N N
N R1 N N
N R2 N N
N R3 N N
N N N N
N N N N
N N N N
N N N N
D1 D1 D1 D1 D1 D1 D1 D1
D2 D2 D2 D2 D2 D2 D2 D2
D3 D3 D3 D3 D3 D3 D3 D3
tRP, precharge command period is 11 clocks. Need wait at least this many before activate.
tRCD, activate to internal read or write is another 11 clocks.
tAA, nCL, internal read to first data is 11 clocks.
As long as we are reading data from an active row of any active bank, we should be able to sustain read transfers of 128-bits per clock. We'll precharge and activate the next bank along the way, so we can sustain this rate indefinitely, ... or at least until the next refresh cycle.