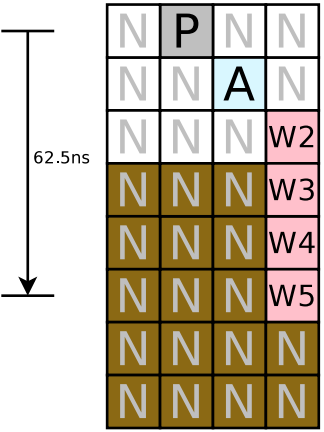
Command Interface



P — Precharge the bank

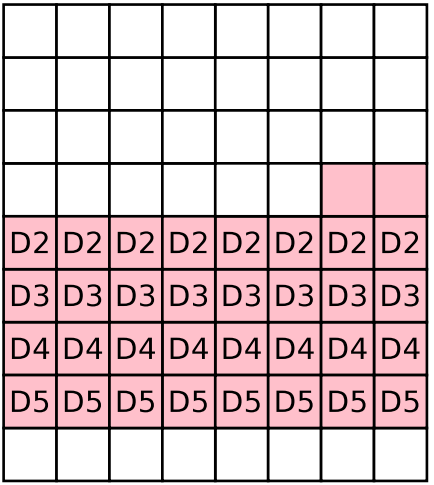
A — Activate a bank

Wx — Is a write command

N — Is a NOOP command

N — A Noop, with ODT is high

Data Lines



An empty data cycle

Empty data cycle, FPGA is driving DQS strobe lines

Dx — Write data cycle, FPGA is driving DQS

In the worst case, the bank of interest will be active to the wrong row. In this case, we will need to precharge that row, and suffer an 5 clock delay, tRP.

tRCD, activate to internal read or write is 5 clocks again. Here we delay another clock in order to keep all of our memory data transfers aligned.

WL, the write latency, is equal to the CAS Write Latency (CWL=5) for our chip, plus the additive latency (AL=0, our choice). Hence, from write command to data on the bus is 5 clocks.

Once the write takes place, 128 bits can transfer to/from the chip every 12.5ns, so we'll make certain that we can achieve and sustain that rate until the next refresh cycle.