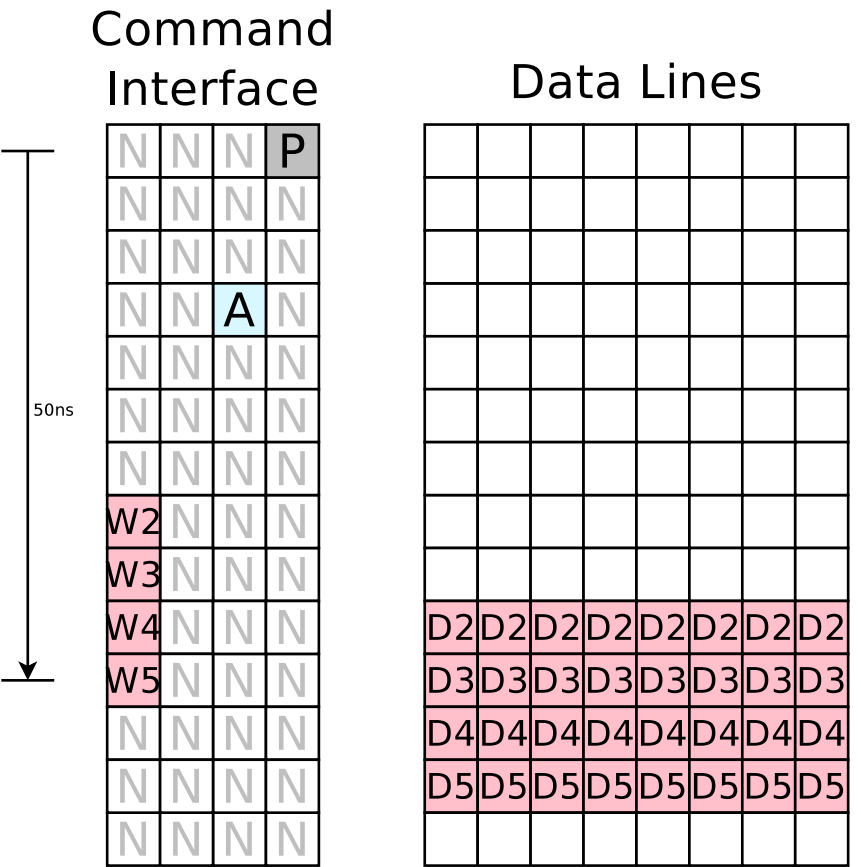

In the worst case, the bank of interest will be active to the wrong row. In this case, we will need to precharge that row, and suffer an 11 clock delay, tRP.

tRCD, activate to internal read or write is 11 clocks again. Here we delay another 3 clocks in order to keep all of our memory data transfers aligned.

WL, the write latency, is equal to the CAS Write Latency (CWL=8) for our chip, plus the additive latency (AL=0, our choice). Hence, from write command to data on the bus is 8 clocks. We choose to

Once the write takes place, 128 bits can transfer to/from the chip every 5ns, so we'll make certain that we can achieve and sustain that rate until the next refresh cycle.