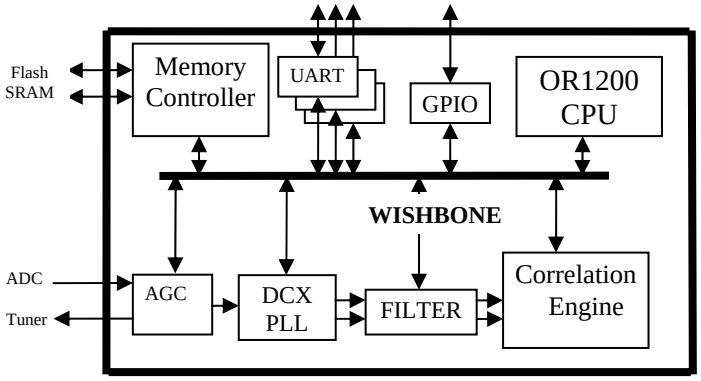
Rosum has developed a technology to determine a mobile user's location by analyzing broadcast television signals. The design provides accuracy capabilities on par with GPS, except that it can operate in challenging indoor locations that GPS signals can not penetrate. Devices equipped with the chip will be able to access enhanced 911 (E911) services, driving directions, and a host of other location-based applications.



The Rosum SOC implements the entire digital portion of the positioning device, except for external Flash and SRAM. It contains numerous signal-processing modules, several UARTs, GPIO, a memory controller, and a 32-bit general-purpose CPU to control them all. The CPU is also used for some non-realtime signal-processing tasks, such as algorithms that filter out RF signal reflections. All the on-chip peripherals and the CPU are tied together with the OpenCores WISHBONE bus.

These are the basic steps of chip operation:

1. **Solicit acquisition aiding information via the serial port**
2. **Tune and digitize TV signal**
3. **Acquire TV signal timing**
4. **Correlate narrow window of incoming signal with reference waveform.**
5. **Model multipath using software to identify best correlation peak.**
6. **Transmit peak-search results via UART to server for position computation.**

When evaluating candidates for the on-chip CPU, Rosum engineers stipulated that it be synthesizable because the FPGA-based design is also to be targeted at an ASIC design flow. Additionally, licensing costs had to be minimized because our high-volume customers were very cost-sensitive. The OpenRISC OR1200 RISC processor was an ideal match for both these requirements. Also attractive was the degree of configurability offered by the OR1200, allowing easy elimination of non-essential functionality to reduce area and increase speed, e.g. caches, MMU. Finally, there was an accompanying plug-and-play library of open-source WISHBONE-compatible peripheral cores that could be used to shorten the SOC development cycle.

The chip application software runs under eCos, a compact, open-source RTOS that Rosum ported to the OpenRISC architecture. eCos provides support to control the UARTs and the Flash ROM as well as the usual array of operating system services. eCos was completely developed before hardware was available for testing by using the OpenRISC development tools, such as the instruction-level simulator and debugger.