WISHBONE - AHB BRIDGE

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Revision No.

1.0

Disclaimer

Introduction

This is a BRIDGE that is used to interconnect WISHBONE Master and AHB Slave

Limitations of Design

- This design will not work for Sequential transfers (ie for wrap and incremental type of transfers).
- No error, retry and split cases have been considered in the design.
- Word size is 32 bits. It can be modified as per requirement.
- All transfers has been considered as non-sequential type.

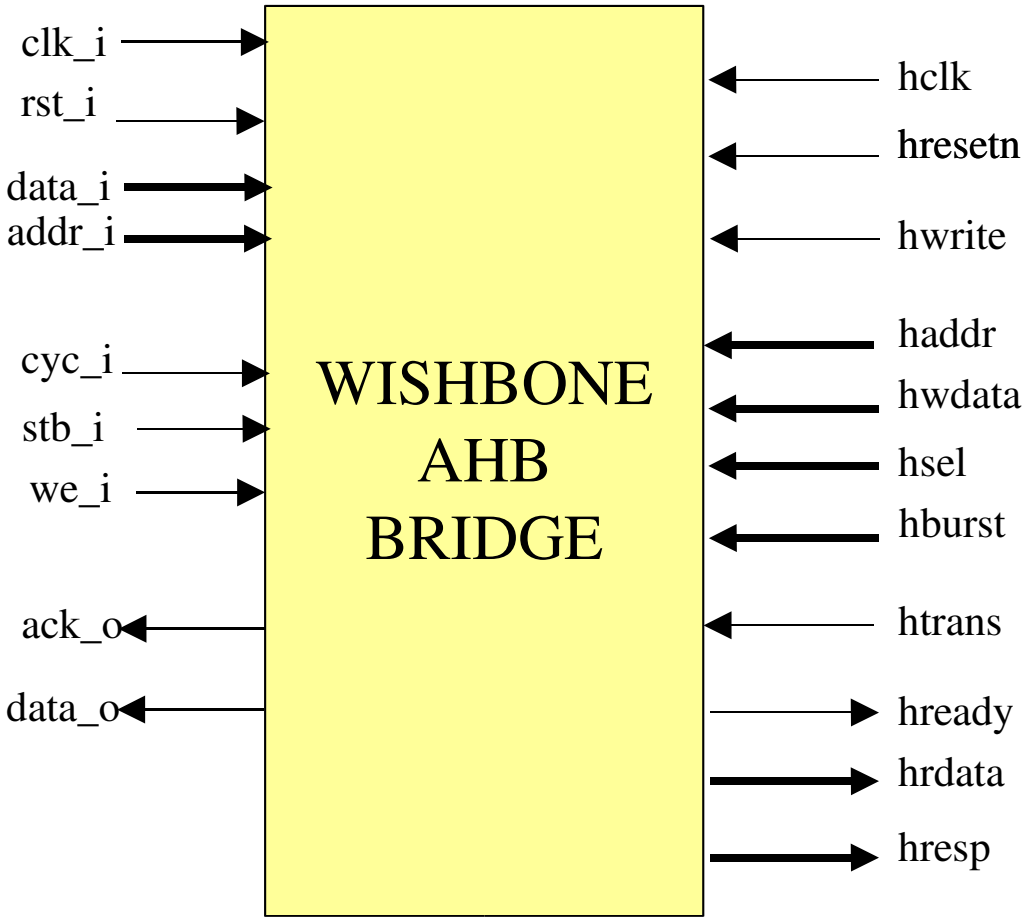
Synthesizability

This code is completely synthesizable. The only care that has to be taken is that the AHB clock(hclk) and reset(hresetn) signals have been left unconnnected inside the design. The whole design is working on Wishbone clock and reset signals that should be provided by Wishbone master.

Port Definations

Port Name	*Direction*	*Size*	*Source*	*Description*
haddr	out	32	AHB Master	Address Bus
htrans	out	2	AHB Master	Transfer Type
hwrite	out	1	AHB Master	Read/Write enable
hsize	out	3	AHB Master	not used
hburst	out	3	AHB Master	Burst Type
hwdata	out	32	AHB Master	Write data bus
hrdata	out	32	AHB Master	Read data bus
hready	in	1	AHB Slave	To indicate bridge is ready
hresp	in	2	AHB Slave	Response
data_o	out	32	WISHBONE Slave	Read data bus
data_i	in	32	WISHBONE Master	Write data bus
addr_i	in	32	WISHBONE Master	Address Bus
clk_i	in	1	WISHBONE Master	Clock
rst_i	in	1	WISHBONE Master	Active Hign Sync. Reset
cyc_i	in	1	WISHBONE Master	To indicate valid bus cycle
stb_i	in	1	WISHBONE Master	To indicate valid data transfer cycle
sel_i	in	4	WISHBONE Decoder	Selection
we_i	in	1	WISHBONE Master	Read/Write enable
ack_o	out	1	WISHBONE Slave	To indicate current transfer status
hclk	in	1	AHB Master	Unconnected
hresetn	in	1	AHB Master	Unconnected

Black Box


clk_i
rst_i
data_i
addr_i
cyc_i
stb_i
we_i
ack_o
data_o
WISHBONE
AHB
BRIDGE
hclk
hresetn
hwrite
haddr
hwdata
hsel
hburst
htrans
hready
hrdata
hresp

Reset operation

The WISHBONE reset signal is active HIGH and is used to reset the system and the bus. This reset has been asserted and deasserted synchronously after the rising edge of clk_i.

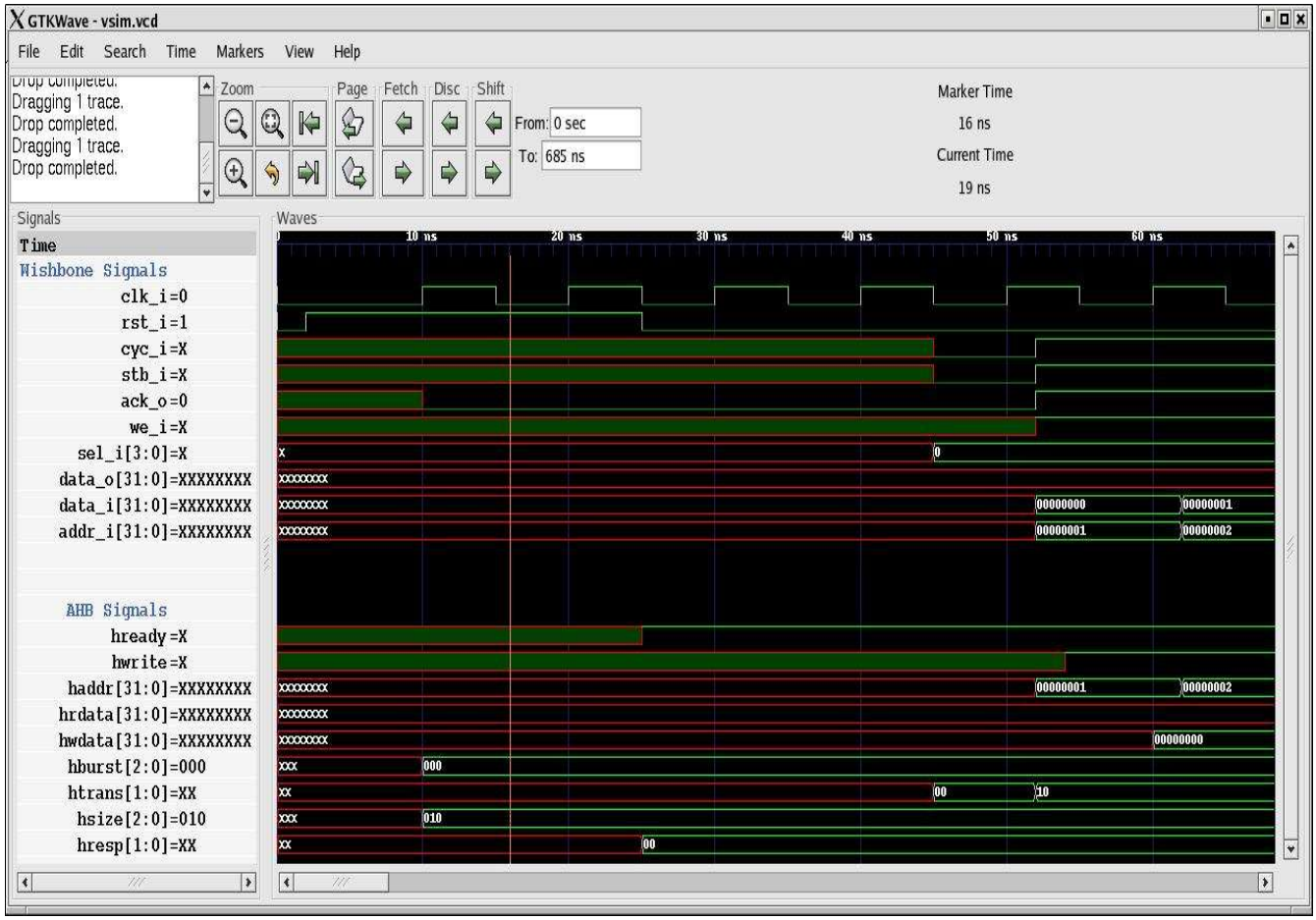


Fig. 1 : Reset operation

Write Cycle

When we_i is HIGH, this signal indicates a write transfer and the master will broadcast data on the write data bus(data_i) when cyc_i and stb_i signal is HIGH.

1) At 1st clock edge the address(A1) and data (D1)is sampled by the WISHBONE slave on addr_i and data_i bus respectively.

2) At 1st clock edge ack_o is also asserted.

3) This address sampled is transfered asynchronously to the AHB master on haddr.

4) At 2nd clock edge Data(D1) for this address is sampled synchronously by AHB master on to hwdata bus irrespective of hready status.

5) This data is written into the AHB slave synchronously on hwdata bus.

6) Htrans is asserted to “Non – Seq (10)” transfer type at clock edge when cyc_i and stb_i are HIGH.

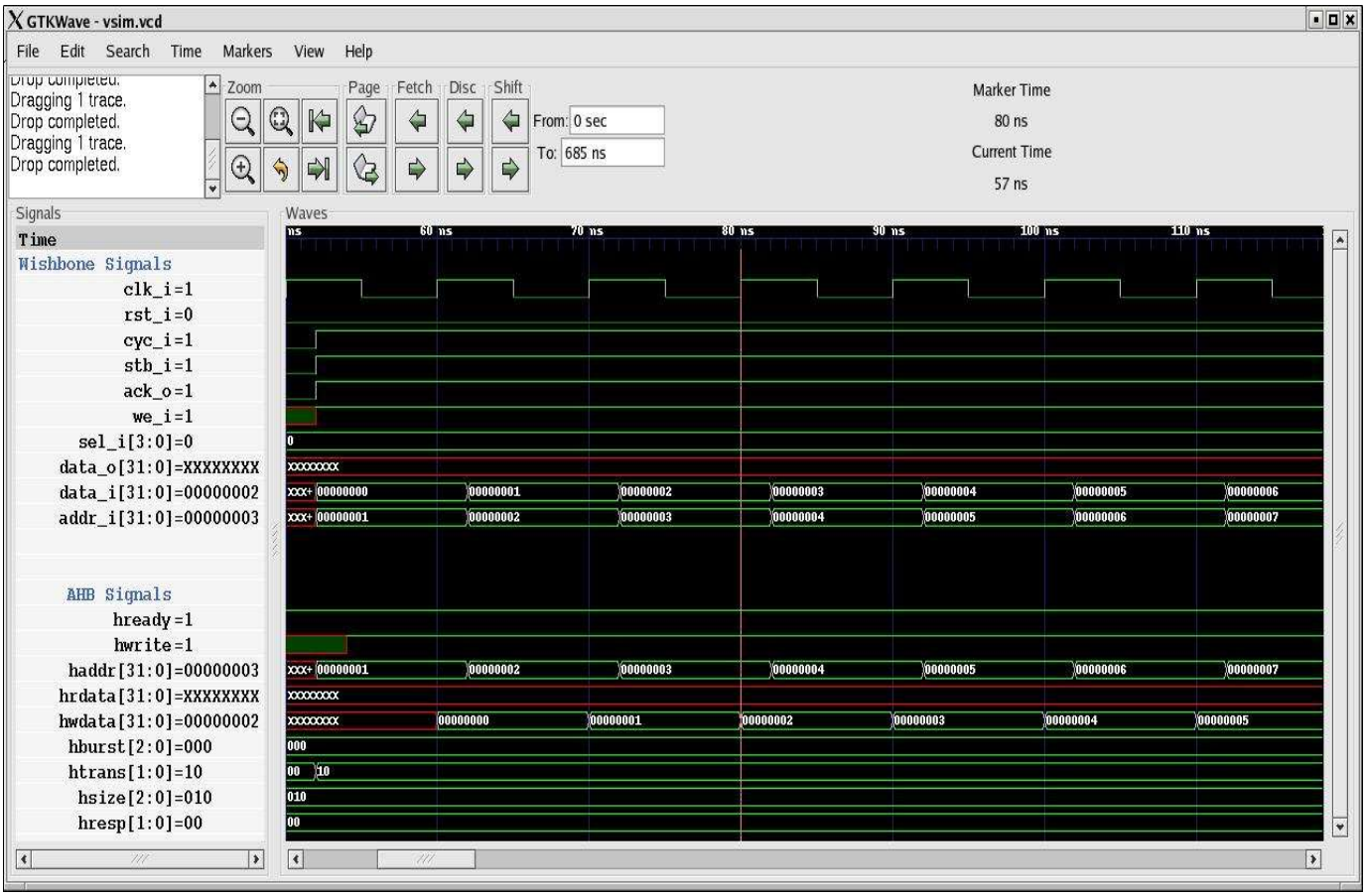


Fig 2 : Write Cycle

Read Cycle

When we_i is LOW, this signal indicates a read transfer and the master will receive data on the read data bus (data_o) provided the ack_o signal is HIGH.

1) At 1st clock edge the address(A1) is sampled by the WISHBONE slave on addr_i.

2) This address will be transfered asynchronously to AHB master on haddr provided hready is HIGH.

3) At 2nd clock edge Data(D1) for this address is sampled synchronously by AHB on hrdata.

4) Data (D1) is latched on hrdata bus asynchronously when hready is asserted.

5) Data (D1) is latched on data_o asynchronously at the same time.

6) At 2nd clock edge ack_o is asserted.

7) Htrans is asserted to "Non – Seq (10)" transfer type at clock edge when cyc_i and stb_i are HIGH.

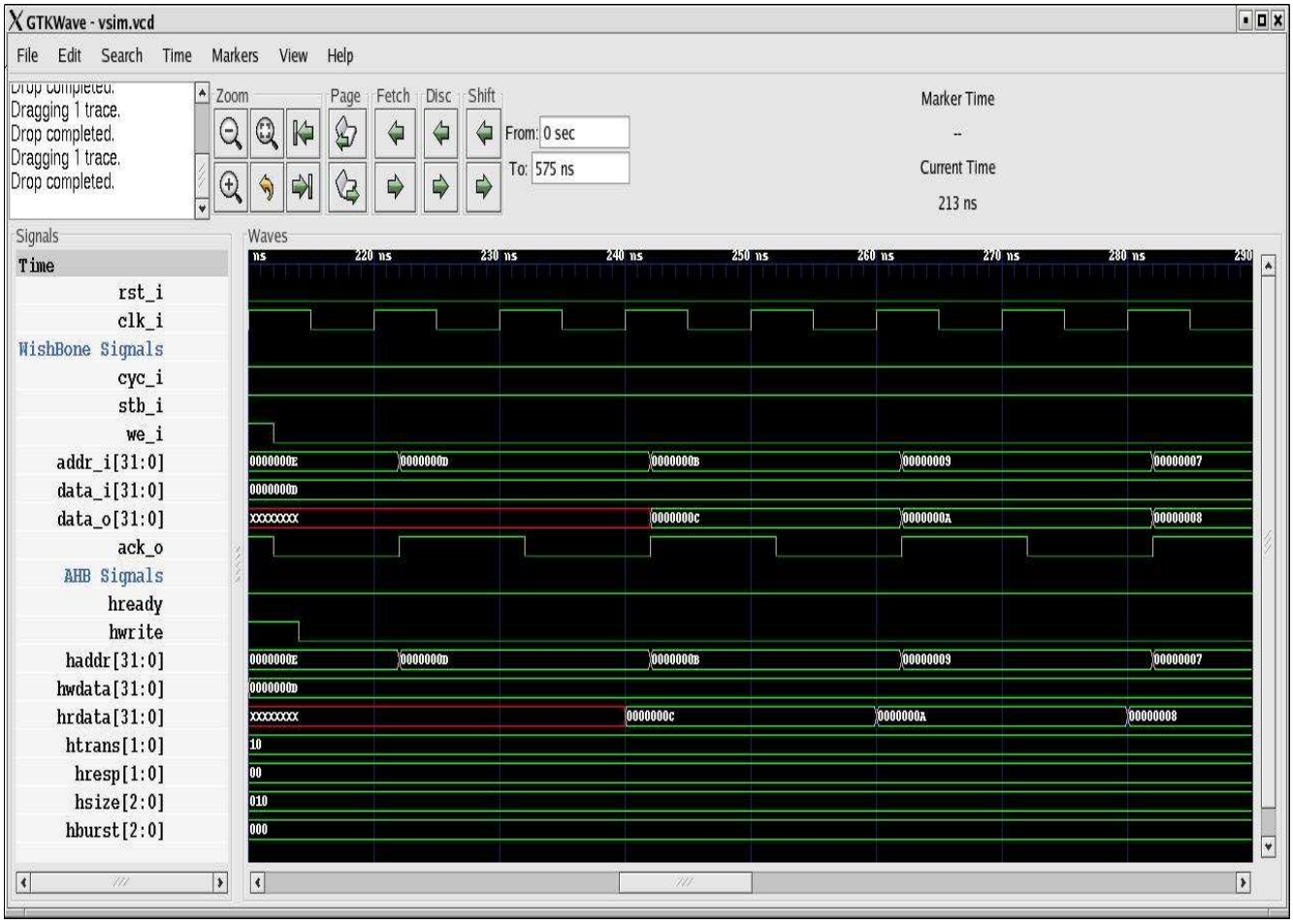


Fig. 3 : Read Cycle

Write with Wait states

Inserted by AHB Slave

1) At 1st clock edge the address(A1) and data (D1)is sampled by the WISHBONE slave on addr_i and data_i bus respectively.
2) At 1st clock edge ack_o is also asserted.
3) This address sampled is transfered asynchronously to the AHB master on haddr.

4) At 2nd clock edge Data(D1) for this address is sampled synchronously by AHB master on to hwdata bus irrespective of hready status.
5) This data is written into the AHB slave synchronously on hwdata bus.
6) At 2nd clock edge if hready is LOW then asynchronously even the WISHBONE slave is also made inactive by deasserting ack_o, so no new address is sampled.
7) At 3rd clock edge if hready is HIGH then address (A2) and data (D2) is sampled by the WISHBONE on addr_i and data_i bus.
8) At 3rd clock edge ack_o is made HIGH asynchronously.

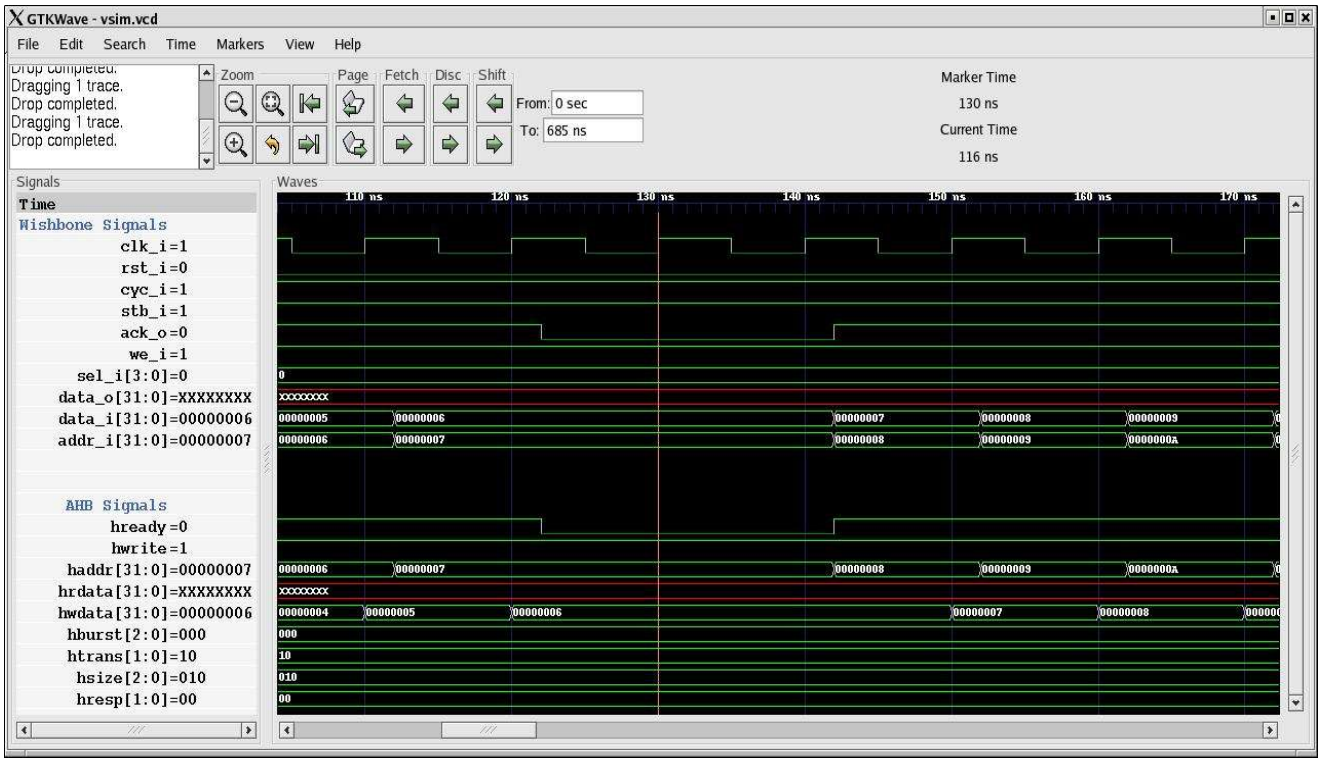


Fig. 4 : Write cycle with wait state inserted by AHB Slave

Inserted by Wishbone Master

1) 1) At 1st clock edge the address(A1) and data (D1) is sampled by the WISHBONE slave on addr_i and data_i bus respectively.
2) At 1st clock edge ack_o is also asserted.
3) This address sampled is transfered asynchronously to the AHB master on haddr.
4) At 2nd clock edge if stb_i is LOW then asynchronously even the ack_o as well as hready is made Low, so no new address is sampled.
5) At 2nd clock edge Data(D1) for this address is sampled synchronously by AHB master on to hwdata bus irrespective of hready status.
6) This data is written into the AHB slave synchronously on hwdata bus.
7) At 3rd clock edge if stb_i is HIGH then address (A2) and data (D2) is sampled by the

WISHBONE on addr_i and data_i bus.

9) At 3rd clock edge ack_o is made HIGH asynchronously along with hready.

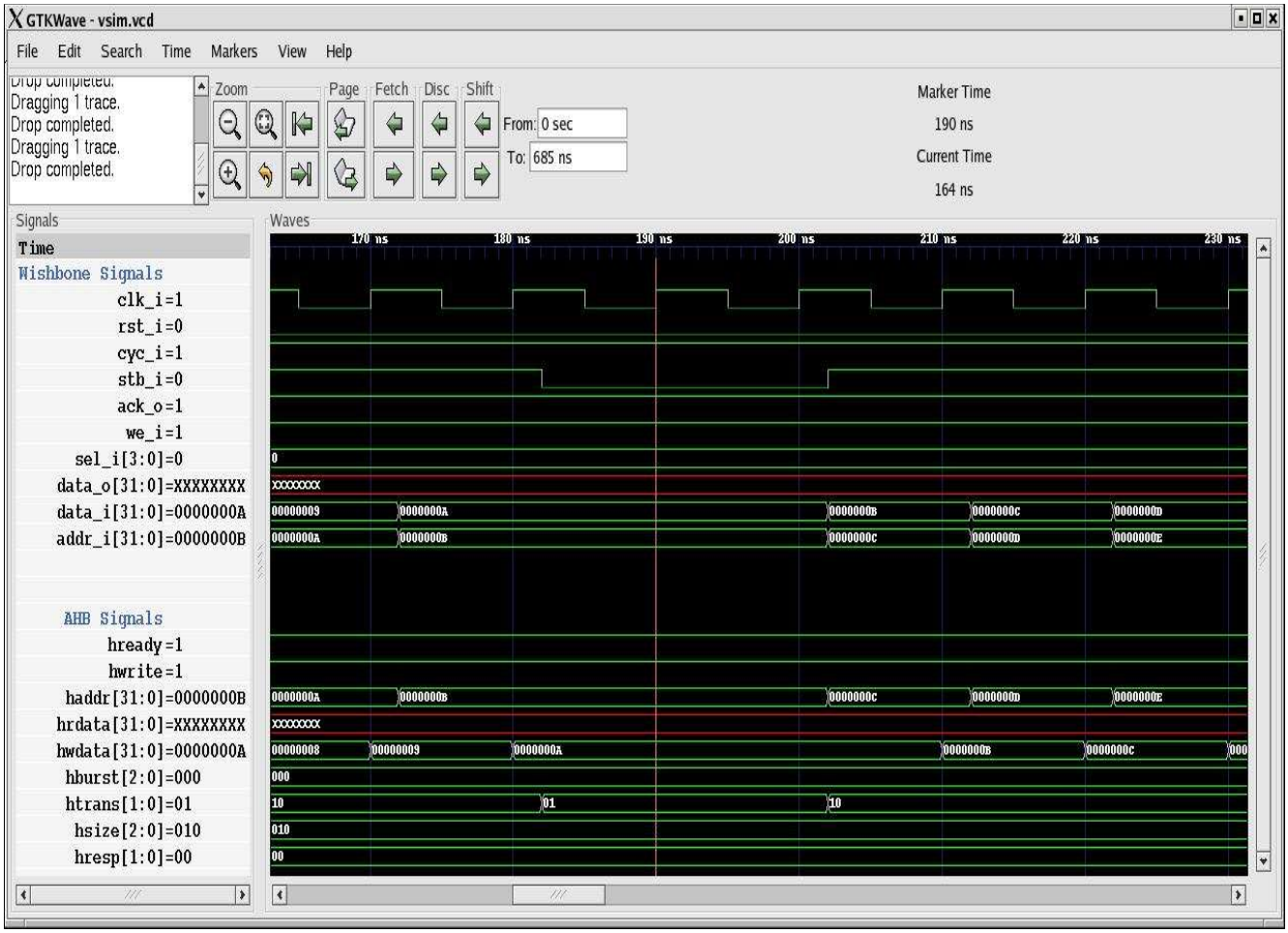


Fig. 5 : Write cycle with wait state inserted by WB Master

Read with wait states

Inserted by AHB Slave

1) At 1st clock edge the address(A1) is sampled by the WISHBONE slave on addr_i.

2) This address will be transfered asynchronously to AHB master on haddr.

3) At 2nd clock edge Data(D1) for this address is sampled synchronously by AHB on hrdata provided hready is HIGH.

4) At 2nd clock edge if hready is LOW then asynchronously even the WISHBONE slave is also made inactive by deasserting ack_o, so no new address is sampled.

5) Data (D1) is latched on hrdata bus asynchronously when hready is asserted.

6) Data (D1) is latched on data_o asynchronously at the same time.

7) When data (D1) appears on data_o, ack_o is asserted same time.

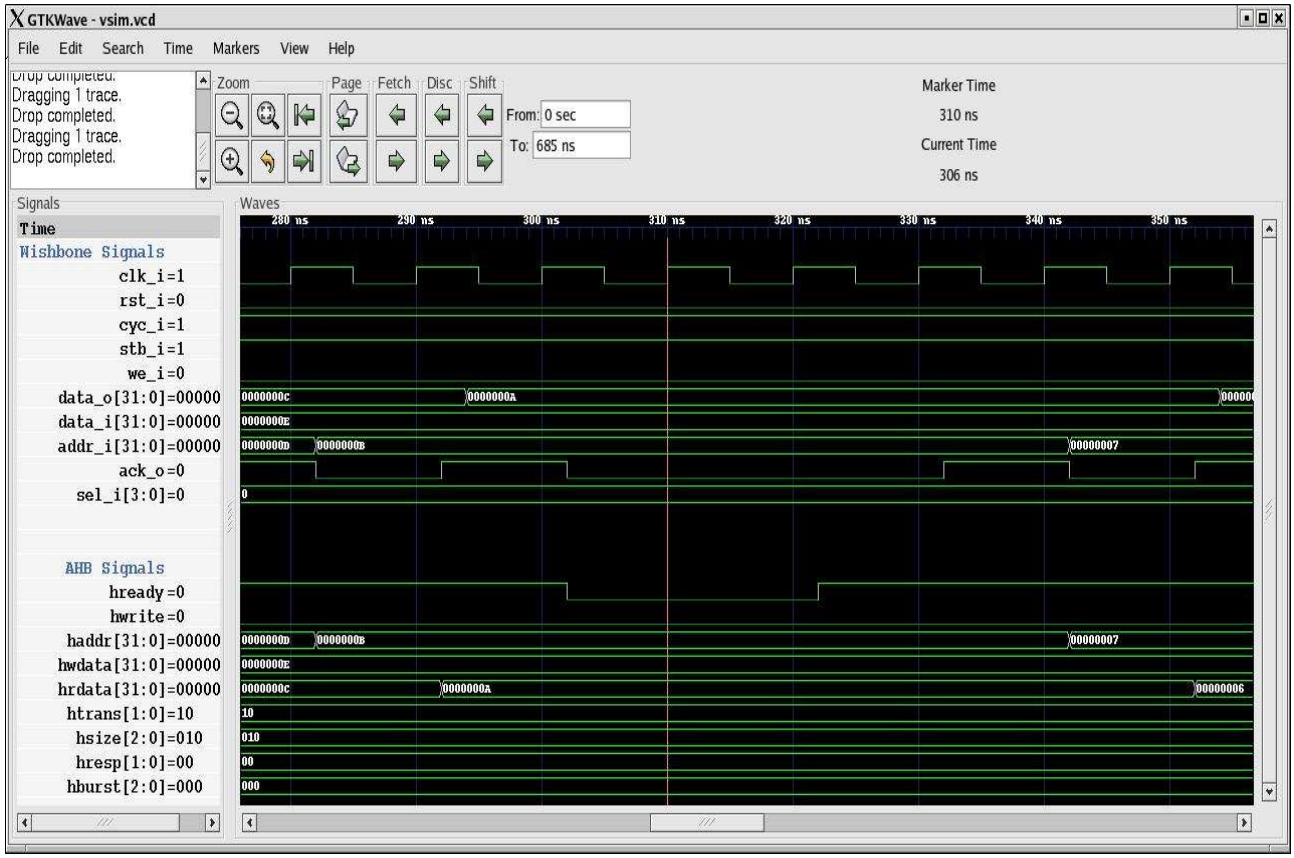


Fig. 6 : Read Cycle with wait state inserted by AHB slave

Inserted by Wishbone Master

1) At 1st clock edge the address(A1) is sampled by the WISHBONE slave on addr_i.
2) This address will be transfered asynchronously to AHB master on haddr.
3) At 2nd clock edge if stb_i is Low, asynchrounsly even the ack_o and hready are made Low.
4) At 3rd Clock edge if stb_i is HIGH then Data(D1) for this address is sampled synchronously by AHB on hrdata provided hready is HIGH.
5) Data (D1) is latched on hrdata bus asynchronously when hready is asserted.
6) Data (D1) is latched on data_o asynchronously at the same time.
7) When data (D1) appears on data_o, ack_o is asserted same time.

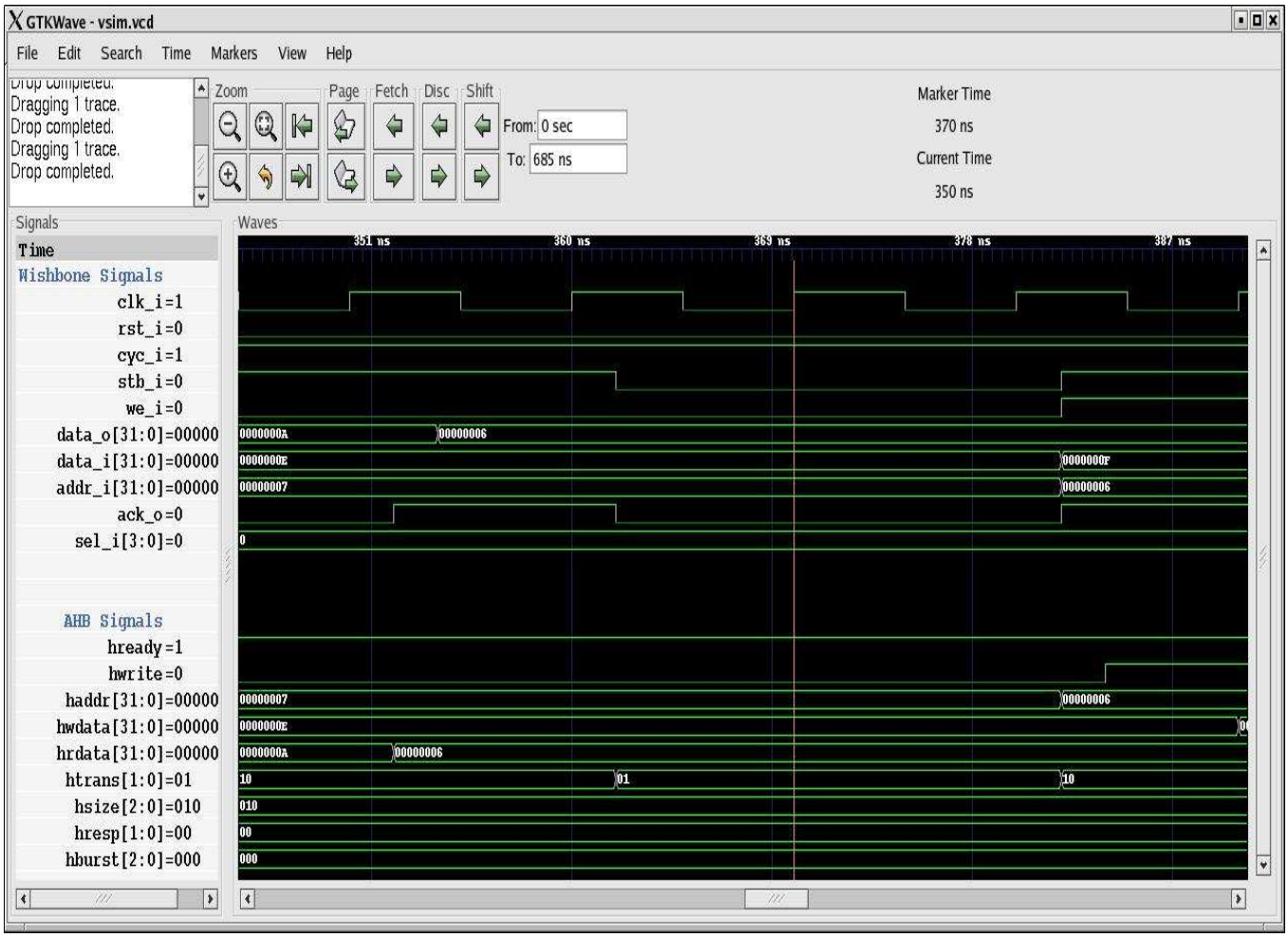


Fig. 7 : Read Cycle with wait state inserted by WB Master

Read after Write :

1) At 1st clock edge the address(A1) and data(D1) are sampled by the WISHBONE Slave on addr_i and data_i along with we_i (Active High) signal and other control signals.
2) This address is transfered asynchronously to the AHB Master on haddr.
3) At 2nd clock edge address(A2) for next transfer is sampled by WISHBONE Slave on addr_i along with we_i signal (Active Low) and is latched asynchronously on haddr bus. Also at 2nd clock edge data(D1) for address(A1) is sampled synchronously by AHB Master on hwdata.
4) hwrite signal is pulled LOW asynchronously at 2nd clock edge.
5) At 3rd clock edge data for address (A2) is latched synchronously on to hrdata bus.
6) Data(D2) for this address is sampled asynchronously by WISHBONE Slave on data_o.

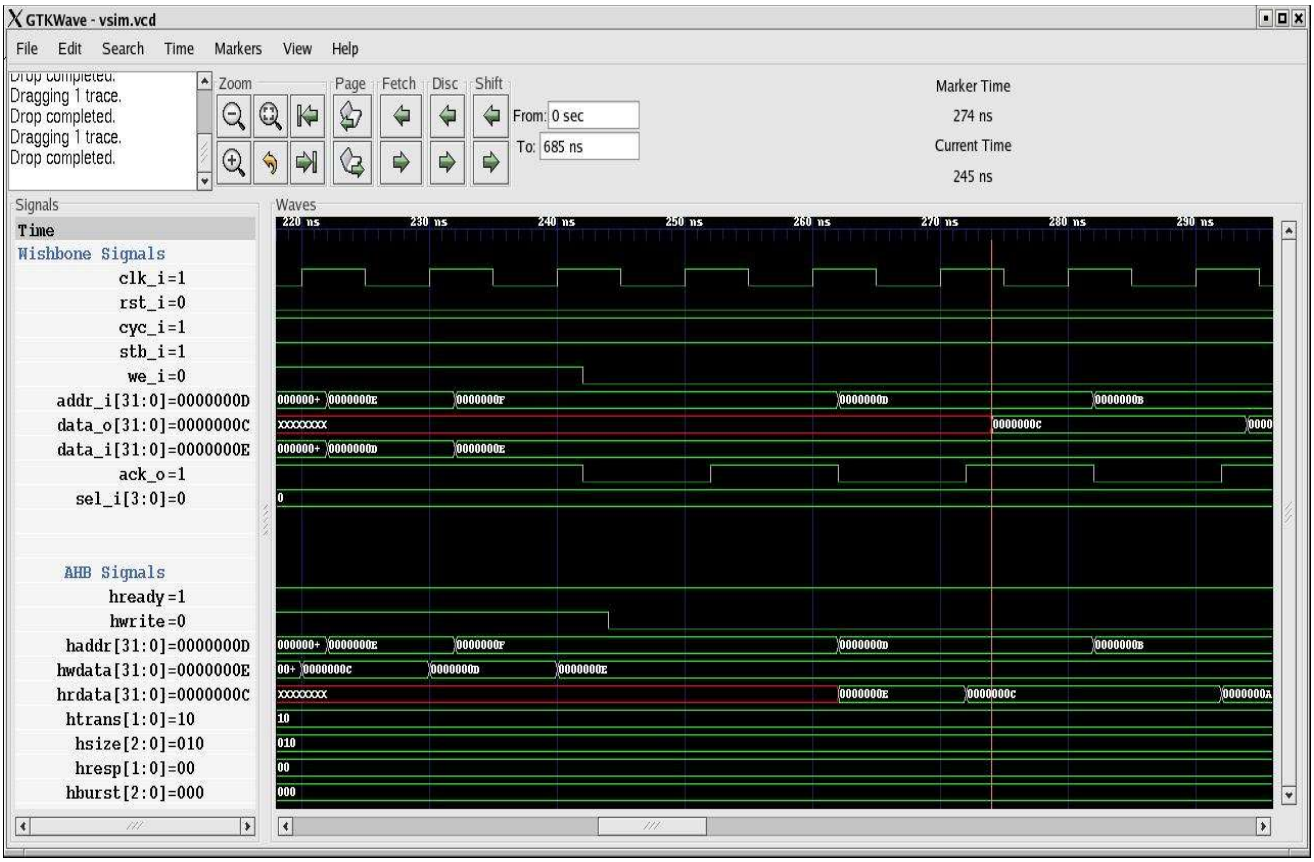


Fig. 8 : Read after Write Cycle

Write after Read :

1) At 1st clock edge the address(A1) is sampled by the WISHBONE Slave on addr_i along with we_i (Active Low) signal and other control signals.
2) This address will be transfered asynchronously to AHB Master on haddr.
3) At 2nd Clock edge data(D1) for this address is sampled synchronously by AHB Master on hrdata.
4) D1 is transfered asynchronously to WISHBONE Slave on data_o and ack_o is asserted as well.
5) At 3rd Clock edge we_i signal is pulled to HIGH logic(for write operation).
6) we_i signal is transfered asynchronously on hwrite.
7) At 3rd clock edge address(A2) and data(D2) is sampled by WISHBONE Slave on addr_i and data_i busses.
8) A2 is transfered asynchronously from addr_i to haddr.
9) At 4th Clock edge data(D2) for address(A2) is sampled synchronously by AHB Master on hwdata.

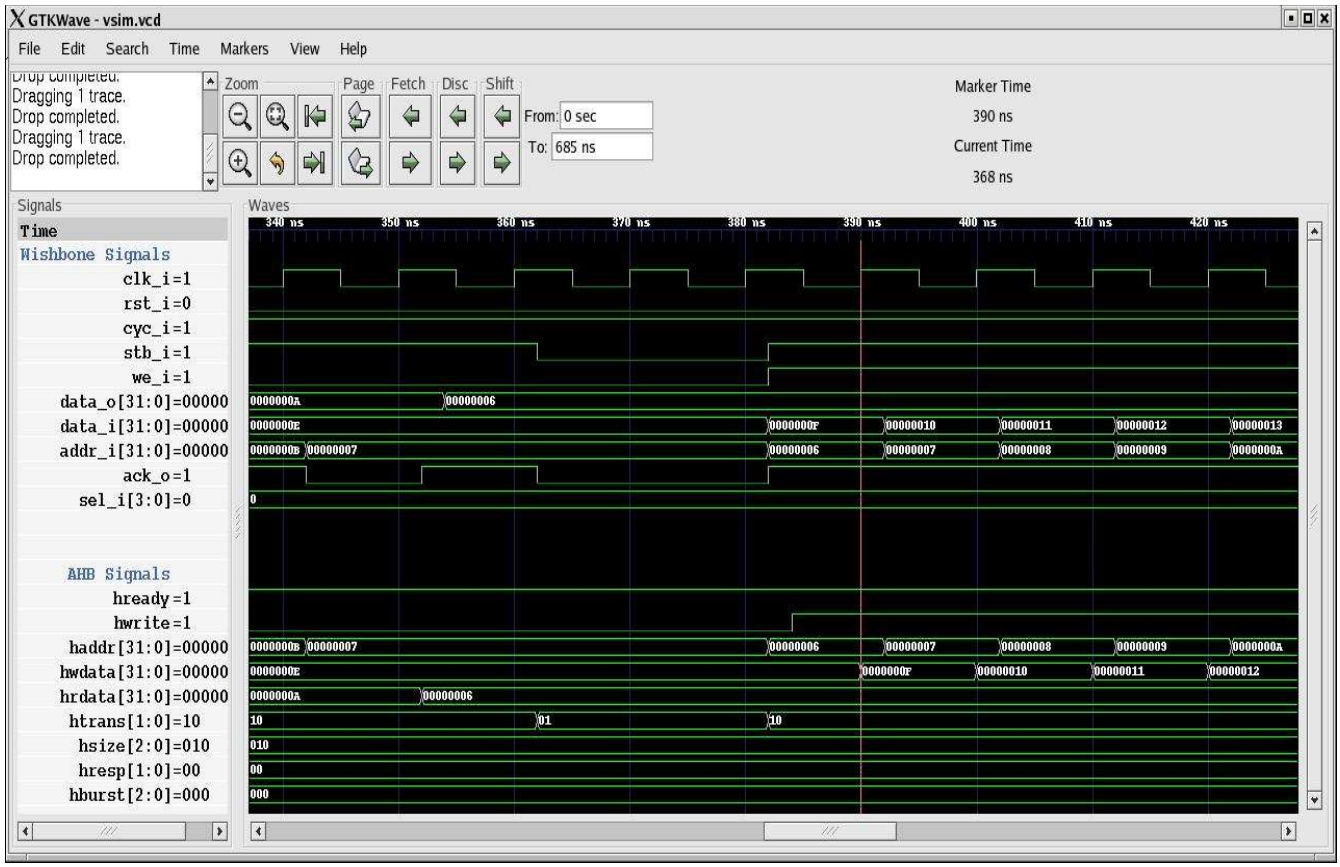


Fig. 9 : Write after Read Cycle

References

AMBA

- http://www.arm.com
- AMBA Specification (Rev. 2.0)

Wishbone

- http://www.opencores.org/wishbone
- WISHBONE specification Rev. B.3