Wishbone Outport From B3 Specification

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Not so much a specification, but cuttings from the

WISHBONE System-on-Chip (SoC) Interconnection Architecture for Portable IP Cores

Revision: B.3, Released: September 7, 2002

All references et all acknowledged.

As at Feb 2008, this directory contains 5 VHDL files,

- WBMEM16X16.vhd
- WBMEM32X16.vhd
- WBOPRT08.vhd
- WBOPRT16.vhd
- WBOPRT32.vhd

WBMEM are two memories for the wishbone bus. 16X16 is 16 registers of 16 bits data, whilst 32X16 is 16 registers of 32 bit data. Single cycle read as per the Wishbone B3 specification examples, Appendix A7.

WBOPRT are three out port registers. 08, is 8 bits data, 16 is 16 bit data, and 32 is 32 bit data. As per Wishbone B3 specification Appendix A6.

Below are the pertinent extracts from the B3 specification.

A.6.1 Simple 8-bit SLAVE Output Port

Figure A-9 shows a simple 8-bit WISHBONE SLAVE output port. The entire interface is implemented with a standard 8-bit 'D-type' flip-flop register (with synchronous reset) and a single AND gate. During write cycles, data is presented at the data input bus [DAT_I(7..0)], and is latched at the rising edge of [CLK_I] when [STB_I] and [WE_I] are both asserted.

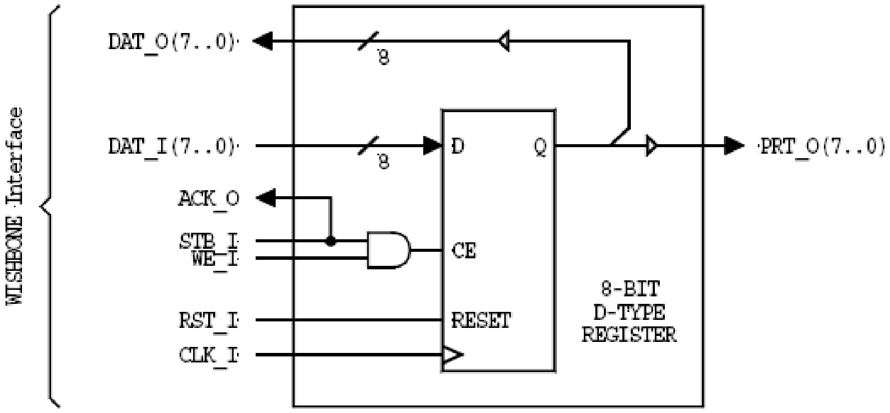


Figure A-9. Simple 8-bit WISHBONE SLAVE output port.

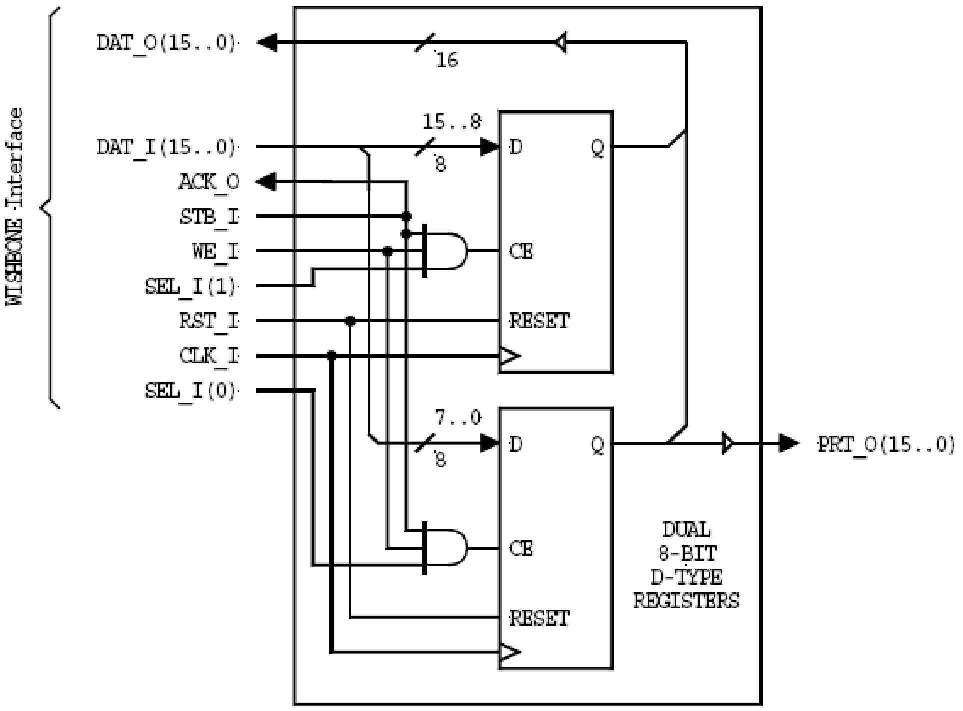
The state of the output port can be monitored by a MASTER by routing the output data lines back to [DAT_O(7..0)]. During read cycles the AND gate prevents erroneous data from being latched into the register.

Table A-1. WISHBONE DATASHEET for the 8-bit output port example.

Description	Specification	
General description:	8-bit SLAVE output port.	
Supported cycles:	SLAVE, READ/WRITE SLAVE, BLOCK READ/WRITE SLAVE, RMW	
Data port, size:	8-bit	
Data port, granularity:	8-bit	
Data port, maximum operand size:	8-bit	
Data transfer ordering:	Big endian and/or little endian	
Data transfer sequencing:	Undefined	
Supported signal list and cross reference to equivalent WISHBONE signals:	Signal Name	WISHBONE Equiv.
	ACK_O	ACK_O
	CLK_I	CLK_I
	DAT_I(7..0)	DAT_I()
	DAT_O(7..0)	DAT_O()
	RST_I	RST_I
	STB_I	STB_I
	WE_I	WE_I

A.6.3 Simple 16-bit SLAVE Output Port With 8-bit Granularity

Figure A-12 shows a simple 16-bit WISHBONE SLAVE output port. This port has 8-bit granularity, which means that data can be transferred 8 or 16-bits at a time.



<table>
<tr><th colspan="3">Table A-3. WISHBONE DATASHEET
for the 16-bit output port with 8-bit granularity.</th></tr>
<tr><th>Description</th><th colspan="2">Specification</th></tr>
<tr><td>General description:</td><td colspan="2">16-bit SLAVE output port with 8-bit granularity.</td></tr>
<tr><td>Supported cycles:</td><td colspan="2">SLAVE, READ/WRITE
SLAVE, BLOCK READ/WRITE
SLAVE, RMW</td></tr>
<tr><td>Data port, size:
Data port, granularity:
Data port, maximum operand size:
Data transfer ordering:
Data transfer sequencing:</td><td colspan="2">16-bit
8-bit
16-bit
Big endian and/or little endian
Undefined</td></tr>
<tr><td rowspan="8">Supported signal list and cross reference to equivalent WISHBONE signals:</td><td>Signal Name</td><td>WISHBONE Equiv.</td></tr>
<tr><td>ACK_O</td><td>ACK_O</td></tr>
<tr><td>CLK_I</td><td>CLK_I</td></tr>
<tr><td>DAT_I(15..0)</td><td>DAT_I()</td></tr>
<tr><td>DAT_O(15..0)</td><td>DAT_O()</td></tr>
<tr><td>RST_I</td><td>RST_I</td></tr>
<tr><td>STB_I</td><td>STB_I</td></tr>
<tr><td>WE_I</td><td>WE_I</td></tr>
</table>

A.7.2 Simple 16 x 8-bit SLAVE Memory Interface

Figure A-16 shows a simple 8-bit WISHBONE memory. The 16 x 8-bit memory is formed from two 16 x 4-bit FASM compatible synchronous memories. Besides the memory elements, the entire interface is implemented with a single AND gate. During write cycles, data is presented at the data input bus [DAT_I(7..0)], and is latched at the rising edge of [CLK_I] when [STB_I] and [WE_I] are both asserted. During read cycles, the memory output data (DO) is made available at the data output port [DAT_O(7..0)].

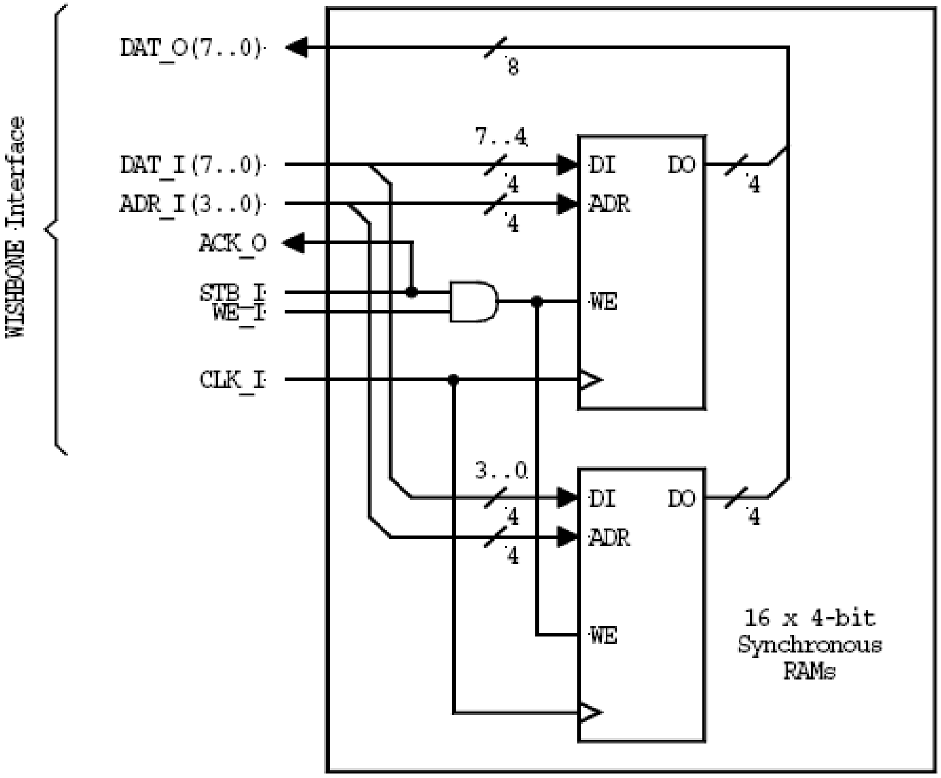


Figure A-16. Simple 16 x 8-bit SLAVE memory.

Table A-4. WISHBONE DATASHEET for the 16 x 8-bit SLAVE memory.

<table>
<tr><th>Description</th><th colspan="2">Specification</th></tr>
<tr><td>General description:</td><td colspan="2">16 x 8-bit memory IP core.</td></tr>
<tr><td>Supported cycles:</td><td colspan="2">SLAVE, READ/WRITE
SLAVE, BLOCK READ/WRITE
SLAVE, RMW</td></tr>
<tr><td>Data port, size:
Data port, granularity:
Data port, maximum operand size:
Data transfer ordering:
Data transfer sequencing:</td><td colspan="2">8-bit
8-bit
8-bit
Big endian and/or little endian
Undefined</td></tr>
<tr><td>Clock frequency constraints:</td><td colspan="2">NONE (determined by memory primitive)</td></tr>
<tr><td rowspan="8">Supported signal list and cross reference to equivalent WISHBONE signals:</td><td>Signal Name</td><td>WISHBONE Equiv.</td></tr>
<tr><td>ACK_O</td><td>ACK_O</td></tr>
<tr><td>ADR_I(3..0)</td><td>ADR_I()</td></tr>
<tr><td>CLK_I</td><td>CLK_I</td></tr>
<tr><td>DAT_I(7..0)</td><td>DAT_I()</td></tr>
<tr><td>DAT_O(7..0)</td><td>DAT_O()</td></tr>
<tr><td>STB_I</td><td>STB_I</td></tr>
<tr><td>WE_I</td><td>WE_I</td></tr>
<tr><td>Special requirements:</td><td colspan="2">Circuit assumes the use of synchronous RAM primitives with asynchronous read capability.</td></tr>
</table>