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Xenie

(Xilinx Kintex-7 based FPGA module)

Xenie User's Manual

Document Information :

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Purpose :

The purpose of this User's Manual is to introduce the Xenie FPGA module, summarize its features and provide additional information useful for its integration into the user's design. The recommended practice is to study the User's Manual simultaneously with schematics of the module and other additional documents (base board reference design, mechanical drawings etc.).

Document Revision History:

Version	Date (mm/dd/yy)	Author	Comments
0.1	30/1/2017	SK	Document created.

Hardware Revision History:

Version	Date (mm/dd/yy)	Author	Comments
1.0	30/1/2017	SK	First prototype.

Note:
Hardware revision number is written after the module name (eg. Xenie 1.0) on the FPGA side of the PCB.

Contents

1 Project overview

The Xenie FPGA module is based on the Xilinx Kintex-7 FPGA, uniquely supporting 10 Gbit/s, 5 Gbit/s, 2.5 Gbit/s Ethernet on UTP/STP copper lines as well as lower speed 1 Gbit/s, 100 Mbit/s and 10 Mbit/s data rates.

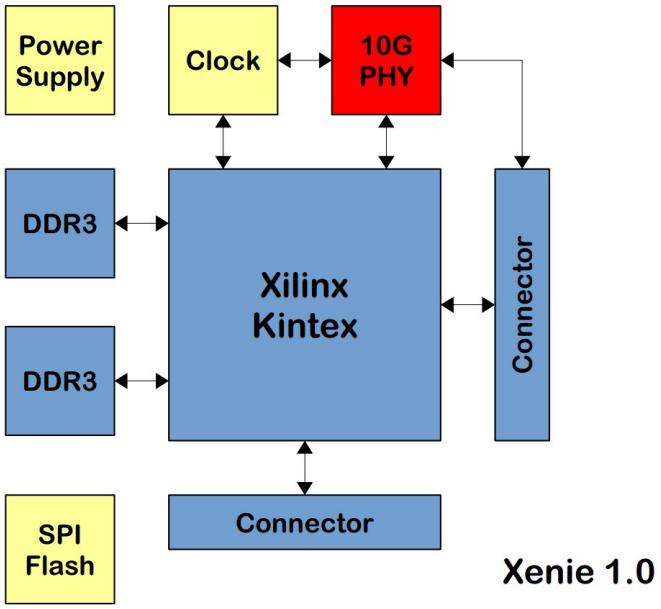
Module is also equipped with 1 GByte of DDR3L SDRAM and 32 MByte of Flash memory as a storage for configuration bitstream. Six GTX multi-gigabit transceivers and three full FPGA I/O banks (in total 150 single-ended I/O or up to 72 differential pairs) with configurable IO voltage are available via two high-speed, high-pin-count, board-to-board connectors. All other necessary supporting circuitry, like clock oscillators and voltage regulators are placed on module, requiring the user to attach literally only connectors and a single DC power supply. Main features of the Xenie module are illustrated in the block diagram below.

Extensive application support, basic communication IP cores and several product variants are available. We would also be happy to quickly develop base board or even customized module according to your exact specification.

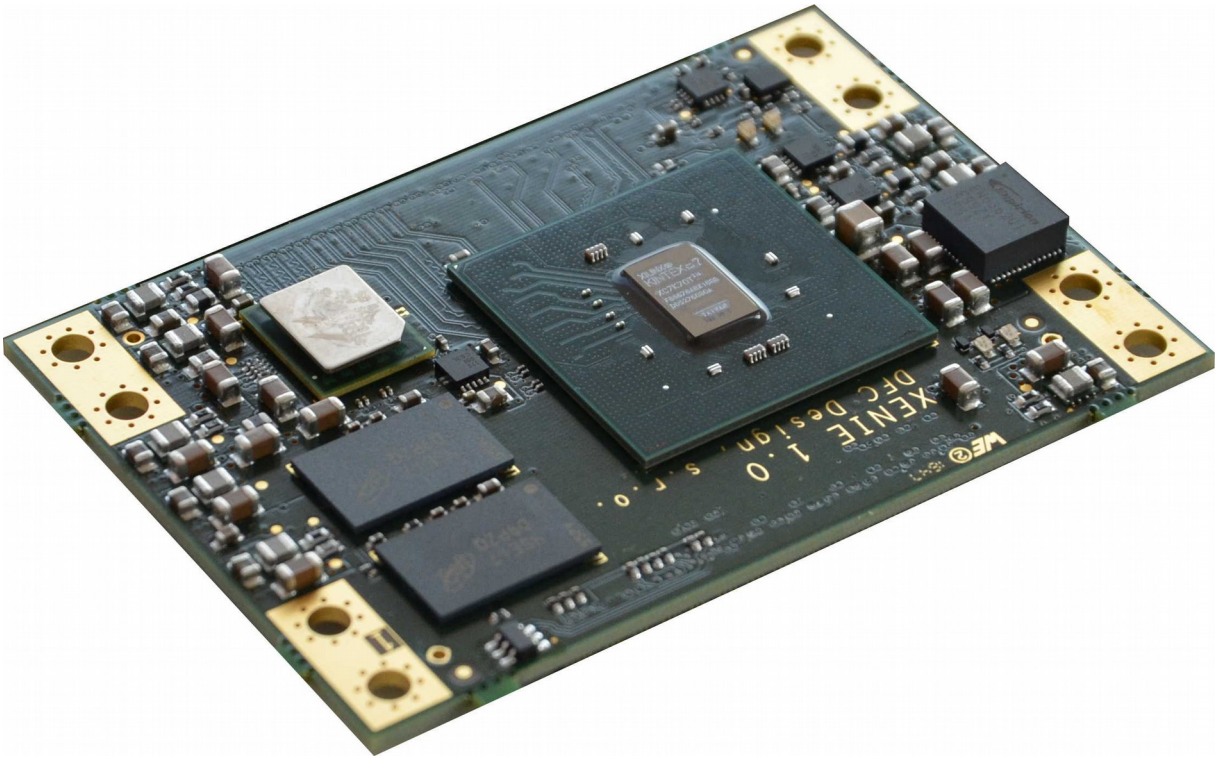
FPGA modules generally are excellent parts for prototype development and low-volume production. Their target applications are for example:

- Custom embedded systems
- High-speed communication
- Data acquisition, DSP applications

1.1 Block diagram (sch. Sheet 1)



1.2 Module features



- Xilinx Kintex-7 FPGA: XC7K160T-2FFG676C or XC7K70T-1FBG676C
- 10M/100M/1G/2.5G/5G/10G-BASE-T Ethernet PHY Marvell 88X3310
- 8 x 6.6 or 10.3125 Gb/s GTX transceivers, 6 available for custom application
- 1 GByte (256M x 32-bit) of DDR3L SDRAM, max. 667 or 1066 Mb/s
- 32 MByte Quad-SPI flash memory
- 2 Kbit I2C EEPROM with EUI-48 unique identifier
- 156.25 MHz and 200 MHz LVDS MEMS oscillators
- 3 x HR I/O bank fully available (150 single-ended I/O or up to 72 differential pairs), externally powered by arbitrary voltage in 1.2 to 3.3 V range
- 2 x user LED, FPGA Done LED, Power OK LED
- Dual high-speed 160-pin Samtec ST5-80-1.50-L-D-P connectors
- Only single external 3.3 V power supply required

- All DC/DC converters on board, some rails also available to the user base board
- Small form factor 76 x 52 mm
- Full documentation, application support and free communication IP cores available

1.4 Accessories

- Simple base board: Xenie_BB (RJ45, SFP+, RS-232, UHD-SDI TX & RX)
- Heatsink: Xenie_HS
- Basic IP cores for Ethernet and peripherals for FREE

1.5 Module variants

Currently available and tested Xenie variants are:

- **Xenie_1.0-XC7K70T-1FBG676C**
- **Xenie_1.0-XC7K160T-2FFG676C**

Xenie FPGA options - selected differences		
FPGA P/N	**XC7K70T-1FBG676C**	**XC7K160T-2FFG676C**
Logic cells	65 600	162 240
Block RAM (36Kb)	135	325
DSP48 slices	240	600
DDR3L max. data rate	667 Mb/s	1066 Mb/s
GTX max. data rate	6.6 Gb/s	10.3125 Gb/s
Package	FBG676	FFG676

Kintex-7 variants 70T and 160T are supported by free Xilinx Vivado WebPACK edition.

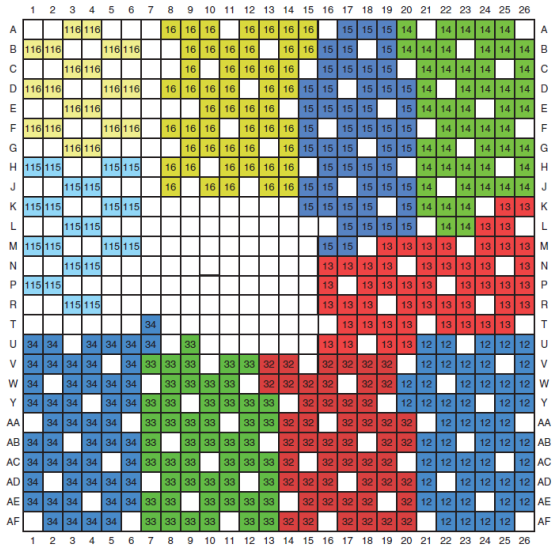
The Xenie can be also ordered in various assembly variants, depending on required features, amount of FPGA logic resources, type of package or speed-grade. Please contact us for further information.

2 FPGA

The table below provides overview of available FPGA banks, their supply voltage VCCO and utilization:

FPGA Bank utilization		
Bank	**VCCO**	**Utilization**
0	V3.3	Configuration bank, JTAG.
12	V1.8	N/A
13	VCCO_13	50 IO (24 diff. pairs). Fully available, connected to J2.
14	V3.3	Module peripherals: Q-SPI Flash, I2C bus, user LEDs, clock inputs, Ethernet PHY management interface
15	VCCO_15	50 IO (24 diff. pairs). Fully available, connected to J1 and J2.
16	VCCO_16	50 IO (24 diff. pairs). Fully available, connected to J1.
32	V1.8	N/A
33	DDR3_VDD	DDR3 – address bus, clock input.
34	DDR3_VDD	DDR3 – data bus.
115	-	2 GTX lines RXAUI (Ethernet PHY) 2 GTX lines + 1 x REFCLK connected to J1.
116	-	4 GTX lines + 2 x REFCLK connected to J1.

The figure below shows a physical location of each bank in the FPGA package:



Source: Xilinx UG475, page 107

2.1 JTAG, Configuration (sch. sheet 4)

Standard JTAG interface pins allowing to download bitstream, configure attached Flash and debug the FPGA are available in B2B connector J2. The corresponding reference voltage (3.3 V) for JTAG is available at pin J2.11.

Mode pins M0, M1 and M2 are hard-wired so that the only available configuration option for FPGA is the Master SPI mode. After power-up, FPGA would automatically load its configuration from attached non-volatile Q-SPI Flash U6, P/N is S25FL256SAGNFI001.

Configuration status is indicated by green LED D1. By default, signal 'FPGA_DONE' changes its state from L to H and LED from off to on after the FPGA configuration is successfully finished. Status signals 'FPGA_DONE', 'FPGA_INIT_B' and 'FPGA_PROG_B' to re-initiate the configuration are available in the B2B connector J2.

2.2 HP banks (sch. sheet 6)

Available High-Performance banks 33 and 34 are used exclusively for 32-bit DDR3 memory interface. The 200 MHz reference clock, output of the LVDS MEMS oscillator X2, is connected to pins AB11 and AC11.

Vref pins of bank 34 are connected to external reference voltage rail 'DDR3_VREF'. Do not use internal reference voltage. DCI pins VRN and VRP of bank 33 are connected via reference resistors to the bank supply voltage and ground. DCI cascading should be used between bank 33 (master) and bank 34.

Would the memory interface not to be used, the bank has no other purpose except of the clock input mentioned above.

2.3 HR banks (sch. sheet 5)

High-Range banks 13, 15 and 16 are fully available to the user via B2B connectors.

Bank 14 contains following signals:

'QSPI.D*'	-	data bus of Q-SPI Flash memory
'I2C.SDA, I2C.SCL'	-	I2C bus, connected to EUI-48 EEPROM memory U8 (I2C address 50h) and to B2B connector J2
'LED0, LED1'	-	user LED D3 and D4, red colour, active-low
'ALL_SRCS_PG'	-	aggregated status signal of voltage regulators
'ETH_PHY.('MDIO', 'MDC', 'GPIO[0..5]', 'INTn', 'RESETn')'		
	-	control signals of the Ethernet PHY
'ETH_PHY_RCLK1'	-	25 MHz clock recovered from Ethernet
'MUX_CLK156M25_SEL'	-	"clock select" control signal of multiplexer U7
'CLK_FPGA_156M25'	-	156.25 MHz LVDS clock input
'CLK_EXT_FPGA0'	-	redundant external LVDS clock input

2.4 GTX transceivers (sch. sheet 8)

The Kintex-7 FPGA used on the Xenie board is equipped with two GTX Quads (4 x GTX each), located in banks 115 and 116. Maximum GTX data rate depends on specific FPGA speed-grade and package type.

2.4.1 RXAUI

Two transceiver lines ‘MGTXRX/TX0_115‘ and ‘MGTXRX/TX1_115‘ are used for RXAUI interface to attach to the Ethernet PHY. Default reference clock 156.25 MHz, generated by MEMS oscillator X1, is connected via clock buffer U7 to the dedicated reference clock input ‘MGTREFCLK0_115‘.

2.4.2 User available GTX

Remaining 6 transceiver lines are made available to the user via B2B connector J1. Reference clock inputs ‘MGTREFCLK1_115‘, ‘ MGTREFCLK0_116‘ and ‘MGTREFCLK1_116‘ are also connected to the connector J1.

Important note:

Transceiver data lines and their reference clock inputs generally require AC coupling capacitors. Since module Xenie does not contain coupling capacitors, they might be required on the user base board.

2.5 Constraints file

The basic XDC constraints file (list of all FPGA pins combined with all necessary constraints for example FPGA design) will be available as a part of the firmware reference design.

3 10G PHY (sch. sheet 9)

The most distinctive feature of the Xenie module is its support of 10M/100M/1G/2.5G/5G and 10G-BASE-T Ethernet over UTP/STP copper lines. This hardware capability is based on Marvell 88X3310 single port PHY.

3.1 RXAUI, management

PHY is attached to higher layers (MAC) in FPGA via fixed speed 10 Gbit/s RXAUI interface (two 6.25 Gb/s GTX transceiver lines).

Other interconnects between FPGA and PHY are signals for its management or additional functions (e.g. 'ETH_PHY.GPIO[0..5]'). Especially important is the Management Data Input/Output (MDIO) bus ('ETH_PHY.MDIO','ETH_PHY.MDC') providing not only basic configuration of PHY but also it is the only available channel to load a firmware to the RAM of the internal microcontroller.

Note:

Xenie is equipped with I2C EEPROM U8 with stored EUI-48 unique identifier, intended as a source of Ethernet MAC address.

3.2 Hardware configuration

Eight hardware configuration pins CONFIG[0..7] are hard-wired to power pins, LEDs or GPIO to set their multi-bit value at the deassertion of hardware reset. It is possible to change this configuration via MDIO, or if necessary to cut across relevant net tie NT[7..14] and connect it by wire to one of test points TP[17..24]. The hard-wired configuration setting can be found in schematics of Xenie module – page 9.

3.3 Device clocking

See Chapter 5 for information about the clock subsystem.

3.4 MDI - copper interface

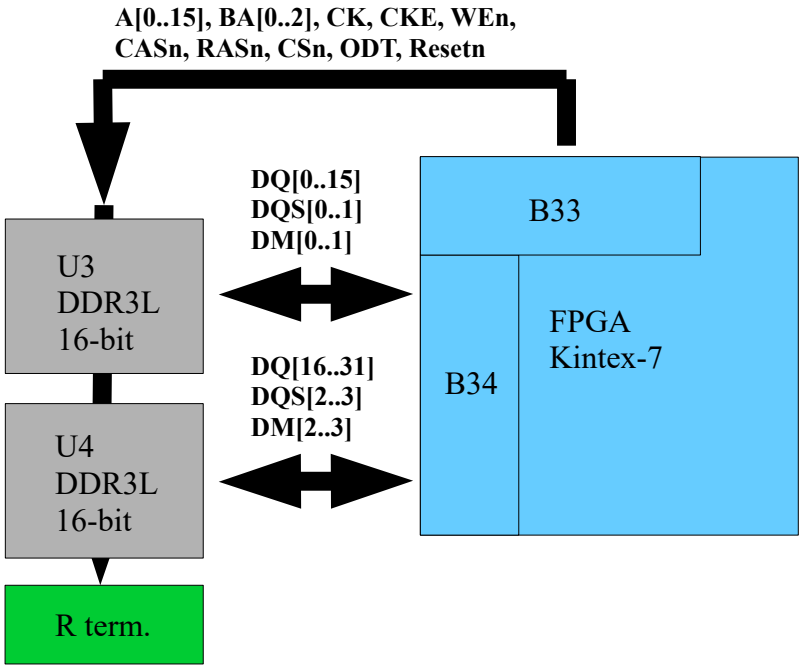
The copper medium (UTP or STP) should be attached to PHY (bus 'ETH_MDI') via appropriate RJ45 Jack and magnetics. To simplify the solution and save base board space, RJ45 Jacks with integrated magnetics are recommended. Actual part type should be selected based on PHY manufacturer requirements. Our recommended, widely available and tested part is Pulse JT7-1104NL.

One of EMI cancellation method is so called Common Mode Sense (CMS). If used, CMS requires 5th channel in the Ethernet magnetics. Positive pin of the magnetics dedicated channel can be connected to 'ETH_MDI.CMS' - pin CMP of the PHY via a filter circuit. Refer to the reference design schematics for details.

PHY can also support the internal CMS – in that case, CMP pin must be connected to GND via 100nF capacitor C6 and 5th channel of the magnetics must be disconnected.

4 DDR3 (sch. Sheet 6, 7)

Module Xenie is equipped with 1 GByte (256M x 32-bit) of DDR3L SDRAM connected to FPGA HP banks. As illustrated in the following picture, the memory data bus is 32-bit wide, physically consisting of two 16-bit memory chips. The data bus topology is point-to-point utilizing On Die Termination. The address, command, control and clock signals are routed in so called fly-by topology and terminated at the end of the line.



Two currently available FPGA variants enable max. data rates 667 Mb/s (-1FBG676C) or 1066 Mb/s (-2FFG676C) provided DDR3L (1.35V) memory chips are used. Higher data rates of 800 Mb/s respectively 1333 Mb/s are achievable with DDR3(1.5V) devices.

4.1 MIG settings

Xilinx provides Memory Interface Generator (MIG) tool to generate memory controllers and interfaces that may be used in user FPGA design. Set of recommended MIG input parameters to create 32-bit DDR3 memory controller for tested Xenie variants is available in the following table:

MIG settings for a MT41K256M16HA-125 …

MIG		
TBD		

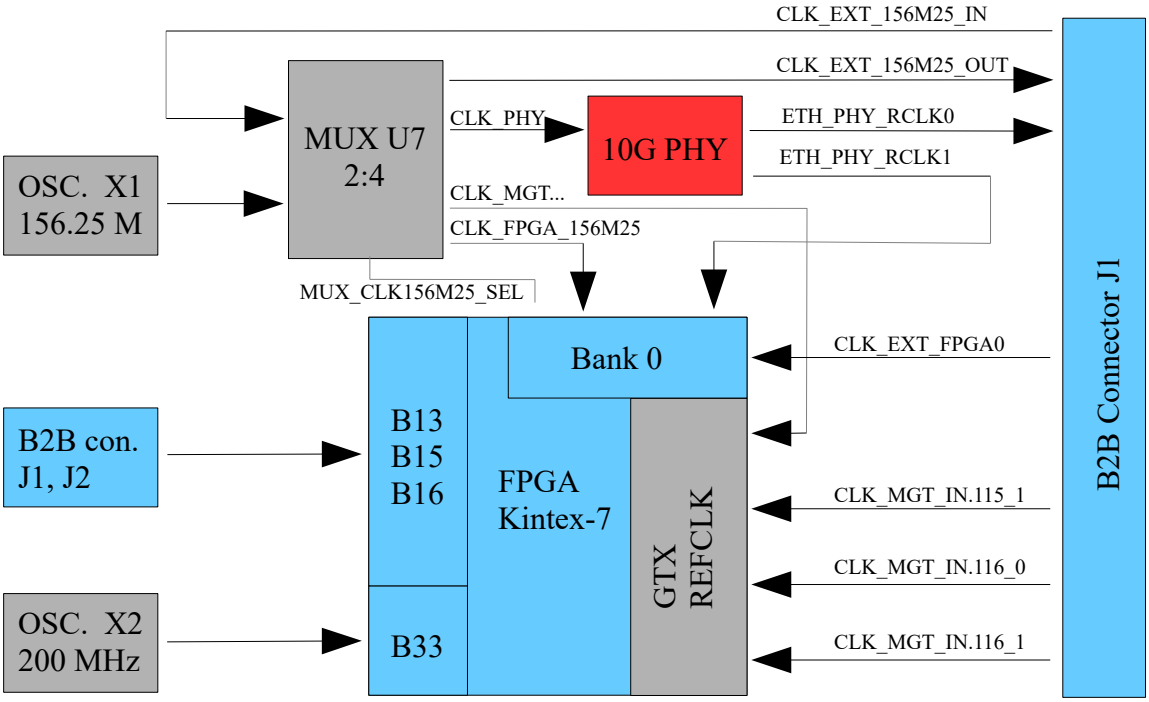
5 CLOCK (sch. sheet 3)

The default clock sources for Xenie module are two differential MEMS oscillators X1 and X2. Oscillator X2 generating output frequency 200 MHz is a clock source for FPGA fabric and reference clock for DDR3 memory interface.

Oscillator X1 generates output frequency 156.25 MHz as a reference for Ethernet communication. Its output is buffered by multiplexer U7 and connected to FPGA fabric, Ethernet PHY, GTX transceivers and B2B connector J1. Second input of the multiplexer U7 is redundant input that enables to connect external reference clock (e.g. from external PLL) as a clock source for Ethernet. May this functionality be required, recovered clocks from the Ethernet PHY ('ETH_PHY_RCLK0,1') may serve as reference for the external PLL. Output clock of the multiplexer U7 is selected by its control signal 'MUX_CLK156M25_SEL'.

Other clock sources for the FPGA fabric can be connected to the dedicated input pair 'CLK_EXT_FPGA0' or any of the MRCC or SRCC pins in banks 13, 15 and 16.

Free GTX transceivers have their dedicated reference clock inputs connected to B2B connector J1, enabling the user to provide reference clock according to the requirements of the communication protocol. Following block diagram shows the clocking of the Xenie module:



Important note:

Externally connected clocks may require AC coupling capacitors and internal or external termination. Logic standard of all differential clocks is LVDS; single-ended recovered clock 'ETH_PHY_RCLK0,1' are LVCMOS33.

6 BOARD POWER (sch. sheet 12)

The Xenie module is designed to operate from a single 3.3 V DC power supply.

All other required voltage rails are generated by step-down switching and LDO regulators integrated on module. Their output voltage, its accuracy and ripple, current supply capabilities and sequencing also complies with all requirements of implemented components. Some voltage regulators have reserved extra current to optionally power FPGA IO banks 13, 15 and 16 or even a part of the target application.

Regulators on the board are grouped into three imaginary sections:

- FPGA: rails *V1.0, V1.8, V3.3, DDR3_VDD, DDR3_VTT*

  - power for FPGA, DDR3 memory and common rails for other circuits on module

- FPGA_MGT: rails *V1.0_MGT, V1.2_MGT, V1.8_MGT*

  - dedicated low noise voltage rails for GTX transceivers of the FPGA

- PHY 88X3310: rails *0.8 V, 1.5 V, 2.0 V, 2.5 V*

  - dedicated rails for the Marvell 88X3310 Ethernet PHY

The proper operating state of all power supplies is indicated by green LED D2 and high state of the power good signal ‘ALL_SRCS_PG‘. This signal is connected to FPGA and B2B connector J2, its voltage in high state is about 2.3 V.

6.1 Power input

Main power input pins of the B2B connectors are designated ‘V3.3_IN‘. It is highly recommended to power the module via all 12 available pins of both connectors. Required parameters of the input rail are presented in the following table:

Board power input	
Power rail name	V3.3_IN
Voltage nominal	3.3 V
Voltage min.	3.2 V
Voltage max.	3.465 V

6.2 External VCCO for FPGA IO Banks (sch. sheet 11)

To allow greater flexibility for the target application, the user available FPGA IO banks 13, 15 and 16 must have their power connected externally to corresponding B2B pins VCCO_13, VCCO_15 and VCCO_16.

Depending on application requirements, VCCO can be powered from one of available power rails of the module (DDR3_VDD, V1.8, V2.5 or V3.3) or from an external source. Supply voltage for HR banks 13, 15 and 16 must be in range between 1.2 to 3.3 V.

Adequate amount of decoupling for each IO bank is located on module, it is not required to connect any additional capacitors externally.

Important note:

Would user need to power the VCCO from an external source, please refer to the Xilinx DS182 – section: Power-On/Off Power Supply Sequencing, for more information.

Rail V3.3 is the last in sequence to be switched on by the load switch U12. User must not power VCCO from rail V3.3_IN nor connect V3.3 and V3.3_IN together.

6.3 Power outputs

The following table contains a list of output power rails available to the target application via B2B connectors. They can power FPGA IO banks or supply limited current for the arbitrary purposes.

Board power outputs				
Power rail name	DDR3_VDD	V1.8	V2.5	V3.3
Voltage nominal	1.35 V	1.8 V	2.5 V	3.3 V
Current max.	0.5 A	0.5 A	0.5 A	0.5 A
Purpose	VCCO, arbitrary	VCCO, arbitrary	VCCO, arbitrary, Ethernet magnetics – center tap	VCCO, arbitrary

7 B2B connectors J1,J2 (sch. sheet 2)

Connector P/N: Xenie Module: Samtec ST5-80-1.5-L-D-P

Xenie BB base board: Samtec SS5-80-3.5-L-D-K-TR

→ Default stacking height is 5 mm.

Other connector variant combinations allows also stacking heights 4.0 or 4.5 mm.

Following table summarizes the pin-out of B2B connectors J1 and J2. All pins are grouped according to their function. Short description and application notes are provided where appropriate.

Pin type abbreviations: P – Power, I – Input, O – Output, IO – Input/Output

B2B Connector J1				
B2B Pin #	**B2B Signal name**	**FPGA Pin #**	**Type**	**Description, note**
Power				
2,4,8,14, 15,20,25, 26,31,32, 37,38,43, 44,49,50, 55,56,61, 62,67,68, 69,74,83, 84,97,98, 111,112, 125,126, 139,140, 150,153, 154,159, 160	GND	-	P	Ground
1,3,5,7	V3.3_IN	-	P	Power input (3.3 V, max. 3.465 V, min. 3.2 V)
9,11	V2.5	-	P	Power output (2.5 V, 0.5 A), power for Ethernet magnetics center tap
145,147	VCCO_15	-	P	Power input, power for FPGA IO Bank 15
146,148	VCCO_16	-	P	Power input, power for FPGA IO Bank 16

Ethernet				
4	ETH_MDI.P0	-	IO	Ethernet MDI, pair 0, pos.
6	ETH_MDI.N0	-	IO	Ethernet MDI, pair 0, neg.
10	ETH_MDI.N1	-	IO	Ethernet MDI, pair 1, neg.
12	ETH_MDI.P1	-	IO	Ethernet MDI, pair 1, pos.
16	ETH_MDI.P2	-	IO	Ethernet MDI, pair 2, pos.
18	ETH_MDI.N2	-	IO	Ethernet MDI, pair 2, neg.
22	ETH_MDI.N3	-	IO	Ethernet MDI, pair 3, neg.
24	ETH_MDI.P3	-	IO	Ethernet MDI, pair 3, pos.
13	ETH_MDI.CMS	-	I	Ethernet - Common Mode Sense cancellation
17	ETH_LED0	-	O	Ethernet LED0
19	ETH_LED1	-	O	Ethernet LED1
21	ETH_LED2	-	O	Ethernet LED2
23	ETH_LED3	-	O	Ethernet LED3
FPGA GTX Transceivers				
27	MGT.115_RX2_N	L3	I	GTX Receiver, bank 115, line 2, neg.
29	MGT.115_RX2_P	L4	I	GTX Receiver, bank 115, line 2, pos.
33	MGT.115_RX3_N	J3	I	GTX Receiver, bank 115, line 3, neg.
35	MGT.115_RX3_P	J4	I	GTX Receiver, bank 115, line 3, pos.
39	MGT.116_RX0_N	G3	I	GTX Receiver, bank 116, line 0, neg.
41	MGT.116_RX0_P	G4	I	GTX Receiver, bank 116, line 0, pos.
45	MGT.116_RX1_N	E3	I	GTX Receiver, bank 116, line 1, neg.
47	MGT.116_RX1_P	E4	I	GTX Receiver, bank 116, line 1, pos.
51	MGT.116_RX2_N	C3	I	GTX Receiver, bank 116, line 2, neg.
53	MGT.116_RX2_P	C4	I	GTX Receiver, bank 116, line 2, pos.
57	MGT.116_RX3_N	B5	I	GTX Receiver, bank 116, line 3, neg.
59	MGT.116_RX3_P	B6	I	GTX Receiver, bank 116, line 3, pos.
28	MGT.115_TX2_N	K1	O	GTX Transmitter, bank 115, line 2, neg.
30	MGT.115_TX2_P	K2	O	GTX Transmitter, bank 115, line 2, pos.
34	MGT.115_TX3_N	H1	O	GTX Transmitter, bank 115, line 3, neg.
36	MGT.115_TX3_P	H2	O	GTX Transmitter, bank 115, line 3, pos.

40	MGT.116_TX0_N	F1	O	GTX Transmitter, bank 116, line 0, neg.
42	MGT.116_TX0_P	F2	O	GTX Transmitter, bank 116, line 0, pos.
46	MGT.116_TX1_N	D1	O	GTX Transmitter, bank 116, line 1, neg.
48	MGT.116_TX1_P	D2	O	GTX Transmitter, bank 116, line 1, pos.
52	MGT.116_TX2_N	B1	O	GTX Transmitter, bank 116, line 2, neg.
54	MGT.116_TX2_P	B2	O	GTX Transmitter, bank 116, line 2, pos.
58	MGT.116_TX3_N	A3	O	GTX Transmitter, bank 116, line 3, neg.
60	MGT.116_TX3_P	A4	O	GTX Transmitter, bank 116, line 3, pos.
Clock				
63	CLK_MGT_IN.115_1_N	K5	I	GTX Reference clock, bank 115, IN 1, neg.
65	CLK_MGT_IN.115_1_P	K6	I	GTX Reference clock, bank 115, IN 1, pos.
64	CLK_MGT_IN.116_0_N	D5	I	GTX Reference clock, bank 116, IN 0, neg.
66	CLK_MGT_IN.116_0_P	D6	I	GTX Reference clock, bank 116, IN 0, pos.
70	CLK_MGT_IN.116_1_N	F5	I	GTX Reference clock, bank 116, IN 1, neg.
72	CLK_MGT_IN.116_1_P	F6	I	GTX Reference clock, bank 116, IN 1, pos.
152	ETH_PHY_RCLK0	-	O	Ethernet PHY recovered clock
149	CLK_EXT_FPGA0.P	F22	I	FPGA LVDS clock input, pos.
151	CLK_EXT_FPGA0.N	E23	I	FPGA LVDS clock input, neg.
155	CLK_EXT_156M25_OUT.P	-	O	Buffered 156.25 MHz LVDS clock, pos.
157	CLK_EXT_156M25_OUT.N	-	O	Buffered 156.25 MHz LVDS clock, neg.
156	CLK_EXT_156M25_IN.N	-	I	Redundant input of multiplexer U7, LVDS, neg.
158	CLK_EXT_156M25_IN.P	-	I	Redundant input of multiplexer U7, LVDS, pos.

FPGA IO Bank 16				
100	B16.L25	J14	IO	FPGA IO Bank 16, IO pin, single-ended only
102	B16.L0	J8	IO	FPGA IO Bank 16, IO pin, single-ended only
71,73,75, 76,77,78, 79,80,81, 82,85,86, 87,88,89, 90,91,92, 93,94,95, 96,99, 101,103, 104,105, 106,107, 108,109, 110,113, 114,115, 116,117, 118,119, 120,121, 122,123, 124,128, 130,132, 134	B16.*	-	IO	FPGA IO Bank 16, IO pins
FPGA IO Bank 15				
127,129, 131,133, 135,137, 141,143, 136,138, 142,144	B15.*	-	IO	FPGA IO Bank 15, IO pins

B2B Connector J2				
B2B Pin #	**B2B Signal name**	**FPGA Pin #**	**Type**	**Description**
Power				
2,4,6,8,9,10,12,14,15,16,17,18,19,20,22,24,26,28,30,32,34,35,37,38,40,42,51,52,65,66,79,80,93,94,107,108,121,122,135,136,149,151	GND	-	P	Ground
153,154,155,156,157,158,159,160	V3.3_IN	-	P	Power input (3.3 V, max. 3.465 V, min. 3.2 V)
11,25,27,36	V3.3	-	P	Power output (3.3 V, 0.5 A), power for JTAG
21,23	DDR3_VDD	-	P	Power output (1.35 V, 0.5 A)
31,33	V1.8	-	P	Power output (1.8 V, 0.5 A)
13	VCCBATT_0	E8	P	Power input – bitstream encryption backup battery
150,152	VCCO_13	-	P	Power input, power for FPGA IO Bank 13
FPGA Config status, I2C				
39	FPGA_PROG_B	P6	I	Active-low reset to configuration logic.
41	FPGA_INIT_B	G7	IO	FPGA Initialization (refer to Xilinx UG470).
43	FPGA_DONE	J7	O	Indication of the completion of configuration.
45	ALL_SRCS_PG	-	O	Aggregated Power-Good of all voltage regulators.
47	I2C.SCL	D25	O	I2C Bus, signal SCL
49	I2C.SDA	D24	IO	I2C Bus, signal SCL (note: addr. 50h reserved)

FPGA IO Bank 15				
48	B15.L25	M16	IO	FPGA IO Bank 15, IO pin, single-ended only
50	B15.L0	K15	IO	FPGA IO Bank 15, IO pin, single-ended only
53,54,55, 56,57,58, 59,60,61, 62,63,64, 67,69,71, 73,75,77, 81,83,85, 87,89,91, 95,97,99, 101,103, 105,109, 111,113, 115,117, 119	B15.*	-	IO	FPGA IO Bank 15, IO pins
FPGA IO Bank 13				
44	B13.L0	N16	IO	FPGA IO Bank 13, IO pin, single-ended only
46	B13.L25	U16	IO	FPGA IO Bank 13, IO pin, single-ended only
68,70,72, 74,76,78, 82,84,86, 88,90,92, 96,98, 100,102, 104,106, 110,112, 114,116, 118,120, 123,124, 125,126, 127,128, 129,130, 131,132, 133,134, 137,138, 139,140, 141,142, 143,144, 145,146, 147,148	B13.*	-	IO	FPGA IO Bank 13, IO pins

7.1 FPGA to B2B trace length/pin delay

The trace delay report will be available as a part of the project data package.

8 MECHANICAL

8.1 Physical characteristics

- Module size: 76 x 52 mm
- Board stacking height: 5 mm, optionally 4.0 or 4.5 mm
- Weight: TBD

8.2 Operating conditions

Default Xenie assembly variants consists of commercial grade components.

Proper operation is guaranteed in a temperature range:

8.3 Module mounting holes

Module Xenie has 8 symmetrically placed mounting holes with diameter of 3.2 mm. All mounting holes are connected to ground potential of the module (GND).

Four outer holes (MH1, MH2, MH3, MH4) are intended for additional mechanical attachment of the module to the base board, via four spacers/standoffs. Spacers are recommended to be made of good thermal conductor (e.g. brass) in order to enhance heat dissipation of the module. Their height must exactly match the board stacking height.

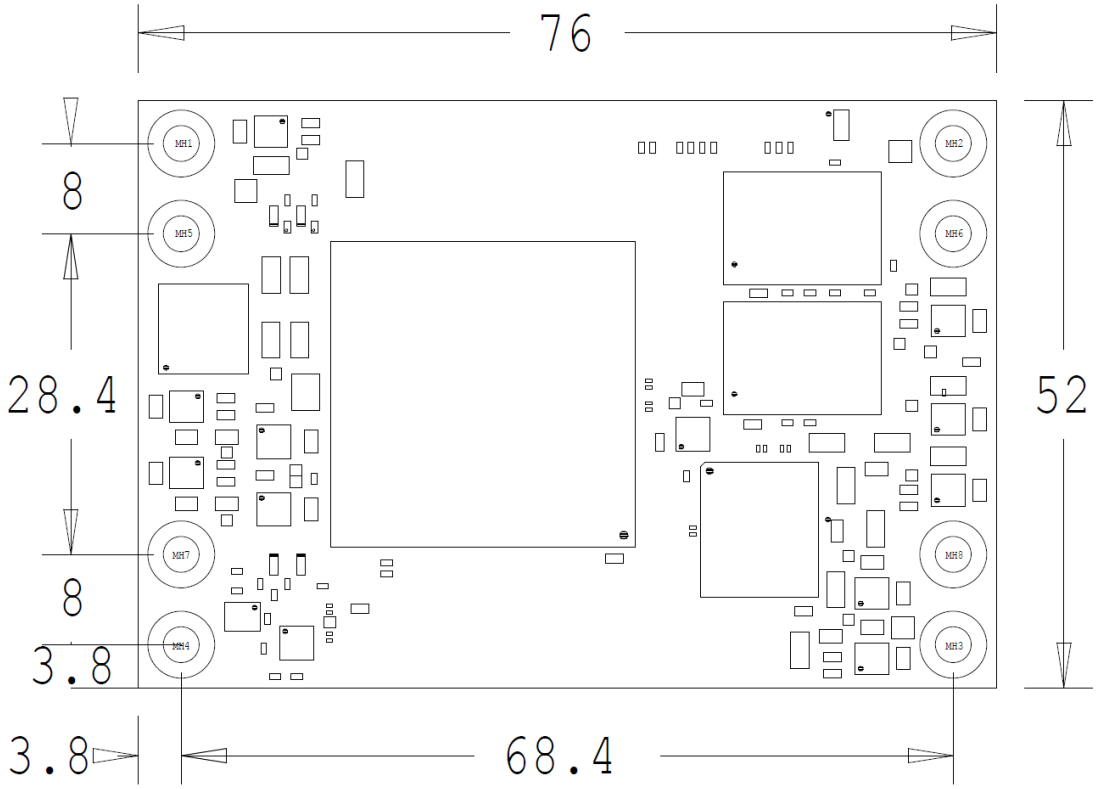
The purpose of four inner holes (MH5, MH6, MH7, MH8) is to attach heatsink to the module by four M3 screws.

8.4 Heatsink

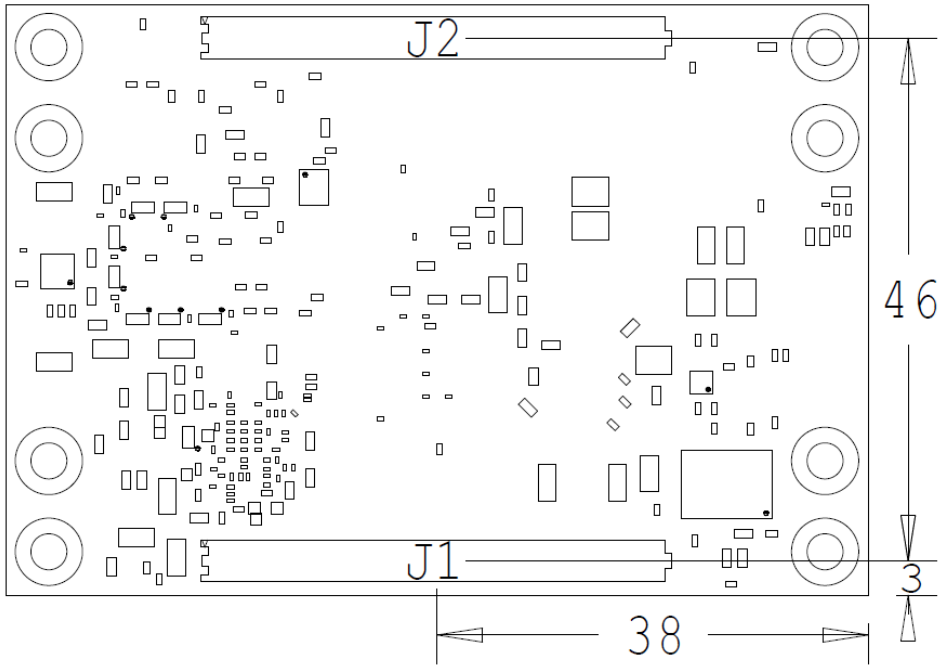
Xenie_HS

8.5 Module dimensions

Top - FPGA side:



Bottom - B2B Connectors side:



9 Base board Xenie_BB

Simple base board for Xenie module, serving a purpose of demonstration and evaluation was designed and made freely available as a reference design for user target applications.

The key features of Xenie_BB are:

- 3.3 V, 8A DC/DC converter with wide input voltage range and precise output current measurement
- 10GBase-T compliant, PoE+ capable RJ45 connector
- SFP+ connector connected to one GTX transceiver line
- 2 x UHD-SDI digital video input, based on TI LMH1219 Adaptive Cable Equalizer
- 2 x UHD-SDI digital video output, based on TI LMH1218 Cable Driver
- 148.5 MHz and 148.35 MHz LVDS oscillators connected to GTX REFCLK inputs
- RS-232 interface
- 100 fully available IO (entire banks B13 and B16) with selectable VCCO, routed as differential pairs and connected to two 2.54 mm headers

9.1 Xenie_BB photo

TBD