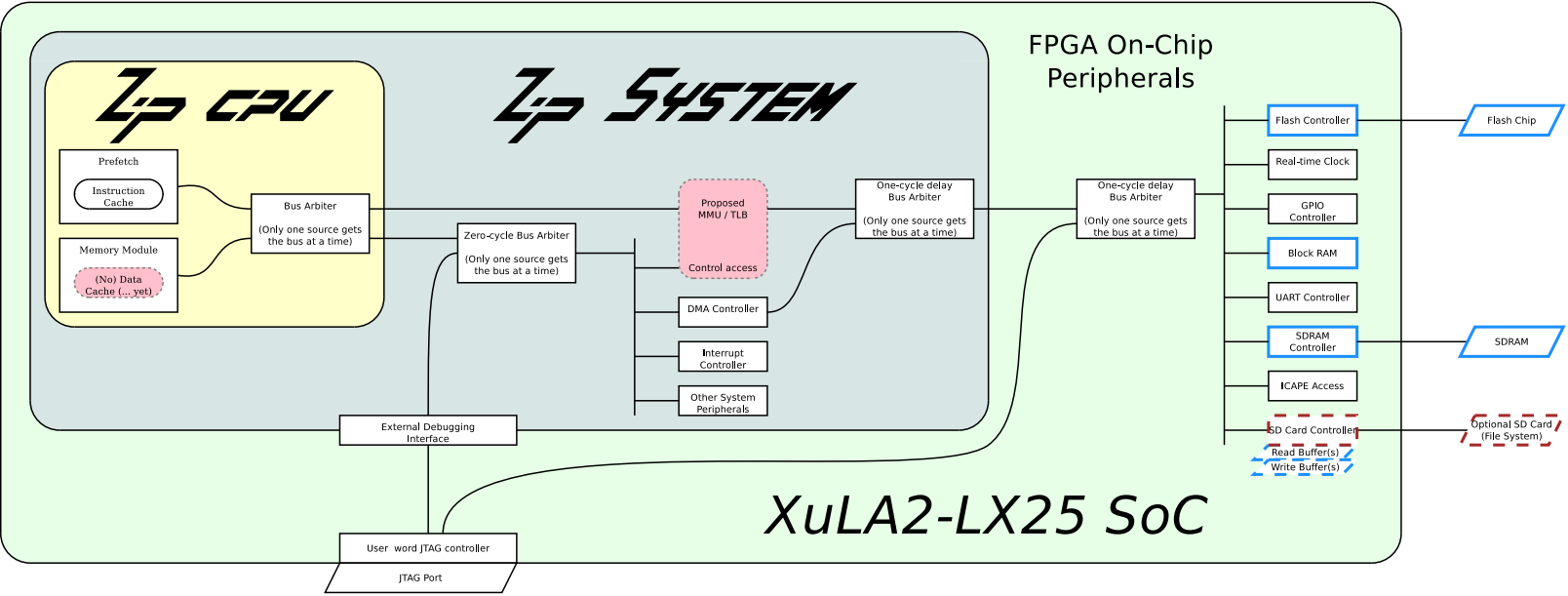

Timing:

Prefetch Cache: No delay, 1 cycle delay on early branches, 5 cycle delay on conditional branches, and indirect jumps (like returns)
Bus access delay: B=3 cycles (1-2 more with MMU?)
Flash: B+64+64N
SDRAM: B+6+2N
BlockRam and other I/O peripherals: B+N
ICAPE access ... takes much longer

SDRAM Load instruction cost: 1+3+6+2=12 clocks
- Subsequent loads (if pipelined): 2 clocks
- Maximum sustained pipeline: 13 loads (limited by number of registers)
- Practical maximum pipeline: 4 loads (without dumping registers)
BlkRAM Load instruction cost: 1+3+1 = 5 clocks
- Subsequent loads (if pipelined): 1 clock each

Cache line miss cost from SDRAM: 1+B+6+2(64) = 138 clocks