sel[2..0]   INPUT
             VCC

sel[2] sel[2] sel[1] sel[1] sel[0] sel[0]

not2   NOT   not1   NOT   not0   NOT

in0   INPUT
        VCC

AND4
and0

in1   INPUT
        VCC

AND4
and1

in2   INPUT
        VCC

AND4
and2

in3   INPUT
        VCC

AND4
and3

OR8

OUTPUT   out

in4   INPUT
        VCC

AND4
and4

inst

in5   INPUT
        VCC

AND4
and5

in6   INPUT
        VCC

AND4
and6

in7   INPUT
        VCC

AND4
and7

PROJECT	A-Z80	MODULE	alu_mux_8	
DESIGNER	Goran Devic			
DATE	May 18, 2014		REV	1.0

alu_mux_8.bdf