## Quad ISA Business Case

Several computer architectures exist, serving several programming styles:

The register file style uses two or three register designators in each instruction. Separate load and store instructions are used to access memory.

The accumulator style combines an operation with a memory reference.

The stack style uses a data stack for operands and results.

The x86 style uses a small register file and a memory addressing mode which includes a scaled index.

Herein two bits of the op-code designate the style and the remainder of the instruction is of the corresponding style. Additionally a set of op-codes is reserved for a macro capability. Macros provide a way to abbreviate instructions whilst keeping the ability to have register fields within the macro.

For each ISA style data sizes can be one of four sizes; typically 8, 16, 32 or 64 bits. An alternate set of sizes is 8, 16, 24 and 48 bits.

The purpose of quad\_isa is to have a research environment with similar implementation of the various architectural styles such that one can easily compare coding and performance between the various styles. There are long standing debates on these matters. Here there is a uniform set of operations, defined instruction formats and eventually FPGA implementation.

In somewhat greater detail:

The macro instructions can be a single byte. This can be used to have a traditional set of zero operand stack operators.

The "accumulator" instructions can use the register file as data and return and frame stacks with offset indexing from data, return and frame register file pointers. They also include memory access by indirection thru the register file.

The register file instructions use 24-bits providing denser code than 32-bit RISC instructions.

The x86 style combines the RISC instructions with the x86 addressing mode instructions.

Prefix bytes are provided which are used to increase the number of op-codes and to increase the size of the register file.

The net result is a "Quad" ISA surpassing most ISAs of a single style and having a uniform means of specifying variable size immediate values.