

# Cereon

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## Processor identification scheme

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## **2 Introduction**

This document describes the processor identification scheme used by Cereon family of processors.

## 3 Microarchitecture identification

A specific Cereon microarchitecture has an identifier of the form:

```
Cereon <architecture version><target><model><features>
```

where:

- `<architecture version>` is a numeric identifier of the Cereon architecture version implemented by a specific microarchitecture (currently 1).
- `<target>` is a one-letter code of the intended processor niche. See Appendix B for the list of target codes.
- `<model>` is a numeric identifier that allows telling apart different processor microarchitectures which have the same `<architecture version>`, `<features>` and `<target>`. Model identifiers can be assigned arbitrarily.
- `<features>` is a list of zero or more characters that specify which optional features are available. Features are enumerated in the order in which they appear in the CPUID identifier, from higher bits to lower (i.e. if Base, Unaligned operand, Floating point and Debug features are all present, the feature string will be “UDFB”).

### 3.1 Microarchitecture code names

Specific microarchitectures can also be assigned code names. Two different microarchitectures cannot have the same code name.

Current naming guidelines prescribe the use of mythological creature names as Cereon microarchitecture code names (for example, the Cereon 1P1B microarchitecture has a code name “Magog”). It is fully understood that these code names cannot be copyrighted or used as a trademark, instead, they are to be used for internal reference only.

## 4 Processor identification

A specific Cereon processor has an identifier of the form:

```
<microarchitecture>-<optimization goal><sequence no>
```

where:

- `<microarchitecture>` is a string identifying a microarchitecture implemented by the processor in question, as described in the previous chapter.
- `<optimization goal>` is a one-letter code specifying the main characteristic that was optimized for the processor in question. See appendix C for the list of optimization codes.
- `<sequence no>` is a numeric identifier that uniquely identifies a specific processor model. Sequence numbers are assigned sequentially starting with 1 and are global across all processors, regardless of their microarchitecture or implementation details.

### 4.1 Processor code names

Specific processors can also be assigned code names. Two different processors cannot have the same code name.

Current naming guidelines prescribe the processor code names to be constructed from a combination of microarchitecture code names and arbitrary colours (for example, the Cereon 1P1B-B1 processor has a code name “White Magog”). It is fully understood that these code names cannot be copyrighted or used as a trademark, instead, they are to be used for internal reference only.

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## 6 Appendix B: Target niche codes

Target code	Intended target niche
A	Application platforms running complex OSES on consumer devices.
M	Deeply embedded cost-sensitive environments (such as mobile).
P	Research prototypes.
R	Real-time embedded environments (such as MCUs).
S	Medium-to-heavy-load server environment.
W	Personal workstations.
Z	Processor not designated for a specific target niche.

## 7 Appendix C: Optimization codes

Target code	Intended target niche
B	A balanced processor, where performance, size and energy consumption are all deemed equally important.
P	Processor optimized for the best performance, regardless of size or energy consumption.
S	Processor optimized for the smallest size (number of gates) regardless of performance or energy consumption.
W	Processor optimized for the smallest energy consumption, regardless of performance or size.