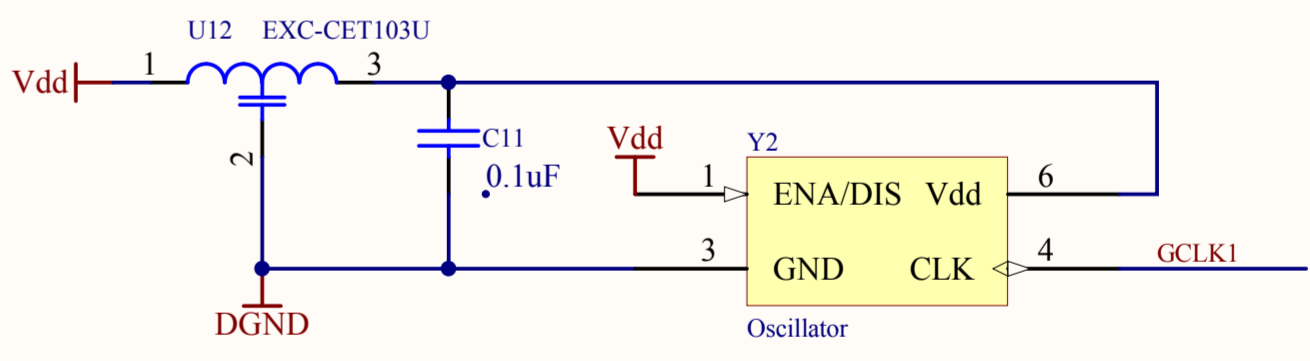
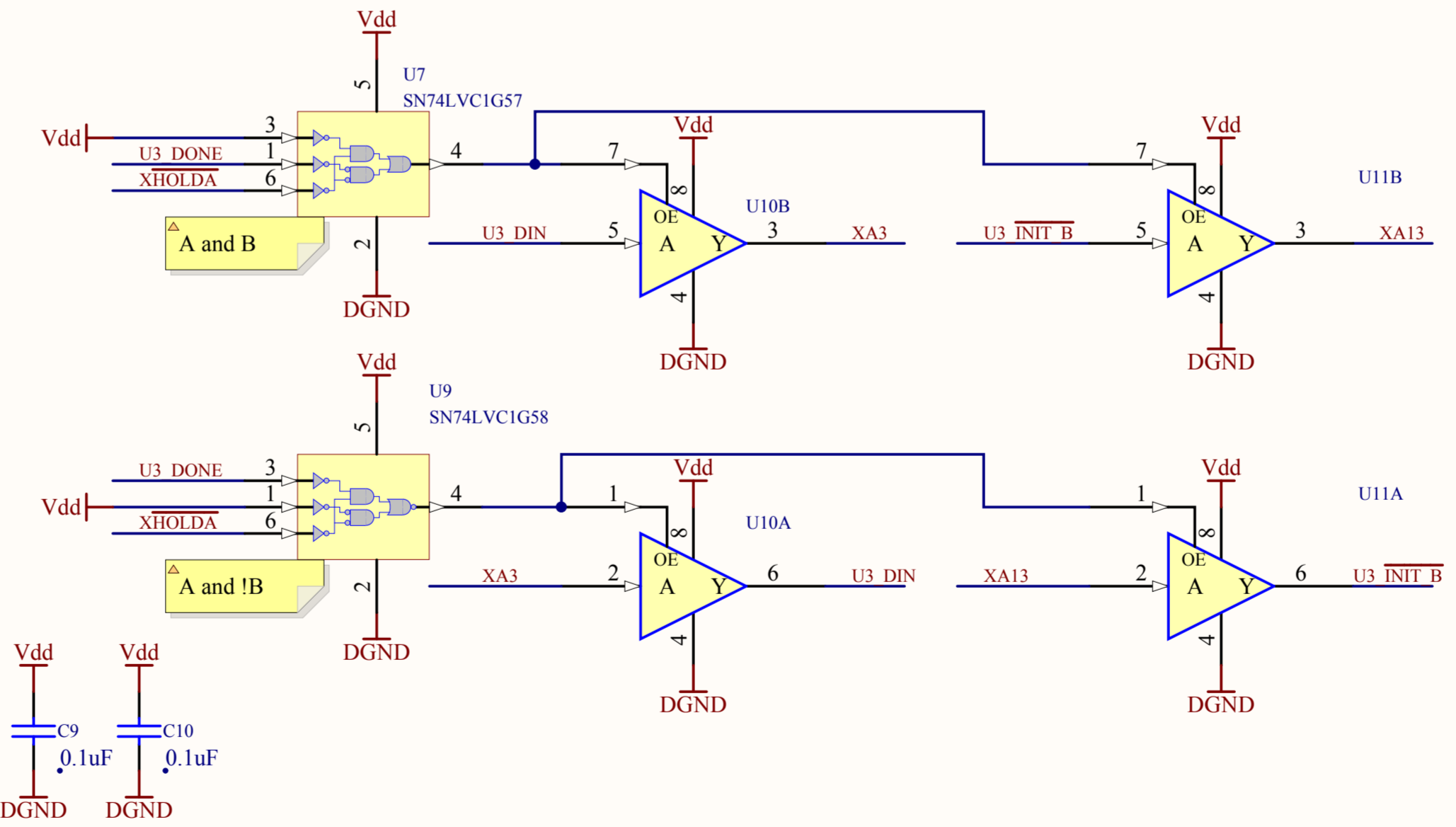


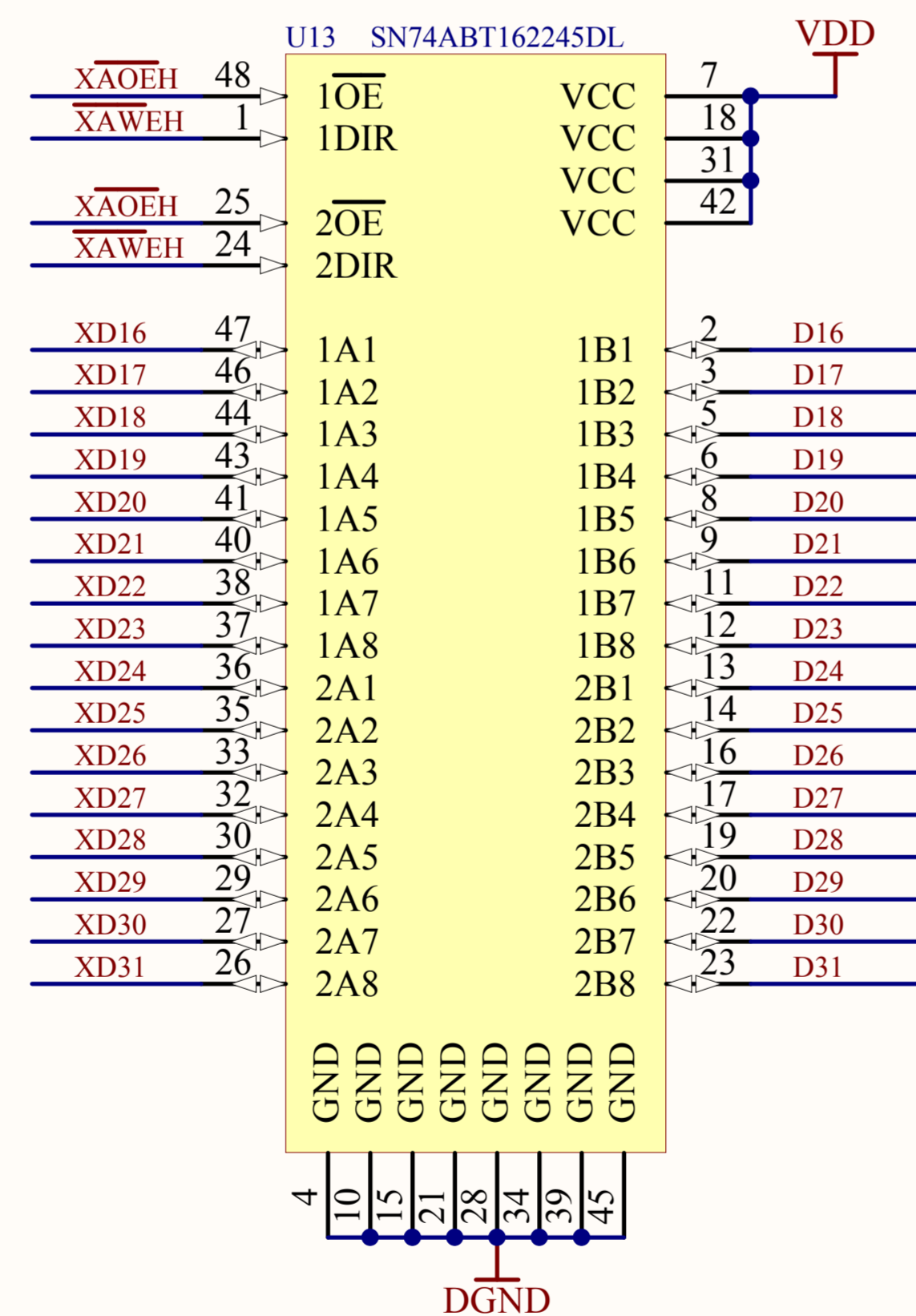
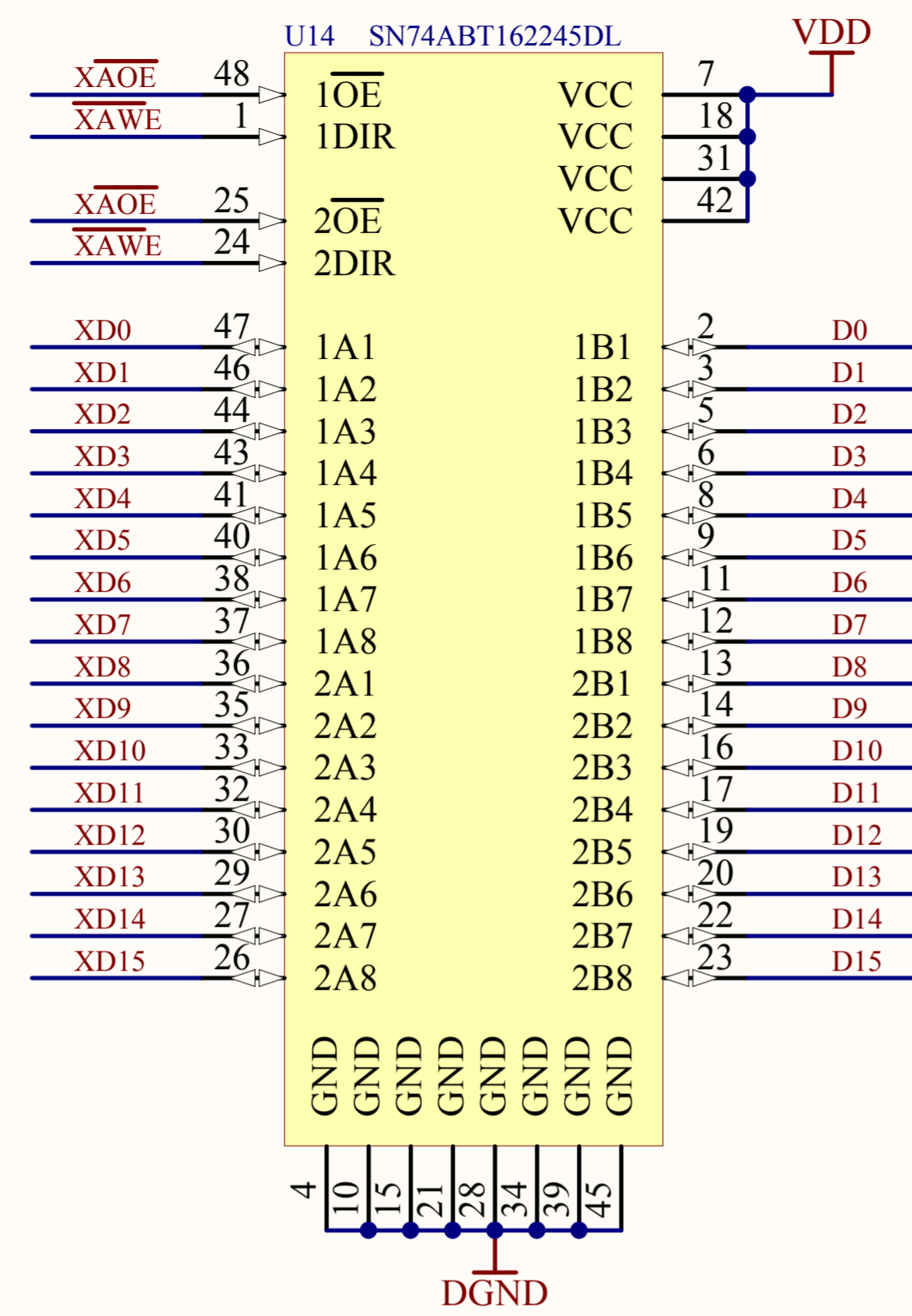
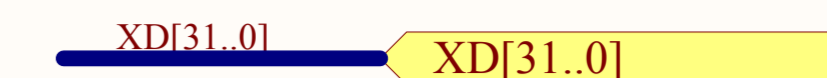
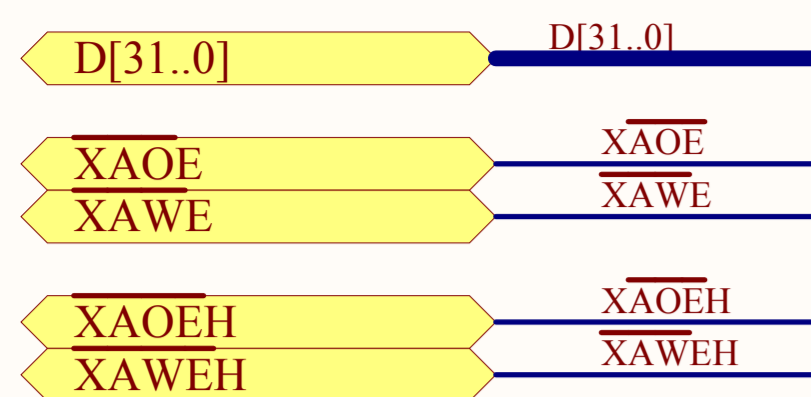
External Interface



IPMB\_PWR  
SMBB\_SDA  
SMBB\_SCL  
SMBB\_RSV

|  |                               |  |                  |
|--|-------------------------------|--|------------------|
| <b>QORTEK INC.</b>   |                               |  |                  |
| Address<br>1965 Lycoming Creek Rd<br>Suite 205<br>Williamsport, PA 17701<br>Phone<br>5700 322 2700 |                               | Title<br><b>cPCI Interface and Ext. DSP A/D Bus Interface FPGA</b> |                  |
| Size<br>Tabloid  | Number<br>QOR-cPCIDSP-4-REV.1 | Revision<br>1  | Date<br>9/2/2005 |
| File<br>D:\Projects\U_Bus_Interfaces.SchDoc  | Sheet of<br>1                 | Drawn By<br>Brian Shea   |                  |



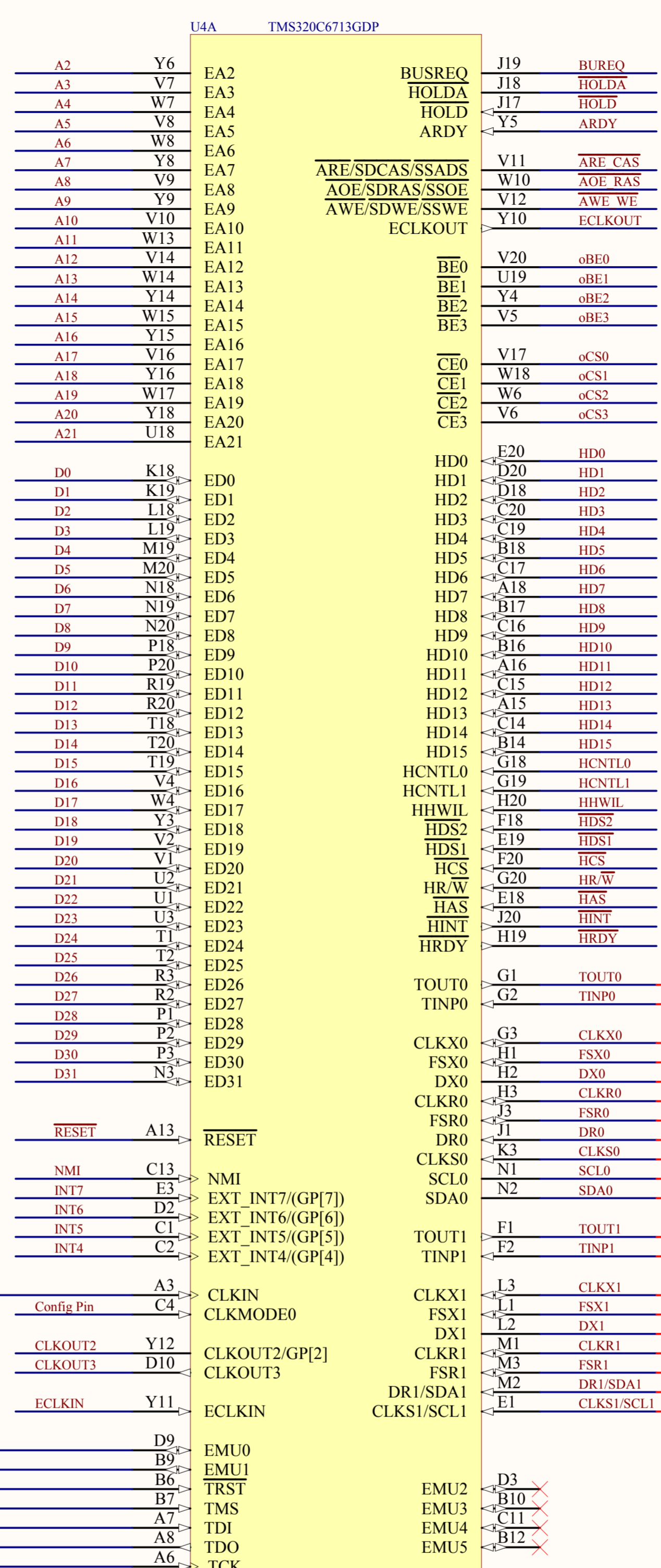
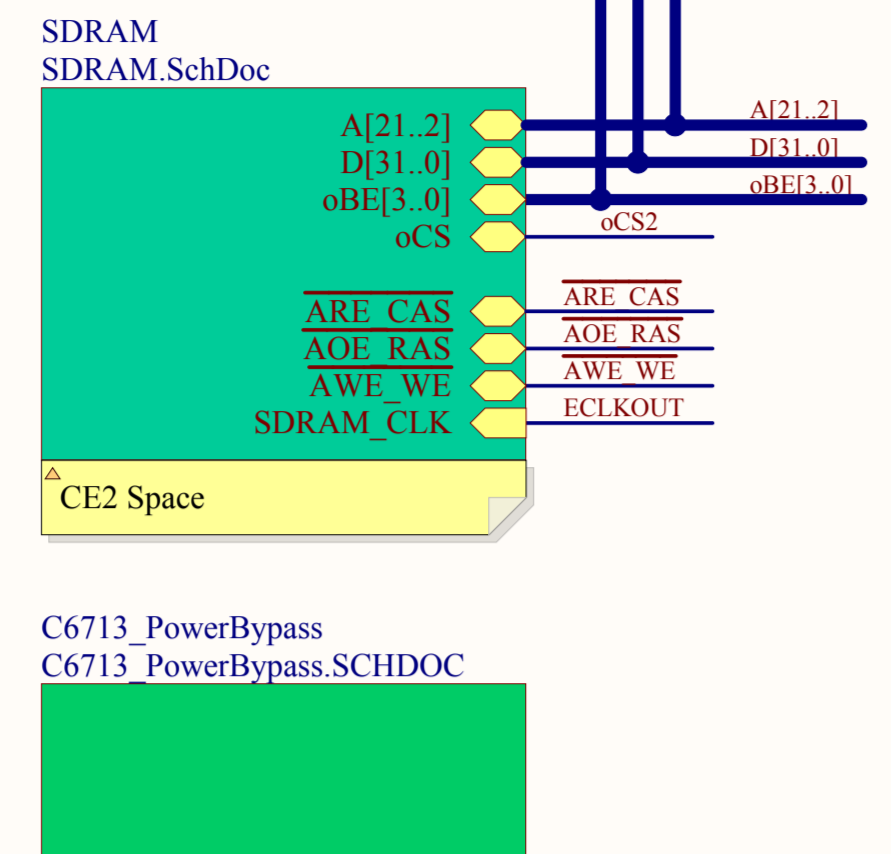
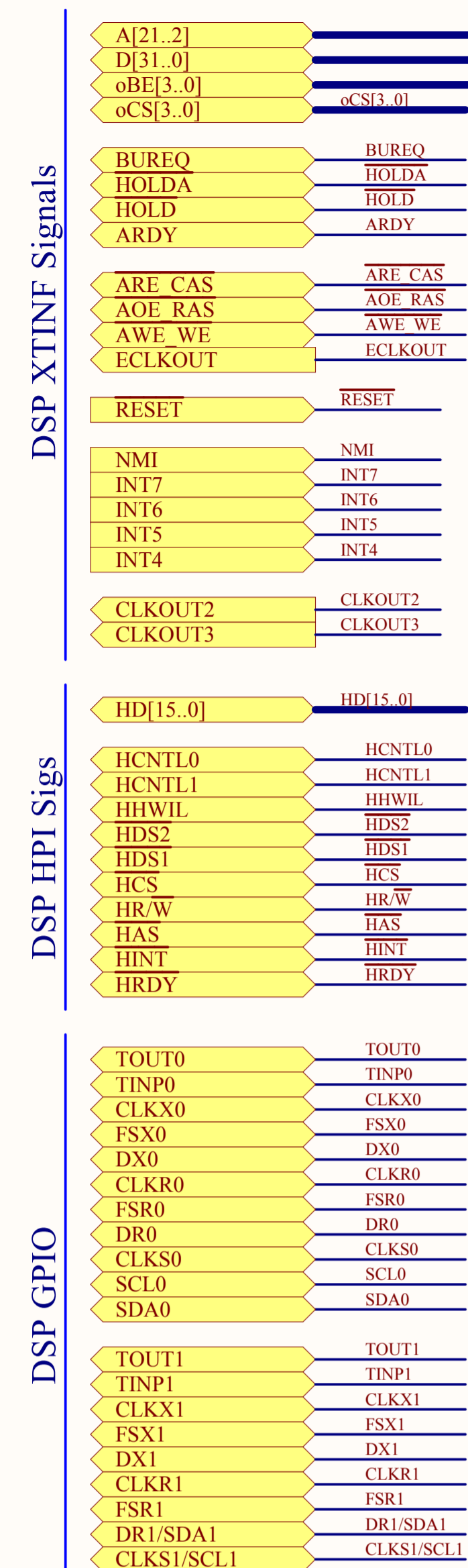


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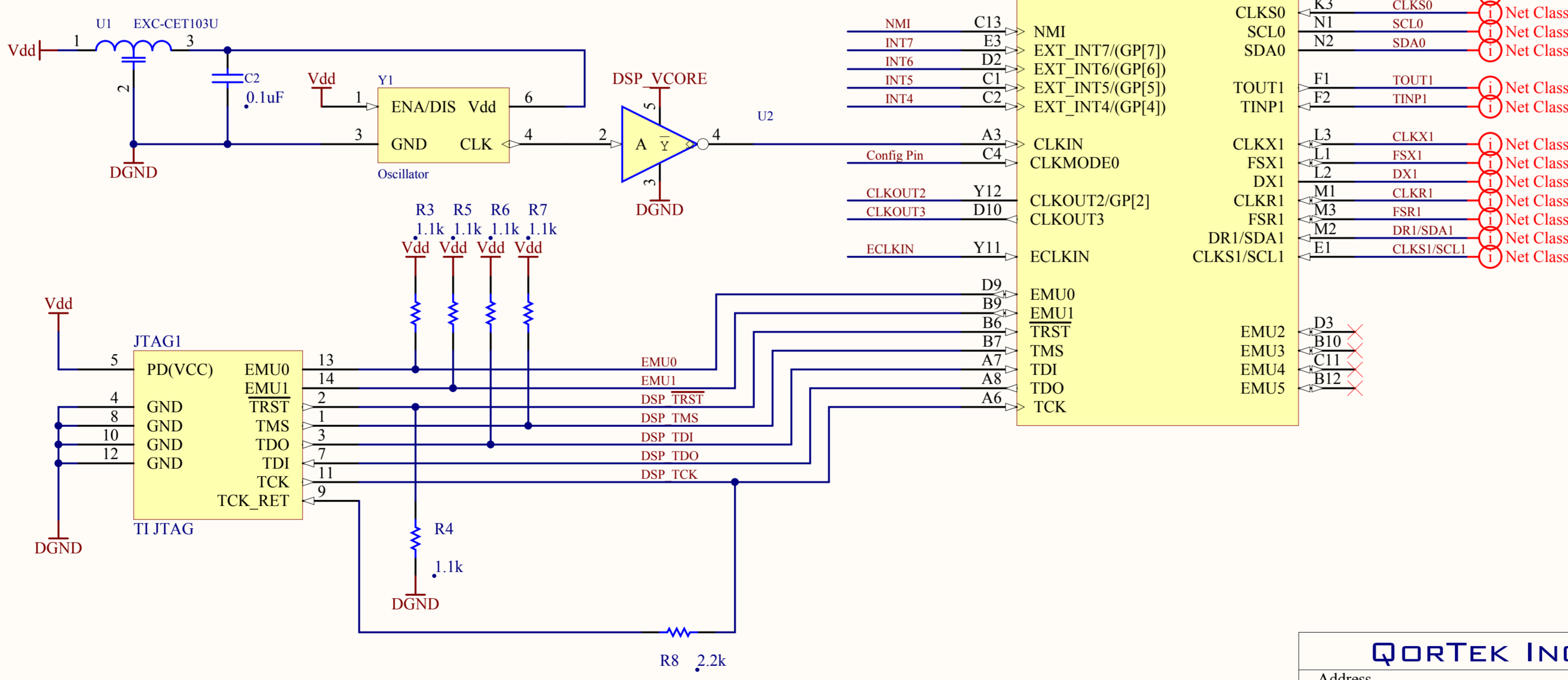
Address  
 1965 Lycoming Creek Rd  
 Suite 205  
 Williamsport, PA 17701  
 Phone  
 570 322 2700



|   |                               |               |
|---|-------------------------------|---------------|
| Title<br><b>Data Bus Isolators/ Bidirectional Buffers</b> |                               |               |
| Size<br>Letter  | Number<br>QOR-cPCIDSP-5-REV.1 | Revision<br>1 |
| Date:<br>9/2/2005   | Sheet of                      |               |
| File:<br>D:\Projects\...\Bus_Isolators.SchDoc             | Drawn By:                     | Brian Shea    |

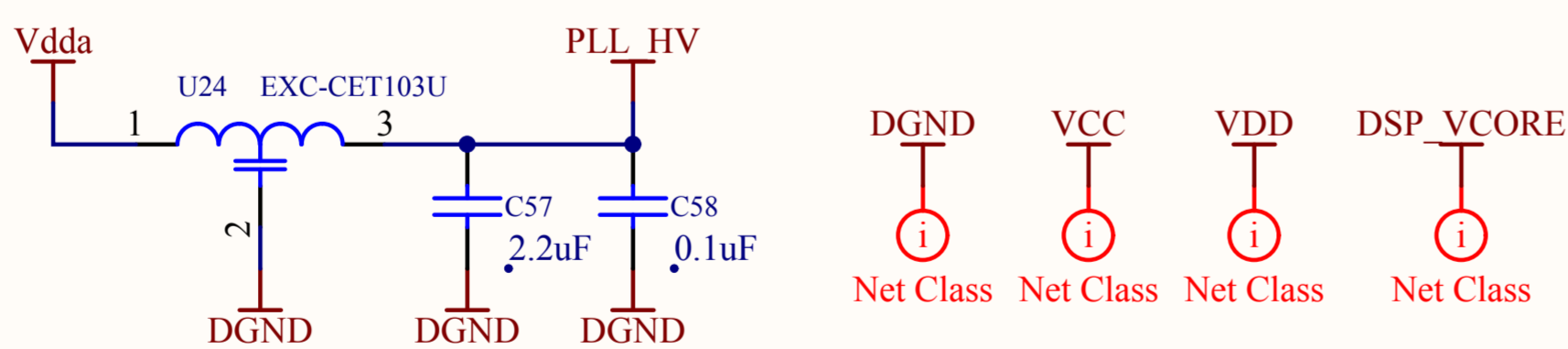
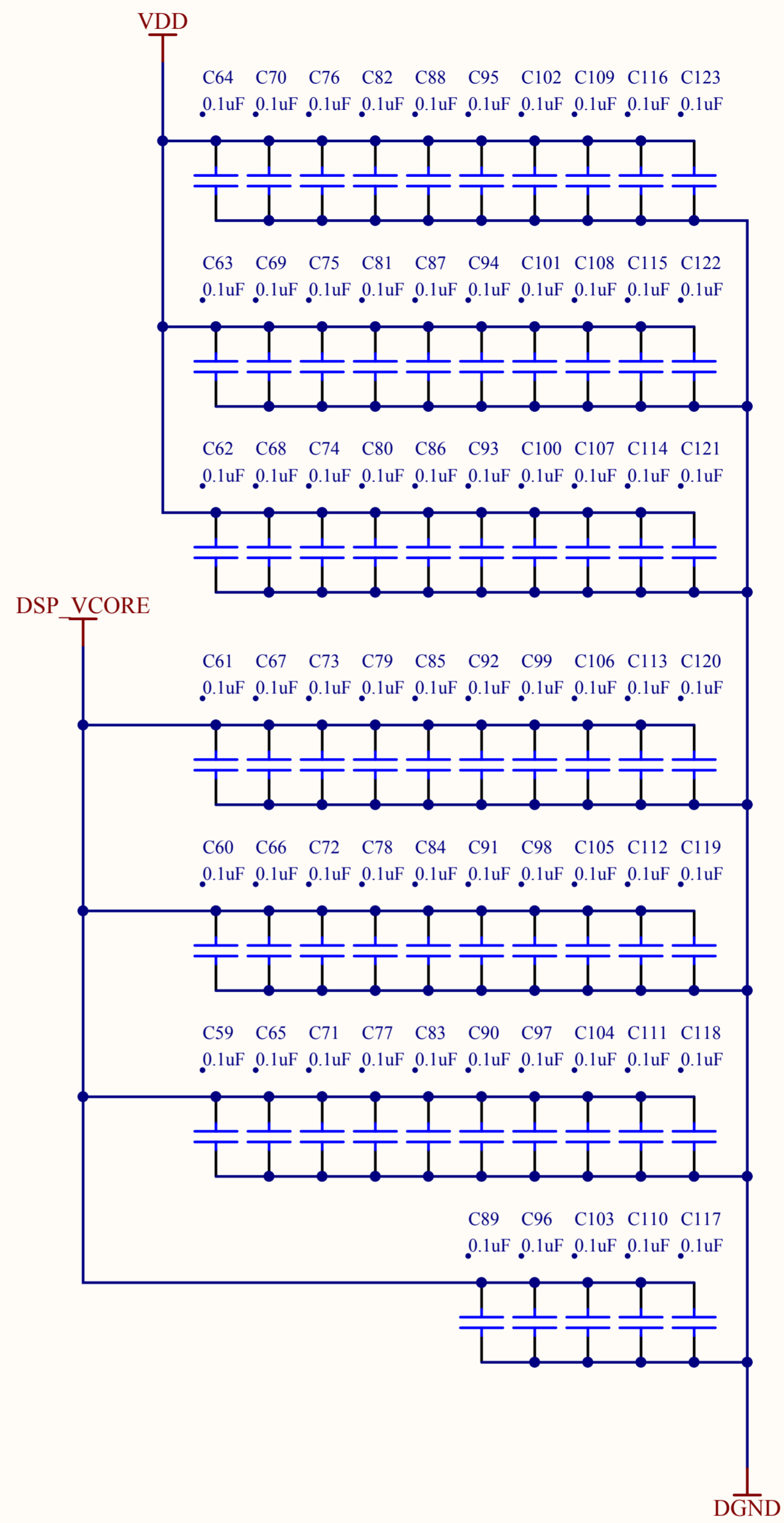
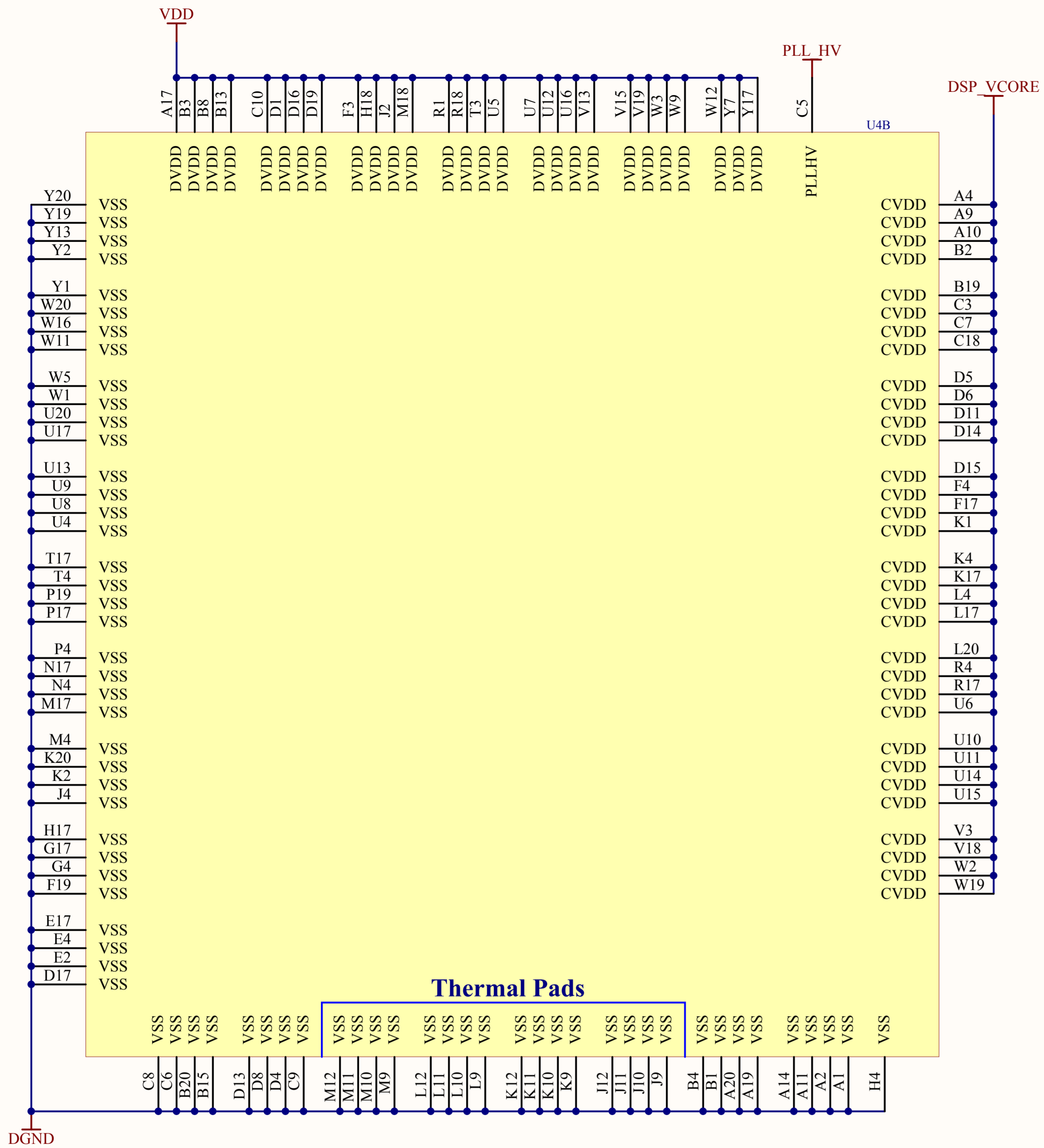


ECLKOUT is based on ECLKIN or SYSCLK3



|   |  |                 |                               |  |  |
|---|--|-----------------|-------------------------------|--|--|
| <b>QORTEK INC.</b>  |  |                 |                               | Title<br>TMS320C6713GDP and JTAG Interface |  |
| Address<br>1965 Lycoming Creek Rd<br>Suite 205<br>Williamsport, PA 17701<br>Phone<br>570 322 2700 |  | Size<br>Tabloid | Number<br>QOR-ePCIDSP-2-REV.1 | Revision<br>REV 1                          |  |
| Date:   | 9/2/2005                               | Sheet of        |                               |  |  |
| File:   | D:\Projects\...C6713_Controller.SchDoc | Drawn By:       | Brian G. Shea                 |  |  |

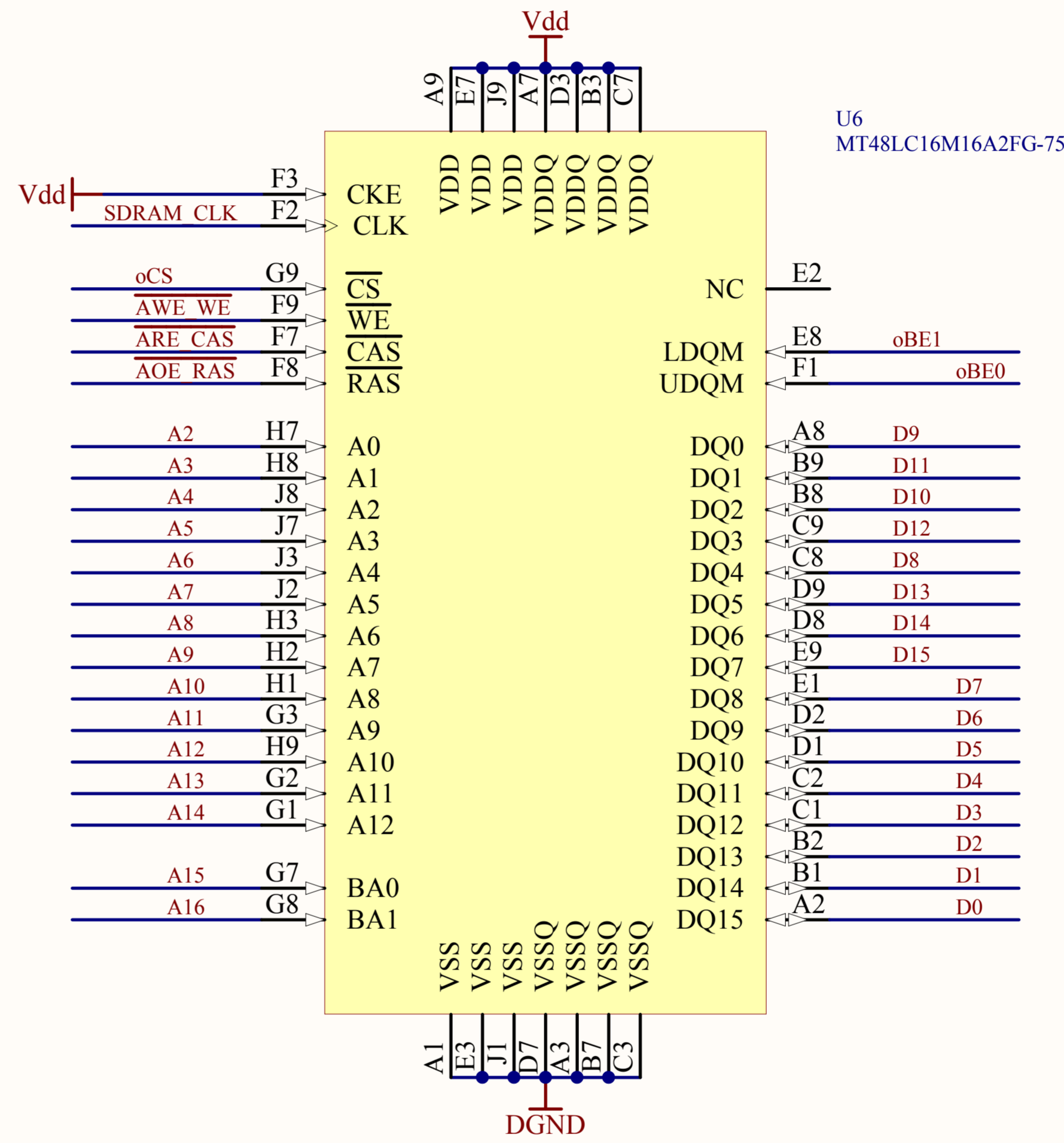
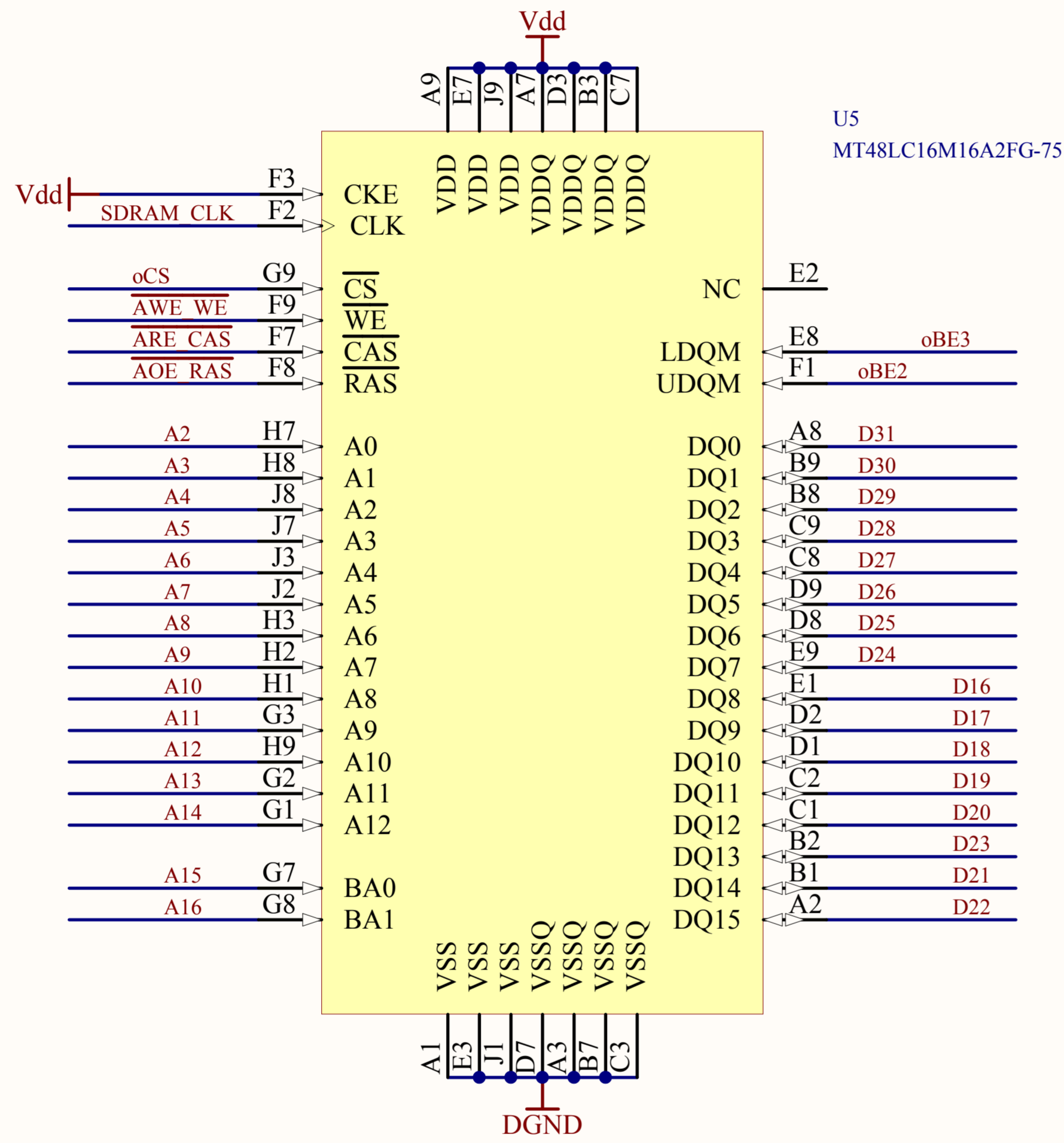
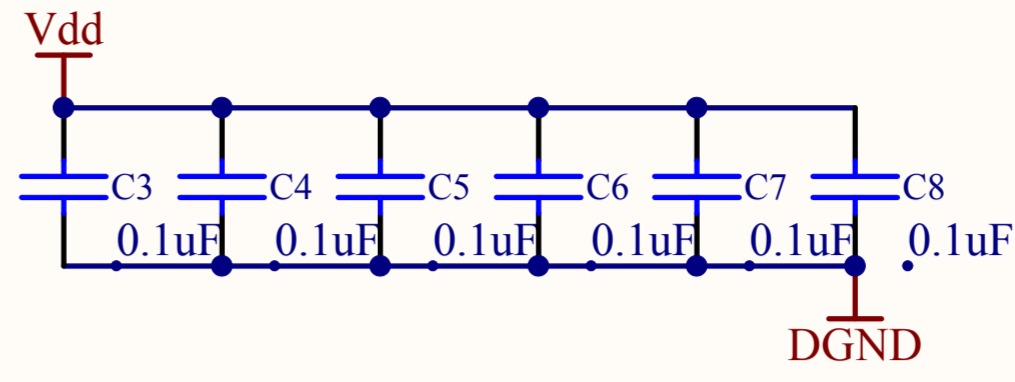
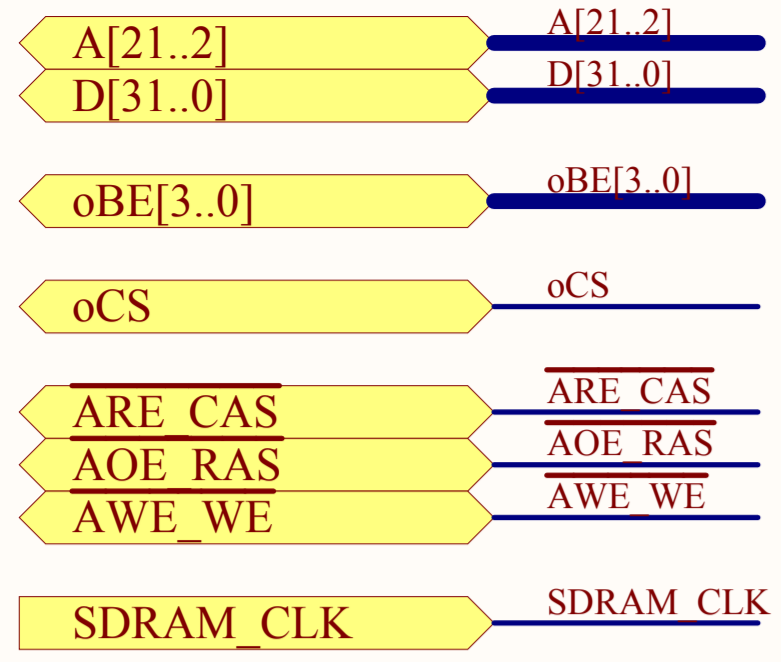




Note: 300MHz Version Uses 1.4v Core. All others are 1.2v. Old revisions of the chip used 1.26v but are compatible with the 1.2v Core Voltage

|   |  |   |                                |   |  |
|---|--|---|--------------------------------|---|--|
| <b>QORTEK INC.</b><br>Address<br>1965 Lycoming Creek Rd<br>Suite 205<br>Williamsport, PA 17701<br>Phone<br>570 322 2700 |  |  |                                | Title<br><b>TMS320C6713 Power Bypass</b>    |  |
|   |  | Size<br>Legal   | Number<br>QOR-cPCIDSP-21-REV.1 | Revision<br>1                               |  |
| Date: 9/2/2005  |  | Sheet of  |                                | File: D:\Projects\...\C6713_PowerBypass.SCH |  |
|   |  | Drawn By: Brian Shea  |                                |   |  |





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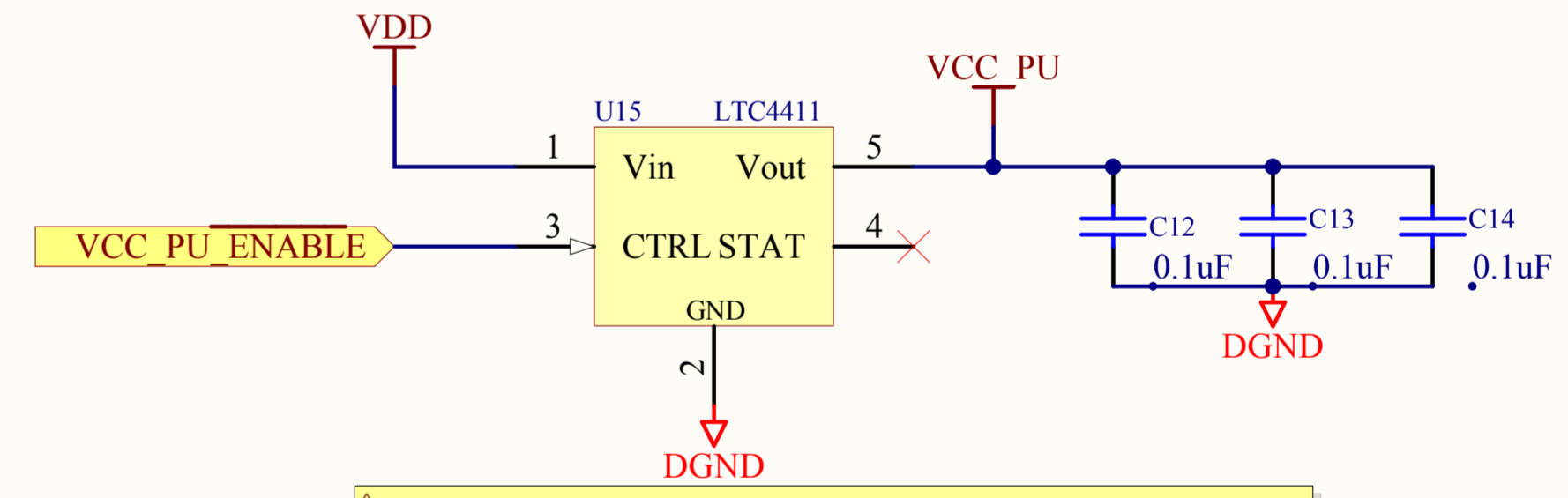
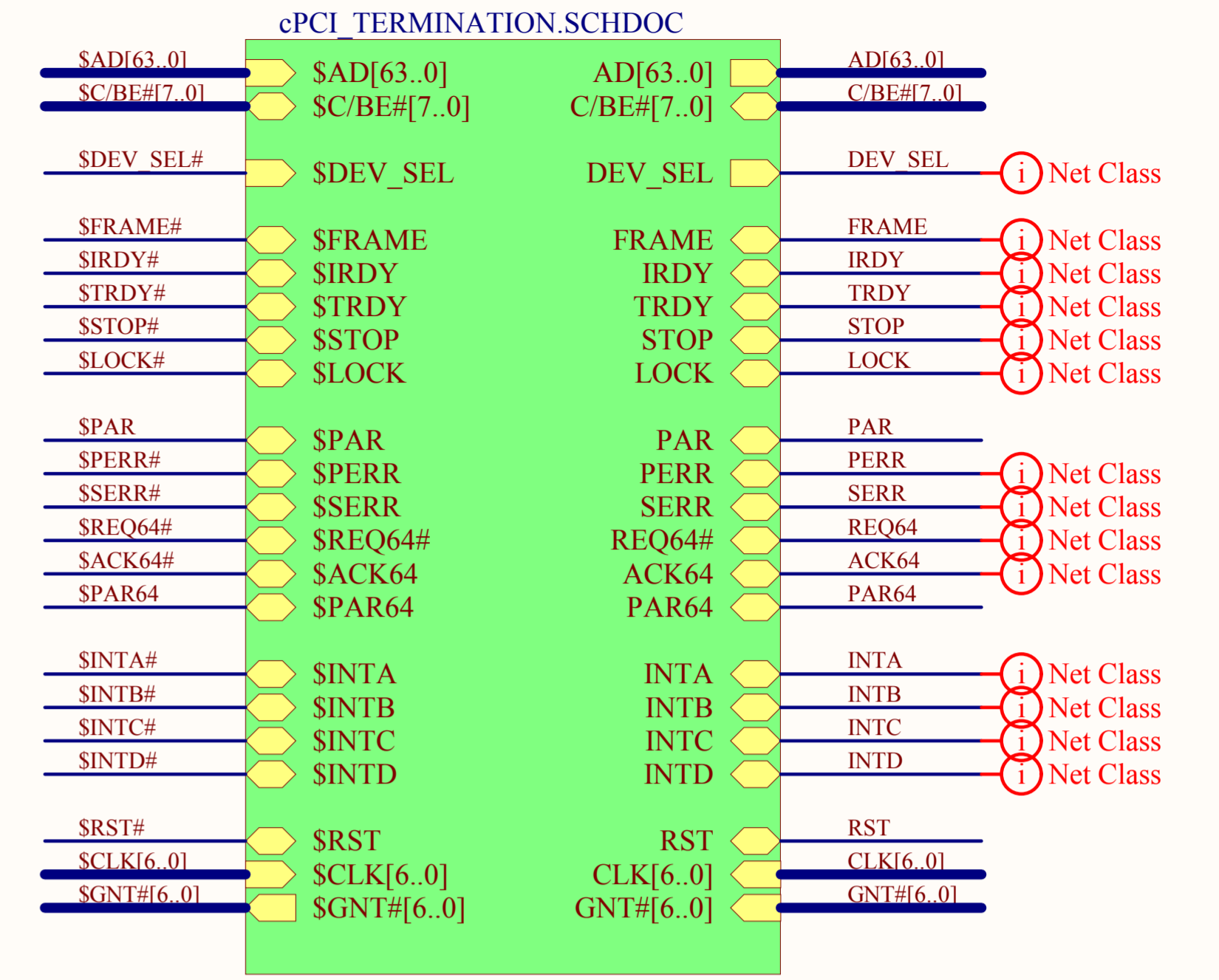
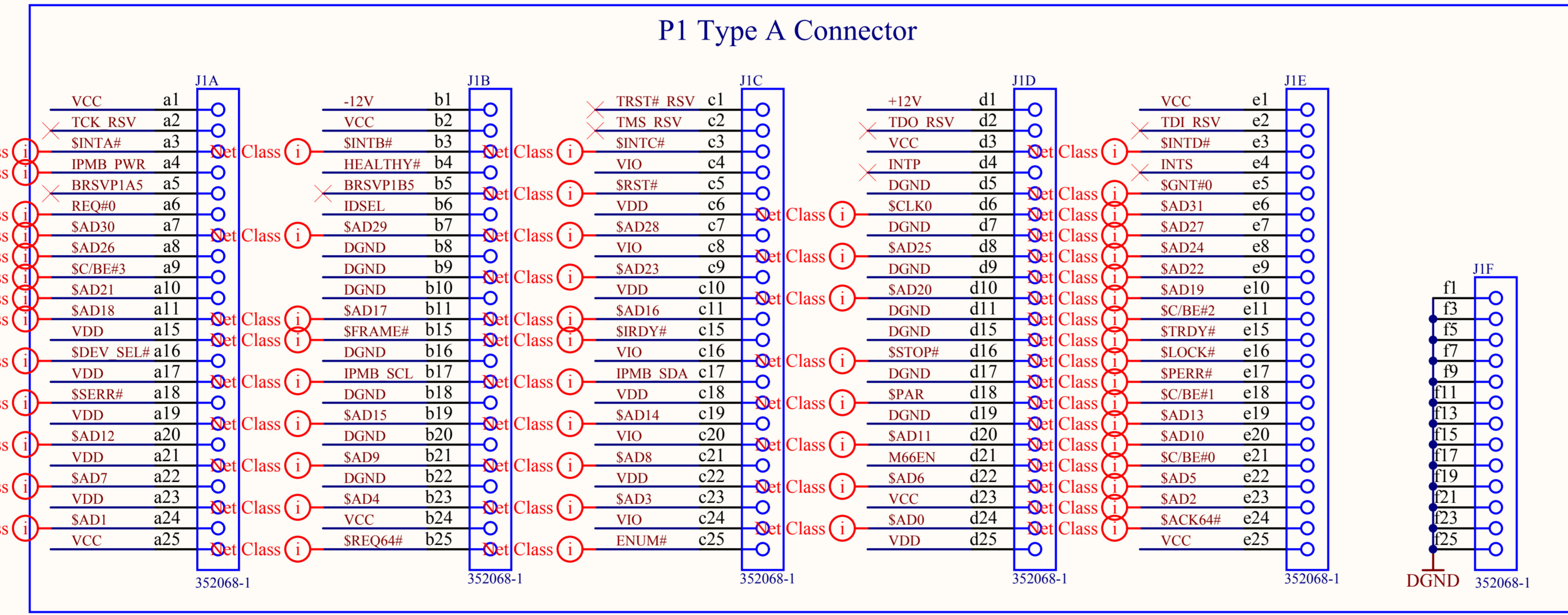
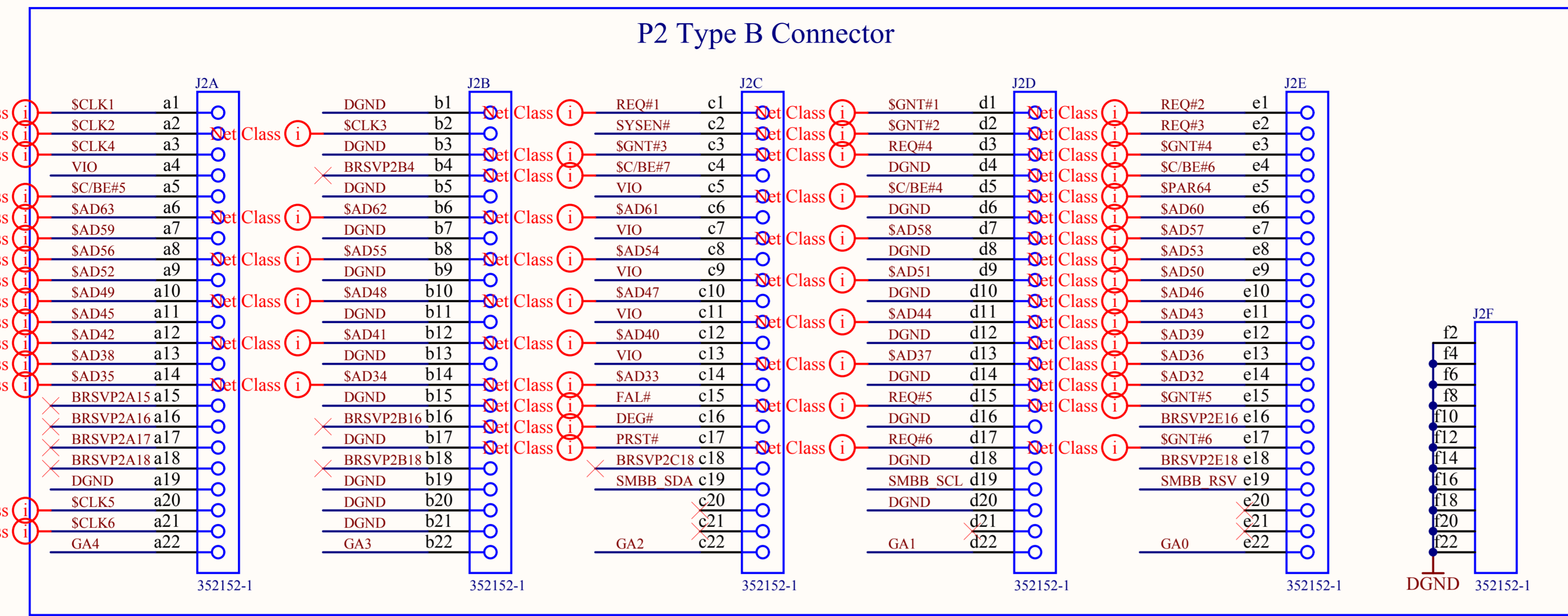
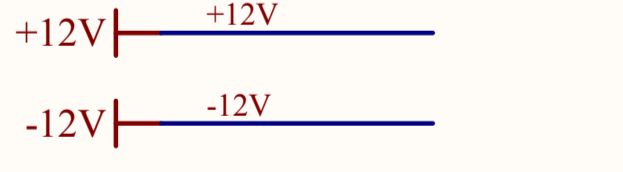
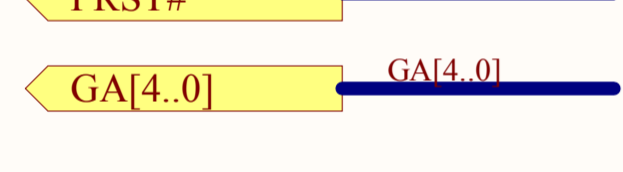
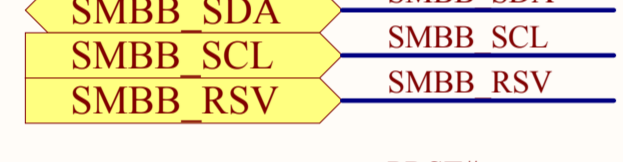
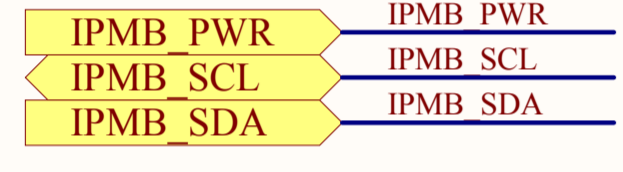
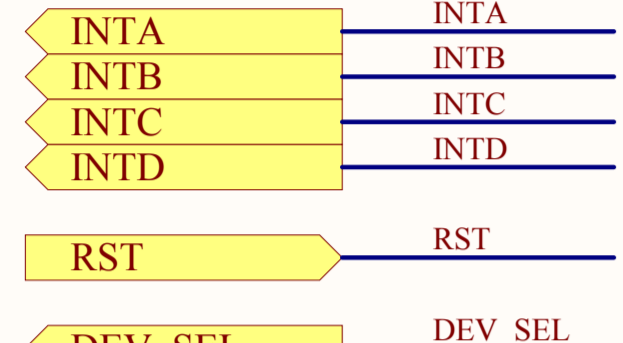
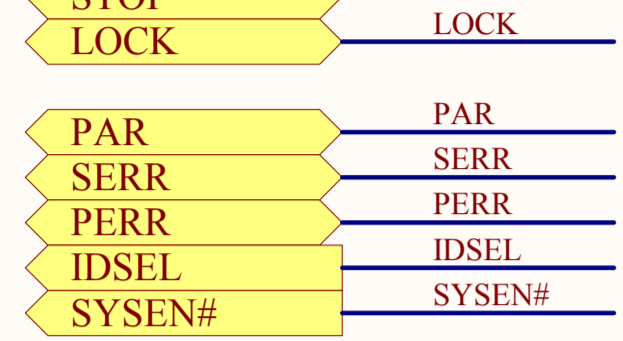
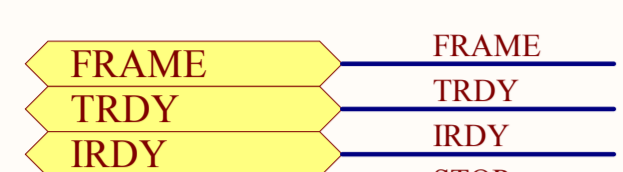
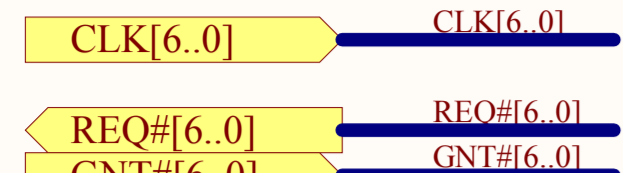
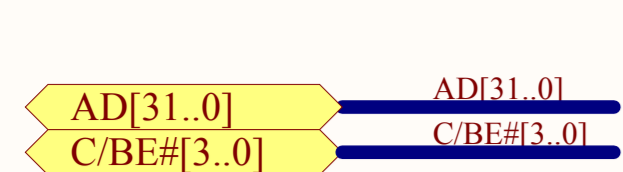


Title  
**256MB SDRAM**

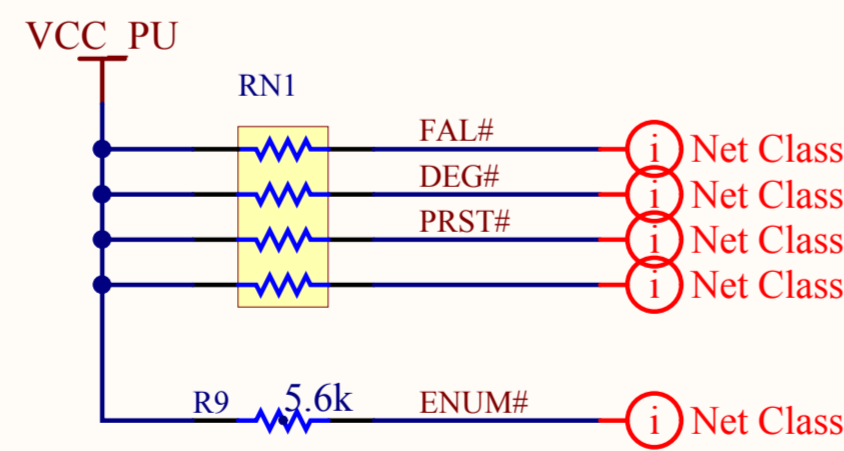
|        |                    |          |
|--------|--------------------|----------|
| Size   | Number             | Revision |
| Letter | QOR-PCIDSP-3-REV.1 | 1        |

|       |                            |                      |
|-------|----------------------------|----------------------|
| Date: | 9/2/2005                   | Sheet of             |
| File: | D:\Projects\..SDRAM.SchDoc | Drawn By: Brian Shea |





This is enabled when card is plugged into a system slot. Active Low Enable



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|  |                              |               |
|--|------------------------------|---------------|
| Title<br><b>cPCI Interface</b>               |                              |               |
| Size<br>Legal                                | Number<br>QOR-PCIDSP-6-REV.1 | Revision<br>1 |
| Date:<br>9/2/2005                            | Sheet of                     |               |
| File:<br>D:\Projects\...\cPCI_SysSlot.SCHDOC | Drawn By:<br>Brian Shea      |               |



5.6kohm Pull Up

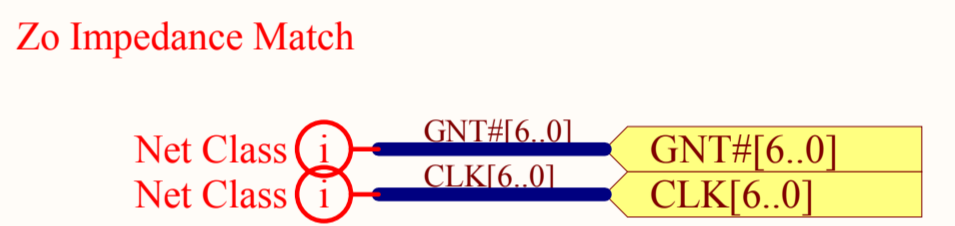
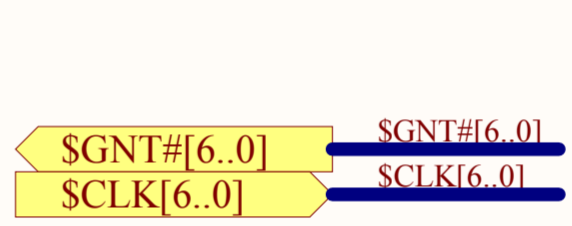
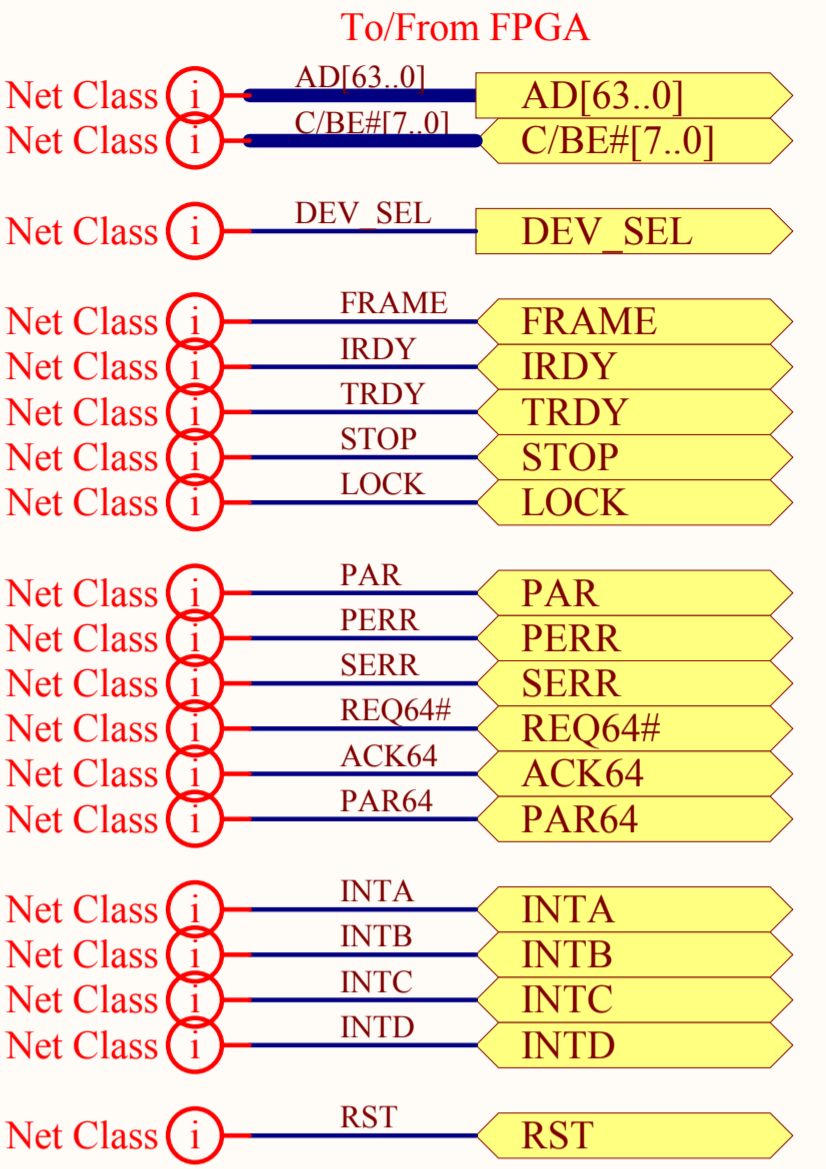
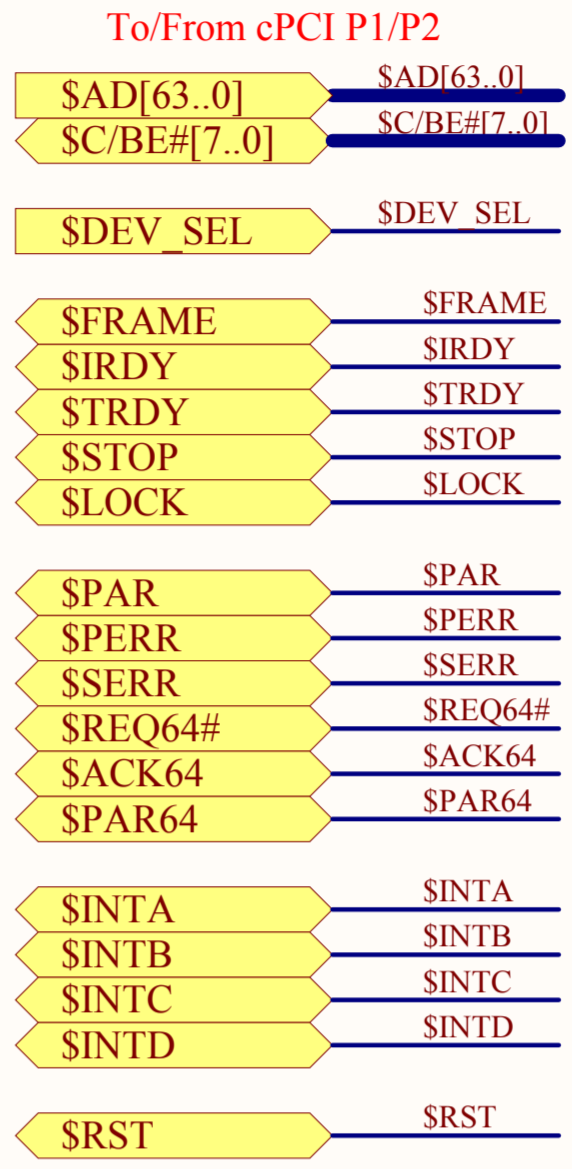
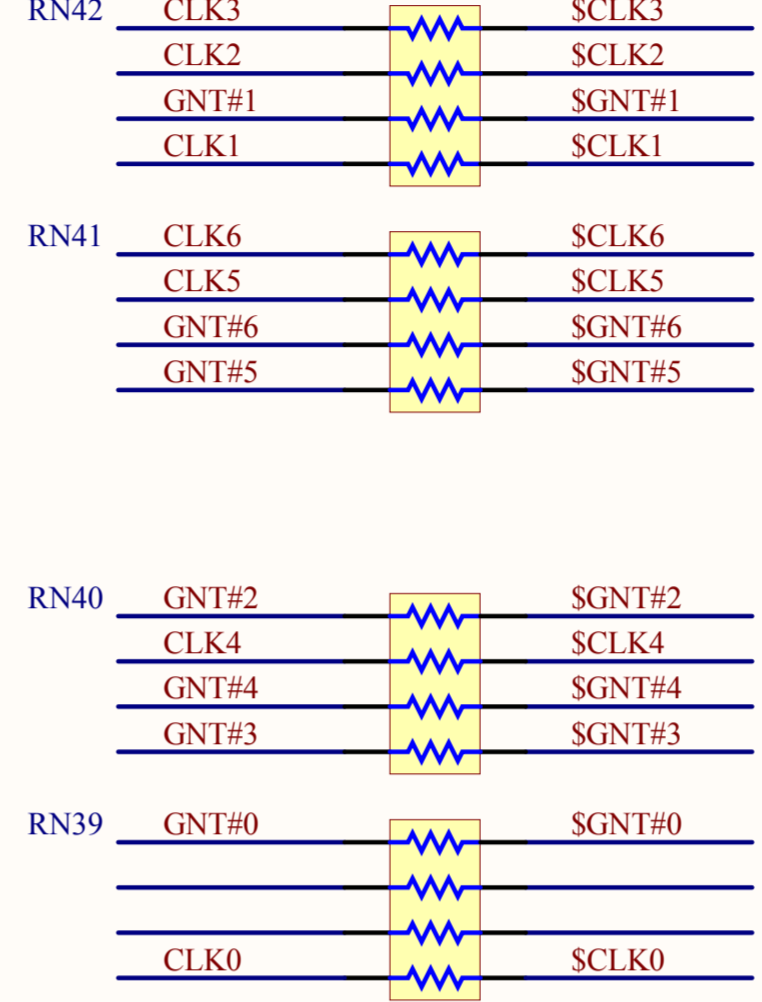
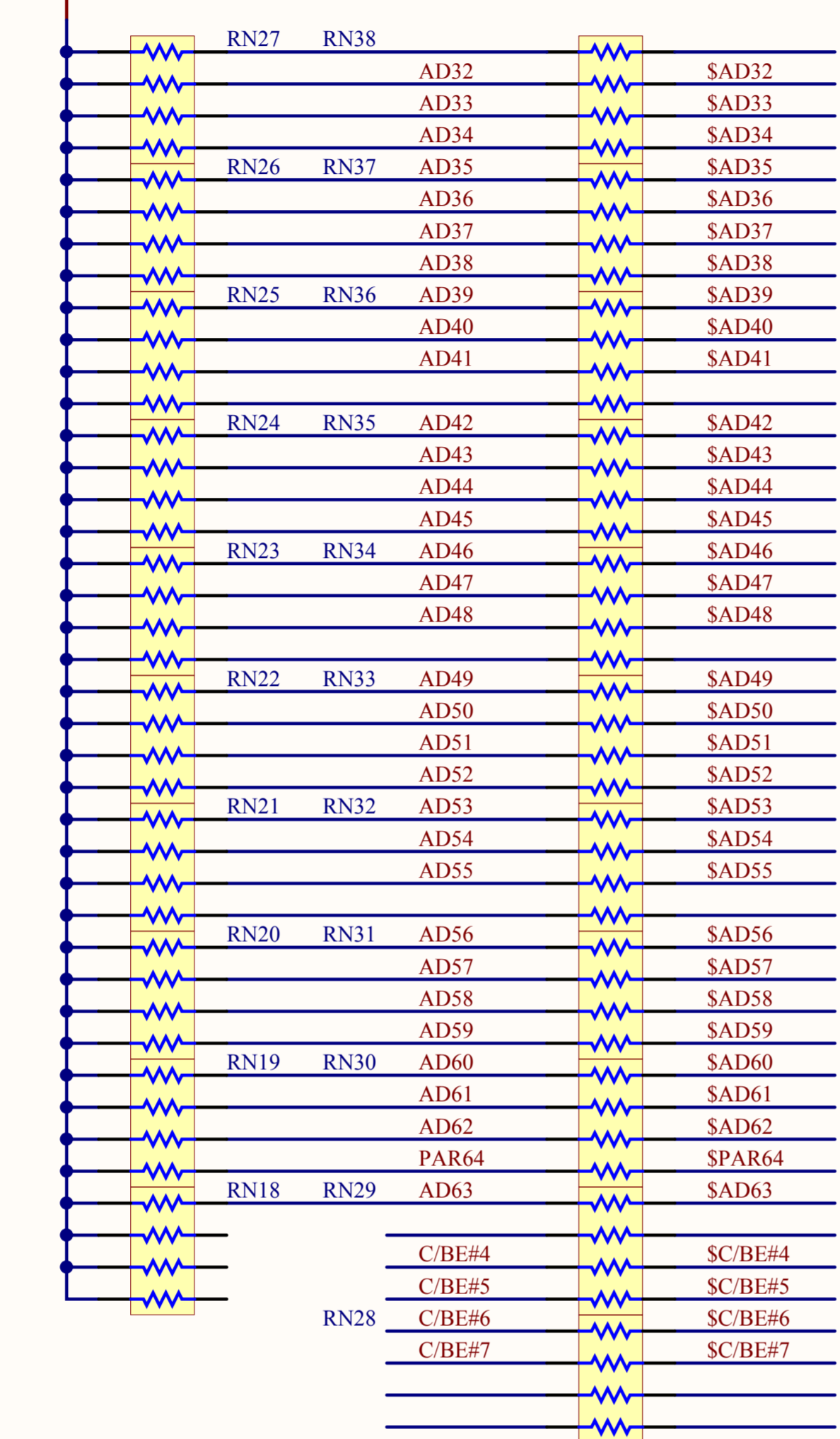
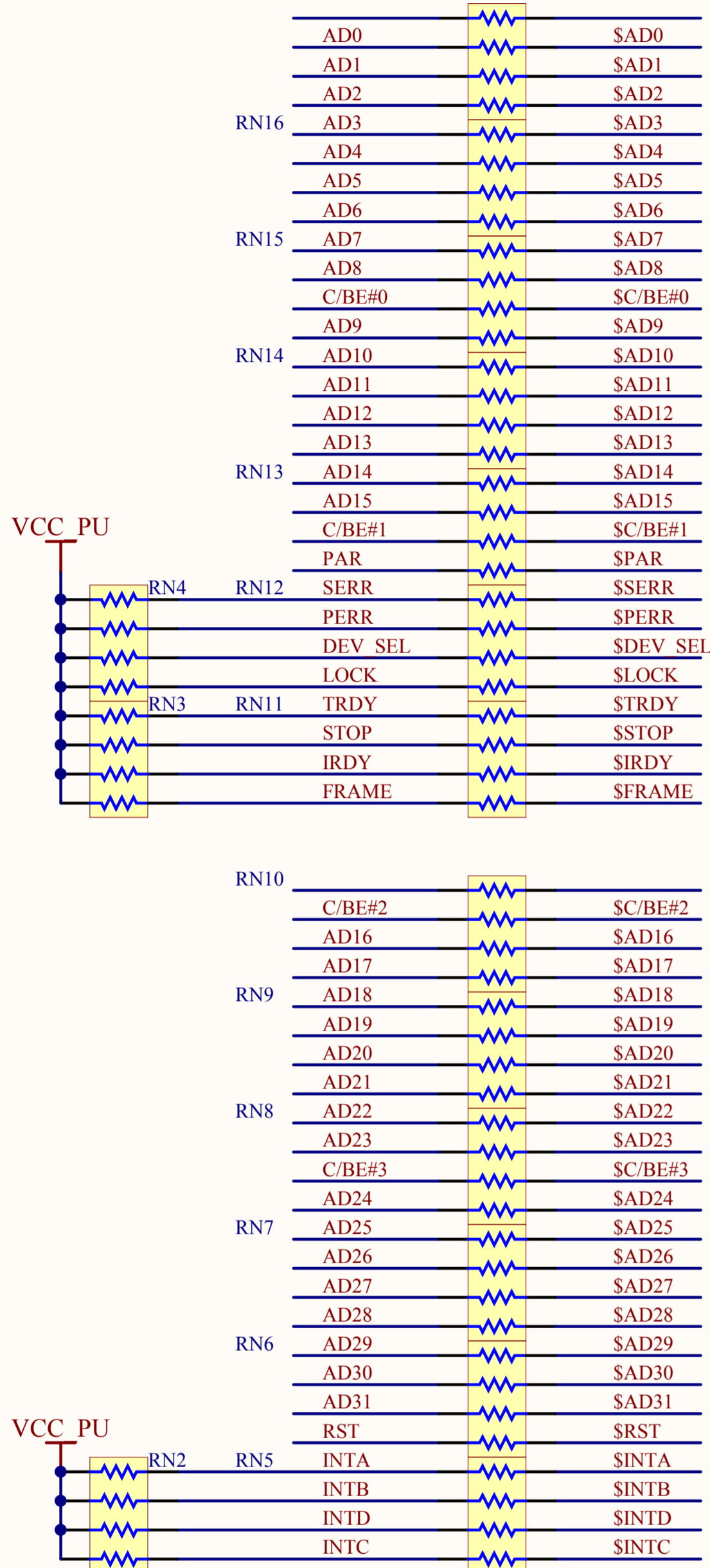
10ohm Stub Term

5.6kohm Pull Up

10ohm Stub Term

Zo Impedance Match

REQUIRED Termination  
10ohm Stub Term



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Title  
cPCI Terminators and Pull Up Resistor Networks

Size  
Legal

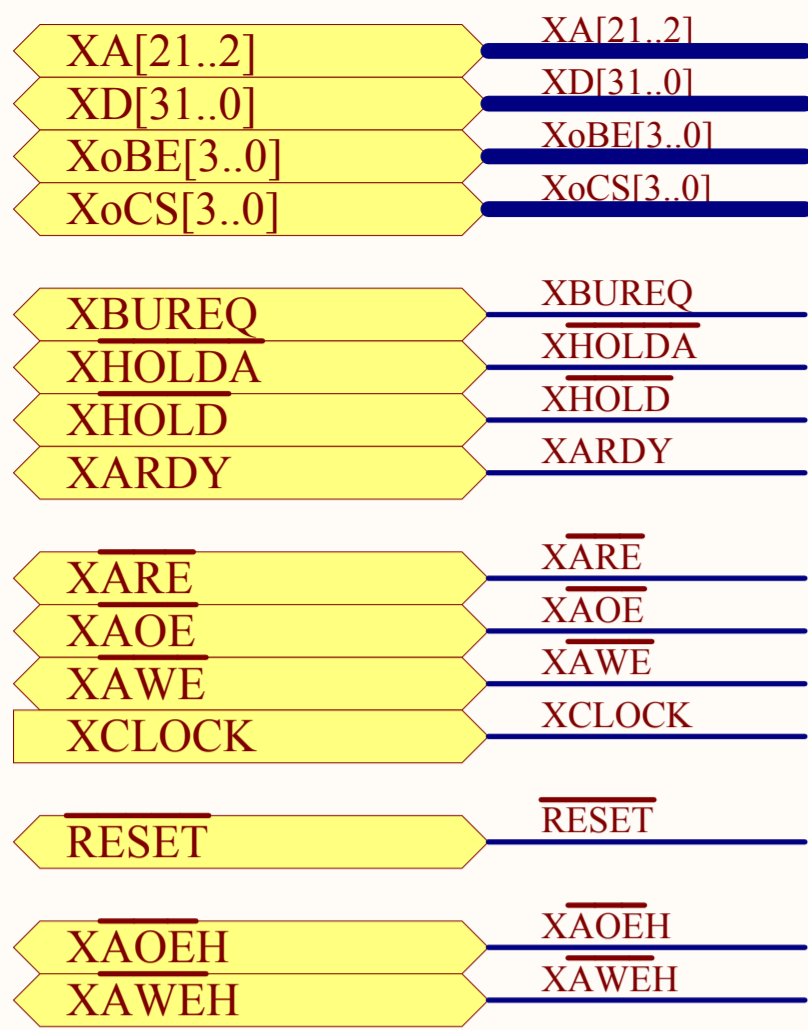
Number  
QOR-cPCIDSP-7-REV.1

Revision  
1

Date: 9/2/2005  
File: D:\Projects\cPCI\_TERMINATION.SCH

Sheet of  
16  
Drawn By: Brian Shea

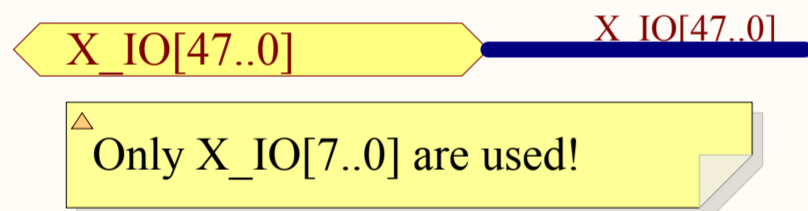
DSP XINTF



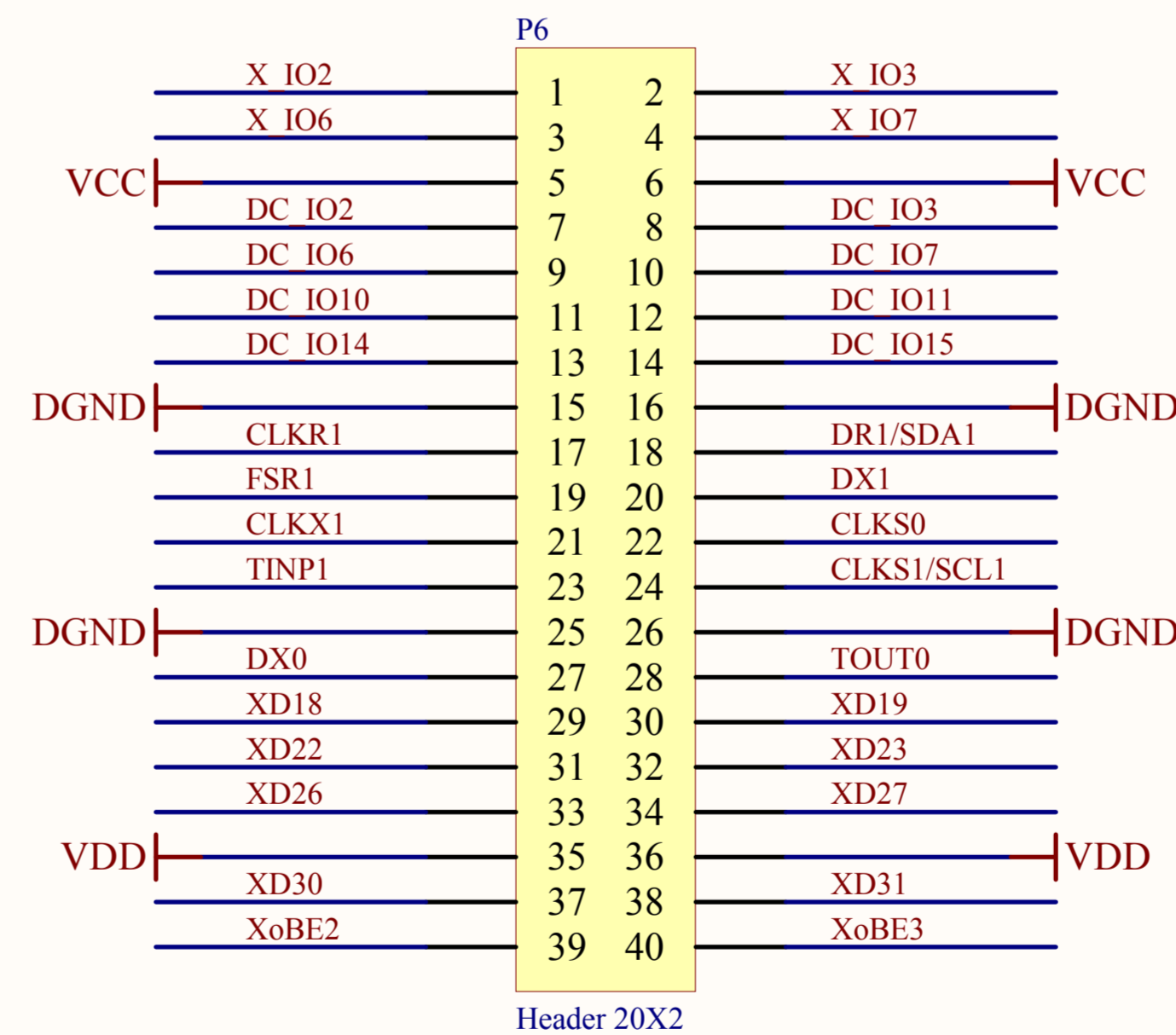
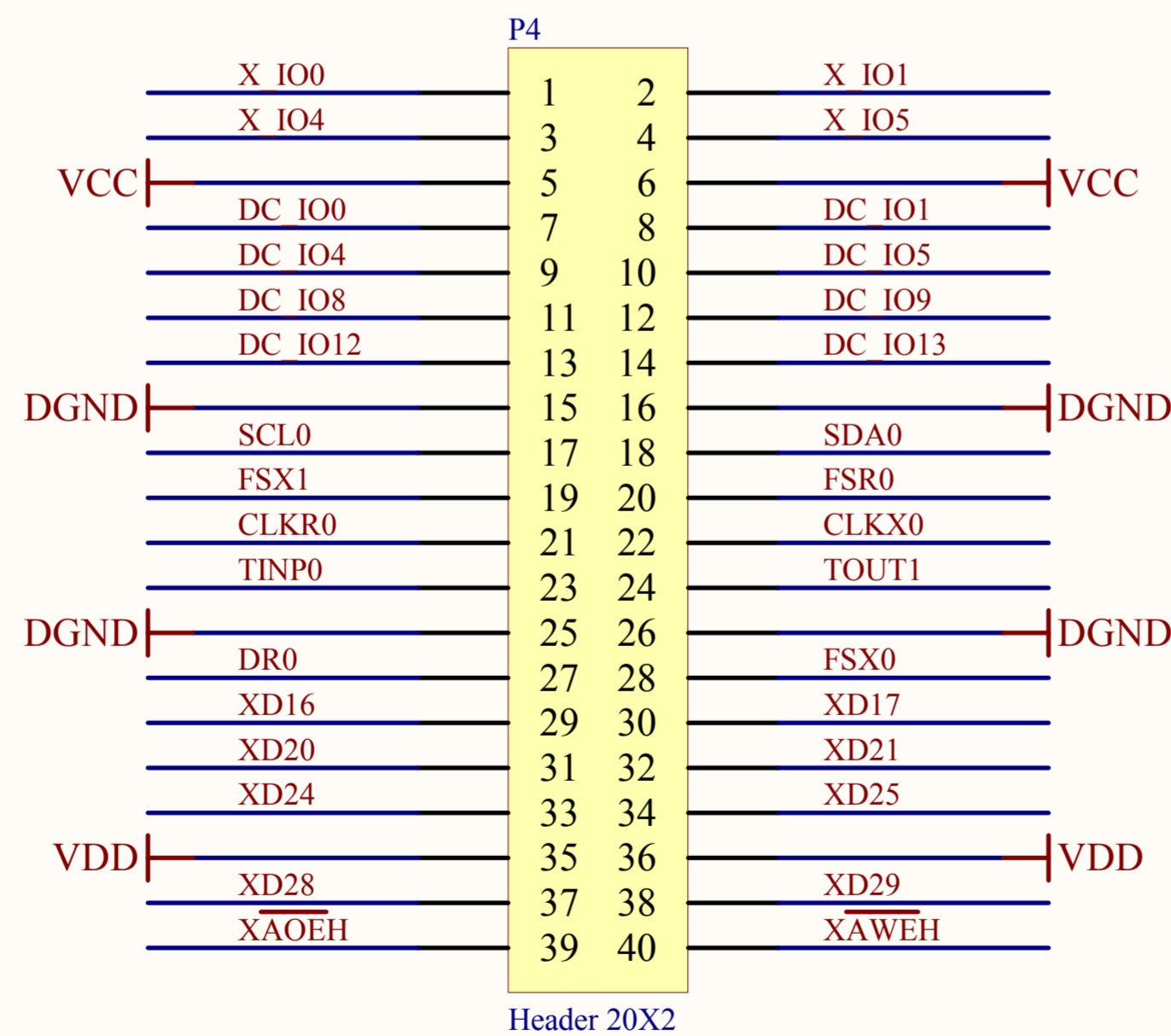
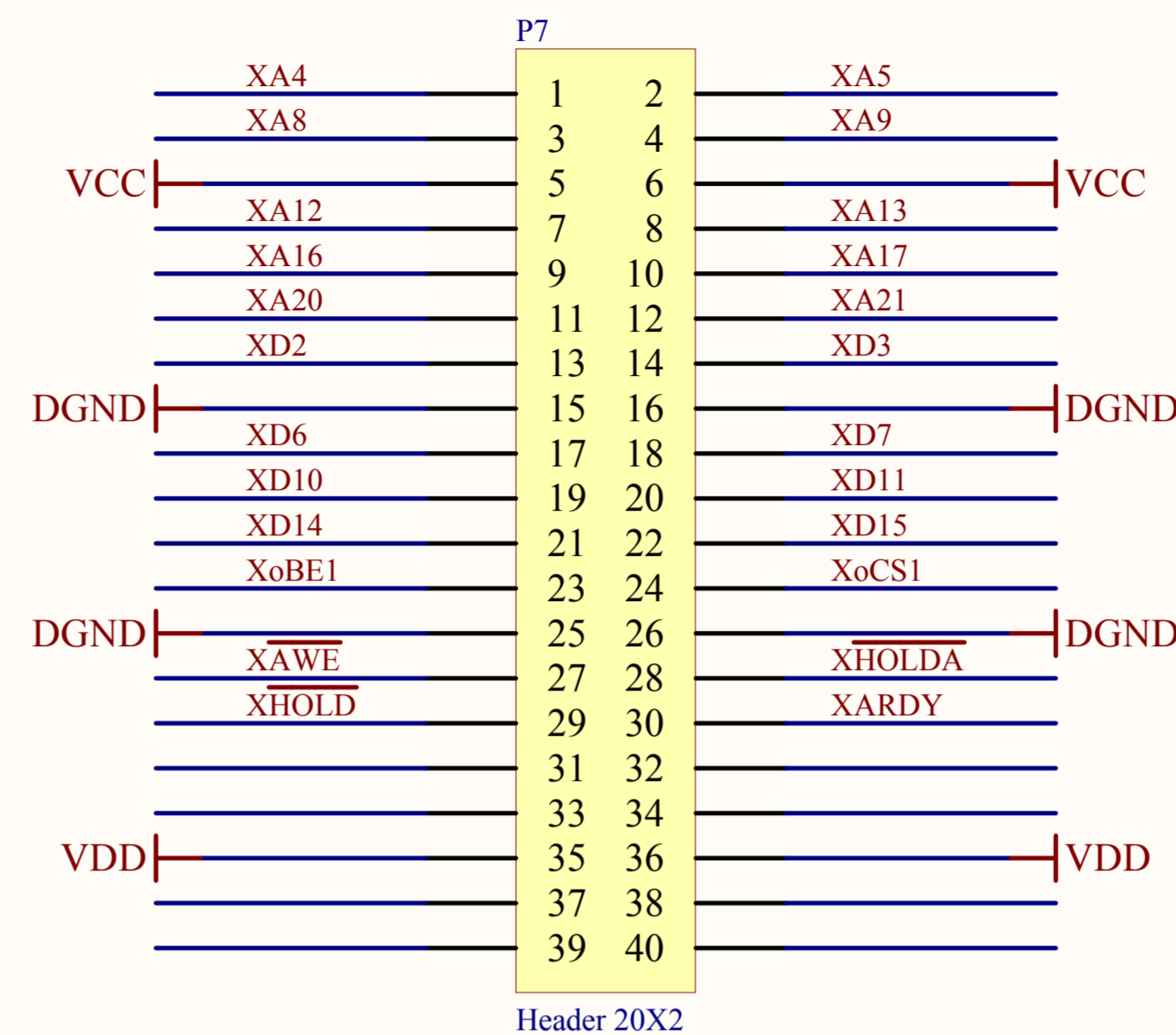
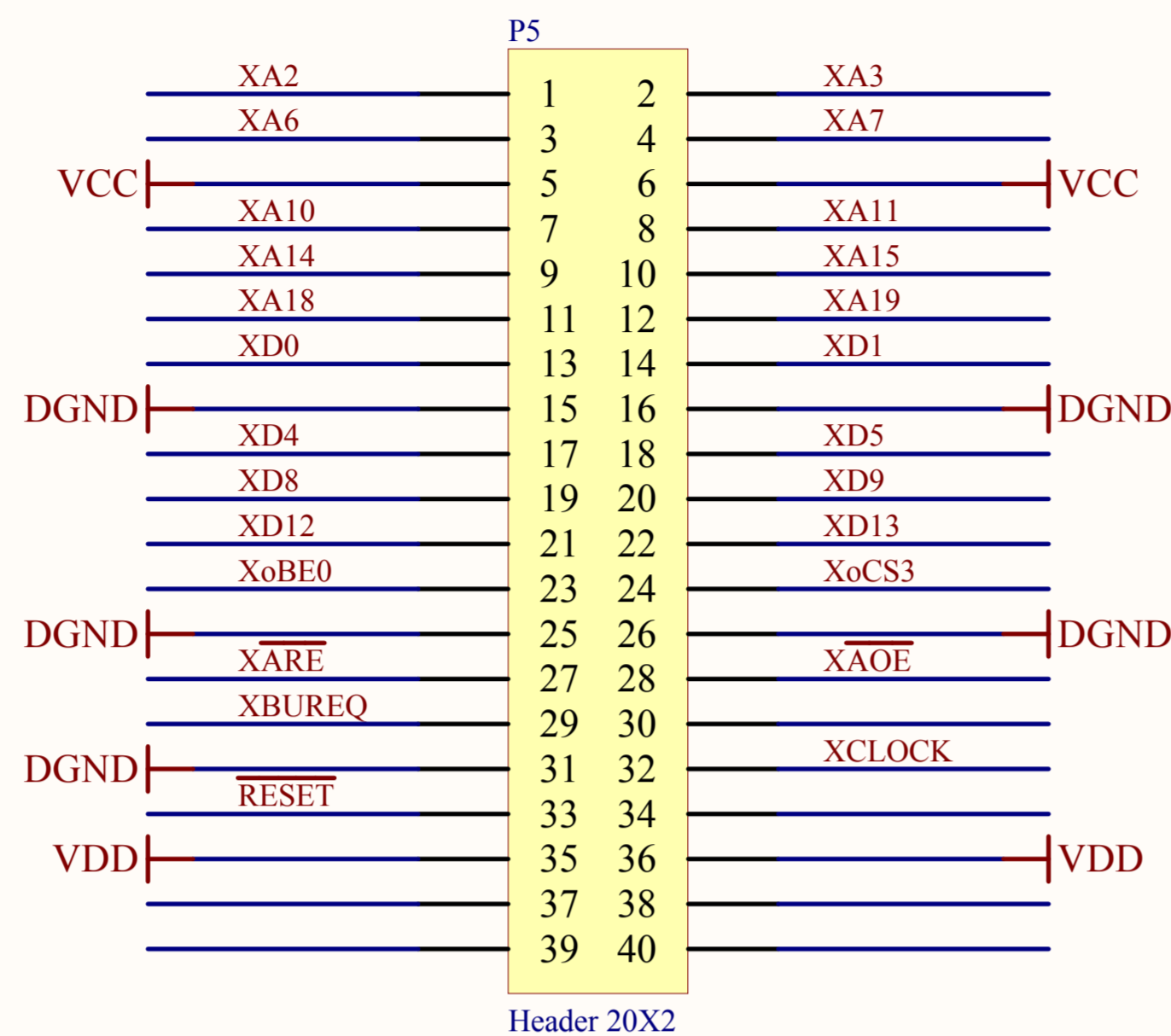
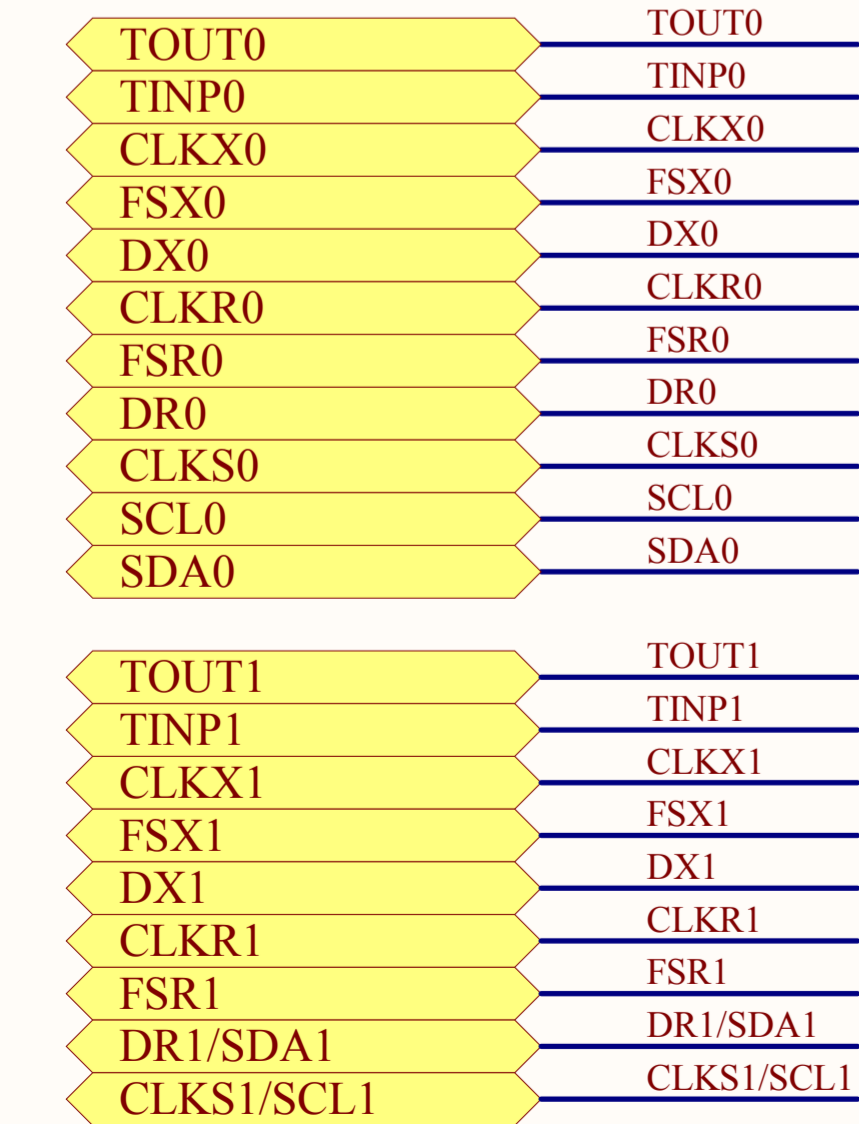
GPIO To Daughter Card



GPIO HD 68Pin Conn



DSP GPIO



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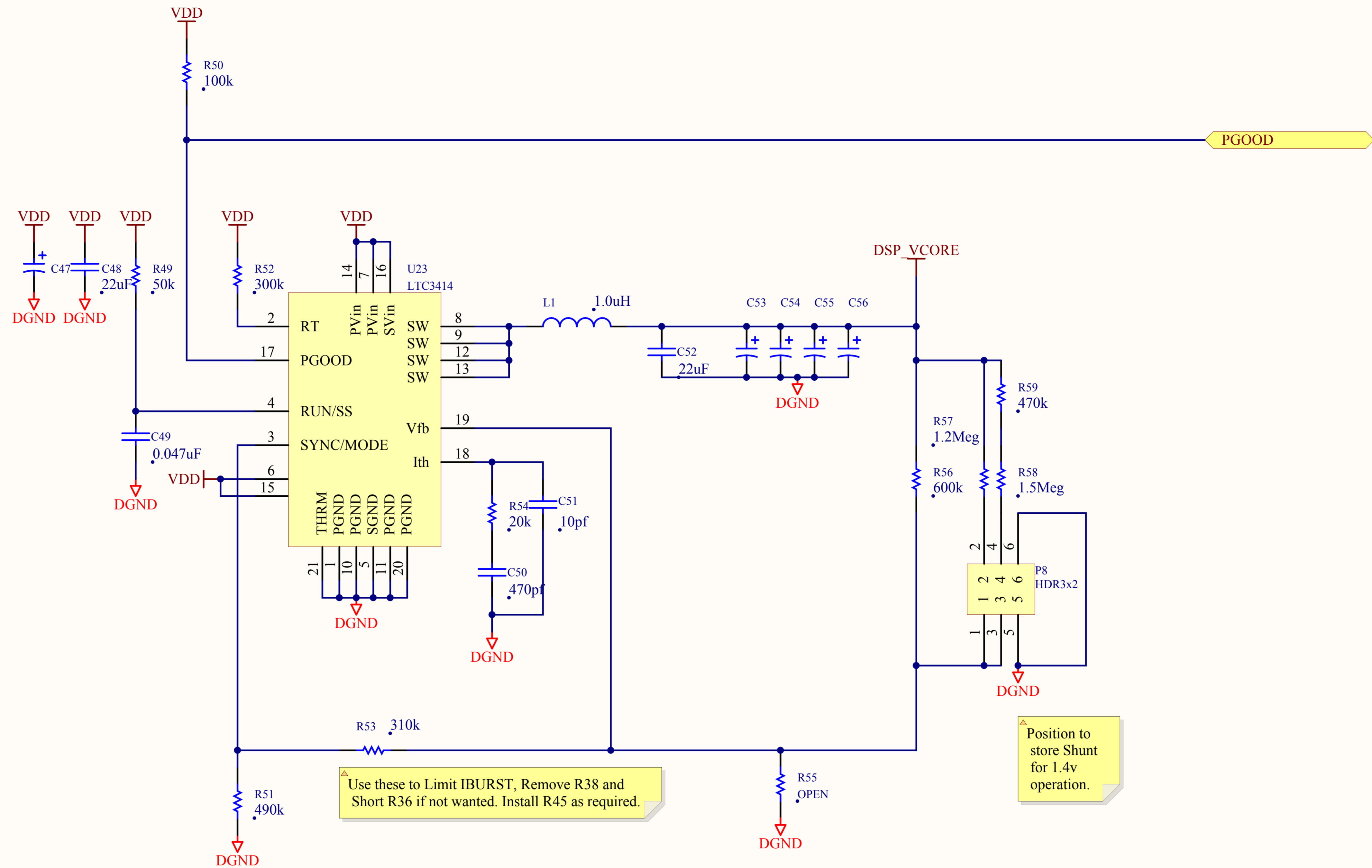
Address  
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|   |                                |                         |
|---|--------------------------------|-------------------------|
| Title<br><b>Daughter Card Interface</b>         |                                |                         |
| Size<br>Letter                                  | Number<br>QOR-cPCIDSP-11-REV.1 | Revision<br>REV 1       |
| Date:<br>9/2/2005                               | Sheet of                       | Drawn By: Brian G. Shea |
| File:<br>D:\Projects\...\DaughterCard_IF.SchDoc |                                |                         |



△ DSP Core voltage range: 1.2 to 1.4v



△ Use these to Limit IBURST, Remove R38 and Short R36 if not wanted. Install R45 as required.

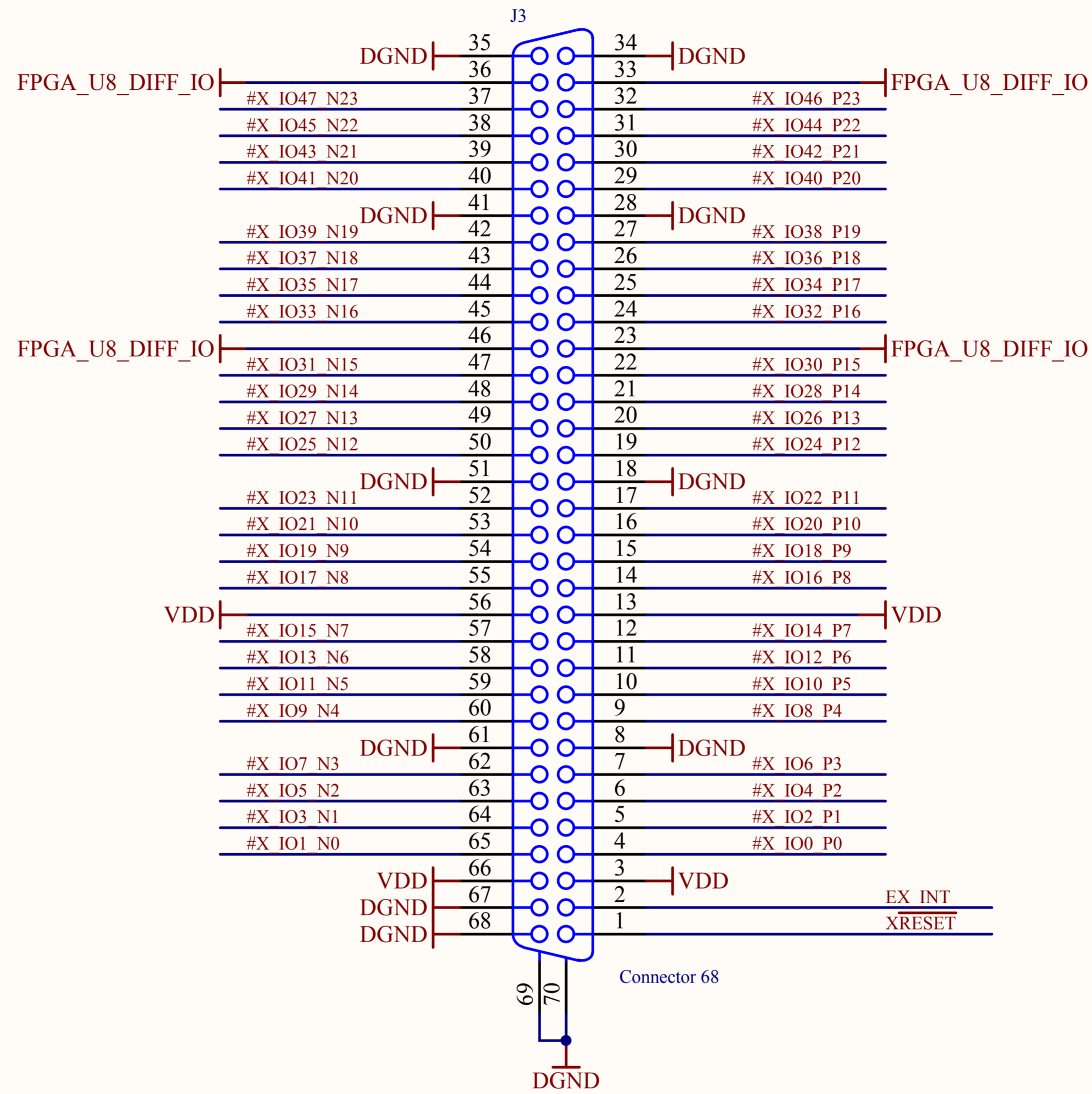
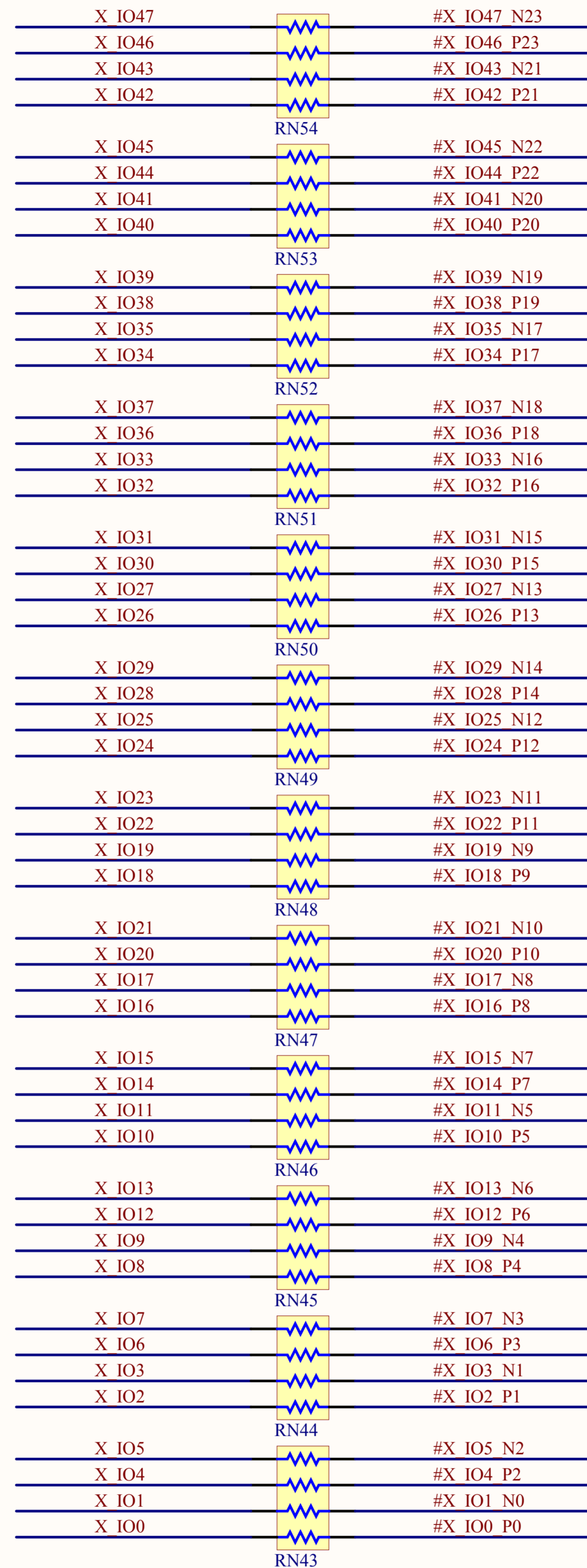
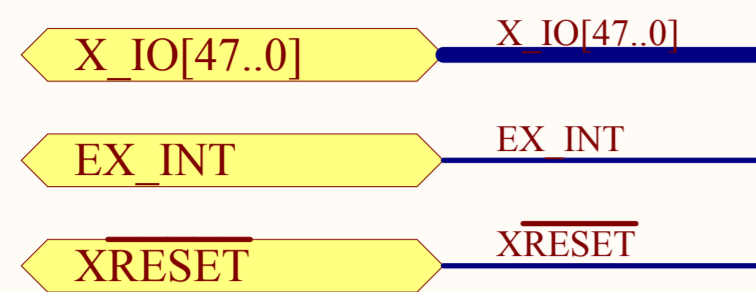
△ Position to store Shunt for 1.4v operation.

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|  |                               |               |
|--|-------------------------------|---------------|
| Title<br>DSP Core Voltage Supply                 |                               |               |
| Size<br>Letter                                   | Number<br>QOR-PCIDSP-17-REV.1 | Revision<br>1 |
| Date:<br>9/2/2005                                | Sheet of                      |               |
| File:<br>D:\Projects\...\DSPCORE_PowerSupply.Sch | Drawn By:<br>Brian Shea       |               |

GPIO HD 68Pin Conn



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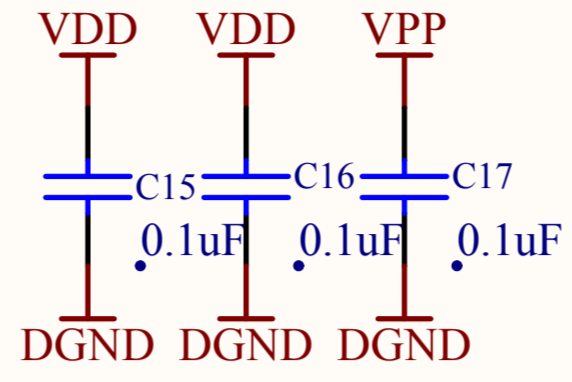
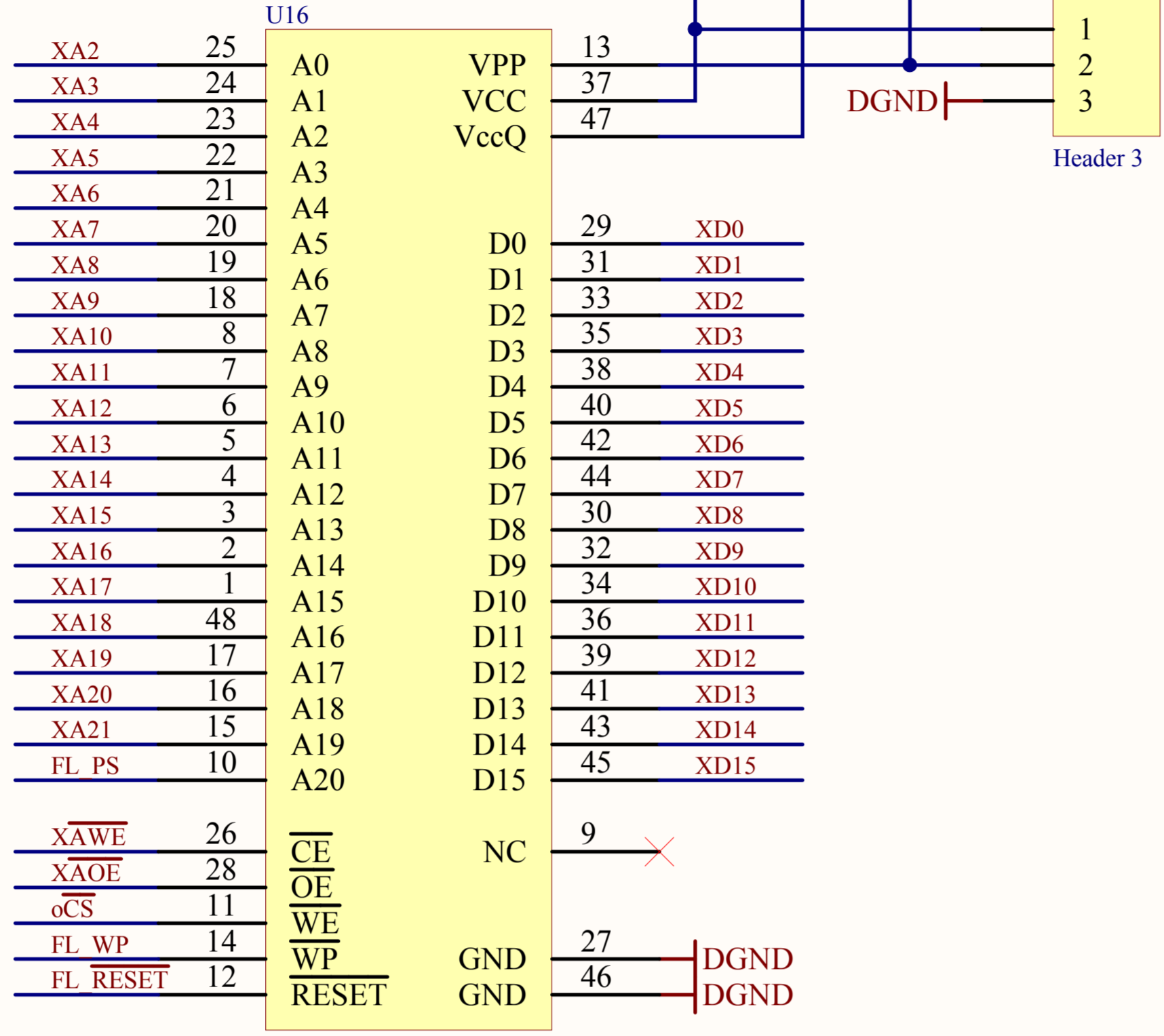
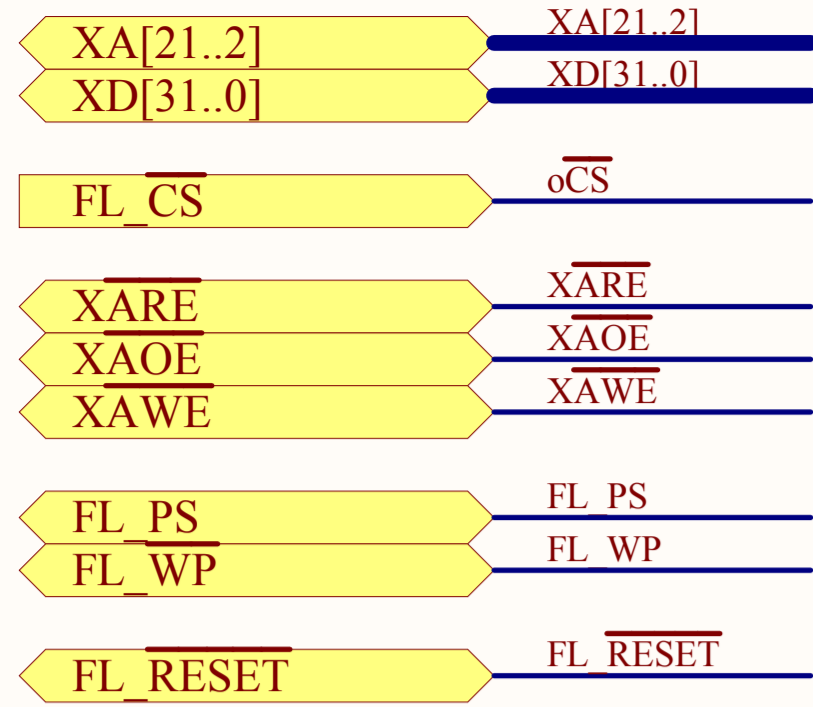
Address  
 1965 Lycoming Creek Rd  
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Title  
**External IO Terminators and Connector**

|        |                                    |                      |
|--------|------------------------------------|----------------------|
| Size   | Number                             | Revision             |
| Letter | QOR-cPCIDSP-10-REV.1               | 1                    |
| Date:  | 9/2/2005                           | Sheet of             |
| File:  | D:\Projects\...\External_IO.SchDoc | Drawn By: Brian Shea |





**AT49BV320C-70TI**

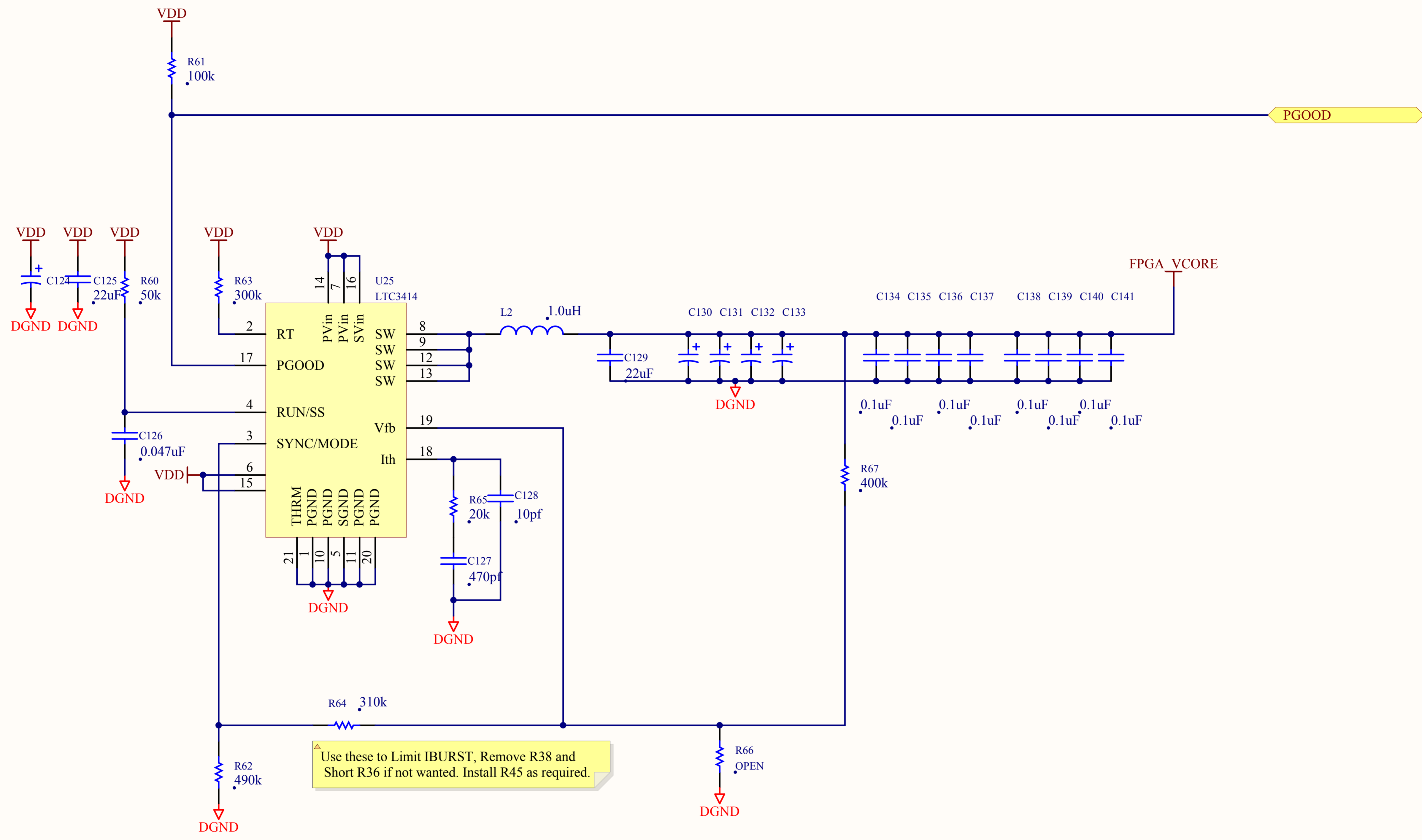
Flash Memory is divided into two pages, the first page (Page 0) should be used to store the user boot loader and program. The second page can be used to store any other data such as system settings, rom tables, or additional program code. It should be noted that accessing the second page (page 1) will require a write to a register to select the flash page. Also, the flash can be disabled through a register allowing the daughter card to have the entire CS1/CS3 memory range.

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|   |                               |                      |
|---|-------------------------------|----------------------|
| Title<br><b>64kB Flash Rom</b>              |                               |                      |
| Size<br>Letter                              | Number<br>QOR-cPCIDSP-8-REV.1 | Revision<br>1        |
| Date:<br>9/2/2005                           | Sheet of                      | Drawn By: Brian Shea |
| File:<br>D:\Projects\...\FlashMemory.SchDoc |                               |                      |



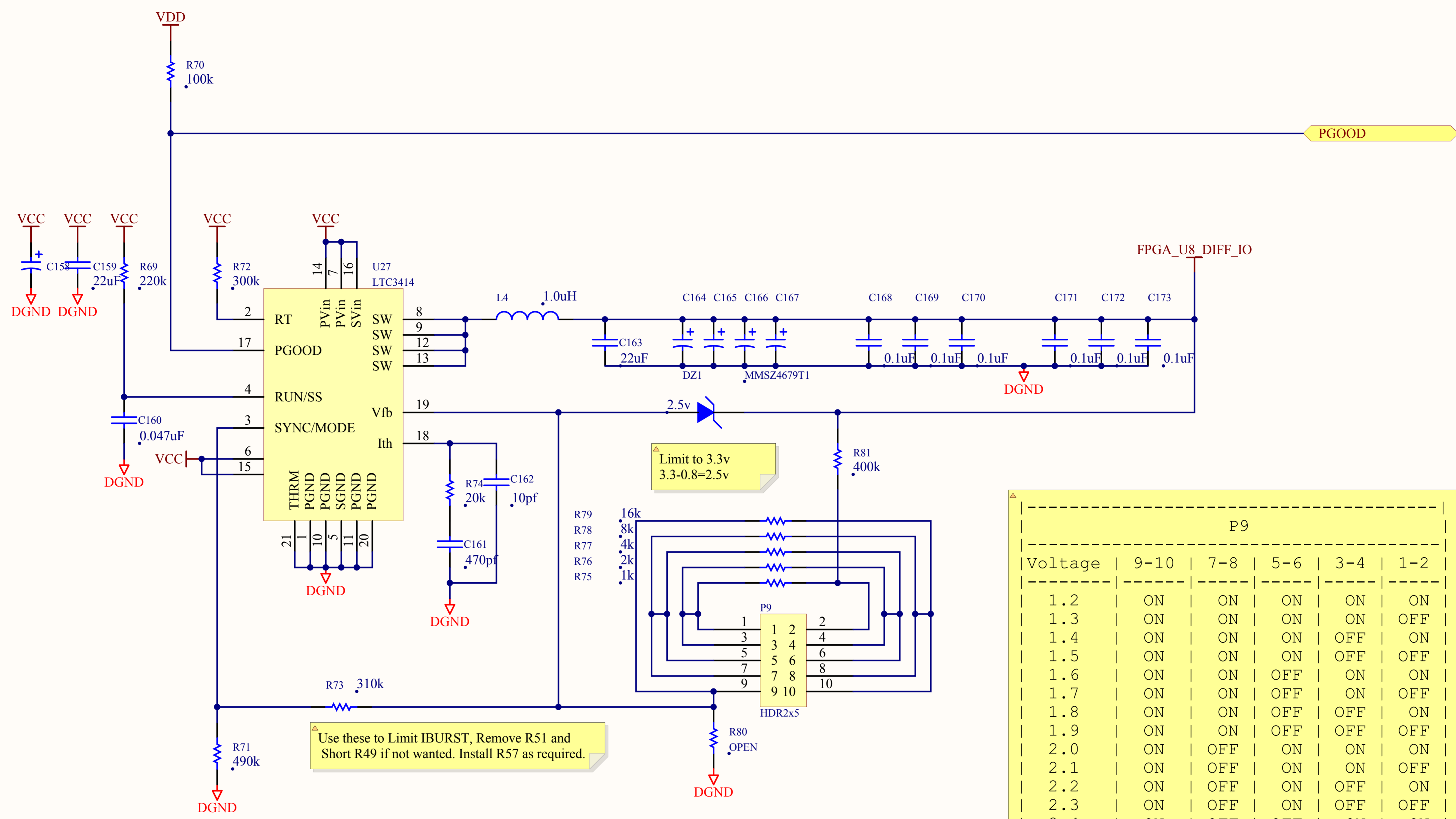
Use these to Limit IBURST, Remove R38 and Short R36 if not wanted. Install R45 as required.

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|  |                               |               |
|--|-------------------------------|---------------|
| Title<br>FPGA Core Voltage Supply            |                               |               |
| Size<br>Letter                               | Number<br>QOR-PCIDSP-19-REV.1 | Revision<br>1 |
| Date:<br>9/2/2005                            | Sheet of                      |               |
| File:<br>D:\Projects\..FPGA_CORE_PowerSupply | Drawn By: Brian Shea          |               |





Use these to Limit IBURST, Remove R51 and Short R49 if not wanted. Install R57 as required.

Limit to 3.3v  
3.3-0.8=2.5v

| P9      |      |     |     |     |     |
|---------|------|-----|-----|-----|-----|
| Voltage | 9-10 | 7-8 | 5-6 | 3-4 | 1-2 |
| 1.2     | ON   | ON  | ON  | ON  | ON  |
| 1.3     | ON   | ON  | ON  | ON  | OFF |
| 1.4     | ON   | ON  | ON  | OFF | ON  |
| 1.5     | ON   | ON  | ON  | OFF | OFF |
| 1.6     | ON   | ON  | OFF | ON  | ON  |
| 1.7     | ON   | ON  | OFF | ON  | OFF |
| 1.8     | ON   | ON  | OFF | OFF | ON  |
| 1.9     | ON   | ON  | OFF | OFF | OFF |
| 2.0     | ON   | OFF | ON  | ON  | ON  |
| 2.1     | ON   | OFF | ON  | ON  | OFF |
| 2.2     | ON   | OFF | ON  | OFF | ON  |
| 2.3     | ON   | OFF | ON  | OFF | OFF |
| 2.4     | ON   | OFF | OFF | ON  | ON  |
| 2.5     | ON   | OFF | OFF | ON  | OFF |
| 2.6     | ON   | OFF | OFF | OFF | ON  |
| 2.7     | ON   | OFF | OFF | OFF | OFF |
| 2.8     | OFF  | ON  | ON  | ON  | ON  |
| 2.9     | OFF  | ON  | ON  | ON  | OFF |
| 3.0     | OFF  | ON  | ON  | OFF | ON  |
| 3.1     | OFF  | ON  | ON  | OFF | OFF |
| 3.2     | OFF  | ON  | OFF | ON  | ON  |
| 3.3     | OFF  | ON  | OFF | ON  | OFF |

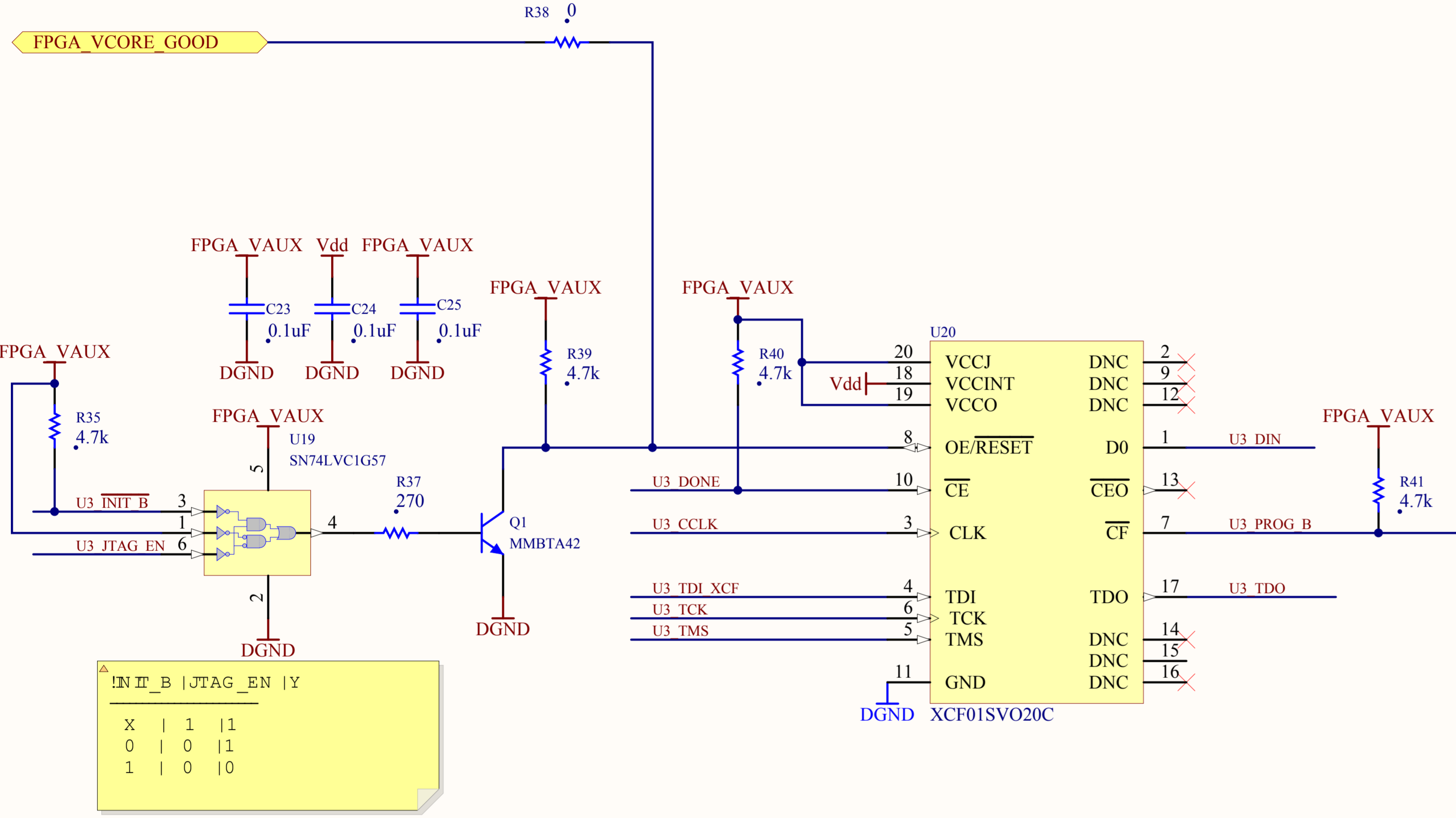
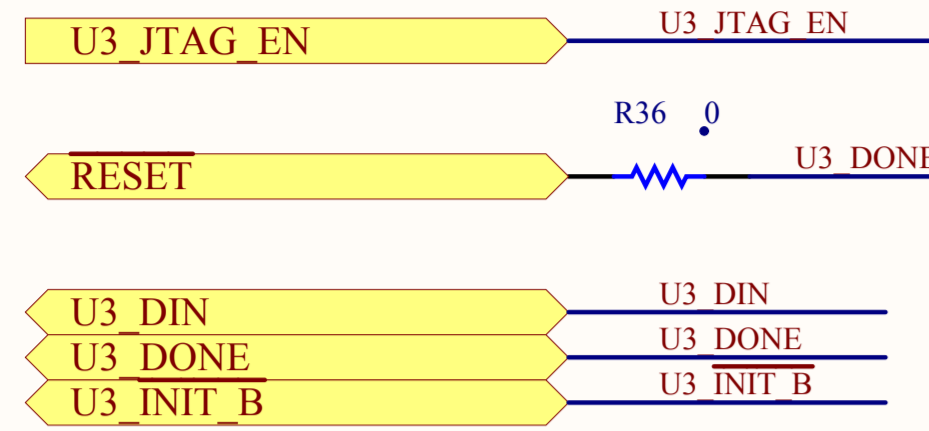
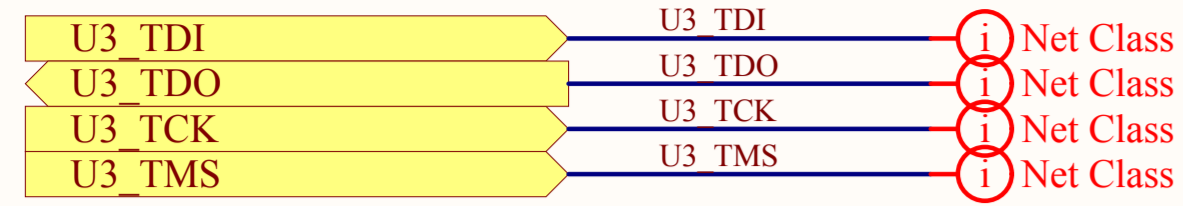
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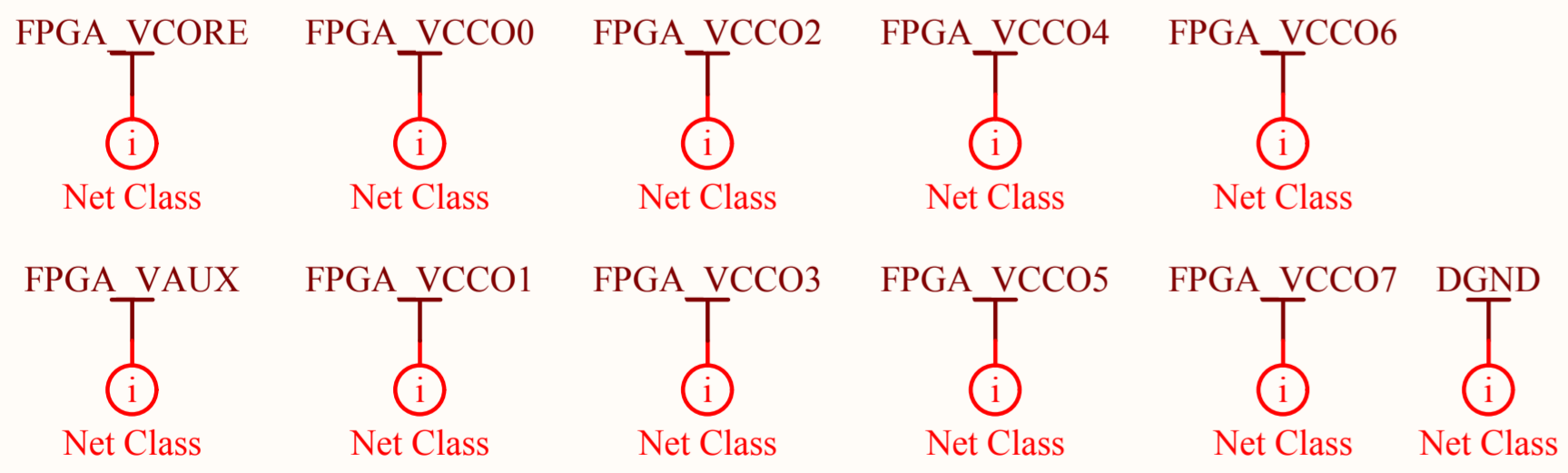
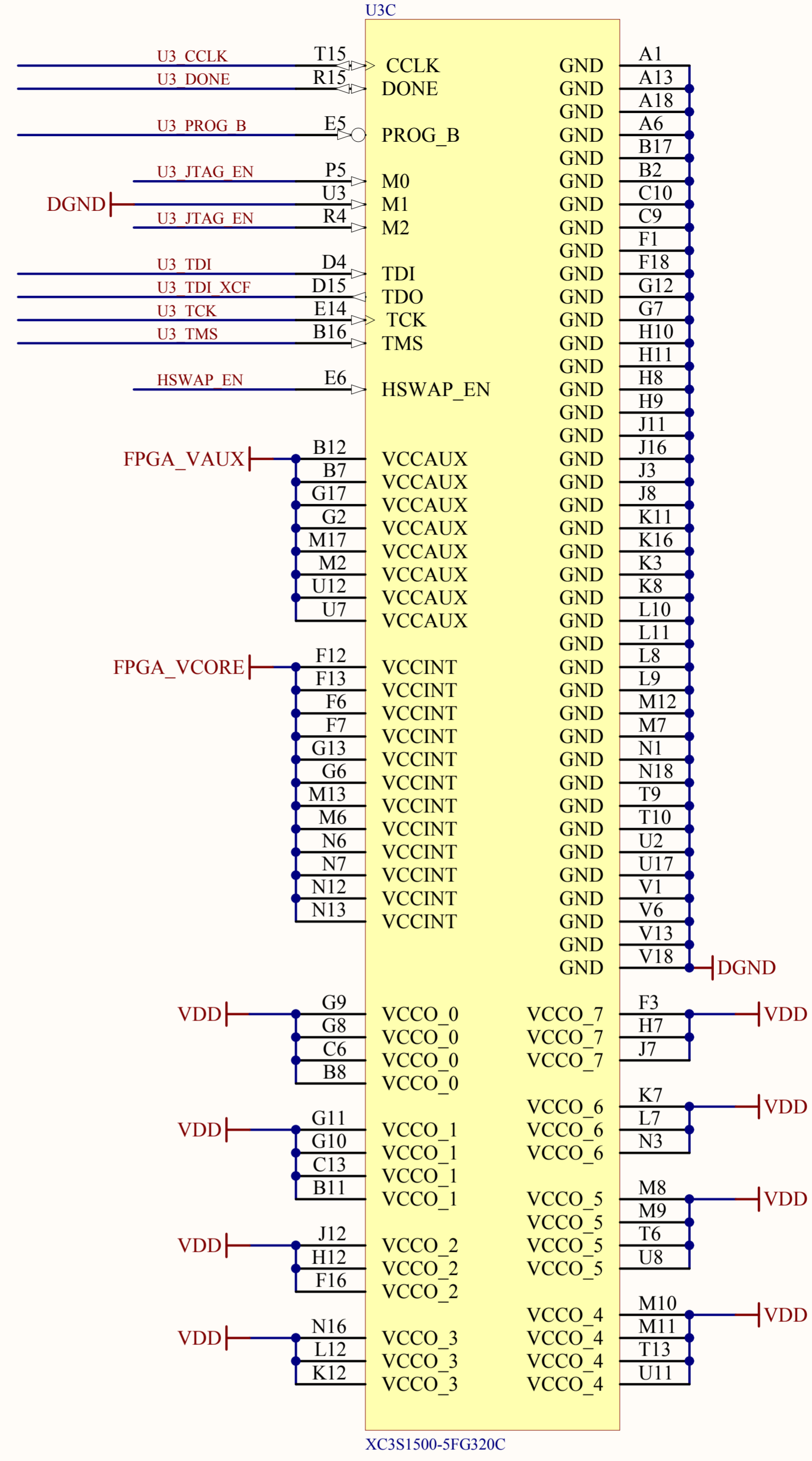
Title  
**FPGA Differential IO Power Supply**

|        |                     |          |
|--------|---------------------|----------|
| Size   | Number              | Revision |
| Letter | QOR-PCIDSP-18-REV.1 | 1        |

Date: 9/2/2005  
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 Sheet of  
 Drawn By: Brian Shea

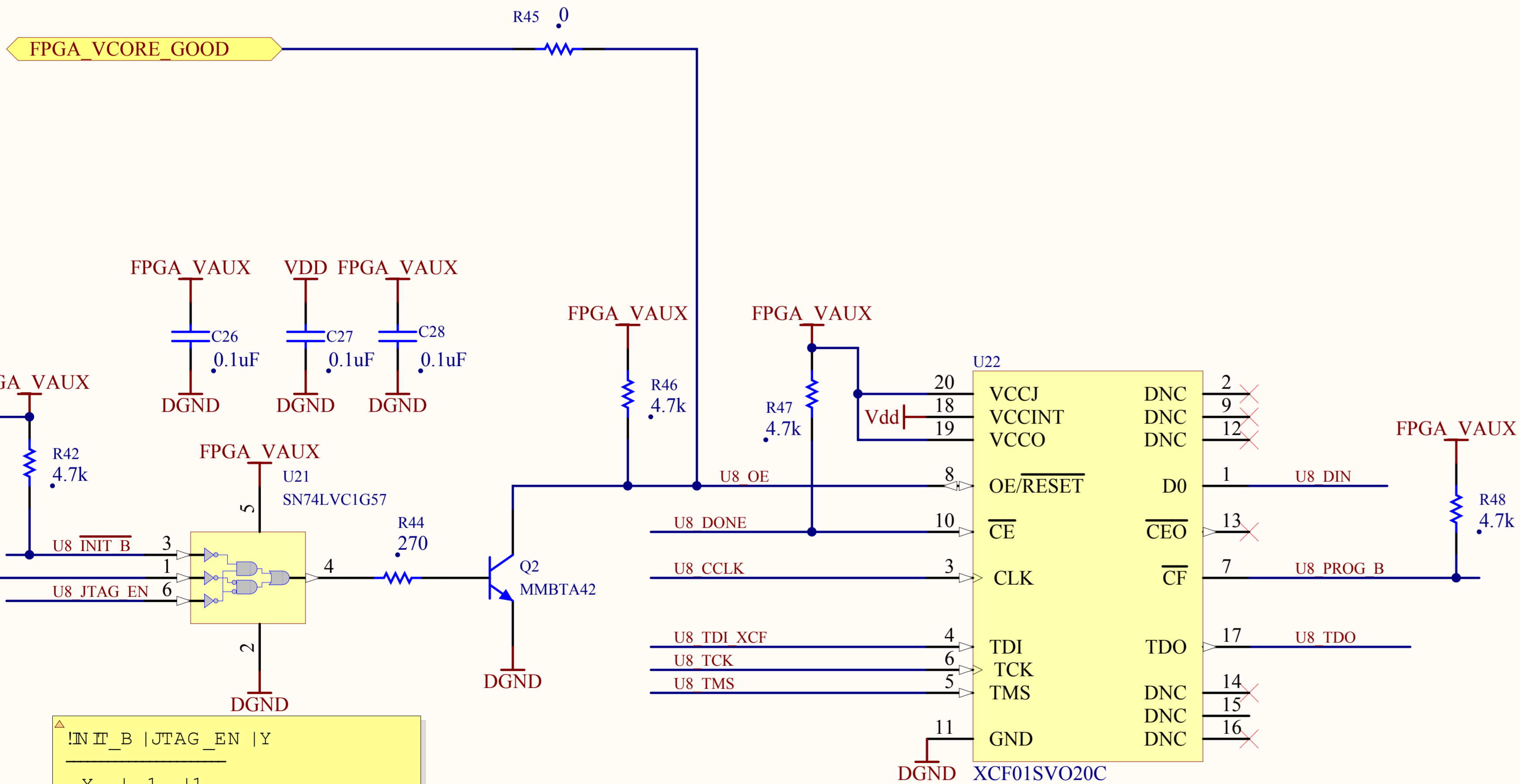
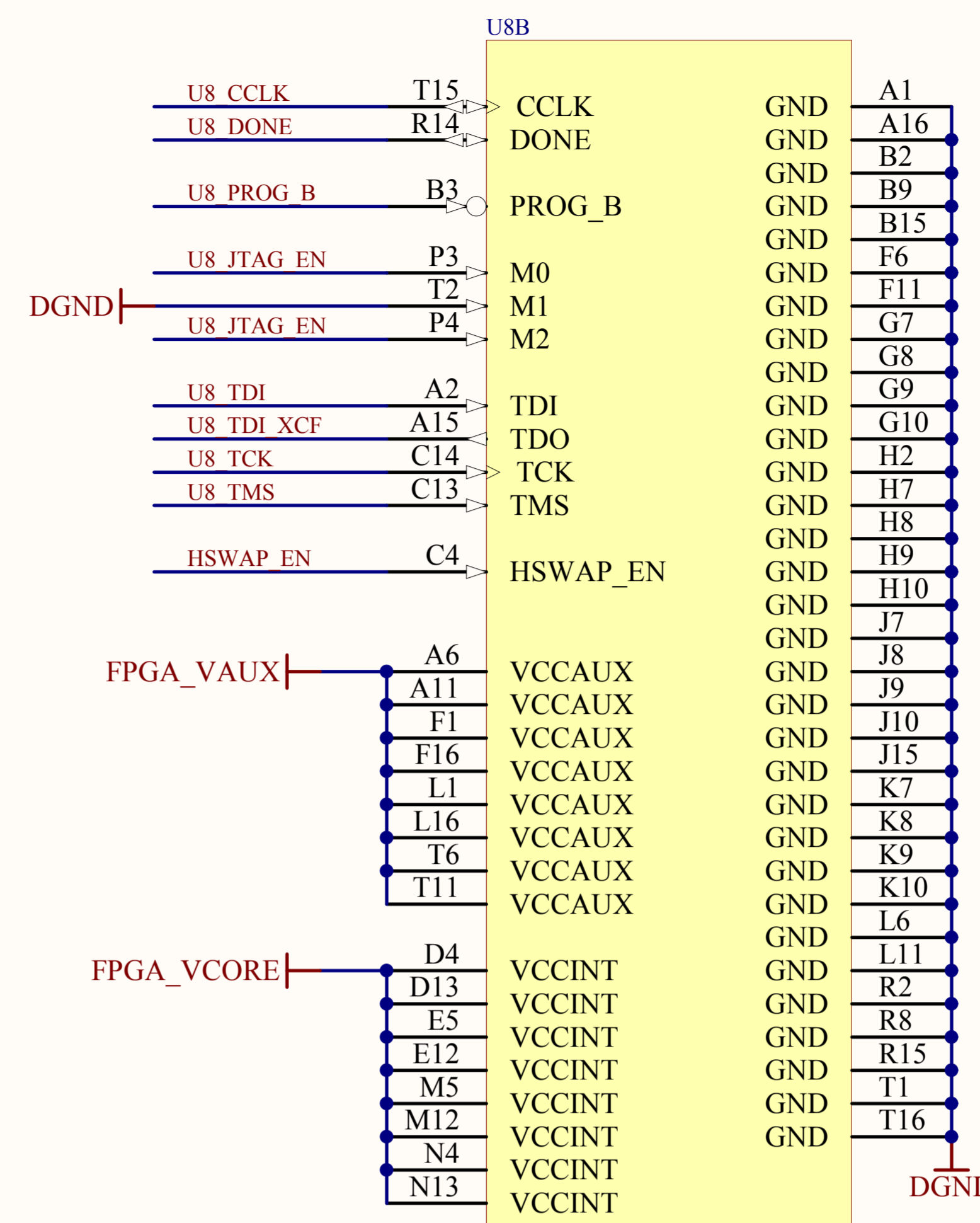
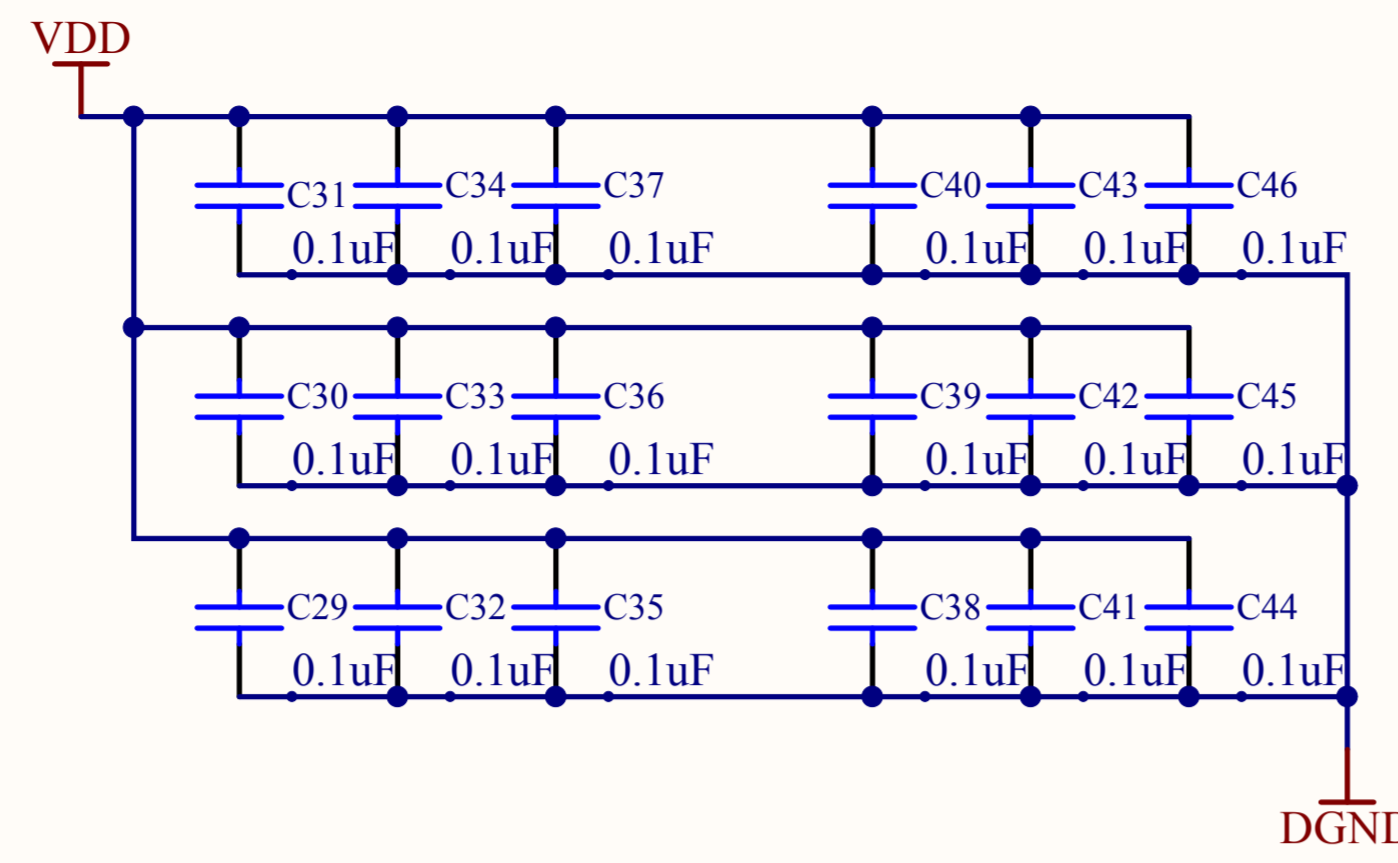
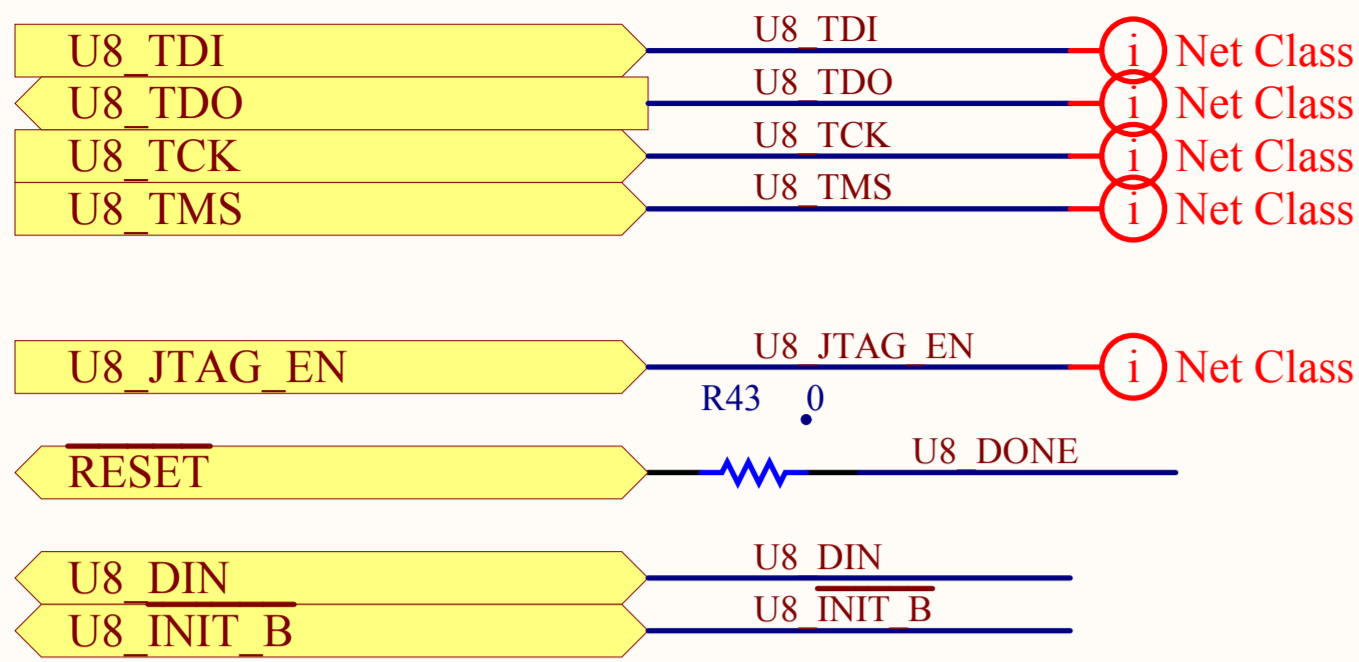


| IN | IT_B | JTAG_EN | Y |
|----|------|---------|---|
| X  | 1    | 1       |   |
| 0  | 0    | 1       |   |
| 1  | 0    | 0       |   |



|   |  |                      |  |   |                                |
|---|--|----------------------|--|---|--------------------------------|
| <b>QORTEK INC.</b><br>Address<br>1965 Lycoming Creek Rd<br>Suite 205<br>Williamsport, PA 17701<br>Phone<br>570 322 2700 |  |                      |  | Title<br><b>cPCI FPGA Configuration and Power</b> |                                |
|   |  |                      |  | Size<br>Legal                                     | Number<br>QOR-cPCIDSP-15-REV.1 |
| Date: 9/2/2005  |  | Sheet of             |  | Date: 9/2/2005                                    |                                |
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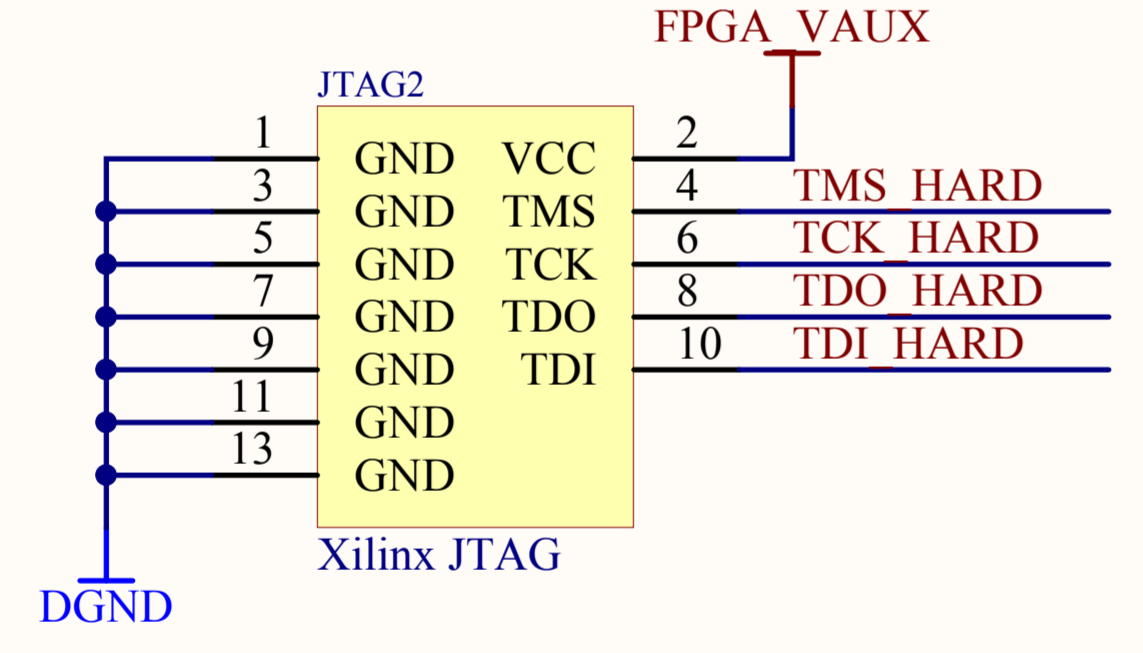
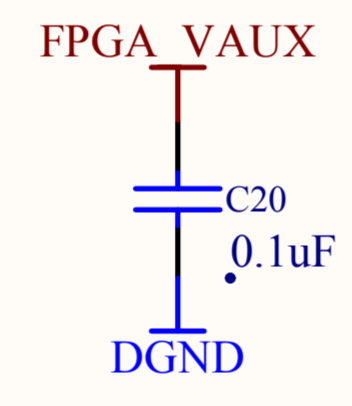
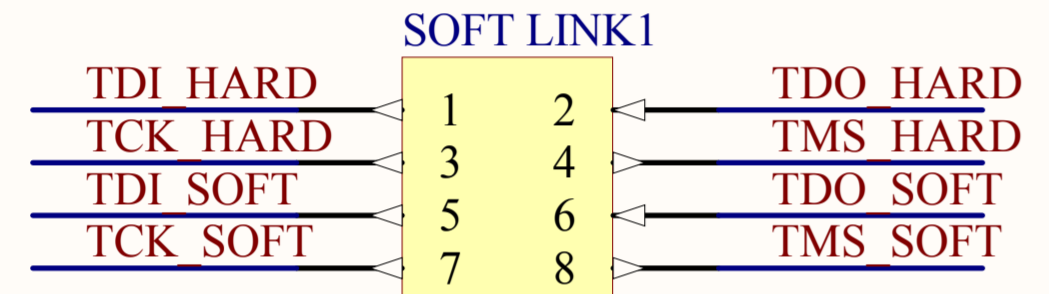
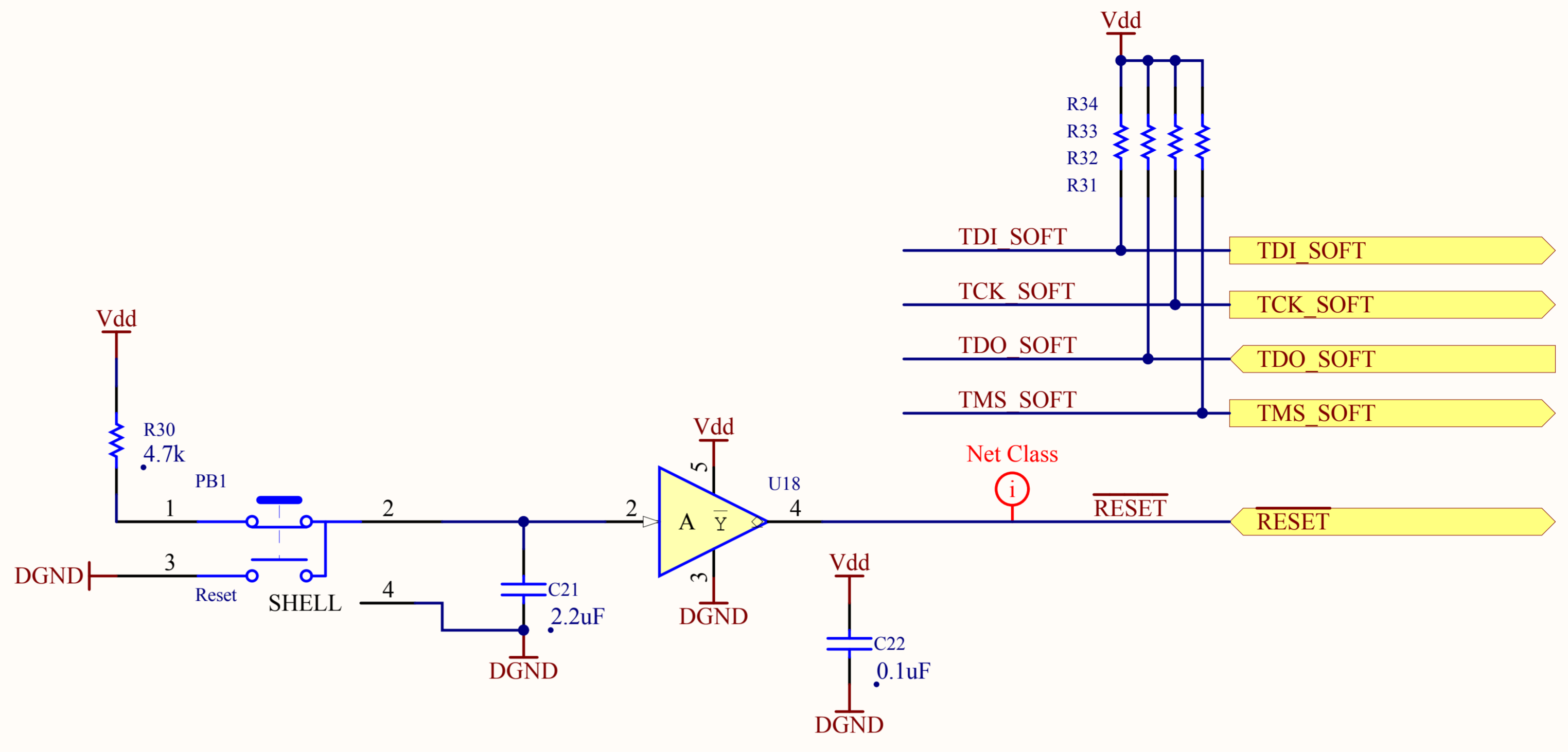
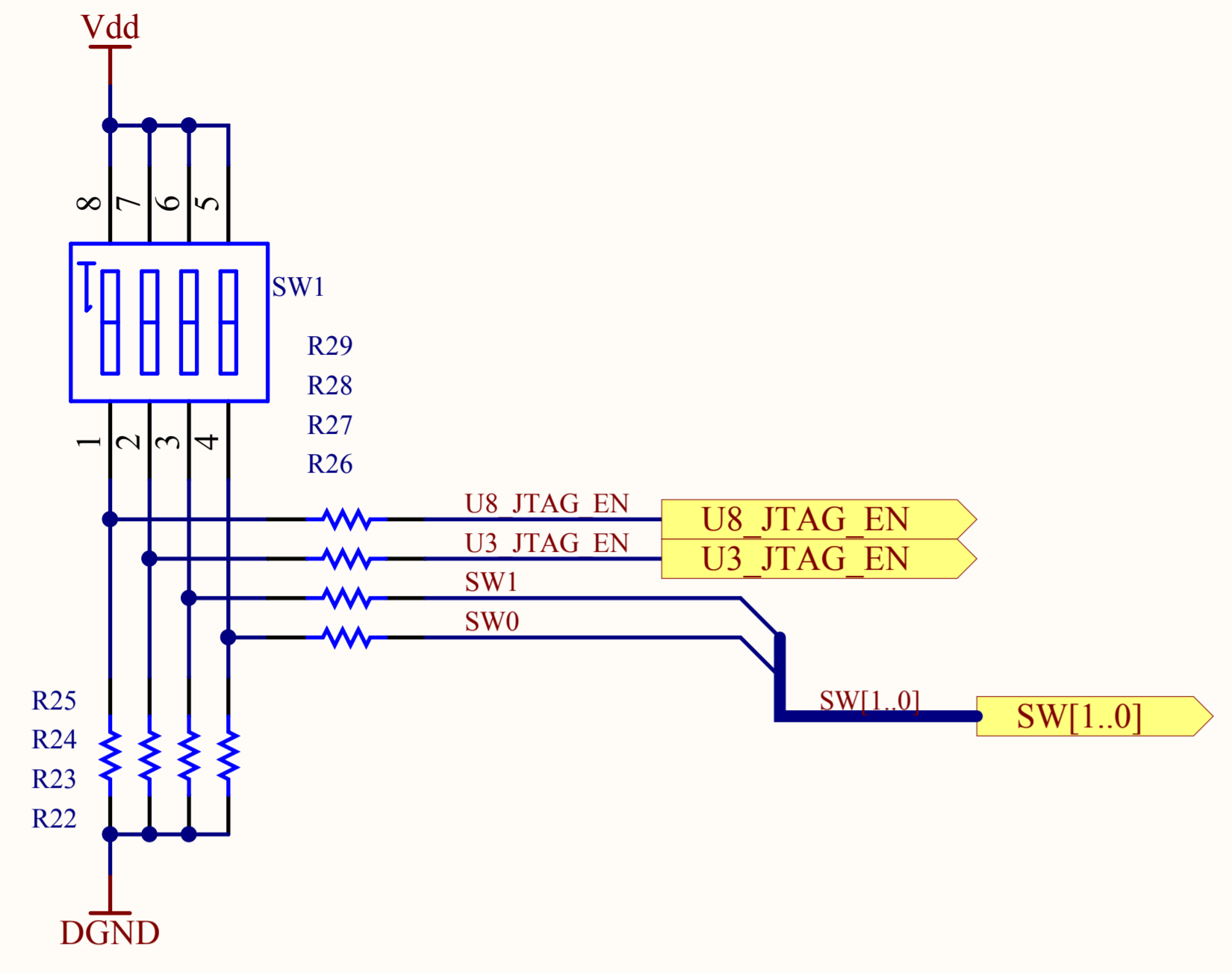
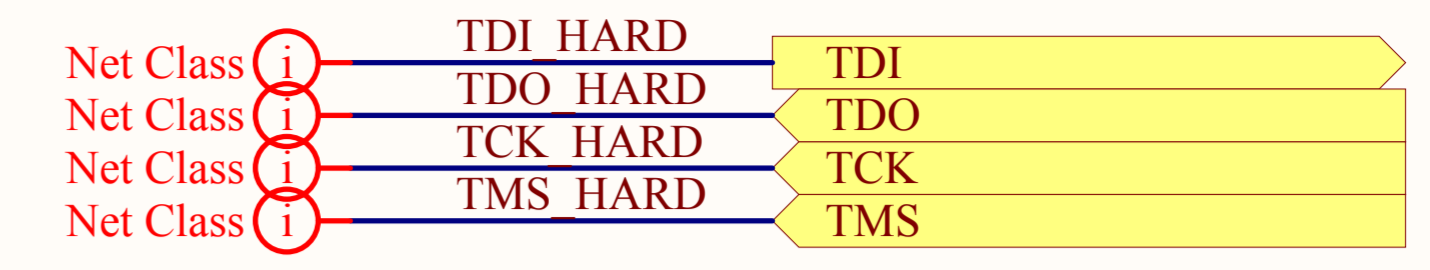


| IN | INIT_B | JTAG_EN | Y |
|----|--------|---------|---|
| X  | 1      | 1       | 1 |
| 0  | 0      | 1       | 1 |
| 1  | 0      | 0       | 0 |

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Title  
**HPI/GPIO FPGA Configuration and Power Bypass**  
 Size Letter Number Revision  
 QOR-cPCIDSP-16-REV.1 1  
 Date: 9/2/2005 Sheet of  
 File: D:\Projects\..FPGA\_FT256\_Power\_JTAG.DSN By: Brian Shea



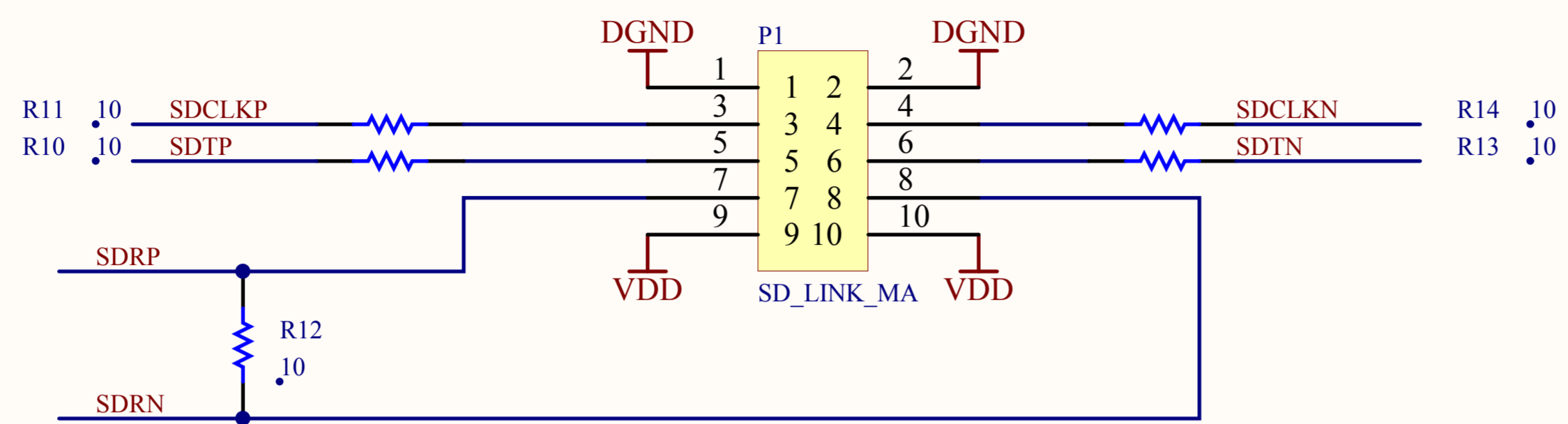
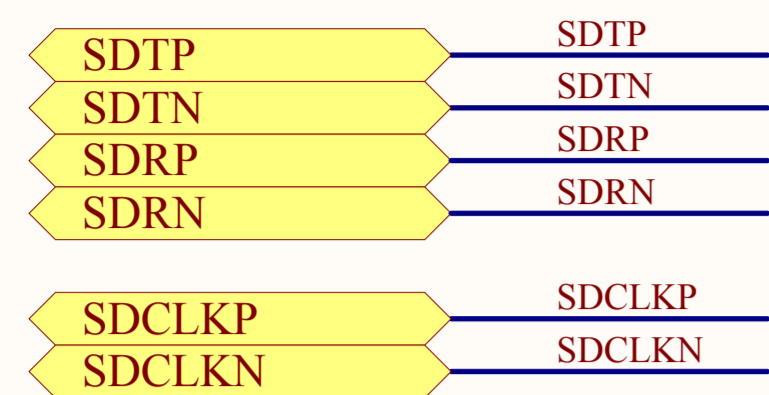
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| Title<br>JTAG Connectors, Configuration and Reset |                                |               |
| Size<br>Letter                                    | Number<br>QOR-cPCIDSP-14-REV.1 | Revision<br>1 |
| Date:<br>9/2/2005                                 | Sheet of                       | Drawn By: *   |
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FPGA SD LINK



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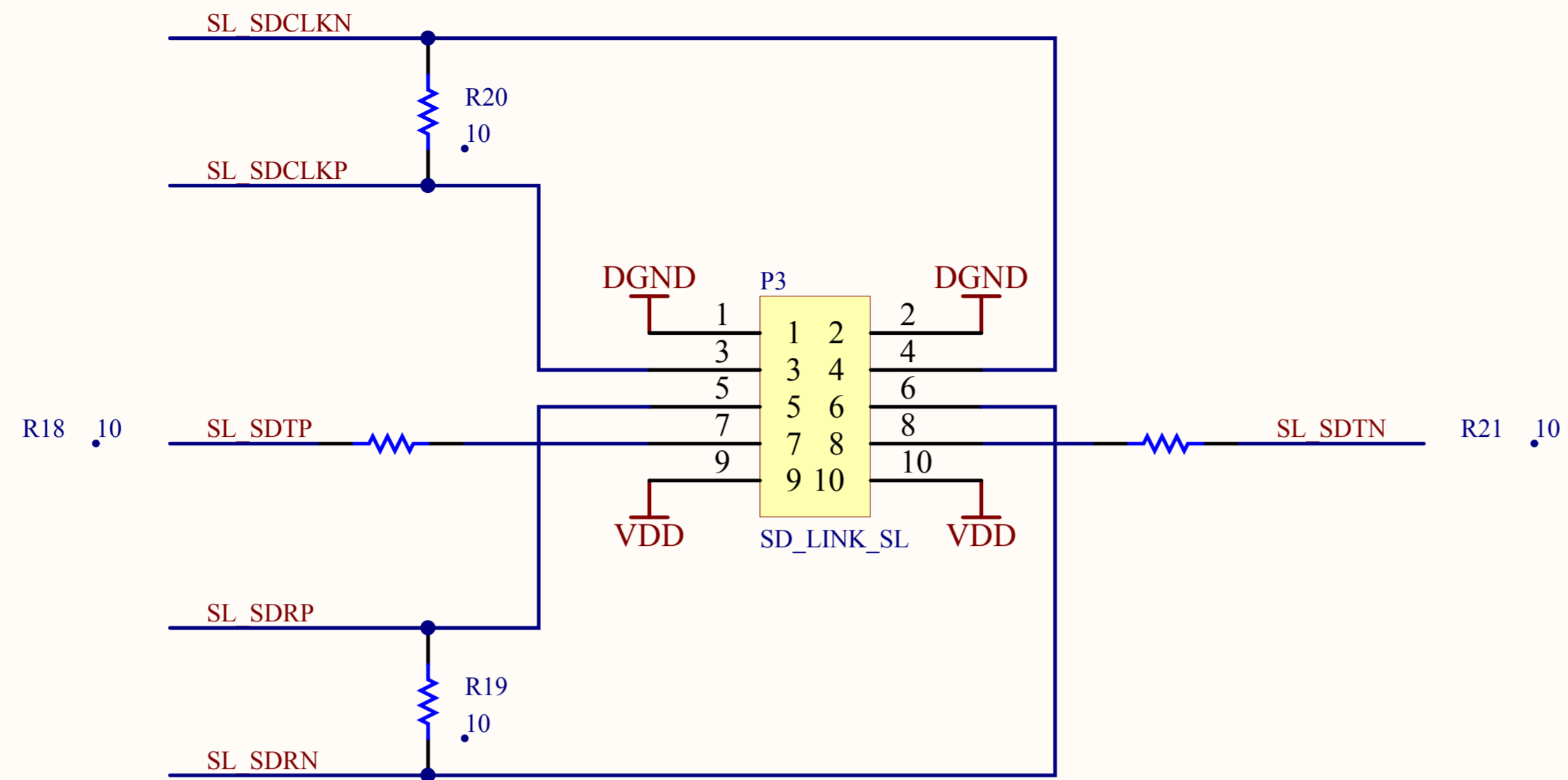
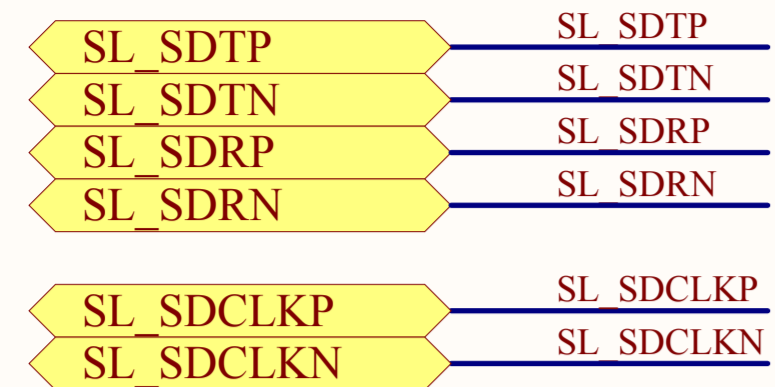


Title  
**Serial Data Link Interface**

|                |                                |               |
|----------------|--------------------------------|---------------|
| Size<br>Letter | Number<br>QOR-cPCIDSP-12-REV.1 | Revision<br>1 |
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FPGA SD LINK



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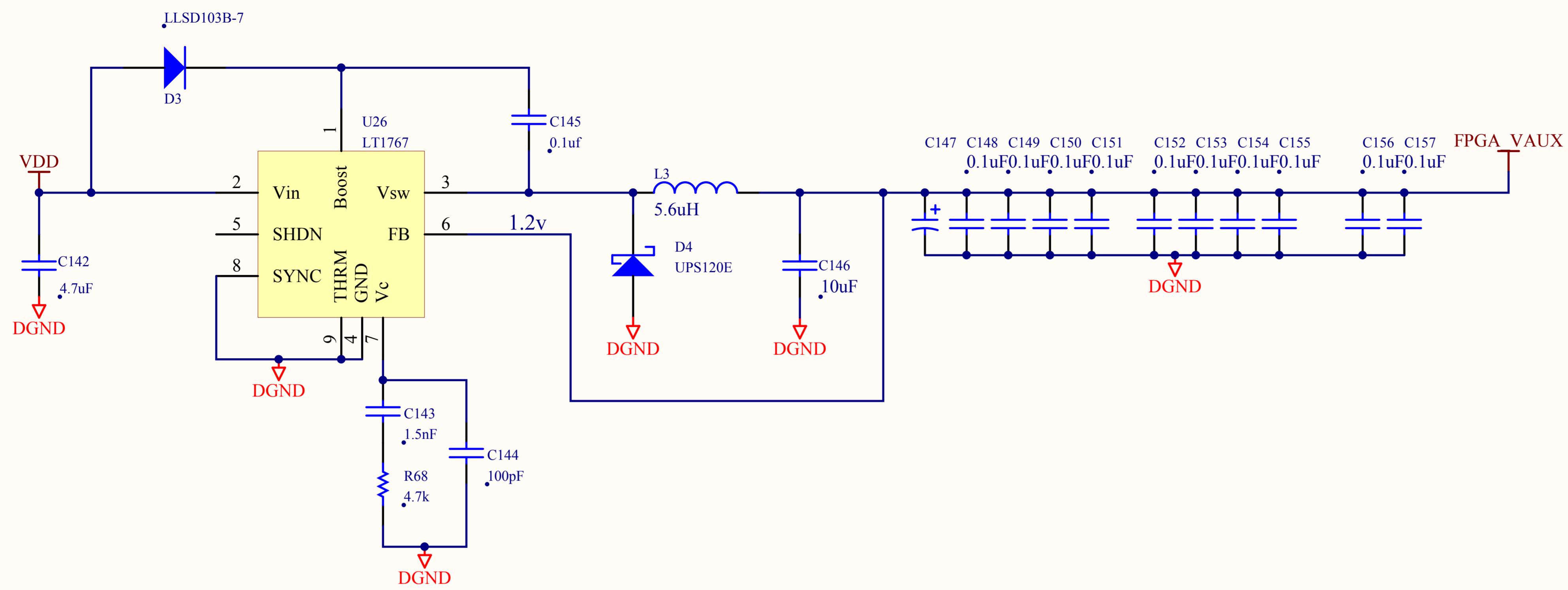


Title  
**HPI/GPIO Serial Data Link**

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|----------------|--------------------------------|---------------|
| Size<br>Letter | Number<br>QOR-cPCIDSP-13-REV.1 | Revision<br>1 |
|----------------|--------------------------------|---------------|

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| Title<br>FPGA Auxiliary Power Supply                  |                                |               |
| Size<br>Letter  | Number<br>QOR-cPCIDSP-20-REV.1 | Revision<br>* |
| Date:<br>9/2/2005                                     | Sheet of                       |               |
| File:<br>D:\Projects\...\FPGA_VAUX_PowerSupply.SchDoc | Drawn By:<br>Brian Shea        |               |

**DSP HPI Sigs**

|           |         |           |
|-----------|---------|-----------|
| HD[15..0] | HD15_01 | Net Class |
| HCNTL0    | HCNTL0  | Net Class |
| HCNTL1    | HCNTL1  | Net Class |
| HHWIL     | HHWIL   | Net Class |
| HDS2      | HDS2    | Net Class |
| HDS1      | HDS1    | Net Class |
| HCS       | HCS     | Net Class |
| HR/W      | HR/W    | Net Class |
| HAS       | HAS     | Net Class |
| HINT      | HINT    | Net Class |
| HRDY      | HRDY    | Net Class |

**FPGA SD LINK**

|           |          |
|-----------|----------|
| U8_SDTP   | U8_DTP   |
| U8_SDTN   | U8_DTN   |
| U8_SDRP   | U8_DRP   |
| U8_SDRN   | U8_DRN   |
| U8_SDCLKP | U8_DCLKP |
| U8_SDCLKN | U8_DCLKN |

**DSP GPIO**

|       |       |
|-------|-------|
| TOUT0 | TOUT0 |
| TINP0 | TINP0 |
| CLKX0 | CLKX0 |
| FSX0  | FSX0  |
| DX0   | DX0   |
| CLKR0 | CLKR0 |
| FSR0  | FSR0  |
| DR0   | DR0   |
| CLKS0 | CLKS0 |
| SCL0  | SCL0  |
| SDA0  | SDA0  |

|            |            |
|------------|------------|
| TOUT1      | TOUT1      |
| TINP1      | TINP1      |
| CLKX1      | CLKX1      |
| FSX1       | FSX1       |
| DX1        | DX1        |
| CLKR1      | CLKR1      |
| FSR1       | FSR1       |
| DR1/SDA1   | DR1/SDA1   |
| CLKS1/SCL1 | CLKS1/SCL1 |

|            |           |
|------------|-----------|
| XA[21..2]  | XA21_21   |
| XD[31..0]  | XD31_01   |
| XoBE[3..0] | XoBE13_01 |
| XoCS[3..0] | XoCS13_01 |

|        |        |
|--------|--------|
| XBUREQ | XBUREQ |
| XHOLDA | XHOLDA |
| XHOLD  | XHOLD  |
| XARDY  | XARDY  |

|        |        |
|--------|--------|
| XARE   | XARE   |
| XAOE   | XAOE   |
| XAWE   | XAWE   |
| XCLOCK | XCLOCK |

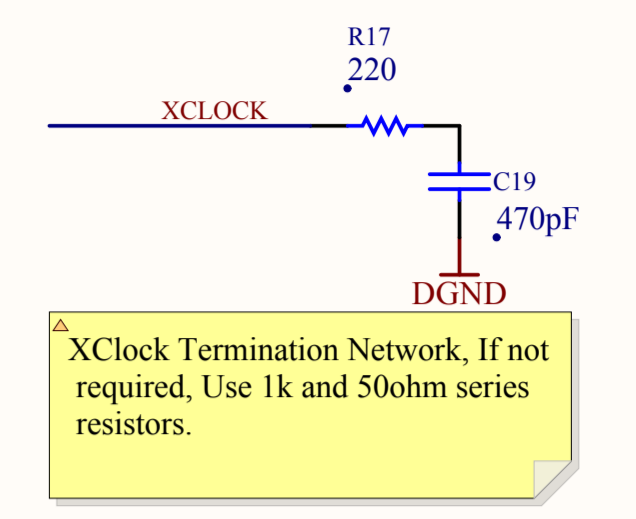
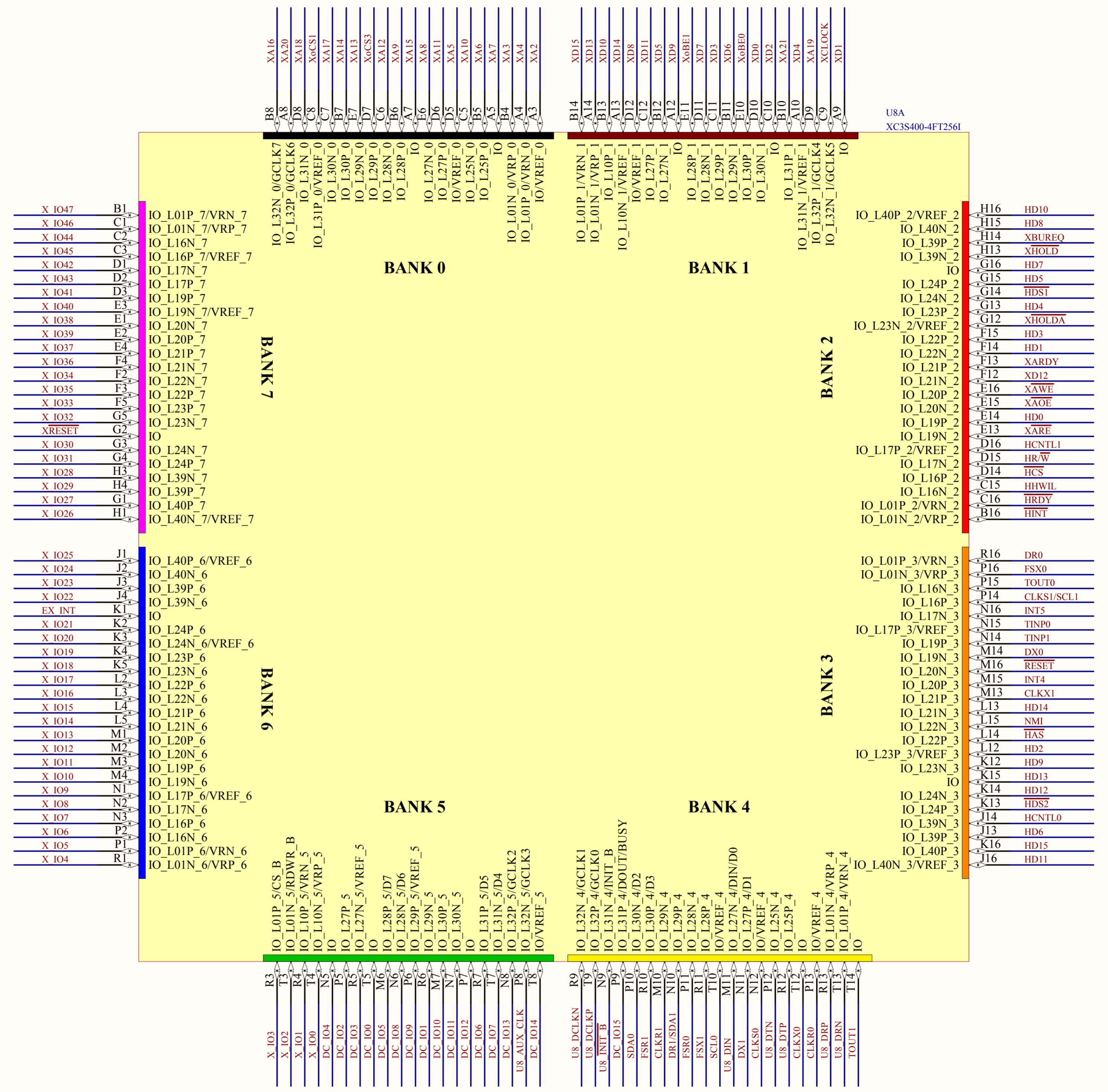
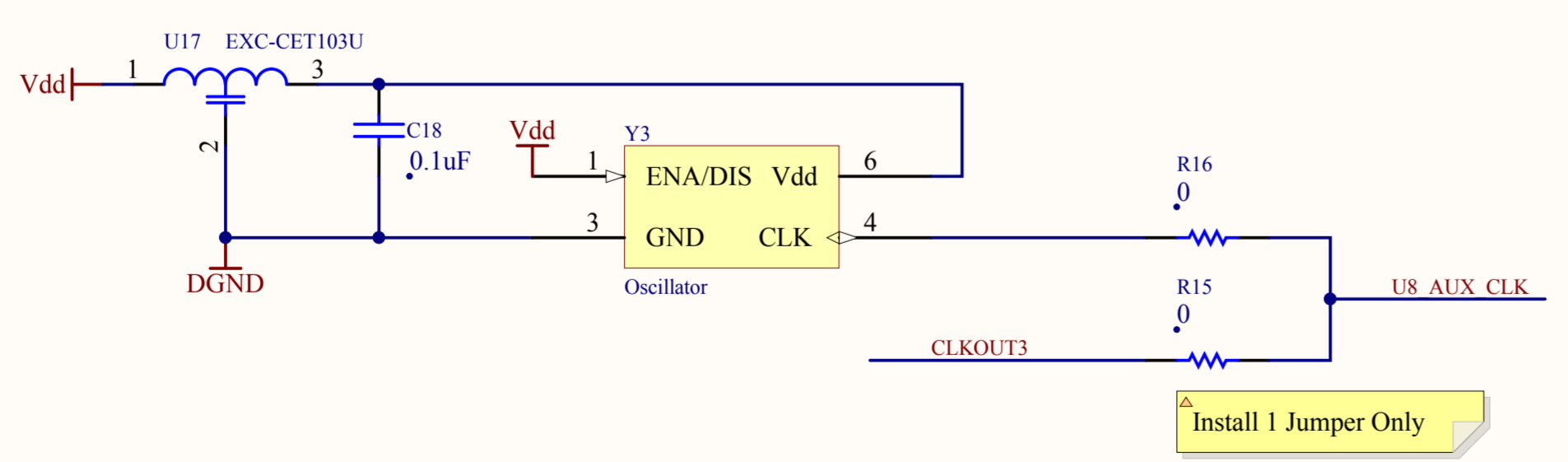
|       |       |
|-------|-------|
| RESET | RESET |
|-------|-------|

|         |         |
|---------|---------|
| CLKOUT3 | CLKOUT3 |
| INT4    | INT4    |
| INT5    | INT5    |
| NMI     | NMI     |

|             |           |
|-------------|-----------|
| X_IO[47..0] | X_IO47_01 |
| EX_INT      | EX_INT    |
| XRESET      | XRESET    |

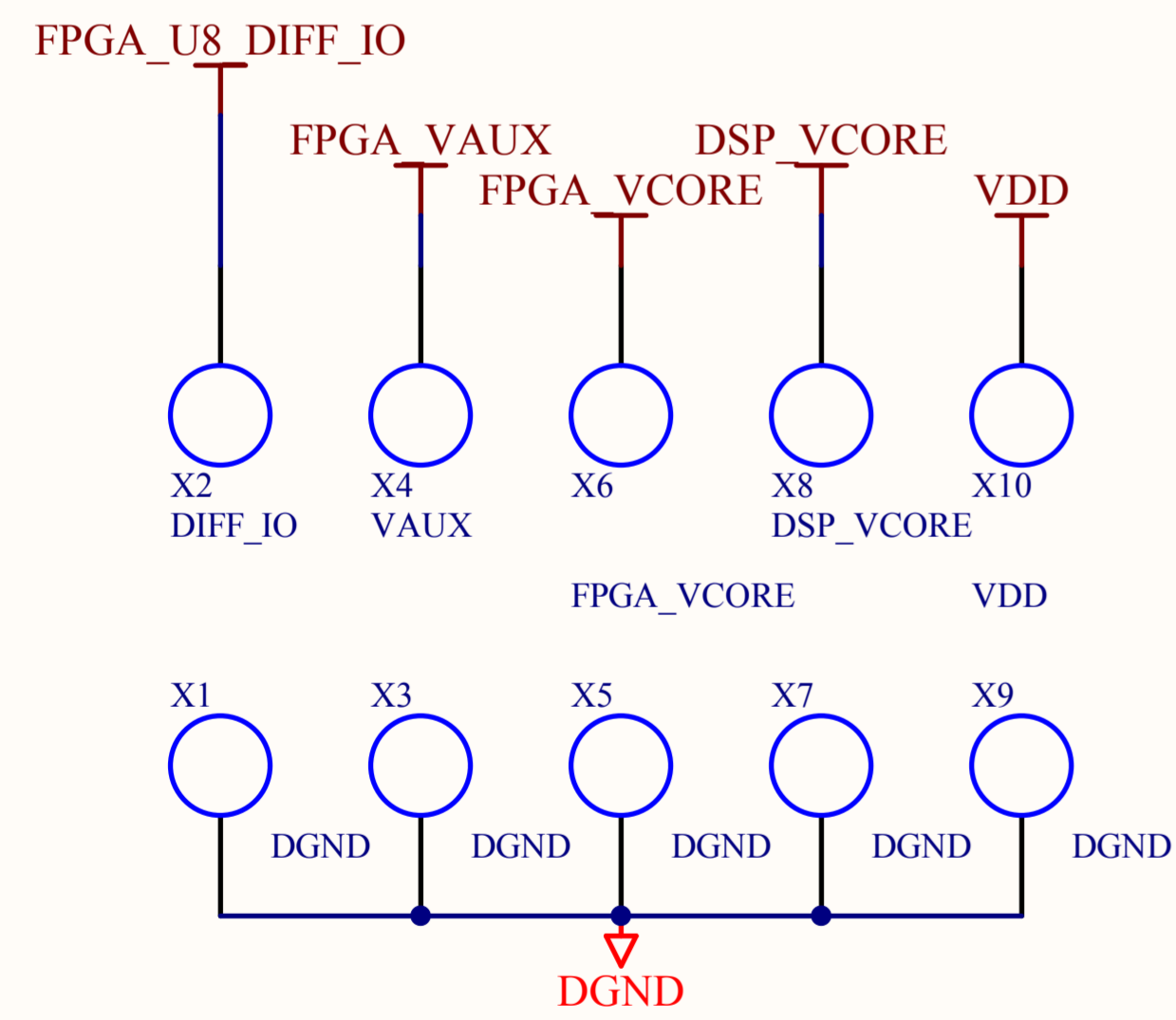
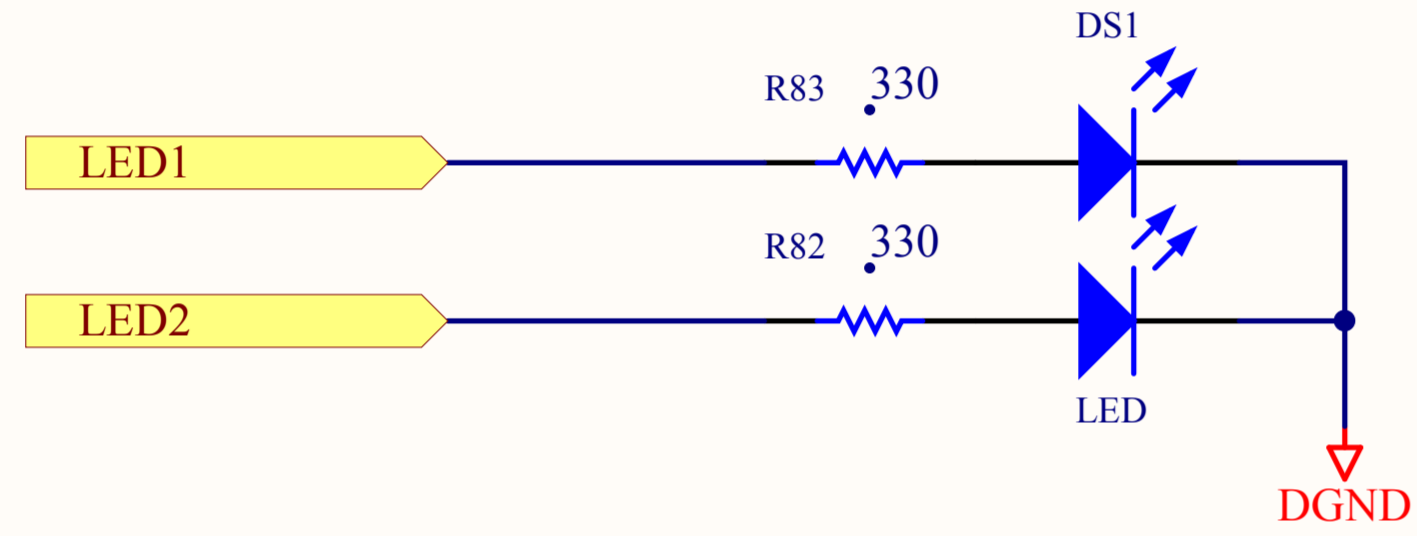
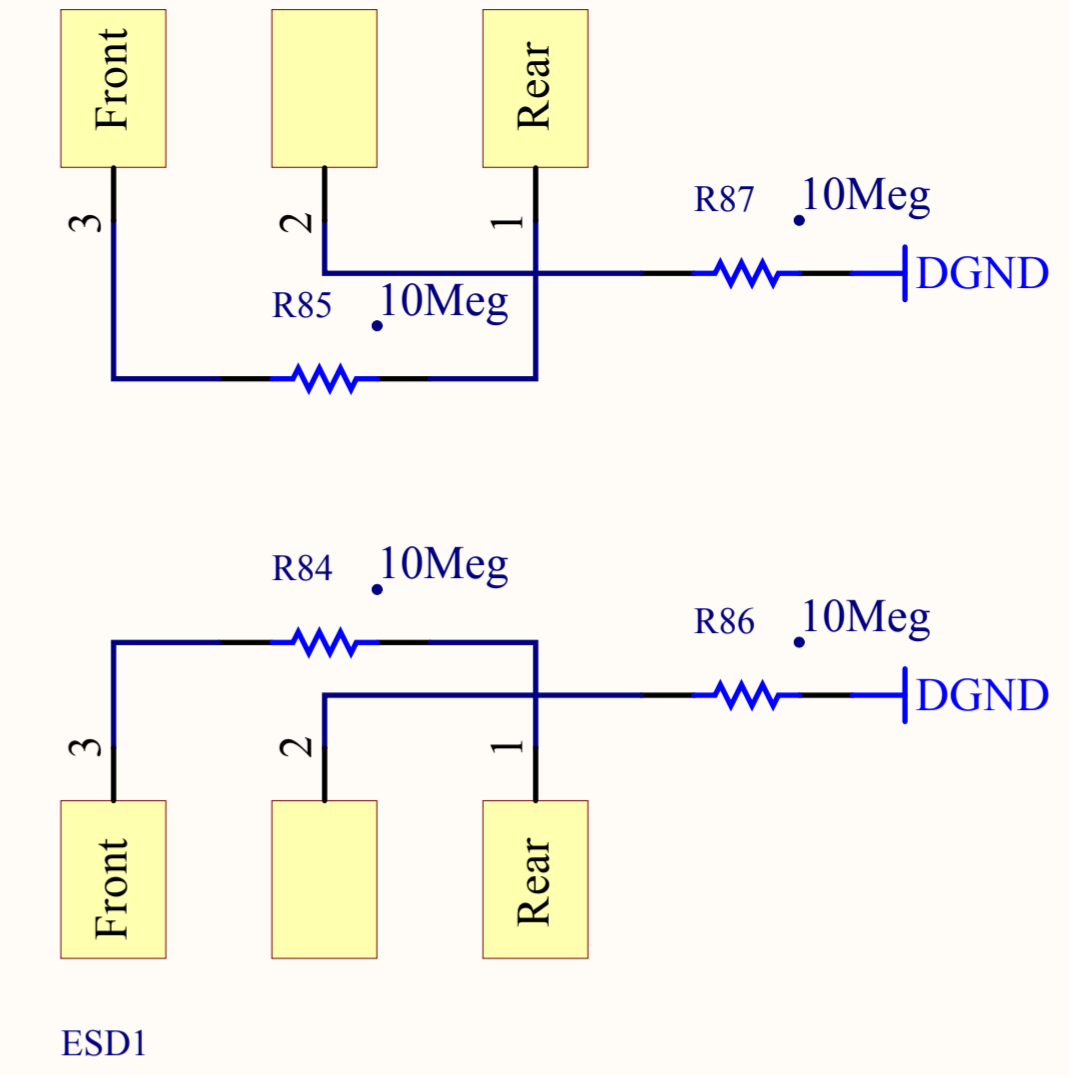
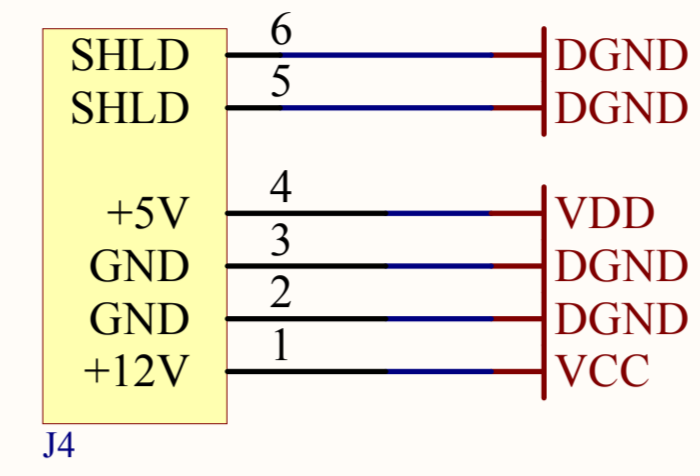
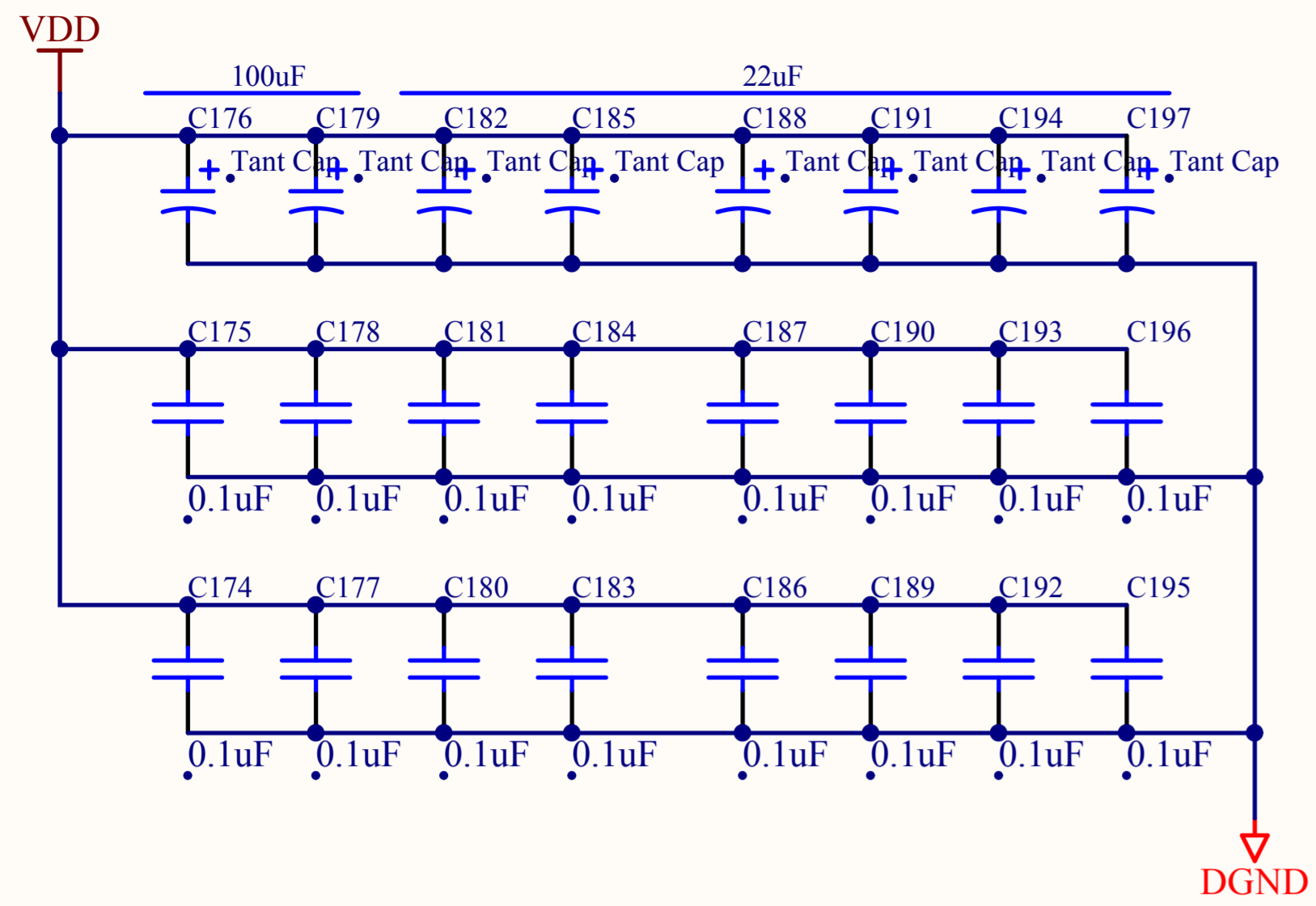
|              |            |
|--------------|------------|
| DC_IO[19..0] | DC_IO19_01 |
|--------------|------------|

|           |           |
|-----------|-----------|
| U8_INIT_B | U8_INIT_B |
| U8_DIN    | U8_DIN    |



|  |  |                                      |                              |
|--|--|--------------------------------------|------------------------------|
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| Phone<br>570 322 2700  |  | Date:<br>9/2/2005                    | Revision<br>1                |
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Title

Misc., Power Bypass and Test Points

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QOR-cPCIDSP-22-REV.1

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1

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